Depleted AlN/Si interfaces for minimizing RF loss in GaN-on-Si HEMTs

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Abstract

GaN-on-Si RF devices offer considerable cost benefit compared to market-adopted GaN-on-SiC devices. Beside a high gain, low RF loss is key for GaN-on-Si RF market penetration. The inherent conductivity of the Si substrate does not leave any freedom for additionally introduced conductivity by epitaxy or process. By controlling the condition of the epitaxial process chamber and the initial growth process conditions, we will demonstrate depleted AlN/Si interfaces that show record-low RF loss.

Introduction

5G market adoption will reach about 25% of the world population in 2025 [1]. At the same time, 6G research has gained traction already [2]. GaN-on-Si technology is expected to deliver the needed performance boost for 5G and 6G applications, both as discrete devices as well as front-end-modules. Aside from the fundamental performance gain over Si-based technology and the expected cost benefit compared to GaN-on-SiC, several challenges have shifted a market adoption towards the future. Such challenges comprise the larger mismatches of lattice constant and coefficient of thermal expansion for the GaN-on-Si system compared to GaN-on-SiC, the lower thermal conductivity of Si compared to SiC and the higher electrical conductivity of the Si substrates originating from the low band gap of Si. This higher electrical conductivity causes RF loss which degrades the quality factor of passives components, the efficiency of power amplifiers, and the linearity of switches.

RF loss is driven by a multitude of factors, most of which are shown in Fig. 1 [3], [4]. In the epitaxial part of the device manufacturing, we have influence on the substrate choice and the epitaxial process parameters. The latter alters the diffusion of Al and Ga into the substrate and the AlN/Si interface itself, both of which will influence the substrate conductivity. In this paper, we will discuss both with a focus on the AlN/Si interface.

Experimental setup

All epitaxial growth runs were performed in AIXTRON Planetary Reactors®, either in the long-proven AIXTRON G5+ C or in the recently introduced AIXTRON G10-GaN.

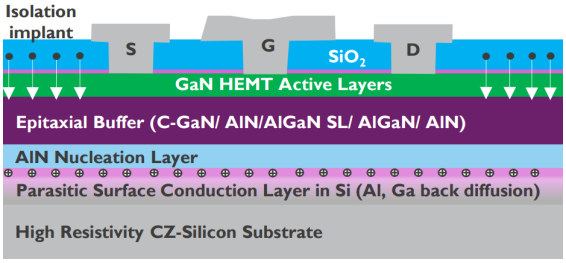

Fig. 1. Substrate RF losses in the GaN-on-Si HEMTs can be impacted by: (i) Starting Si substrate resistivity and interstitial impurity (e.g., O) concentration, (ii) III-N epitaxy leading to Al and Ga diffusion into the substrate, traps, and unintentional conductive channels in the epitaxial layers and at interfaces, (iii) HEMT device processing. [4]

Both systems rely on *in-situ* chamber cleaning with Cl_2 which is crucial to allow for low RF loss. The epitaxial layer growth was performed on mCZ HR-Si (111) substrates with a typical resistivity above 3 or 5 kΩ·cm. Prior to growth, the Si substrate surface was prepared with an oxide removal step under H_2 at 1050 °C. The growth was initiated with an Al predose step at a temperature between 700 °C and 800 °C in which TMAl is supplied to the chamber without NH_3 and followed by the growth of AlN at relatively low temperatures between 1000 °C and 1050 °C. Different epitaxial stacks (Fig. 2) were grown to analyze RF loss and the process parameters were modified to achieve the desired low RF loss. To assess the performance of the epitaxial stacks, coplanar waveguides were fabricated on the samples using photolithography and a Ni/Au stack. Different geometries were used and are indicated with *W* and *S*, where *W* is the width of the signal line and *S* the spacing between signal and ground line. S-parameter measurements between 1 and 40 GHz were then performed, and the effective resistivity (ρ_{eff}) was extracted as an average between 1 and 5 GHz according to [5].

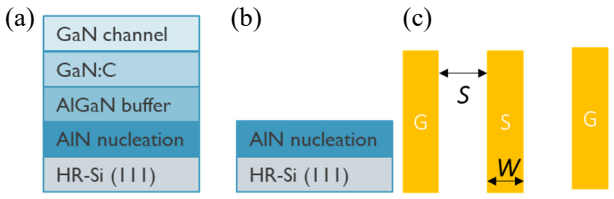

Fig. 2. (a) GaN buffer stack for initial results, (b) AlN-on-Si stack for in-depth analysis, (c) co-planar waveguide setup with *S* = spacing, and *W* = width of the signal line.

RESULTS

In the past, we improved the RF loss by decreasing the thermal budget of the epitaxial stack without sacrificing the crystal quality [6]. The thermal budget has direct influence on the amount of (mostly) Al that is diffusing and acting as an additional dopant into the Si substrate, making the p-type substrate (B-doped) more conductive. In Fig. 3, the insertion loss at 28 GHz vs. a calculated nominal diffusion length is shown. The diffusion length was calculated using Fick's second law and a diffusion profile that follows an Arrhenius-like temperature dependence [6]. A clear trend towards lower insertion loss is visible when minimizing the diffusion of the Al into the Si substrate. The remaining insertion loss has a significant contribution from the conductor losses in the CPW metal which can be higher than the substrate losses. Consequently, the measured $|S_{21}|$ in low-loss samples does not significantly change in response to reduced substrate losses. To quantify substrate losses in low-loss samples, the effective resistivity approach is used with following definitions. [4]:

$$\rho_{eff} = \frac{C_{eq}}{\epsilon_{eq}} \cdot \frac{1}{G} \quad (1)$$

where

$$C_{eq} = \sqrt{C_o \cdot C} \quad (2)$$

and

$$\epsilon_0 \cdot \sqrt{\frac{\epsilon_{r,eff} \cdot (\epsilon_{r,eff} - 1)}{\epsilon_{r,Si} - 1}} \quad (3)$$

where G, and C are the small-signal extracted conductance and capacitance, C_0, the air-filled capacitance and $\epsilon_{r,eff}$ the effective dielectric constant.

Using Eq. (1), we replotted Fig. 3 and the result is shown in Fig. 4, in which an increase of ρ_{eff} is clearly visible for lower diffusion length.

Based on the minimized diffusion length, we performed various experiments on the epitaxial growth stacks [Fig. 2 (a)] and epitaxial growth conditions. The results are plotted in Fig. 5. The various experiments show that despite the reduced thermal budget, ρ_{eff} was varying over a rather wide range with low values of about 800 Ω·cm well below the substrate resistivity. To investigate the influence of the process on ρ_{eff} further, we focused on AlN/Si samples. This allowed us to analyze the influence the process conditions in the AlN nucleation layer on ρ_{eff}. Specifically, we solely looked at the process conditions during the Al predose step, comparing various parameters such as predose temperature, predose flow, and predose duration. Results are shown exemplarily for the temperature variation (*cf.* Fig. 6) between roughly 700 and 800 °C. A huge impact of temperature on ρ_{eff} is apparent. For the lowest temperature (blue), a ρ_{eff} of around 1 kΩ·cm is obtained. The CPW with the narrower spacing shows a lower value, which is a clear sign of an AlN/Si interface that shows accumulation of carriers, i.e. the conductivity of the AlN/Si interface is larger than the bulk value of the Si substrate [4]. For the sample with the 2nd highest tested temperature, ρ_{eff} values of 4 and 7 kΩ·cm for the wide and narrow spacing, respectively, show the opposite trend, a clear sign of a depleted AlN/Si interface. The temperatures in the range of 700 to 800 °C are so low, that only negligible diffusion of Al into the Si substrate is occurring. The origin of the parasitic conductivity is hence encountered at the AlN/Si interfacial layer of which the control is becoming of utmost importance. Nucleation conditions inappropriate for optimized RF loss can lead to ρ_{eff} even below 100 Ω·cm. TEM microscopy was used to characterize the interfaces with low ρ_{eff} ~80 Ω·cm and high ρ_{eff} ~8 kΩ·cm. HAADF-STEM images for the samples with low and high ρ_{eff} are shown in Fig. 7 (a) and (b),

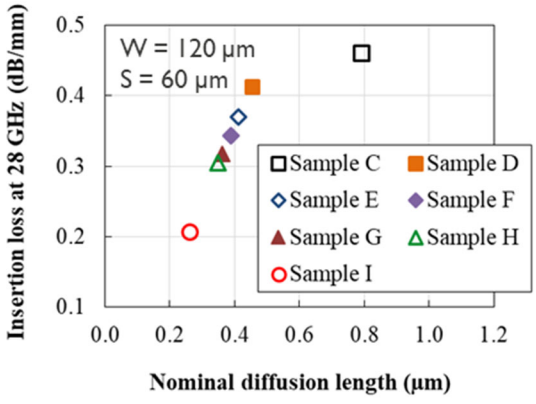

Fig. 3. Plot of insertion loss vs. calculated diffusion length for various GaN-on-Si samples. [6]

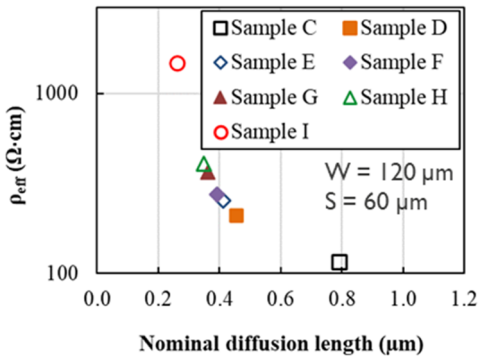

Fig. 4. Plot of effective resistivity (ρ_{eff}) vs. calculated diffusion length with the samples reported in [6].

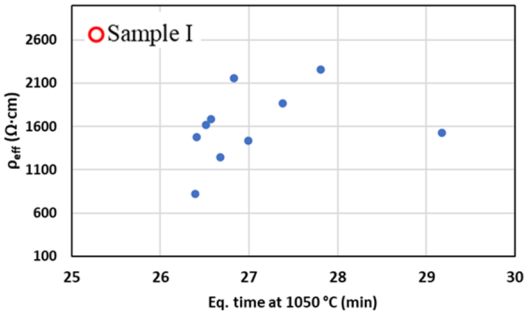

Fig. 5. Plot of effective resistivity (ρ_{eff}) vs. equivalent time at 1050 °C for GaN buffers stacks grown under different process conditions and with slight modifications in the buffer stack. No correlation between thermal budget and ρ_{eff} is visible.

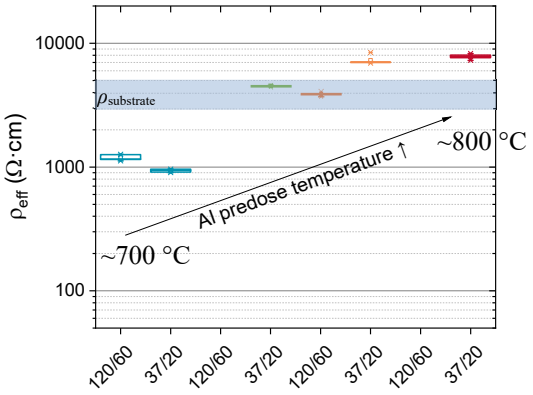

Fig. 6. Effective resistivity vs. temperature variation of the Al-predose for two different *W*/*S* (120 µm/60 µm and 37 µm/20 µm), showing an accumulated AlN/Si interface for the lowest temperature (blue) and a depleted AlN/Si interface for the higher temperatures (orange). ρ_{eff} is well beyond the specified Si substrate resistivity (shaded area).

respectively. The interfacial layer is in both cases amorphous but shows a clear difference in contrast indicating different elemental species. EDS plots highlighting the C content of that same region for the low and high ρ_{eff} sample are shown in Fig. 7 (c) and (d), respectively.

A higher C intensity and a broader C-rich region is observed for the samples with higher ρ_{eff}. Performing a vertical cut through the full EDS maps (full maps not shown) provides lines scans of the individual elements. These are shown for the low and high ρ_{eff} sample in Fig. 7 (e) and (f), respectively. Whereas for the sample with low ρ_{eff}, a SiN layer has formed at the AlN/Si interface, for the high-resistive sample, the SiN layer is very thin, and a SiC layer occupies a significant part of the interfacial layer. SiC formation at the AlN/Si interface has been described in earlier reports [7]. When the predose step is made even stronger using a higher TMAl volume compared to the sample analyzed in Fig. **7** (b), (d), and (f), we obtain an even stronger C signal, and the SiC interfacial layer is further increasing at the expense of the SiN interfacial layer (not shown). While one could expect a further improvement of ρ_{eff} for the narrow CPW dimension, we found however, ρ_{eff} to be decreased. We could correlate these findings with C-V measurements on diodes which shows the formation of an inversion layer (n-type) at the AlN/Si interface for the low ρ_{eff} sample, whereas a weak p-type layer is visible for the best performing samples and a strong p-type layer for the samples with the strongest pre-dose. It is hence crucial to obtain the optimal process window. It is expected, that the predose optimization of the single AlN/Si will differ slightly from that of a full GaN HEMT stack on Si or even a fully processed RF device. Full device processing and RF characterization are necessary here.

We used the gained knowledge to further increase ρ_{eff}. With the optimized process conditions very high ρ_{eff} levels were obtained. To verify the principal mechanisms, we performed the same experiments in a different nucleation process

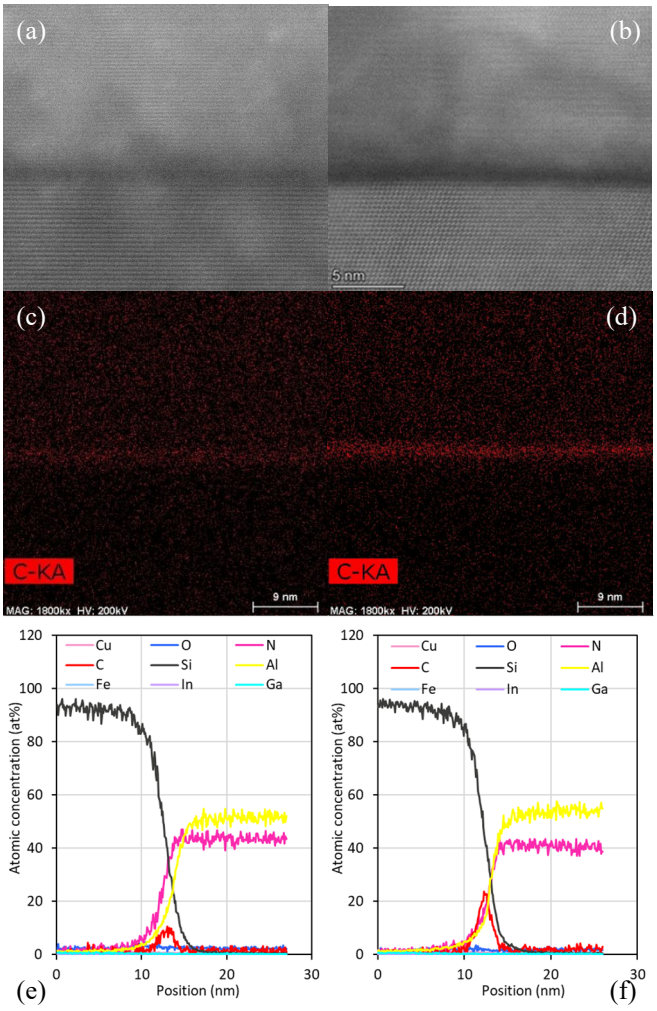

Fig. 7. HAADF-STEM images of the AlN/Si interfacial area of a sample with (a) low ρ_{eff} and (b) high ρ_{eff}, showing already a visible difference of the interfacial layer. EDS maps of C for the (c) low ρ_{eff} and (d) high ρ_{eff} samples showing significantly higher C density and C-containing layer width for the samples with higher ρ_{eff}. EDS line scans across the interfacial area for the (e) low ρ_{eff} and (f) high ρ_{eff} samples quantifying the EDS map for the different elements The scans show a certain thickness of SiN interfacial layer for the low ρ_{eff} sample, whereas no apparent SiN (but SiC) formation for the high ρ_{eff} sample is visible.

window. In the different process window, the same trends were observed, which validates our observations. Optimized results for both process windows are shown in Fig. 8. For the process window A, we obtained a record-high ρ_{eff} above 10 kΩ·cm for the narrow CPW dimensions. For the process window B, ρ_{eff} is at a high 8 kΩ·cm. Minor variations of the Si substrate doping level will also affect these values, i.e. we consider the obtained ρ_{eff} values as equally good.

A GaN-on-SiC reference sample from our lab yields a ρ_{eff} of about 3.8 kΩ·cm for the wide CPW dimensions, about the level we obtained for our optimized AlN/Si stack. The value for the latter is mainly dominated by the Si substrate

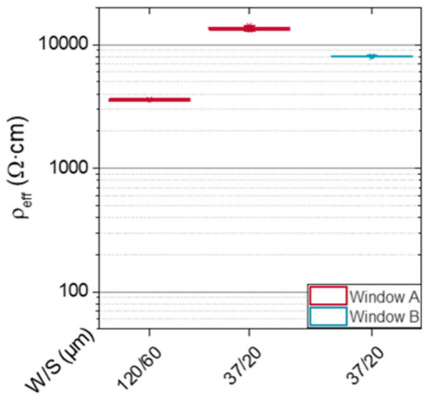

Fig. 8. Effective resistivity for two different process windows showing very high ρ_{eff} for the narrow CPW spacing.

resistivity. Our optimized results here have not been applied for a full buffer stack which will bring ρ_{eff} into a slightly smaller range as the GaN-on-SiC reference. Nonetheless, we have a clear indication that optimized epitaxial growth conditions can lead to RF loss performance parity of GaN-on-Si compared to GaN-on-SiC. As an outlook, we have replotted H2 vs. ρ_{eff} in Fig. 9. A clear correlation between harmonic distortion and ρ_{eff} is visible. Existing GaN-on-Si yielded H2 at around -80 dBm at H1 = 15 dBm [4]. More recently, -85 dBm have been obtained [8]. It is expected that by employing optimized nucleation conditions with ρ_{eff} at several kΩ·cm, H2 values around -90 dBm or even below could be obtained. The demonstration thereof will be done in future work.

Conclusions

We have shown the impact of the nucleation on RF loss for two different nucleation process windows. A depleted AlN/Si interface is obtained with optimized parameters for both process windows. A ρ_{eff} above the specified substrate resistivity has been achieved in both cases. To further increase the specific resistivity and hence to lower the RF loss, a reduction in Si substrate doping level (O_i, B) is necessary.

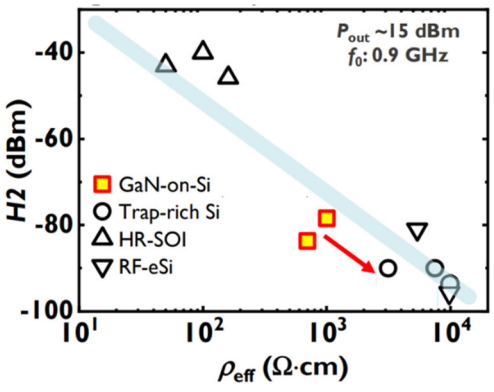

Fig. 9. H2 benchmarking of GaN/Si technology against various RF technologies at H1 (~ Pout) of 15 dBm. Optimized GaN-on-Si technology can achieve performance on par with trap-rich Si and RF-eSi technologies (red arrow).

Yet, already at this stage the values for GaN-on-Si are very well comparable to GaN-on-SiC and open the door for GaN-on-Si RF performance parity.

Acknowledgements

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Acronyms

EDS: Energy dispersive X-ray spectroscopy
H2: 2nd harmonic
HAADF-STEM: High angle annular dark field scanning transmission electron microscopy
HEMTs: High-electron mobility transistors
HR: High-resistive
mCZ: magnetic Czochralski
TEM: Transmission-electron microscopy
TMAl: Trimethylaluminum