Ultra low power CMOS circuits working in subthreshold regime for high temperature and radiation environments

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Abstract

We present three ultra-low-power CMOS circuits: a temperature sensor, a voltage reference and a comparator developed for an ultra-low-power microsystem (ULP-MST) aiming at temperature sensing in harsh environments. The microsystem has 3 main functions: detecting a user-defined temperature threshold T_0, generating a wake-up signal that turns on a data-acquisition microprocessor (located in a safe area) above T_0, and measuring temperatures above T_0.

To achieve ultra-low-power operation, the three CMOS circuits are implemented in Silicon-on-Insulator (SOI) CMOS technology and are optimized to work in the subthreshold regime of the transistors. Since our application is mainly for harsh environment (i.e. high temperature and radiation), the chip has been designed using a suitable 1-µm SOI-CMOS technology. Simulations have been performed over the different process corners to verify functionality after fabrication. The typical power dissipation at high temperature (up to 240°C) is less than 100 µW at 5 V supply voltage. Measurements have validated correct operation in the temperature range from -40°C to 300°C before radiation and to 125°C after radiation up to now which will be extended further with a new set-up.

Irradiation has been performed from 10 to 30 kGy. Such very high doses cause a shift down of output voltage values, which leads to a change of the temperature detection level and also increases the power dissipation by up to six times. Annealing effects help the partial recovery of the device operation at high temperature and the remote microprocessor enables calibration after radiation to readjust the temperature detection level.

Key words: Ultra low power, High Temperature, Radiation environment, Annealing effect, Temperature sensor, Voltage generator, Comparator, Subthreshold MOS regime

I. Introduction

SOI (Silicon-on-Insulator) technology is most often used in harsh environments applications such as space and biomedical, for its attractive features such as extended range of working temperature (up to 300°C), reduced parasitic effects, high speed and its lower sensitivity to transient radiation effects comparing to others technologies [l-4]. Using this suitable technology with CMOS process node of 1µm, an ultra-low-power and high-temperature microsystem was developed for harsh environment applications. This microsystem has three main functions: firstly it detects a user-defined temperature threshold T_0, secondly it generates a wake-up signal turns on a data-acquisition microprocessor, and thirdly it operates as a temperature sensor in harsh environment.

This work presents the analog part of this microsystem (Fig.1), which is composed by three ultra-low-power CMOS circuits: a voltage reference, a temperature sensor, and a comparator. These circuits were optimized to work in the subthreshold regime of the transistors to achieve ultra-low-power dissipation (less than 100 µW) at high temperature (up to 250°C).

The first part of this paper presents the designs and the simulation results of the three circuits. The second part shows the measurements results of the three circuits before and after 10 to 30 kGy irradiation dose. The last part discusses the annealing effect on the circuits and gives conclusions.

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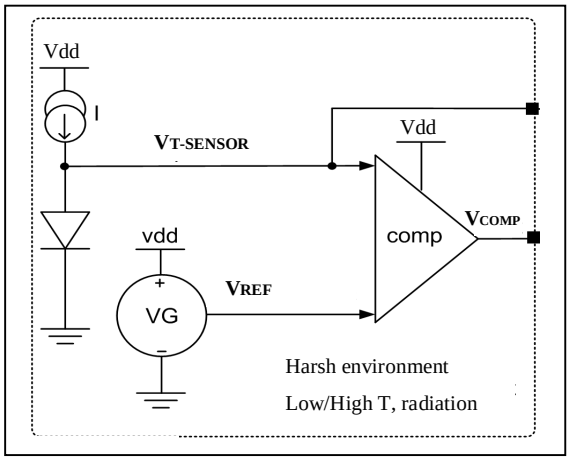

Fig.1: Analog part of the microsystem

II. Circuits design and Simulations results

The designs of blocks used in this microsystem were developed in 1µm partially-depleted (PD) SOI CMOS technology for a supply voltage of 5 V and a temperature range of -50°C to 250°C.

II.1- Voltage reference circuit:

A. *Circuit description*

The voltage reference circuit (Fig.2) used in this microsystem is a CMOS design circuit based on gate-source voltage difference between a pair of PMOS and NMOS transistors [5]. Comparing to previous work [5], our design circuit was extended to operate in a very large temperature range from -50°C to 250°C, it is designed using a 1µm PD SOI CMOS technology and to reduce the power dissipation, the transistors used in our circuit are optimized to work in subthreshold regime. Our design has a current consumption of about 2 µA at 100°C which is 5 times less than the current consumption of the work [5].

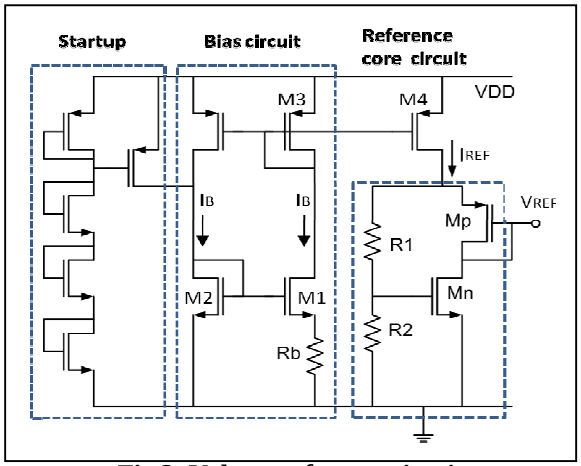

Fig.2: Voltage reference circuit

B. *Design principles*

1) V_{REF} *expression*

For a MOSFET working in the subthreshold regime [6], the *I-V* characteristics can be expressed by:

- For a NMOS

$$I_{D_N} = \mu C_{OX} V_T^2 . \frac{W_n}{L_n} \cdot \exp\left(\frac{V_{GSn} - V_{thn}}{n V_T}\right) . \left[1 - \exp\left(\frac{V_{DS}}{V_T}\right)\right]$$

- For a PMOS

$$I_{D_P} = \mu C_{OX} V_T^2 . \frac{W_p}{L_p} \cdot \exp\left(\frac{V_{SGp} - |V_{thp}|}{n V_T}\right) . \left[1 - \exp\left(\frac{V_{SD}}{V_T}\right)\right]$$

where $V_T = k_B.T/q$ is the thermal voltage (k_B is the Boltzmann constant, q the elementary charge and T the absolute temperature), n is the subthreshold slope parameter, µ is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, V_{thn} and V_{thp} are the threshold voltages of NMOS and PMOS respectively, W_N, W_P and L_N, L_P, are the channel width and length, respectively. V_{GSn} (V_{SGp}) and V_{DS} (V_{SD}) are the gate-to-source voltage and the drain-to-source voltage respectively for the NMOS (PMOS) transistor.

For $V_{DS} > 3V_{th}$ I_D becomes almost independent on V_{DS} [7]-[8], thus I_D for NMOS and PMOS can be expressed respectively by:

$$I_{D_N} = \mu . C_{OX} . V_T^2 . \frac{W_N}{L_N} \cdot \exp\left(\frac{V_{GSn} - V_{thn}}{n . V_T}\right) \quad (1)$$

$$I_{D_P} = \mu . C_{OX} . V_T^2 . \frac{W_P}{L_P} \cdot \exp\left(\frac{V_{SGp} - |V_{thp}|}{n . V_T}\right) \quad (2)$$

From equations (1) and (2) we can extract the following equations:

$$V_{GSn} = n . V_T \ln\left(\frac{I_{D_N}}{\mu . C_{OX} . V_T^2 . \frac{W_N}{L_N}}\right) + V_{thn} \quad (3)$$

$$V_{SGp} = n . V_T \ln\left(\frac{I_{D_P}}{\mu . C_{OX} . V_T^2 . \frac{W_P}{L_P}}\right) + |V_{thp}| \quad (4)$$

In the circuit in *Fig.2* and using the equation (1), the current I_B through the transistor M_1 (same current through M_2, and L_1=L_2=L) is given by

$$I_B = \mu . C_{OX} . V_T^2 . \frac{W_1}{L} \cdot \exp\left(\frac{V_{GS\,1} - V_{thn}}{n . V_T}\right) \quad (5)$$

$$I_B = \mu . C_{OX} . V_T^2 . \frac{W_2}{L} \cdot \exp\left(\frac{V_{GS\,2} - V_{thn}}{n . V_T}\right) \quad (6)$$

From equations (5) = (6) we obtain:

$$V_{GS.2} - V_{GS.1} = n.V_T \cdot \ln\left(\frac{W_1}{W_2}\right) \quad (7)$$

Also from the circuit in *Fig.2*, we derive the equation

$$V_{GS.2} - V_{GS.1} = R_B \times I_B \quad (8)$$

By substituting the equations (7) and (8), we have

$$I_B = n.V_T \cdot \ln\left(\frac{W_1}{W_2}\right) \Big/ R_B$$

In the circuit design (Fig.2) and assuming that $I_{REF}=m.I_B$ where m is the gain of the mirror (transistors M_3 and M_4) and assuming that the current flowing through the resistors R1 and R2 is negligible (since R1 and R2 > 1MΩ), the reference voltage V_{REF} and I_{REF} are given by (9)

$$V_{REF} = (1 + \frac{R_1}{R_2}).V_{GSn} - \left|V_{GSp}\right|$$

$$I_{REF} = m.n.V_T \cdot \ln\left(\frac{W_1}{W_2}\right) \Big/ R_B$$

Using the equations (3) and (4) we have

$$V_{GSn} = n.V_T \ln\left(\frac{m.n.\ln\left(\frac{W_1}{W_2}\right)\Big/R_B}{\mu.C_{OX}.V_T.\frac{W_n}{L_n}}\right) + V_{thn}$$

$$\left|V_{GSp}\right| = n.V_T \ln\left(\frac{m.n.\ln\left(\frac{W_1}{W_2}\right)\Big/R_B}{\mu.C_{OX}.V_T.\frac{W_p}{L_P}}\right) + \left|V_{thp}\right|$$

By choosing in the design of circuit (Fig.2), R1=R2 and $W_p=2*W_n$ and $L_N = L_P$, from (9) and (10) the reference voltage V_{REF} is given by

$$V_{REF} = 2.V_{GSn} - \left|V_{GSp}\right|$$

By changing the value of V_{GSn} and V_{GSp} we get the following expression of V_{REF} (10)

$$V_{REF} = n.V_T\left[\ln(2.n.A) - \ln(\mu.V_T.B)\right] + 2.V_{thn} - \left|V_{thp}\right|$$

where the A and B are two constants versus temperature and depend only of the design and the used technology. (R_B can be an external constant resistor)

$$A = m.\ln\left(\frac{W_1}{W_2}\right)\Big/R_B \qquad B = C_{OX}.\frac{W_n}{L}$$

The mobility μ and threshold voltages of MOSFET have the following temperature dependencies [9]-[10]

- $\mu = K_\mu.T^{-\alpha}$ with $\alpha > 1.3$
- $V_{TH} = V_{TH\,0} + K_T\left(\frac{T}{T_0} - 1\right)$

where K_μ is a positive constant and K_T is the temperature coefficient of threshold voltage, which is a negative quantity for NMOS transistor.
The subthreshold slope parameter n is associated with the variation of space charge capacitance and it is usually given by the equation [11]

$$n = \left(1 + \frac{C_S}{C_{ox}}\right)$$

where C_S is the capacitance between the inversion layer and the back-gate electrode. This capacitance is not a constant but a nonlinear function of temperature. The Fig.2 in [11] gives curve of C_S versus temperature.

2) *Temperature Coefficient of V_{REF}*

The temperature dependence of the voltage reference generated by the circuit in Fig.2 must be as low as possible particularly at the temperature threshold T_0 of the application. The aforesaid dependence is expressed by evaluating the temperature coefficient (TC); and it is defined at T_0 by the following expression:

$$[TC]_{T0} = (1/V_{REF})_{T0}.[dV_{REF}/dT]_{T0} \quad (11)$$

where, T_0 is 0°C (300K) in our example.
From equations (10) and (11) the TC versus temperature has the following equation: (12)

$$TC(T) = \frac{\frac{k_B}{q}\left[\left(n + \left(\frac{\sigma n}{\sigma T}\right).T\right).\left[\ln(2.n.A) - \ln(\mu.V_T.B)\right] + T + n(\alpha - 1)\right] + K_T}{n.V_T\left[\ln(2.n.A) - \ln(\mu.V_T.B)\right] + 2.V_{thn} - \left|V_{thp}\right|}$$

To calculate the temperature coefficient TC using the equations (12) is complex due to the parameter n which has nonlinear temperature dependency. This question will be studied in another work.
However, to get a small TC for our design, numerous simulations were launched on Spectre simulator (Cadence) for different process corners from -40°C to 300°C and by fitting the parameters A and B which depend on (W_1, W_2, L_N, m), we minimized the TC at T_0. Fig.3 shows the TC parameter of the voltage generator which is about -55 ppm/°C at 0°C and lower than 1000 ppm/°C

(i.e. 1 mV/°C) for the total temperature range from -40°C to 300°C.

The simulation results of V_{REF} for the temperature range of [-40°C, 250°C] are presented in Fig.4.

As a conclusion, the proposed voltage generator circuit gives an average voltage of 2 V with a temperature coefficient less than 55 ppm/°C for the temperature range of (-25°C to 50°C) which is our initial required application range. The current consumption is about 3.05 µA at 100°C, and the power dissipation is less than 40 µW at 300°C (Fig. 9).

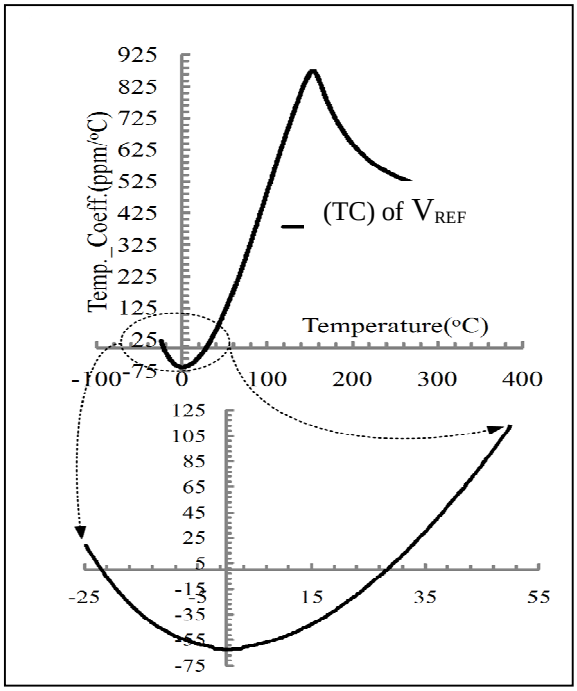

Fig.3: Temperature Coefficient vs Temperature

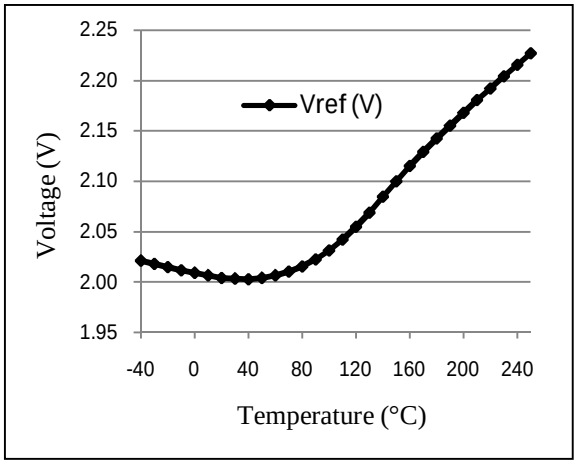

Fig.4: Voltage reference V_{REF} vs temperature

II.2- Temperature sensor circuit:

The second proposed circuit (Fig.5) is a diode-based temperature sensor composed by a current source driving a contact current on three series diodes. The current source is the same as that used in the previous voltage generator circuit with transistors optimized to work in subthreshold regime.

The diode used for this technology has a voltage slope of 2 mV/°C. Thus, the three series diodes give a quasi linear characteristic versus temperature with a slope of 6 mV/°C (Fig.6).

The current consumption of this circuit is about 0.4 µA at room temperature, and the power dissipation remains less than 10 µW at high temperature (250°C) with a power supply of 5 V (Fig. 9).

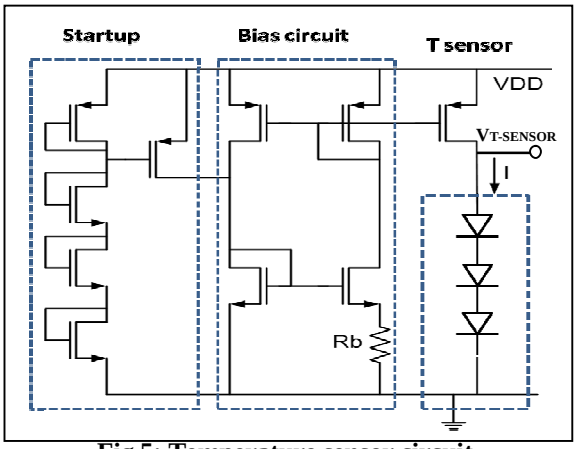

Fig.5: Temperature sensor circuit

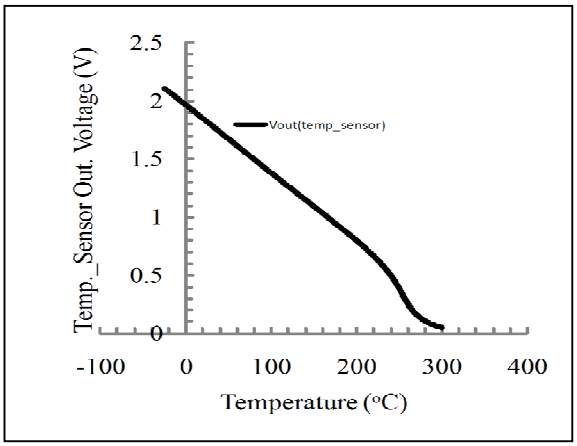

Fig.6: Temperature sensor output voltage versus temperature

II.3- Comparator circuit:

The comparator circuit (Fig.7) is a traditional 3-stage based comparator [12]. As showed in Fig.8 the comparator uses the same bias current circuit than the two previous circuits always with transistors optimized to work in subthreshold regime. This leads to a biasing current about 2.11 µA at 27°C and less than 40 µW at 300°C and 5 V power supply (Fig. 9).

As illustrated in Fig. 8 the comparator generates a wakeup signal when the sensor output voltage passes below the V_{REF} at the threshold level of

temperature T_0 (corresponding to 0°C); this turns on a power switch and hence the remote microprocessor.

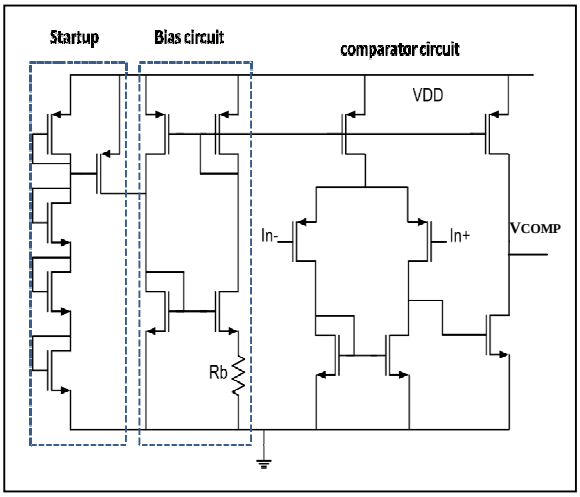

Fig.7: Temperature comparator circuit

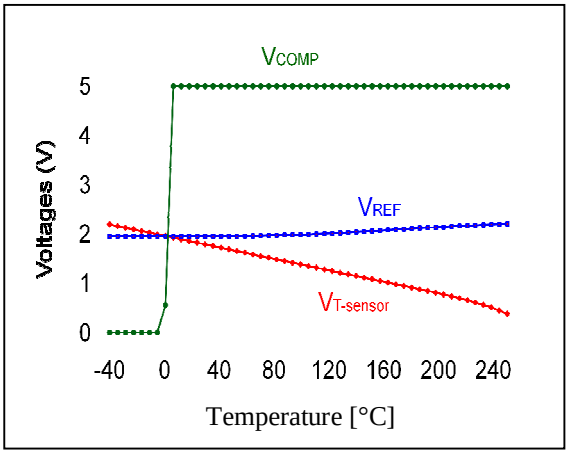

Fig.8: Output voltages of the microsystem

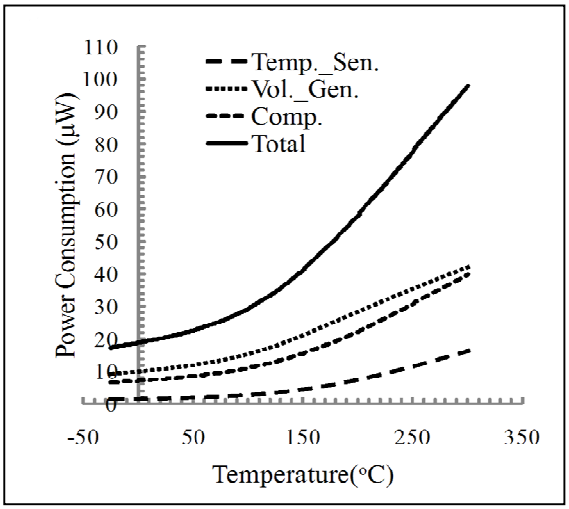

Fig.9: Power consumption of circuits versus temperature with power supply of 5V

III. Measurement results and Annealing effects on the circuits

The main application of our microsystem is to work under harsh environments such as high range of temperature and radiation. To validate this feature, we first confirmed our simulation results by measuring the microsystem in a large range of temperatures from -40°C to 300°C. After that, we exposed the chips of the microsystem to radiation up to total doses from 10 to 30 kGy (i.e. 1 to 3 MradSi), and we tested our microsystem again for temperature range of -40°C to 125°C.

1- Measurements before radiation

Fig. 10 presents the measurements of one microsystem versus temperature. As expected, the comparator shifts from 0 to 5 V at the temperature threshold T_0 = 0°C, and the temperature sensor has a quasi-linear characteristic versus temperature with a slope of 5.4 mV/°C for the temperature range -40°C to 250°C. But for the initial required temperature range (-25°C to 50°C) the slope is closer to the theoretical 6 mV/°C (Fig. 11).

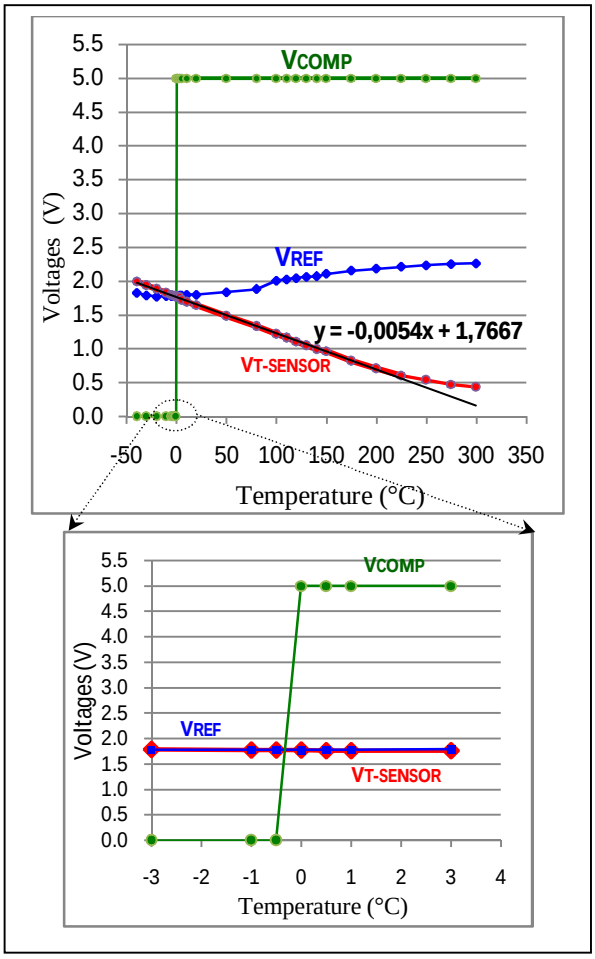

Fig.10: Output voltages of the microsystem

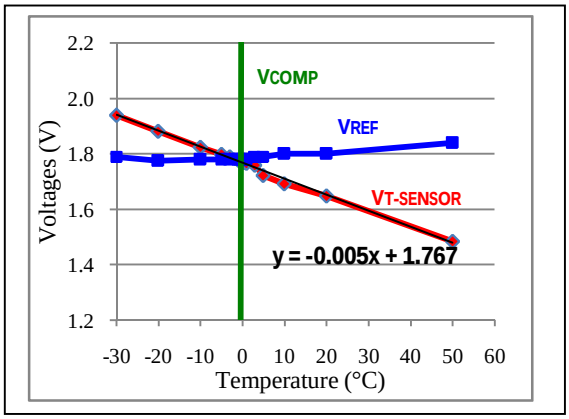

Fig.11: Output voltages of the microsystem

Fig. 12 shows the total current consumption of the microsystem versus temperature. This current dissipation remains less than 20 µA (100 µW at 5 V power supply) at 250°C.
With this power dissipation, the microsystem corresponds to an ultra low power application up to 250°C.

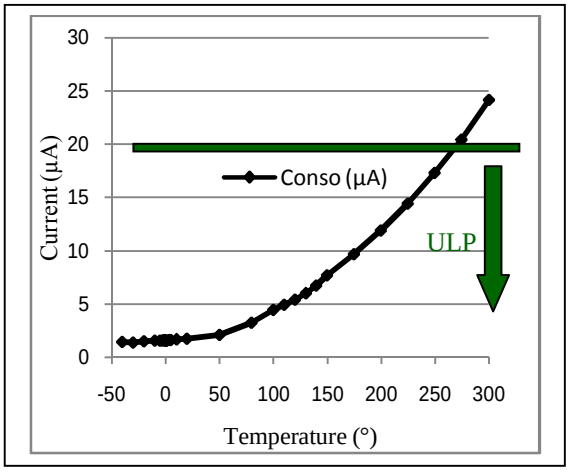

Fig.12: Measured current consumption of the microsystem versus temperature

2- Measurements after radiation

As a consequence of the irradiation tests on the designed CMOS circuits, first Fig. 13 and Fig. 14 show a shift down of output voltages values for the temperature sensor and also the voltage reference. Fortunately the output characteristic of the temperature sensor remains quasi linear versus temperature with the same slope (Fig. 13).
This shift down of output voltages leads to a change of the temperature detection level of the microsystem from T0 = 0°C to T0 = 60°C (Fig. 15), so it disturbs the microsystem application.
Secondly, as presented in Fig. 16, the current consumption measured for 6 different chips at three irradiation doses; 10 kGy, 20 kGy and 30 kGy (1 MRad, 2 MRad and 3MRad) at 27°C, was increased by six times.

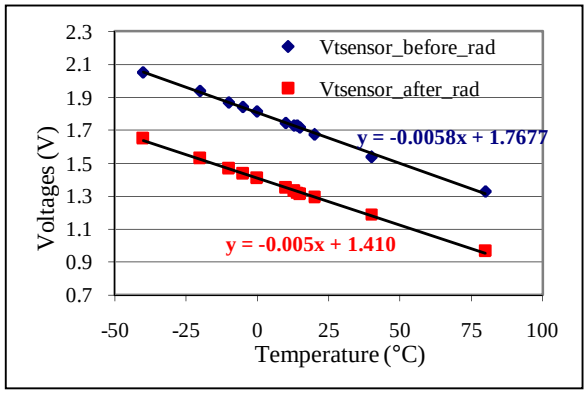

Fig.13: Temperature sensor output versus temperature before and after radiation

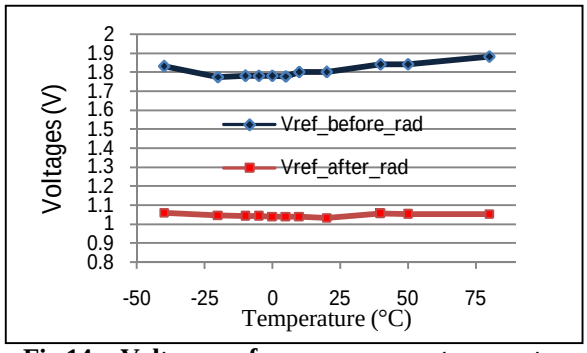

Fig.14: Voltage reference versus temperature before and after radiation

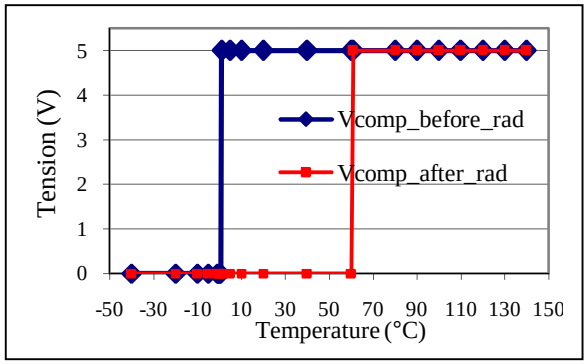

Fig.15: Shift of level detection from 0 to 60°C

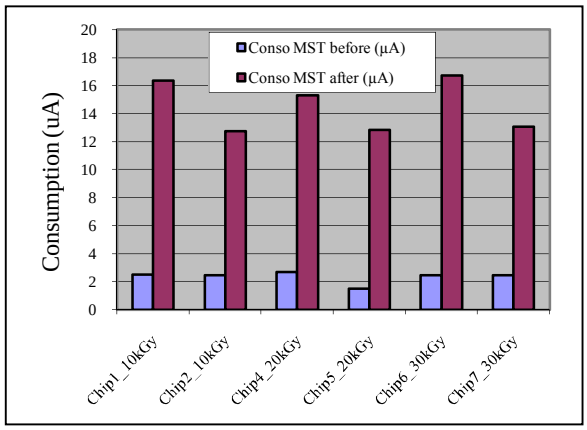

Fig.16 Microsystem consumption before & after radiation at room temperature

3- *Proposed solutions*

To readjust the temperature detection level of the microsystem at T0 = 0°C we can shift up the output value of the voltage reference by tuning the value of the external resistor R_B (equation 10). Fig.17 demonstrates this possible readjustment of T_0 from 60°C to 0°C.

For example this tuning can be done automatically by a calibration process using a connected microprocessor and its embedded ADC.

For the current consumption, the annealing effects [13] help the partial recovery of the device operation at high temperature. Fig.17 shows the current consumption after one temperature cycle for a chip irradiated at dose of 3 MRad. Thus at the temperature 0°C the consumption was reduced from 11 µA to 5 µA with just one cycle and a maximum temperature of 120°C. Moreover by increasing the temperature of the circuit up to 300°C and after several temperature cycles, the consumption is further reduced. This hypothesis still remain to be confirmed in later measurements.

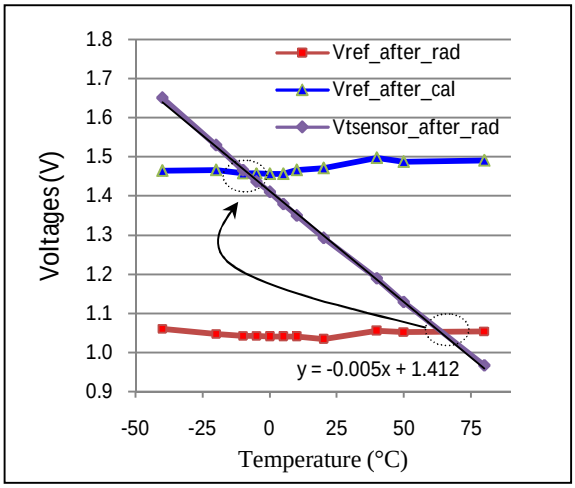

Fig.17 Shift back of the detection level after one cycle of annealing at 120°C

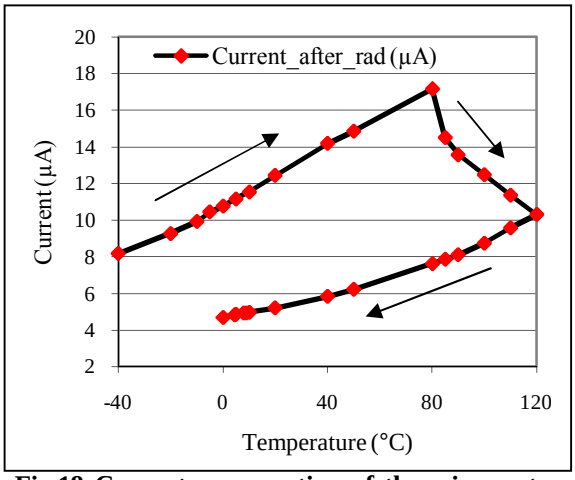

Fig.18 Current consumption of the microsystem after one cycle of annealing at 120°C

IV. Conclusion

We presented in this work three ultra-low-power CMOS circuits: a temperature sensor, a voltage reference and a comparator, designed in the subthreshold regime of the transistors, developed to work under harsh environment (high temperature and high radiation dose) and using 1µm PD SOI CMOS technology. These circuits were demonstrated to be functional up to 300°C and consume, before radiation, less than 100 µW at 250°C with a power supply of 5 V. After very high radiation doses in excess of 1 MRadSi, which decrease the threshold voltage of the transistors, the current consumption of the microsystem was increased by more than 6 times. The output voltage values of the voltage reference and temperature sensor were also shifted down. This shift disturbs the functionality of the microsystem which has to wake a microprocessor when the temperature crosses a defined threshold temperature T_0.

As a solution for these issues, we first studied the annealing effect which helps the partial recovery of the device operation at high temperature. Secondly to readjust the threshold temperature detection, so the functionality of the microsystem, we shift up the voltage reference output value, by fitting the external resistor R_B used in the design. This operation could be automated with a regular calibration process after radiation by a remote microprocessor, its embedded ADC and a programmable resistor.

Acknowledgements

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