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Etch rate modification by implantation of oxide and polysilicon for planar double gate MOS fabrication

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Abstract

The constant increases of the microelectronic devices performances forces the engineer to scale down continuously the transistors size to produce chips with larger calculation capacity.

Scaling down the size of the MOS transistors faces technological problems, like the smallest dimension that optical lithography can achieved but also physical limitations. The use of new materials such as high-k dielectrics, SOI substrates and metallic gates or slight modifications to the transistor structure like like spacers and complex source and drain design are ways to counterbalance the problems arising with miniaturization. However the largest improvement in transistor performances is made by changing its architecture.

The FinFET architecture allows a better electrostatic control of the channel thanks to the use of two gates. However this architecture requires a multi fingers structure for the transistors as the W of a single finger is limited by the silicon film thickness. To get ride of the multi fingers architecture, which is a source of parasitic capacitances, planar double gates architecture has been proposed. However, this solution induces complex process flow to achieve the fabrication of planar double gate MOS. The alignment of the front and back gate is a critical issue which has been solved by some research groups but the respective size of the two gates remains an issue to be solved.

We proposed in this work three process flows based on the use of buried mask which could allow the fabrication of the front and back gate self-aligned and with the same size.

The novel concept of buried mask consists into modifying the etch rate of a buried polysilicon or oxide layer. This etch rate modification being defined by ion implantation, etch stop or scacrificial zones aligned with the implantation mask can thus be fabricated. This technique solve the alignment of the front and back gate.

Ion implantation causes damages to the implanted target, and is used to dope semiconductor material. If the implanted atoms have a small radii they can induce stress to the implanted lattice. These three consequences of ion implantation, damage, doping and stress are used to modify the etch rate of oxide and polysilicon. High etching selectivity are reached, which allow the fabrication of a localized buried

sacrificial or etch stop zone, called buried mask. The definition of the buried mask being done by ion implantation, it opens the possibility to fabricate a buried mask aligned with the implantation mask.

This concept of buried mask, which could also be called anisotropic wet and vapor etching, is foreseen as a very promising technique in MEMS micromachining and for bio sensor applications.

Scientific Publications

R. Charavel and J.P. Raskin, "Tuning of etching rate by implantation: silicon, polysilicon and oxide", *Proceedings of IIT 2006*, Marseille, 4 p., May 2006

R. Charavel and J.P. Raskin, "Buried Mask Revelation in Silicon Dioxide for Double Gate MOS Fabrication", *IEEE NTC Review on Advances of Micro, Nano, and Molecular Systems*, 5 p., May 2006

R. Charavel and J.-P. Raskin, "Underetch reduction by highly selective etching of oxide", *Proceedings of IEEE-NEMS 2006*, 2 p., May 2006

R. Charavel and J.-P. Raskin, "Etch Rate Modification of SiO₂ by Ion Damage", *Electrochemical Solid-State Letters*, vol. 9, pp. G245-248, 2006

R. Charavel and J.-P. Raskin, "Self-alignment method by buried mask implantation for double gate MOS and nanodevices fabrication", *Proceedings SPIE*, Vol. 5592, pp. 362-372, Jan 2005

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R. Charavel and J.-P. Raskin, "Fabrication of self aligned double gate MOS transistor", *Union Radio-Scientifique Internationale (U.R.S.I.)*, Royal Military Academy, Brussels, Belgium, 1 p, December 2002.

L.D. Madsen, R. Charavel, J. Birch and E.B. Svedberg, "Assessment of MgO (1 0 0) and (1 1 1) substrate quality by X-ray diffraction ", *Journal of Crystal Growth*, Vol. 209, n° 1, pp. 91-101, January 2000.

J.-P. Raskin, R. Charavel, patent application n° L3642-EP, Etch of implanted oxide in VHF, self-aligned DG MOS and release MEMS

List of Abbreviations

amu	Atomic mass unit
BHF	Buffered HF
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
DELTA	DEpleted Lean channel TrAnsistor
DIBL	Drain Induced Barrier Lowering
ELO	Epitaxial Lateral Overgrow
FinFET	Fin Fiel Effect Transistor
GAA	Gate All Around
HDD	Highly Doped Drain
HF	Hydrofluoric acid
HNA	HF / HNO ₃ / CH ₃ COOH
ITRS	International Technology Roadmap for Semiconductors
LDD	Lowly Doped Drain
MILC	Metal Induced Lateral Recrystallization
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapor Deposition
RCSE	Reverse Short Channel Effect
RIE	Reactive Ion Etching
SOI	Silicon On Insulator
SON	Silicon On Nothing
TMAH	Tetra Methyl Ammonium Hydroxide
VHF	Vapor HF

Introduction

Micro and nano technologies are present in most of the aspect of our lives. At work, applications such as computers, cash registers, or even radiology equipment contain micro-electronic devices. In our daily life, microelectronic devices take also a large part which does not stop growing. From mobile phone to GPS and DVD player, the diversity and the constant novelty of the offers succeed to sustain and increase the demand for more microelectronics applications. The microelectronics applications gained during the last 40 years a large place in technological and industrial domains but also, by their weight, in the world market. In 2004, a global estimation of the turn-over generated by the semi-conductor market was 200 billions of US \$. A growth of 11 % is expected for 2007 [1]. The market leaders of microelectronics are Intel, Samsung and Texas Instruments. The European market is dominated by ST Microelectronics and Infineon.

The MOSFET (Metal-Oxide-Field-Effect-Transistor) is the basic element of all the microelectronic devices. All types of microelectronic applications contain transistors. Since the sixties, the performances of the microelectronic device drastically improved at an exponential rate, the number of transistors per chip area being doubled every 18 months. This increase of the integration density and of the transistors performances is possible thanks to the size shrinking of the transistors. The parameter which is commonly used to differentiate one technology generation from the following is the transistor gate length. Intel has just started this year the production of transistors with a gate length of 35 nm [2]. The ITRS roadmap predicts that the transistor gate length will be scaled down to 9 nm in 2016 [3]. Scaling down the transistor size to such dimensions faces technological challenges, and physical limits. The question of the size limit for the gate length of conventional MOSFET is still open. The technological problems induced by the size downscaling have been until now solved by the use and development of new materials and substrates. High- κ dielectrics, metallic gates, SOI substrates have successfully been introduced to the fabrication process. However, further downscaling of the MOSFET cannot rely only on the choice of new materials. The transistor architecture must also evolve.

Multi-gate transistors are foreseen as promising solutions for the next technological generation with gate length below 25 nm. In single gate transistors, the channel is controlled by the gate, on top of the silicon active film. The thickness of the conduction channel in the silicon is on the order of a few nm. The whole silicon thickness below the channel is useless for the electrostatic control of the channel. The idea of multigate transistor is that the channel could be controlled by more than one side. The first proposed multigate transistors were made of a vertical thin silicon film on which the gate was deposited on its sidewalls. A number of research groups showed a lot of creativity in finding new process solutions for multiple gate devices, with vertical gates or planar gates. All these proposed architectures face complicated process flows which makes the downscaling of the devices complicated or limit the performances due to parasitics induced by the chosen architecture. For example the multi gates transistor must adopt multi fingers architecture in order to tune the W/L ratio, when the planar double gate architecture must solve the alignment of the front and back gate. The self-aligned planar double gate that has been already fabricated had either the source and drain or the channel silicon that were regrown by epitaxy or recrystallization.

In this context, the starting idea of this work was to fabricate self-aligned planar double gate MOS solving the main challenges that faced previous published work. We thus proposed new process flows in which the self-alignment and the respective size of the two gate was solved. Our processes preserved also the integrity of the active silicon film. The new concept common to all of our processes is the use of a buried mask. This technique is used to align a top structure with a buried structure. The buried mask were formed by modifying the etch rate of silicon or oxide by ion implantation to create buried sacrificial or etch stop zones. The etch rate modification and buried mask revelation is the main achievement of this thesis. Unfortunately, no double gate transistors were achieved but new research fields were opened thanks to the development of the buried mask.

The first Chapter of this thesis makes an extensive review of the proposed solutions for multigate transistors. FinFETs, Ω - and Π -gates and gate all around transistors solve the self-alignment issue of the two gates but necessitate a multi-

finger architecture. The planar multigate architecture gets rid of the multifinger structure and can achieve any W/L ratio with a single finger transistor. However in this case the alignment of the front and back gate is a critical issue. Some groups solved this problem by building the source and drains and regrowing the channel silicon film afterward or by defining the gates stack and regrowing the source and drain areas once the gates have been processed. We proposed three processes for self-aligned double gate transistor fabrication where neither the source and drain or the silicon channel are regrown. Our solutions are based on the revelation of buried mask defined by ion implantation and thin film reports by wafer bonding and grinding for two of them.

The second chapter is the core of this work. Our novel processes are all based on the revelation of buried mask defined by ion implantation. The etch rate modification of oxide and polysilicon by ion implantation is intensively studied, from the physics of ion implantation to chemical reaction of the etching. Selective etching of implanted oxide in VHF is due to the highest reactivity of the damaged oxide by implantation and to the autocatalytic behavior of the oxide etching in HF. Selective etching of boron doped polysilicon in TMAH is due to the tensile stress induced by the smaller boron atoms presents in the silicon lattice which stops the reaction between silicon and TMAH. The selective etching of doped polysilicon in HNA is attributed to the presence of the free carriers which enhances the reactivity of the silicon in HNA.

The third chapter characterizes the revelation of buried mask, which is the critical step of our process proposal for self-aligned double gate fabrication, using the etch rate modification of oxide and polysilicon by ion implantation. Parameters such as maximal dimensions of the cavities revealed in implanted oxide, overetch of positive and negative buried mask in polysilicon, surface roughness of the sidewall of the revealed structures are investigated. Conclusions about the feasibility of the self-aligned double gate transistors are drawn.

The fourth chapter proposes a wide variety of applications using the buried mask concept on which research has to be performed.

The appendix describe the characterization of some of the critical process steps used in these fabrication processes. Wafer bonding of recrystallized Si- α used for

the fabrication of the starting wafers is demonstrated. PECVD oxides in which the back gate is embedded before bonding and film report is characterized, mechanically and electrically. RIE recipes are developed for selective etching of silicon and oxide.

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CHAPTER 1

NEW PLANAR DOUBLE GATE MOSFET

The first part of this Chapter reviews the evolution of the multiple gates transistors toward the planar double gate transistors. The process flows of the different types of DG MOS that have already been fabricated are described and their weaknesses or advantages are pointed out. Self-aligned planar DG MOS fabrication processes from literature are then compared with three new fabrication methods that we propose.

1.1 Evolution of the multiple gates MOSFETs

1.1.1 Introduction

Over the last 40 years there has been an enormous growth in the semiconductor and consumer electronic industry, much of it fueled by the evolution of the planar silicon MOSFET-based integrated circuit. During this time, critical dimensions (gate length typically) have decreased by a factor of roughly 100 whether the number of transistors per chip area was multiplied by more than 100 000 000. The evolution rate of the chip capacitances followed the Moore's law, which states that the number of transistors per chip area doubles every 18 month. This drastic increase of the number of transistors per chip area thanks to transistor size reduction was made possible thanks to the improvement of the MOSFET technology like self-aligned source and drains, silicidation to reduce the source and drain resistance, use of spacers and pocket implants to reduce the influence of the source and drain in the channel, multi-level interconnects, high-k dielectrics, metal gate, etc... Due to the actual dimensions of the transistors, the physical limits of the transistor size will be reached if the effort is only concentrated on improving parameters such as gate material, gate dielectrics, source and drain resistance. To push further down the miniaturization of transistors new MOS architectures have to be developed. The ITRS roadmap (Fig. 1.1) foresees that multiple gate transistors are very attractive

options for the 45 nm node and beyond [1].

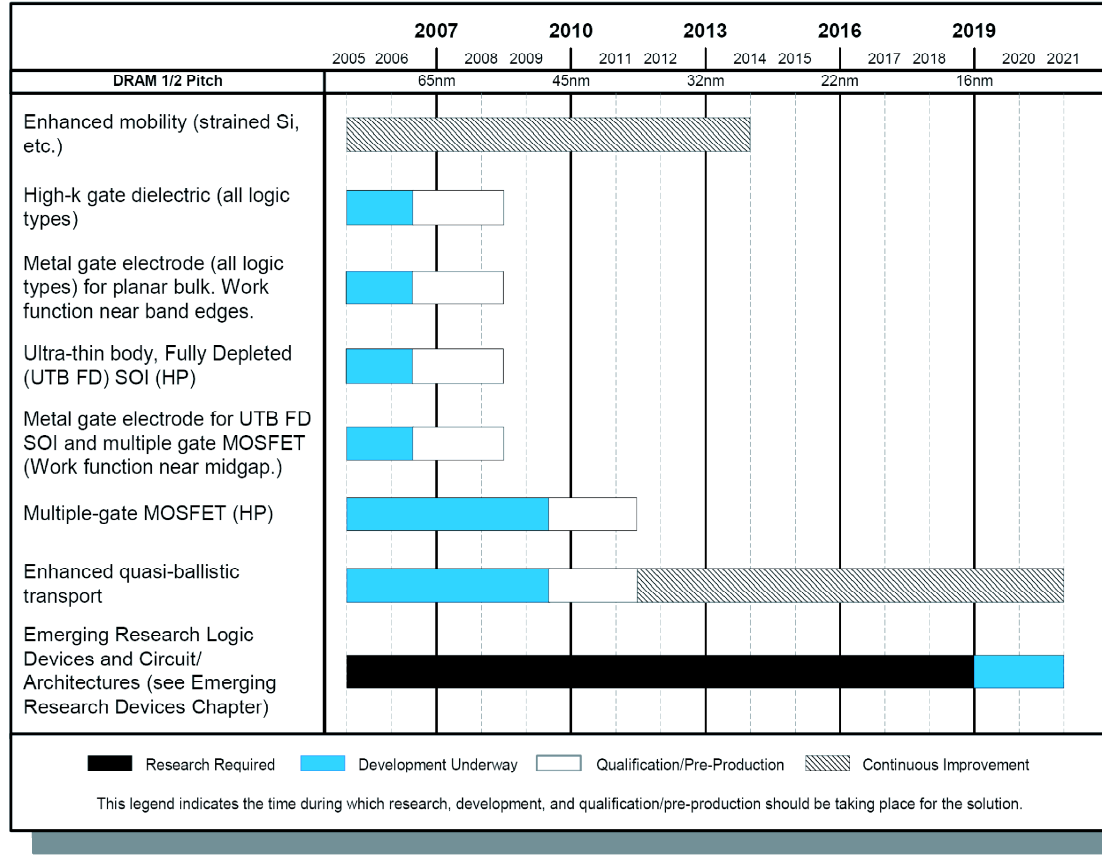


Figure 1.1: New architectures proposed to follow the miniaturization trend of microelectronics [1].

The next Section details the evolution of the MOSFET performances made possible by the use of advanced materials.

1.1.2 Material based improvement

Reducing the transistors size induces new types of defects for which technological solutions have to be found. The gate length reduction is responsible for the so-called Short Channel Effects (SCE), which is a loss of electrostatic control of the channel from the gate. As the channel dimension gets smaller, the electrostatic influence of the source and drain areas on the channel cannot be neglected any more in front of the gate electric field. This effect is called the Charge Sharing Effect (CSE) and is responsible for the lowering of the potential barrier between the source and drain. The barrier potential can also be affected by the potential of the drain, which is called Drain Induced Barrier Lowering (DIBL). The DIBL and CSE contribute

to threshold voltage diminution when decreasing the gate length of the transistor and varying the drain potential. The combination of CSE and DIBL, which are denominated as SCE causes the threshold voltage to drop when decreasing the gate length. A Reverse Short Channel Effect (RSCE) which is an unexpected increase of the threshold voltage when decreasing the gate length is also observed for gate length slightly larger than the one at which arise the SCE (Fig. 1.2).

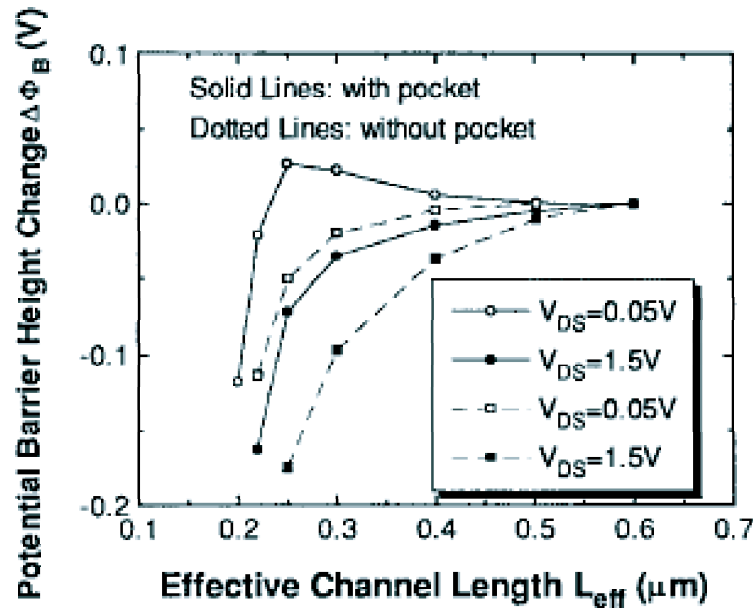


Figure 1.2: Example of short channel effect. The potential barrier between source and drain decreases with gate length [2].

The RSCE is caused by dopant pile-up at the gate oxide / silicon interface [3]. The first technological paradigms that have been found to minimize SCE and RSCE were based on new architectures of the source and drain regions. Highly doped zones, called pockets were thus implanted on the source and drain extensions to limit the source and drain influence in the channel [4]. The Source and drain architecture was later improved by halo implantation under the pocket to avoid the formation of a buried conduction channel non controlled by the gate [5].

Further increase of the transistor performance was done by reducing the parasitic capacitances between the source and drain areas and the channel. The thickness of the X_j junctions and their lateral diffusion has therefore to be reduced. The implantation of source and drain extensions is done in two steps which consist in a shallow and low dose implantation close to the channel area called the Low Doped Drain

(LDD) and a highly doped zone in the source and drain contact areas called the Highly Doped Drain (HDD) [6],[7]. Another amelioration of the transistor performances is brought by the reduction of the source and drain resistance by silicidation of the contact areas [8]. Fig. 1.3 shows a schematic of the source and drain engineering of the classical MOSFETs.

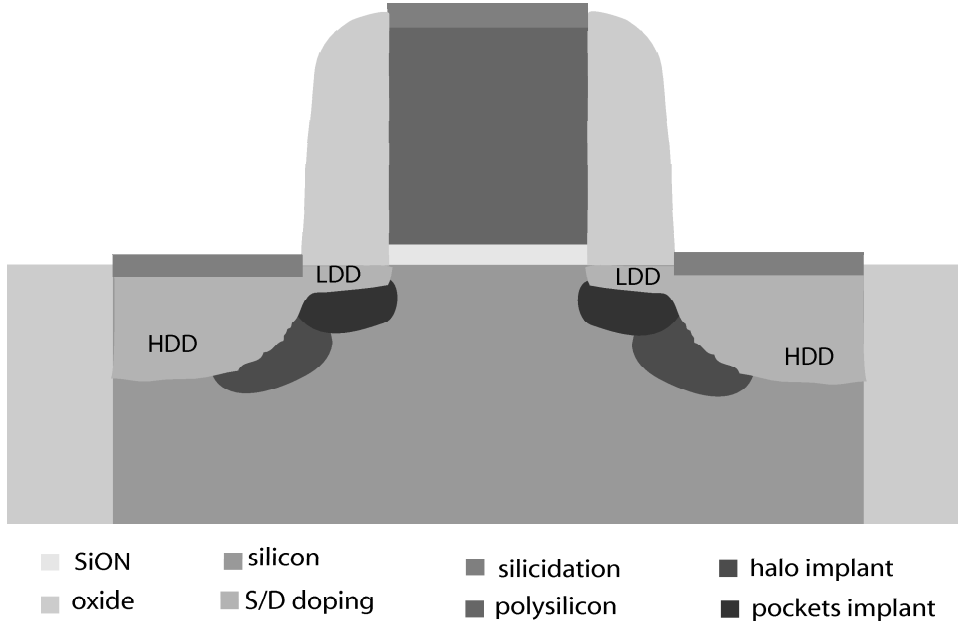


Figure 1.3: Schematic of the state of the art MOSFET on silicon bulk substrate.

The source and drain engineering is not the only way to increase the MOSFET performances. Amelioration of the mobility of the channels free carriers is also a solution which is achieved by inducing a compressive stress of the channel material in the transport direction. It is done by depositing tensile nitride on the source and drain areas and on the gate or by growing by epitaxy the source and drain areas in SiGe [9],[10].

The parasitic capacitances which are responsible for performance degradation at high frequencies are strongly reduced by the use of Silicon on Insulator (SOI) wafers. Nowadays the thin SOI wafers are used with a SOI film thickness ranging between 20 and 50 nm. It allows the fabrication of fully depleted MOSFETs.

Strong efforts have also been invested into developing new gate dielectrics. Indeed, the ITRS roadmap forecasts a constant diminution of the gate dielectric. In order to reduce the gate tunneling current that would be unavoidable for too thin silicon dioxide, high-k gate dielectrics are investigated. Their higher permittivity

allows the use of thicker dielectrics which reduces the gate leakage current [11].

Research is also done to replace the gate material in order to reduce the gate resistance which increases as the gate size decreases. Metallic gates in W, NiSi, NiGe are promising solutions to reduce the gate resistance but also the threshold voltage pinning [12],[13].

Despite the strong efforts put into ameliorating the common planar bulk MOSFET by this innovative source and drain engineering and the use of materials with better physical properties, the performances achieved for the state of the art bulk planar MOSFET is far below the trend that the ITRS expects (Fig. 1.4).

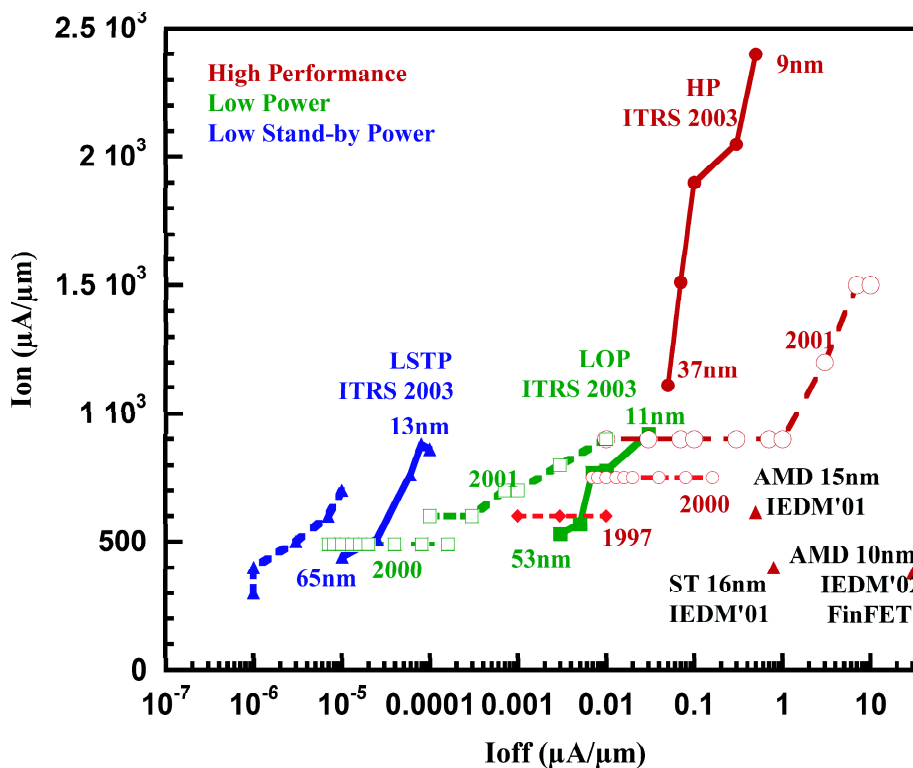


Figure 1.4: ITRS I_{on} - I_{off} targets compared with the state of the art transistors [14].

Solutions must then be found to allow further downscaling of the transistor size but with maintaining a good control of the channel area by the gate. New MOSFET devices with multiple gates are seen as good candidates to fulfill the drastic requirements in terms of performances for the future device generations. The next Sections deal with the different types of multiples gate transistors that have already been developed.

1.1.3 Early architecture based improvement

The first fabricated multiple gate MOS can be decomposed into tow categories: the vertical double gate transistors and the multiple gate transistors.

1.1.3.1 Vertical Double gate transistors

- *Depleted Lean Channel Transistor (DELTA)*

The first double gate architecture (Fig. 1.5) proposed by Hisamoto in 1989 was based on a vertical architecture, with a current flow in the horizontal direction [15],[16]. A RIE step into the bulk silicon defines the active area thanks to a nitride mask. The active area is a silicon beam from which the height corresponds to the transistor width, the length to the active area length and the width to the thickness of the future channel transistor. The active area is then isolated from the bulk silicon by a thick oxidation which extends below the active area. The gate oxidation, deposition and patterning is realized after nitride removal.

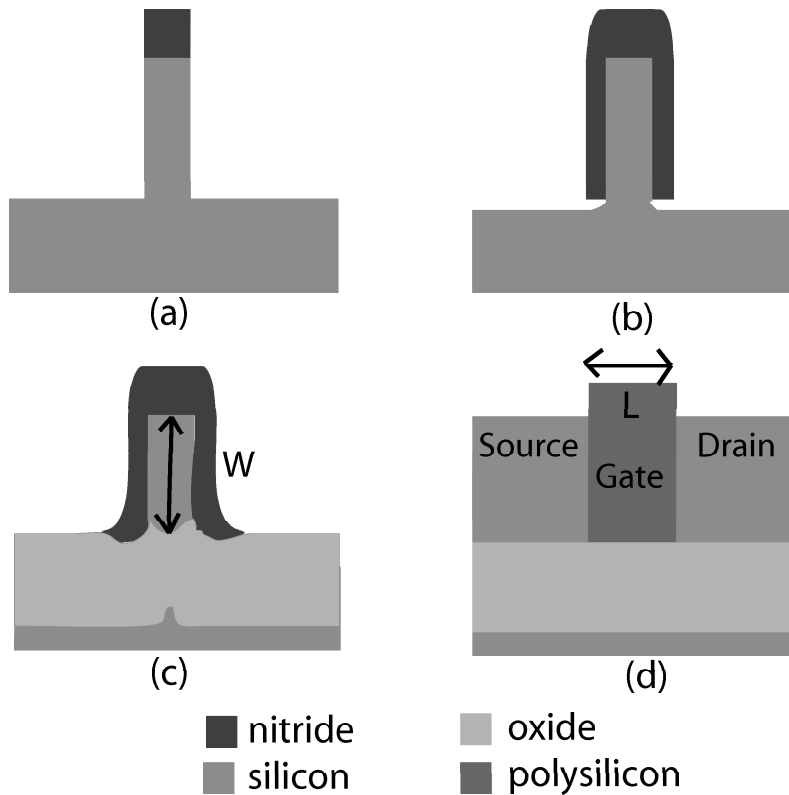


Figure 1.5: Process flow of the DELTA MOSFET. (a) Definition of the channel by RIE. (b) Nitride spacer capping. (c) Oxidation to form the buried oxide film. (d) Polysilicon gate deposition (longitudinal view). [17].

The DELTA transistors offered at that time better behavior with respect to short channel effect and gate transconductance than conventional single gate MOSFET built in bulk technology and even in SOI technology. The gate length and the channel thickness were respectively 570 nm and 150 nm due to the limitation of the lithography at that time [18].

- *FinFET*

A direct improvement to the DELTA technique was made possible thanks to the better reliability of SOI substrates. In 1999 Hu [19] proposed the first FinFET. The structure is identical to the DELTA structure apart that the oxide buried below the silicon Fin is not grown by oxidation but is the BOX from a SOI wafer. A silicon beam, called 'Fin', is done by RIE into the SOI layer. As for the DELTA architecture, the height of the silicon beam is the width of the FinFET transistor and its length is the length of the active area of the FinFET (Fig. 1.6). Once the silicon beam has been defined, the gate oxide and the source and drain areas are processed in the same way as the DELTA process.

As the width of the transistor is limited by the silicon film thickness (t_{Si}), the Fins are put in parallel (multi finger transistor) to increase the width of the device [20]. A small Fin width which means a thin channel, induces that the transistor will be able to be fully depleted and will not suffer of floating body effect. The smallest dimensions achieved for the FinFET was made by Yu *et al.* [21]. A gate length of 10 nm was achieved for a channel thickness of only 12 nm and a Fin height (h_{Si}) of roughly 35 nm. For such dimensions, the Fin height is not limited by the SOI film thickness but by the shape factor that is achievable by RIE. Some groups have therefore done the Fin definition by TMAH etching [22],[23]. In addition to the fact that they achieve perfectly rectangular shape of the Fin, the Fin surfaces are in the (111) plane, which is an etch stop plan for TMAH etching, and in which the hole mobility is higher than in the (100) plane commonly used in MOSFET fabrication [24],[25]. These structures are of interest for pMOS devices.

FinFETs with independent gates have also been fabricated [26].

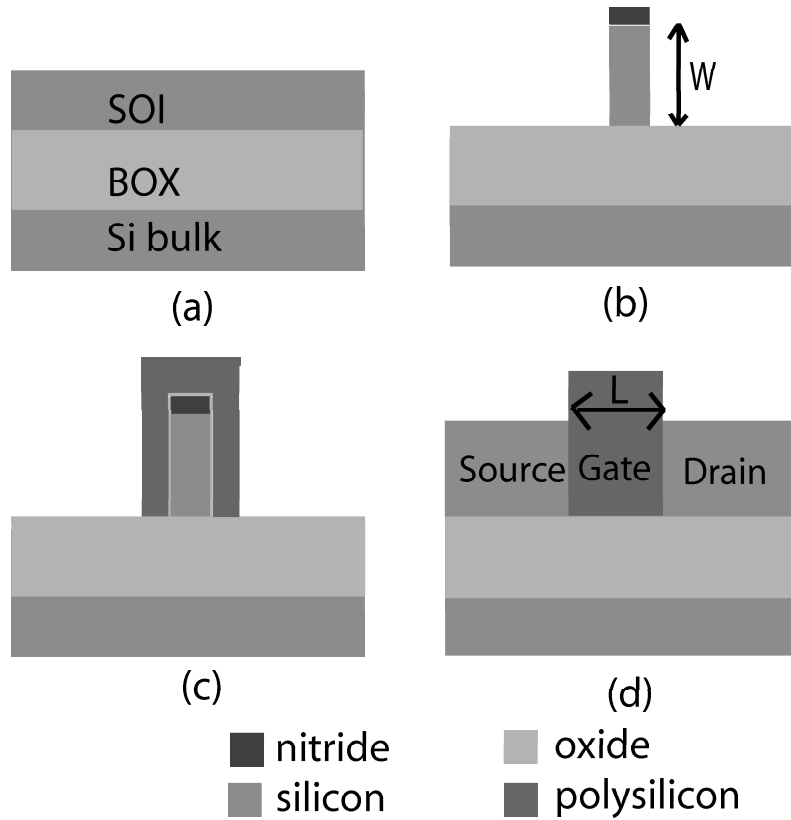


Figure 1.6: Process flow of the FinFET. (a) SOI starting wafer. (b) Fin definition by RIE. (c) Lateral cross section of the FinFET. (d) Longitudinal view of the FinFET.

1.1.3.2 Multiple gates transistors

The ratio between h_{Si} and t_{Si} differentiates Tri-gates transistors from FinFETs. When t_{Si} equals h_{Si} , the electrostatic control from the gate on the channel is increased and the device is called a Tri-gates. Dixit *et al.* [27] showed that Tri-gates devices have a better $1/f$ noise at low frequency. In the case of Tri-gate transistors, the transistor conduction width, usually called W is here equal to $(2 \cdot h_{Si} + t_{Si})$. Raskin *et al.* [28] showed that for FinFET with lower W/L ratio, the parasitic capacitances were reduced, which means that for short gates transistors the Tri-Gate architecture would be source of less parasitic capacitances and would therefore increase the cut-off frequency of the devices. Structures have already been fabricated with a gate length of 20 nm and a silicon fin thickness t_{Si} of 8.5 nm [29]

As the control of the silicon channel on three sides on the silicon beam thanks to the Tri-Gates transistors showed good results, Π - and Ω -Gates transistors were designed and showed even better performances than the Tri-Gates transistors. The Π -Gate architecture is like the Tri-gate architecture with extended gates in the

buried oxide on the both side of the device [30],[31]. The extended gates allow a better control of the channel, expanding the electrostatic control of the gate on the back side of the channel.

The electrostatic control of the channel was improved by extending the buried gate below the channel. The shape of this new structure looking like the Greek letter Ω , the structure was called the Ω -Gate [32], [33],[34]. In this structure the gate control tends to the one of the Gate All Around structure that will be described later.

Pushing further the miniaturization, beam in form of a wire were developed to give the Nano-Wire FinFETs. The silicon beam had a diameter of 10 nm and the gate length achieved was 5 nm [35].

Fig.1.7 shows schematics of the Tri-gate, Π -Gate, Ω -Gate and Nano-Wire FinFET transistors. All these architectures are derived from the FinFET structure.

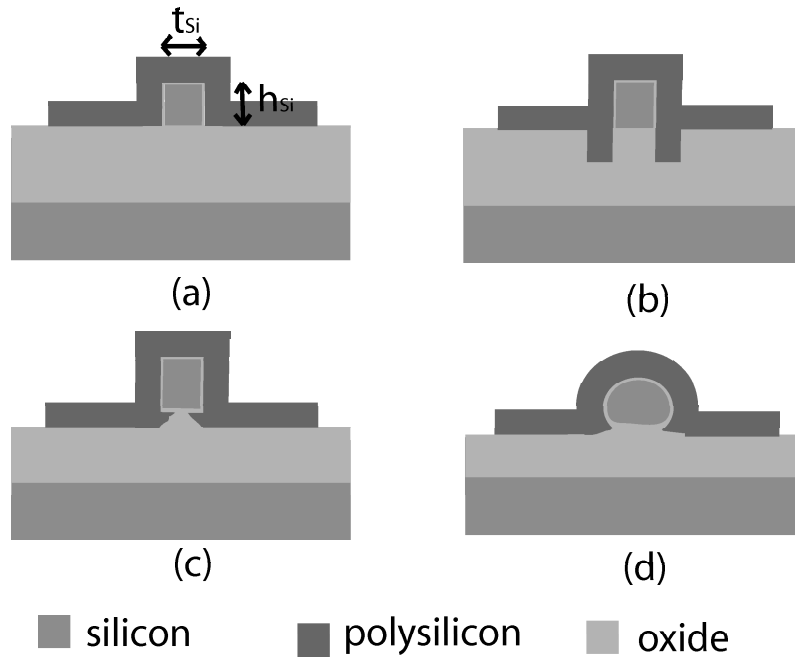


Figure 1.7: Cross section of (a) Tri-Gate . (b) Π -Gate (c) Ω -Gate (d) Nano-Wire FinFET transistors.

Their advantages and disadvantages will be discussed in the following section.

1.1.3.3 Pros and cons of Vertical DG and MG FETs

The advantage of the FinFET, Tri-Gates, Π -Gate, Ω -Gate and Nano-Wire FinFET transistors is that no alignment, film report or silicon regrowth is required during

the process flow, which makes it simple compared to other DG MOS architectures. As the hole mobility is higher in the (111) plane than in the commonly used (100) plane, the performances of pMOS transistors can be enhanced. Despite the good performances of these transistors compare to single gate planar devices, the W/L ratio of a transistor cannot be varied so easily. Indeed, the width of a transistor finger is limited by the silicon film thickness. Multiple fingers transistor must therefore be designed to tune the W/L ratio. The multiple fingers architecture is source of parasitic capacitances. Decreasing the parasitic capacitance by increasing the pitch between the fingers would decrease the total density of current per unit of silicon.

1.1.4 From multiple gates to Planar Double gate MOS - Existing solutions

As seen in the previous Section, the finFET architecture and the derived multi gates architectures are good solutions in terms of fabrication process and electrical performance but an architecture where the W/L ratio of the double gate transistor could be varied without the use of multiple fingers would be useful to reduce further the parasitic capacitances. The planar Double Gate architecture meets this requirement. Number of solutions have been proposed since 1990 for planar Double Gate architectures. The first part of this Section presents the non self-aligned processes, while the second part will present self-aligned structures.

1.1.4.1 Non self-aligned process

- *Gate-All-Around MOSFET*

The first planar Double Gate MOS was realized in 1990 by Colinge [36]. Fig. 1.8 shows a schematic of the GAA architecture. Silicon mesa was defined by RIE on a SIMOX wafer. A cavity was done by wet etching in the oxide below the silicon beam. The free standing silicon membrane was then oxidized to form the gate oxide. The polysilicon gate was deposited by LPCVD and etched by RIE to form the gate. The disadvantage of such a process is that the front and back gate are not perfectly self-aligned and that the front gate is of smaller dimension. The demonstrator build

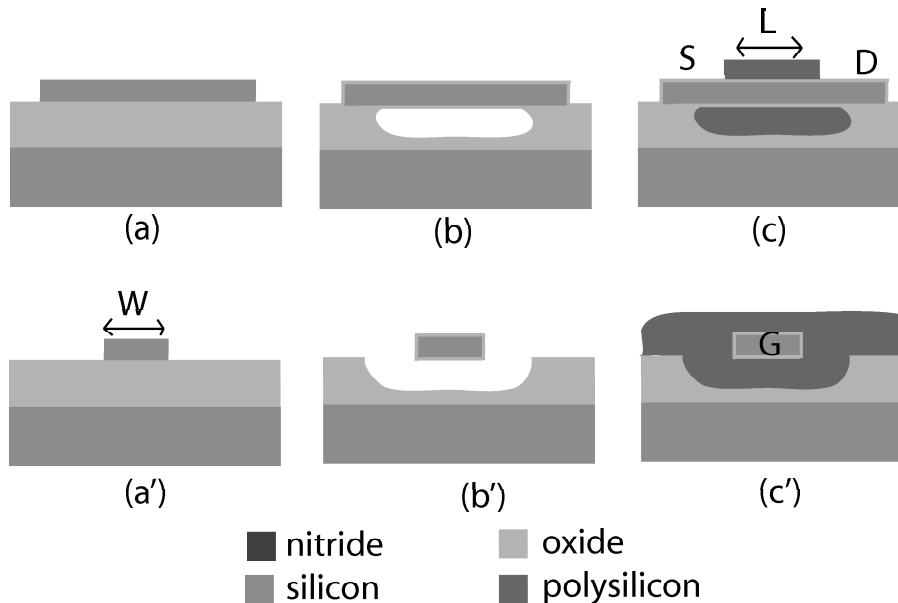


Figure 1.8: Process flow of a the first GAA proposed architecture [36]. (a) definition of the active zone, (b) definition of the back gate cavity by wet etching, gate oxidation, (c) polysilicon gate definition. (x) and (x') are respectively, longitudinal and lateral cross sections.

at that time had a channel length of $3 \mu\text{m}$. Moreover in order to avoid a too large underetch outside of the active area W/L ratio larger than 1 must be avoided.

- *Wafer bonding of pre-patterned cavities*

One of the drawbacks of the previous method was the isotropic etching of the back gate cavity. This inconvenient has been solved by Chung [37]. Cavities are defined in a oxidized bulk wafer by RIE. The top silicon film of a SOI wafer is then reported on the bulk wafer where the cavities have been defined by wafer bonding, grinding and CMP of the bulk from the SOI wafer. Once the silicon film has been transferred, mesa are defined by RIE in the SOI film. The following of the process is likely to the one from Colinge [36] (Fig. 1.9).

Thanks to the possibility to build transistors with large W , the this GAA transistor has a Double-Gate like behavior, the influence of the vertical walls of the gate being negligible. The maximal length of the transistor is however limited by the filling of the back gate cavity during the polysilicon gate deposition. For transistors with a gate length of $2 \mu\text{m}$, the largest width obtained was $20 \mu\text{m}$ [37]. Although the electrical performances reached by this new type of GAA are comparable with the classical Double-Gate and the fact that it offers a better definition of the back

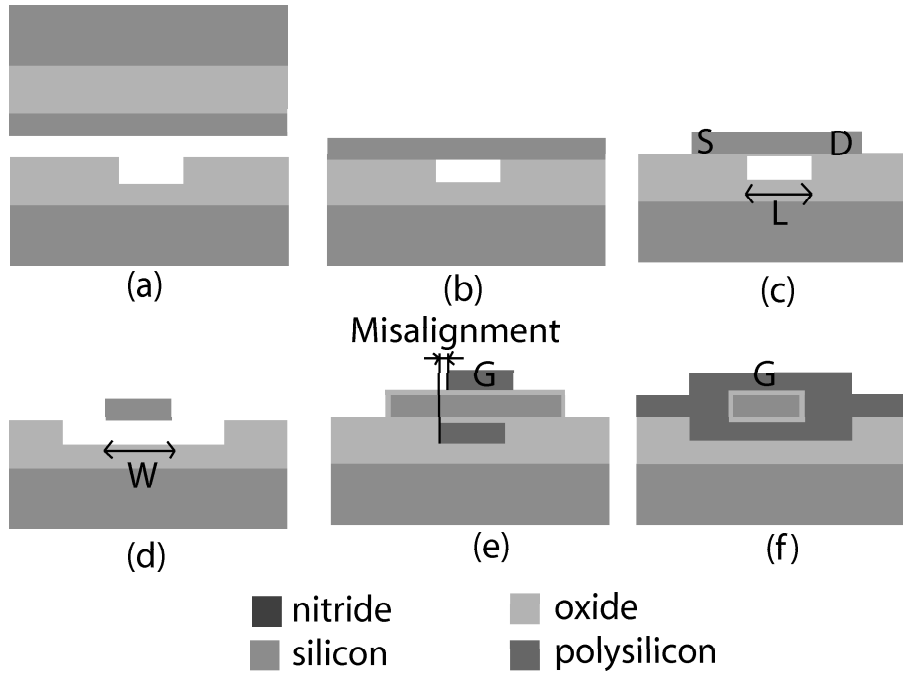


Figure 1.9: Process flow of the planar GAA fabricated by wafer bonding over pre-patterned cavities. (a) wafer bonding, (b) flip, grinding and CMP, definition of the mesa (c) longitudinal cross section, (d) lateral cross section, gate oxidation and polysilicon gate fabrication (e) longitudinal cross section, (f) lateral cross section. [37].

gate as the process from Colinge [36], this technique does not solve the systematic misalignment between the front gate and the back gate cavity, which was in this case made by optical lithography. It is furthermore impossible to connect the front and back gate separately.

- *Wafer bonding of the encapsulated back gate*

The LETI proposed another method for fabricating non self-aligned Double Gate MOS with independent back and front gate. Their process is also based on film report. Fig. 1.10 describes the process of the LETI non self-aligned Double Gate MOS [38].

The back gate is processed on a SOI wafer and embedded in PECVD oxide. A CMP planarizes the PECVD oxide which allows the bonding on an handle wafer. The silicon bulk and the buried oxide from the starting wafer is removed by grinding and CMP. Once the SOI film is reached, the stack for the back gate is deposited as follows: 2 nm gate oxide, 10 nm TiN by CVD and 50 nm in situ doped polysilicon. The alignment mark were processed before bonding and regenerated after substrate

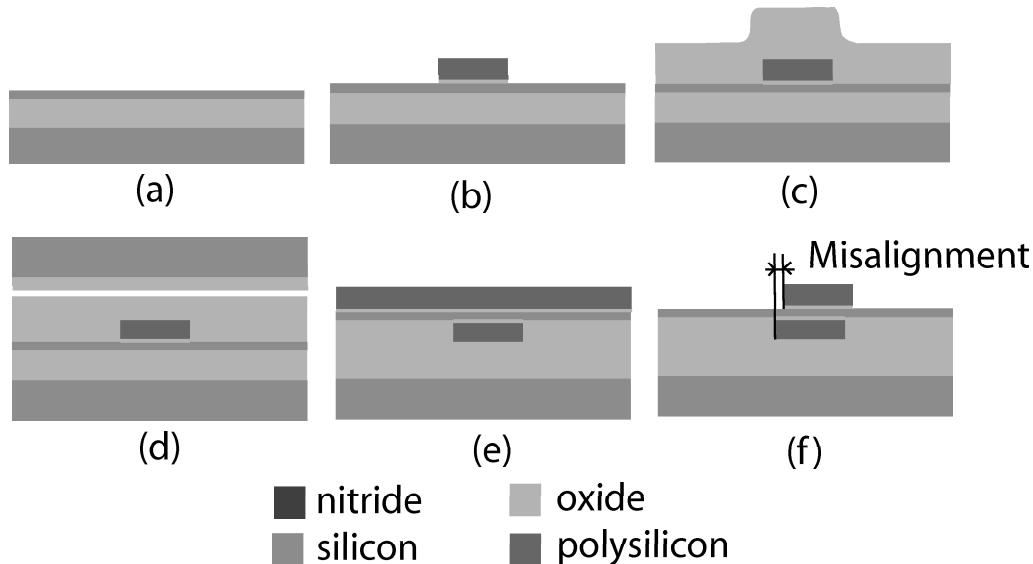


Figure 1.10: Process flow of the planar DG fabricated by wafer bonding over pre-fabricated back gate. (a) starting SOI wafer, (b) back gate processing (c) oxide deposition, (d) CMP and bonding to a handle wafer (e) front gate stack deposition, (f) front gate patterning. [39].

removal [40]. The relative misalignment is thus limited to the e-beam precision which is presently 7 nm [41]. After the front gate definition, the process ends up classically: extensions implantation, spacers formation, raised source/drain epitaxy and implantation and finally salicidation [42]. As the back gate is fabricated before bonding, there is no problem of maximal W/L ratio for the back gate. Any dimension can be chosen. Widiez *et al.* [40] fabricated perfectly aligned 40 nm double gate transistors thanks to a on-mask vernier, and the use of larger back gates. Although this was the first step toward the 10 nm transistors that they fabricated later [41], this process solution provides good Double-Gate demonstrators in the 10 nm range but is difficult to transfer to mass production.

- *Lateral Epitaxy Overgrow*

A process flow for non self-aligned planar Double-Gate without wafer bonding was proposed by Denton et al. [43]. A cavity is realized in a bulk silicon wafer and is then oxidized. The back gate is deposited in this cavity. The gate oxide is deposited and the channel is grown by epitaxy thanks to a seed in the substrate. The front gate is then realized after the gate oxide deposition. Fig. 1.11 shows a schematic of the process flow called Epitaxy Lateral Overgrow (ELO).

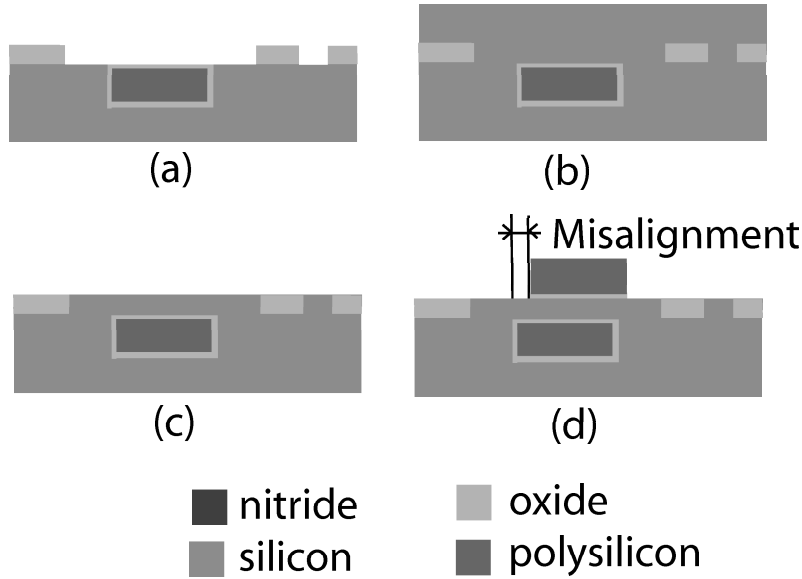


Figure 1.11: Process flow of the planar DG fabricated by Lateral Overgrow Epitaxy. (a) the back gate is formed into the bulk and oxide defines the active area and an epitaxy seed, (b) silicon channel epitaxy, (c) CMP, (d) front gate formation. [43].

The drawback of this process is the poor quality of the channel silicon and the misalignment of the front and back gate inherent to lithography. No short channel transistors were demonstrated with this architecture, the smallest structure having a gate length of $2\ \mu\text{m}$.

- *Silicon on Nothing*

Harrison *et al.* [44] proposed also an architecture based on epitaxy of the channel called the Silicon On Nothing (SON) technology. The active area is delimited by two Shallow Trench Isolation (STI). SiGe is then grown by epitaxy in the active area. The silicon channel is grown by epitaxy starting from the SiGe layer until the STI. The SiGe is then removed by isotropic etching leading a cavity below the epitaxied silicon film. The gate oxide is formed and the polysilicon gate is deposited by LPCVD. The front gate and source and drain areas are then formed by lithography. In this process the front gate is unfortunately not aligned with the back gate (Fig. 1.12) and does not have the same size.

Devices with a gate length of 40 nm and a silicon film thickness of 15 nm were fabricated [44].

- *Metal Induced Lateral Overgrow*

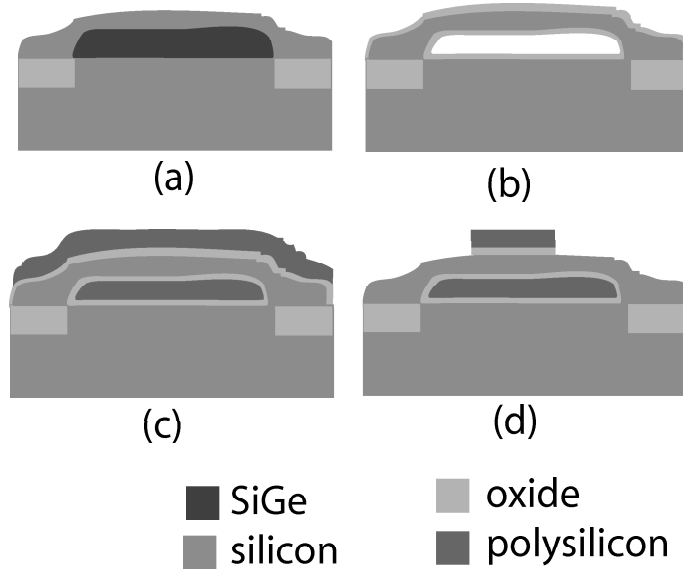


Figure 1.12: Process flow of the planar DG fabricated by SON method. (a) STI formation, epitaxy of SiGe and silicon channel, (b) sacrificial SiGe removal and gate oxidation, (c) Polysilicon deposition, (d) front gate formation [44].

Chan *et al.* proposed a process similar to the SON technology [45]. The architecture uses also a suspended membrane for the channel. The differences are that the sacrificial layer is made of nitride instead of SiGe and that the active film is polysilicon instead of epitaxied silicon. The recrystallization of the channel is done by the use of metallic seeds (Nickel) in the source and drain areas. This Metal Induced Lateral reCrystallization (MILC) yields polysilicon films with electrical properties close to the one of crystalline silicon [46]. Here also the main drawbacks of this technique are the misalignment of the front and back gates and the metallic contamination [47]. The gate length achieved for this process proposal was 550 nm.

- *Lateral Solid Phase Epitaxy*

Liu *et al.* proposed also a solution based on the recrystallization of an amorphous silicon film where they avoided the metallic contamination [48]. Their process is based on Lateral Solid Phase Epitaxy (LPSE) (Fig. 1.13).

A cavity defining the back gate is formed in the silicon film and the BOX of an SOI wafer. Sacrificial Low Temperature Oxide LTO is deposited and polished by CMP. The oxide in the trench serves as dummy gate. Amorphous silicon is then deposited and recrystallized by annealing. A single sided Si and Ge implantation is used to avoid twin boundary in the middle of the channel and to enhance the lateral

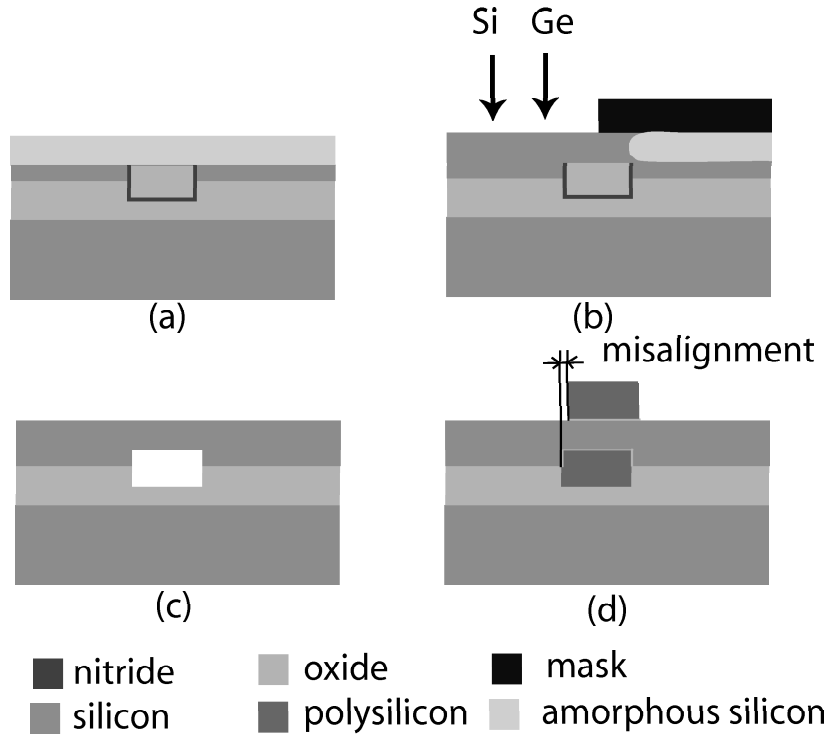


Figure 1.13: Process flow of the planar DG fabricated by LPSE method. (a) Formation of a cavity in the SOI and BOX, LTO filling, Si- α deposition, (b) recrystallization thanks to Si and Ge implantation, (c) dummy gate removal, (d) gate oxidation, polysilicon deposition and front gate formation. [49].

crystallization. Once the channel is grown the active area is defined by RIE, the sacrificial dummy gate is etched away, the gate oxide is grown, and the polysilicon gate is deposited. The front gate and source and drain area are then processed. Despite the simplicity of this process and the correct devices properties this method suffers also from misalignment from the front and back gates [49]. The shortest gate achieved was 510 long.

Although all of these processes demonstrate the good performances of the planar double gate MOS none of them is self-aligned. It is not a critical issue for demonstrators with transistor gate length of a few hundreds of nanometers. However, the Double-Gate transistor is foreseen to take over the standard technology at the 32 nm node. At this size range, the misalignment of the front and back gate will be a critical issue. The alignment accuracy of the state of the art deep-UV lithography machine will not be negligible any more compare to the size order of the gate length. For example a deep-UV scanner with a resolution of 65 nm has an alignment accuracy of 8 nm when for 45 nm resolution this accuracy is 7 nm [50], [51].

Despite the very good technological performance, the alignment accuracy is roughly 15% of the resolution and this ratio tends to increase as far as the resolution is scaled down. For such misalignment of the top and bottom gates, the transistor performance would be strongly affected [52],[53],[54],[55],[56]. Methods for aligning the top and bottom gates other than through lithography are therefore required to conserve the physical advantages of double gate over single gate. The following section presents the process flows of self-aligned planar double gate MOSFETs.

1.1.4.2 Self-aligned Process by regrow of the source and drain or of the silicon channel

The previous Section showed that crystalline silicon could be grown by epitaxy or crystallized from amorphous silicon by germination on metallic seed or crystalline silicon. Using this property, self-alignment of double gate transistors is made possible by regrowth of the silicon channel after the processing of the source and drain areas or by regrowth of the source and drain areas after processing of the gates and channel stack.

Recrystallization of the silicon film

- *Metal Induced Lateral Recrystallization*

Zhang *et al.* proposed a process (Fig. 1.14) for a Self-Aligned Electrically Separable Double-Gate (SA ESDG) MOS in which the channel and source and drain areas are regrown [57].

A bulk silicon wafer is oxidized and the back gate stack is deposited (polysilicon and gate oxide) and covered by nitride. The back gate is then patterned by RIE. The vertical walls of the gate are then oxidized and amorphous silicon is then deposited and planarized by CMP, using the nitride layer as etch-stop. The nitride is then removed to form a shallow trench, which later on will confine the geometry of the front gate, while the remaining amorphous silicon defines the source and drain areas. Amorphous silicon is then deposited to form the future channel. The recrystallization is done through a window in a LTO layer using a nickel seed. Once the

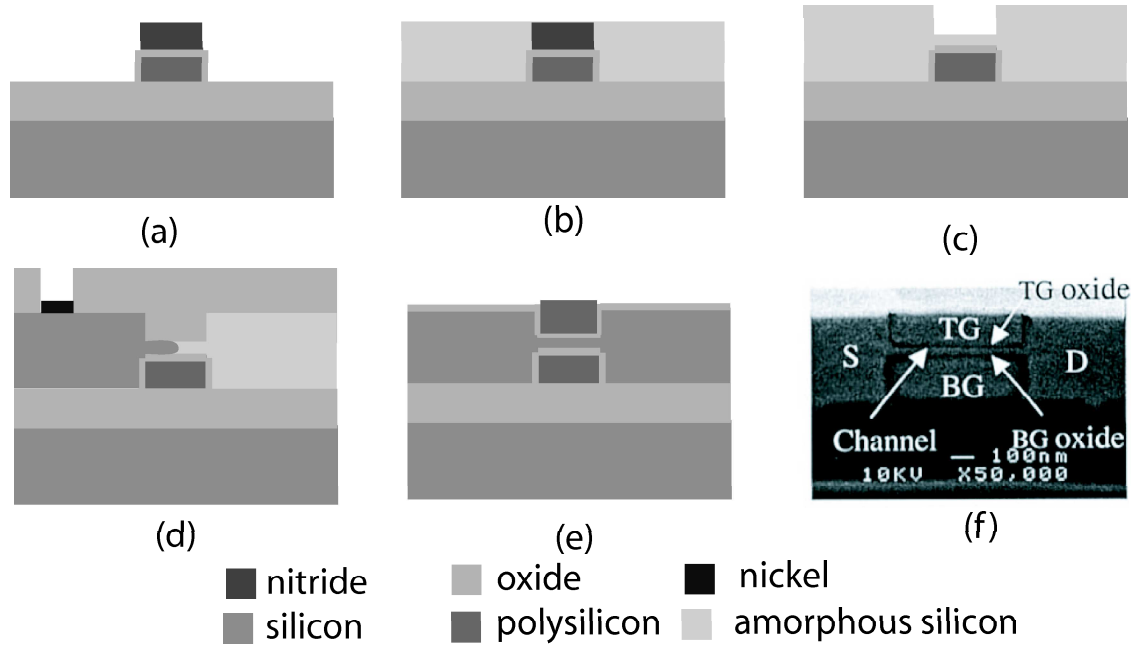


Figure 1.14: Process flow of the SA ESDG MOS. (a) Formation of the back gate on an oxide layer and nitride covering, (b) Si- α deposition and CMP, (c) nitride removal and Si- α deposition, (d) LTO deposition and recrystallization thanks to nickel germination, (e) front gate processing, (f) SEM cross section of a fabricated device [58].

channel has been recrystallized, the front gate is realized in the remaining trench on the surface [58]. The great advantage of this structure is of course its self-alignment. However, the regrown film might not be of very good quality. Furthermore the architecture of the source and drain area might induce large capacitances between source and drain areas and the gate area. The achieved gate length was 350 nm.

- *Tunnel epitaxy*

Wong *et al.* proposed a self-aligned planar double gate architecture also based on the regrowth of the channel and source and drain areas using the bulk silicon as seed for the silicon epitaxy (Fig. 1.15) [59],[60].

A bulk wafer is oxidized and nitride is deposited. Thanks to RIE and LPCVD steps, a stack of oxide, Si- α and oxide is deposited in the future channel area. A thick nitride layer is deposited and etched by RIE to define the source and drain areas defining thus the channel length by the distance between the source and drain areas. The Si- α is removed by wet etching, defining a tunnel in which the channel will be grown by epitaxy. LTO is later deposited on the nitride sidewall. A window is then

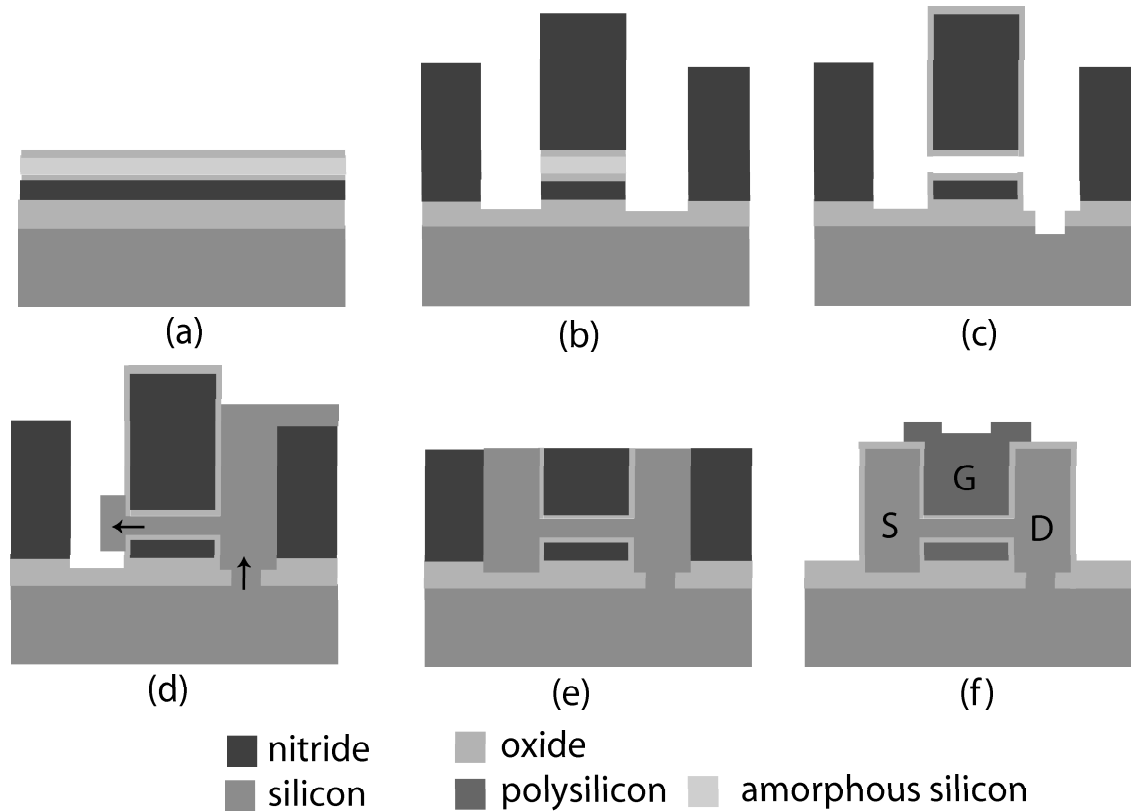


Figure 1.15: Process flow of the Tunnel Epitaxy fabrication method. (a) Stack formation of the dummy channel, (b) source and drain area definition, (c) removal of the dummy channel and opening of the oxide layer to reach the bulk silicon (germination seed for epitaxy), (d) epitaxial grow of the silicon, (e) CMP of the silicon after epitaxy, (f) dummy gate removal, gate oxidation and polysilicon gate deposition [60].

opened in the oxide layer to reach the bulk silicon, which is the germination seed for the following epitaxy. Once the channel and source and drain areas have been grown, the excess silicon is planarized by CMP. The dummy gates in nitride are then removed by wet etching. The free standing silicon beam is the future channel. After gate oxidation, the polysilicon gate is deposited. Although this solution provides a self-aligned structure, it also induces large capacitances between the gate and the source and drain areas. Moreover, as a contact exists between the drain and the bulk, the high performances brought by the SOI structure are reduced. A gate length of 660 nm was achieved.

- *Selective epitaxy*

Shenoy *et al.* proposed a self-alignment method based on selective epitaxy of Si and SiGe, used as sacrificial layers (Fig.1.16) [61].

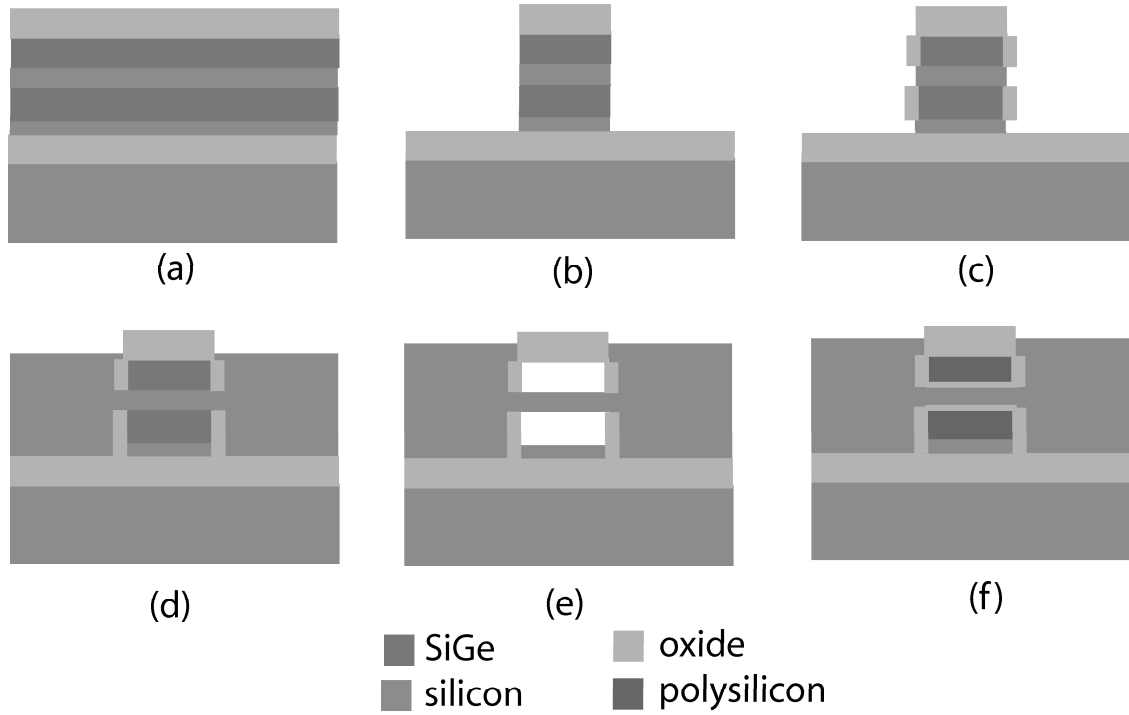


Figure 1.16: Process flow of the Selective Epitaxy fabrication method. (a) Stack formation of the dummy channel, (b) channel length definition, (c) differential oxidation, (d) epitaxial grow of the source and drain areas, (e) etching of the sacrificial SiGe, (f) gate oxidation and polysilicon gate deposition [61].

A stack SiGe / Si / SiGe is grown by epitaxy on a n^+ doped SOI wafer and covered by LTO. The channel length is defined by RIE. Spacers are formed by differential oxidation of SiGe, n^+ doped Si and SiGe being oxidized at a larger rate than undoped silicon. The source and drain areas are then regrown by epitaxy, using the silicon channel as seed. The sacrificial SiGe is then removed by wet etching. The two gates are then processed in the obtained cavities. This process is a great amelioration compares to the one of Wong *et al.* as spacers have been added to the structure and as the bulk contact has been removed. Gates with a length of 400 nm have been realized.

Regrow of the source and drain area

The method from Shenoy *et al.* has the advantage that the front and back gate are defined at the same time, which ensures a perfect self-alignment. Moreover the source and drain fabrication at the end of the process ensures the possibility to fabricate spacers easily. Other groups have also based their process on the definition

of the channel area before the creation of the source and drain areas. However, in the process presented before, the channel was grown by epitaxy. The process can be simplified by the use of the silicon film from an SOI wafer instead of epitaxied silicon. In the following processes, the back gate stack is reported below the silicon channel film by wafer bonding on a handle wafer. The regrowth of the source and drain areas is done after back and front gate definition.

- *Oxidation rate difference and selective epitaxy*

The process proposed by Taraschi *et al.* (Fig. 1.17) looks similar to the one of Shenoy *et al.* [62]. The difference lies in the fabrication of the starting stack: back gate / channel / front gate.

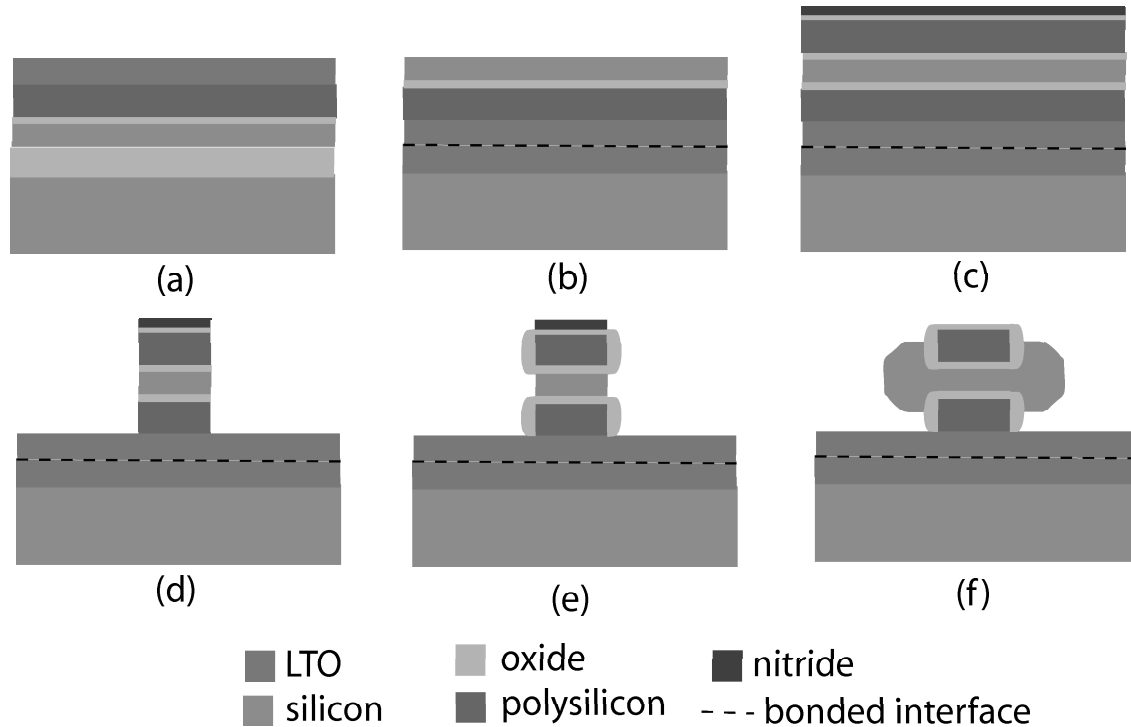


Figure 1.17: Process flow of Taraschi's process. (a) gate oxidation, polysilicon gate deposition, LTO deposition, (b) bonding on a handle wafer and grinding of the initial substrate, (c) front gate stack formation, (d) channel length definition, (e) selective oxidation of the spacers, (f) grow of the source and drain by epitaxy [62].

The back gate oxide is grown on the silicon film of an SOI layer. Doped polysilicon (future back gate) is then deposited and covered by LTO. The wafer is then flipped and bonded to a handle wafer on which LTO has been deposited. The bulk silicon and BOX of the SOI wafer are removed by grinding and CMP. Once the SOI

film is reached the front gate stack is deposited. The Channel length is then defined by RIE. Selective oxidation of polysilicon is used to grow spacers. The source and drain area are then grown by epitaxy, using the SOI film as growing seed. No devices were fabricated yet.

- *Vertical source and drain*

Garini *et al.* proposed a variation to the previous process [63],[64]. The principal innovation is to form the source and drain from a silicon sidewall on the sides of the front gate stack and removing the silicon from the horizontal source and drain areas. The FET is thus folded up along the sides of the front gate allowing access to the back gate. The beginning of the process is similar to the one of Taraschi *et al.* in the sense that the back gate stack and active film are reported on a handle wafer by wafer bonding and grinding. Their process is known as the PAGODA process (Fig. 1.18).

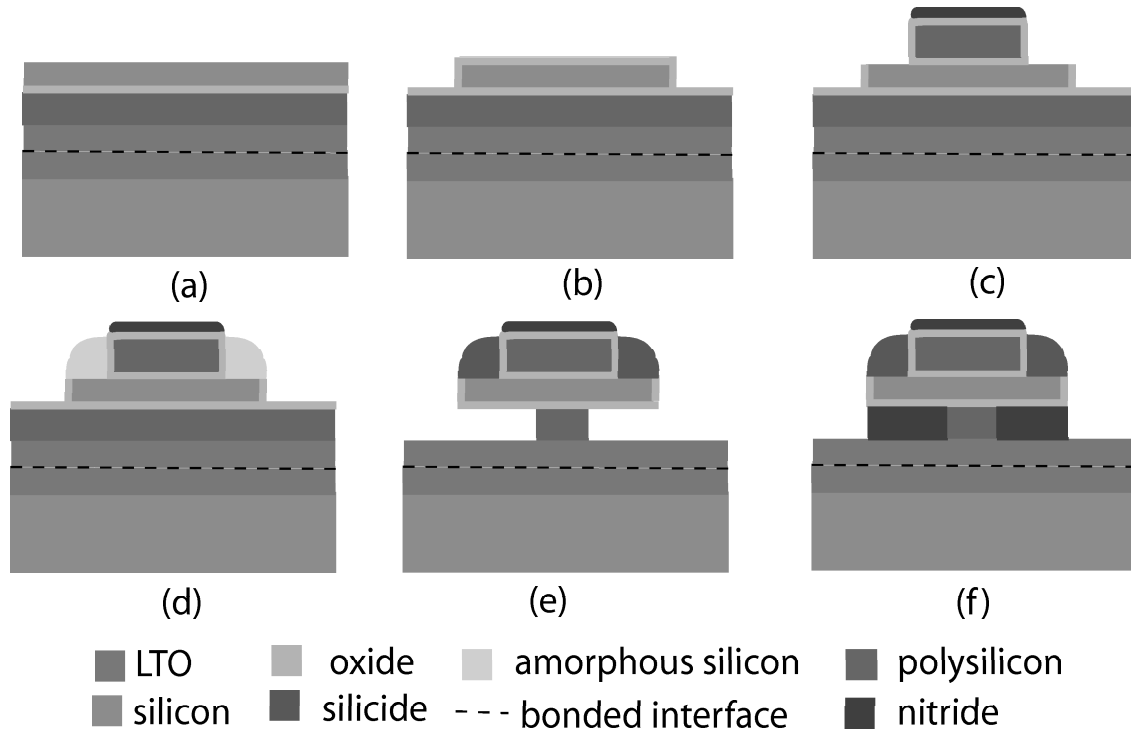


Figure 1.18: Process flow of the PAGODA process. (a) back gate stack definition by oxidation, LPCVD, flip and bond and grinding, (b) active zone definition, (c) front gate processing and oxide spacers formation, (d) Si- α deposition and vertical source and drain extension realization, (e) silicon spacers silicidation, (f) nitride isolation of the back gate [63].

The active area is first defined by RIE and the front gate oxide is grown on the silicon film. The front gate is then processed defining thus the channel length. Oxide spacers are formed on the gate sidewall. Si- α is deposited to form vertical sidewall source drain extensions. After Co silicuration the CoSi₂ spacers are used as mask for the back gate etching. The back gate is isolated by nitride before the source and drain contact formation. Although this process offers a perfectly self-aligned structure, the control of the back gate dimension is done only by controlling the etching time, which is source of differences between the back and front gates dimensions. Indeed the etching being performed in KOH the etch rate of polysilicon is highly dependent on temperature. Moreover the etch rate of KOH is fairly high compare to the dimensions of the structure, which makes difficult an accurate definition of the back gate. The smallest gate achieved had a length of 125 nm.

- *Metallic source and drain*

Deleonibus proposed an architecture identical to the PAGODA structure, but replaced the silicided Si- α source and drain by metallic ones [65]. The gate dielectric is also replaced by a high-k material and the gates are composed of a stack of TiN / polysilicon. The TiN avoids gate depletion and allows thus a lightly doped channel. The polysilicon contributes to decreases the gate resistance. The Process does not solve the problem of the different dimensions for the front and back gates (Fig. 1.19).

The gate stack is composed of a high-k dielectric, HfO₂ on which 5 nm of TiN encapsulated in 50 nm polysilicon are deposited. Once the back gate stack has been reported with the SOI film on a handle wafer by wafer bonding, CMP and grinding, the active area is defined. The front gate stack is then deposited and patterned. Once the front gate has been defined, nitride spacers are added to protect the source and drain extension during the etching of the silicon film of the channel. A new set of spacers is then added to protect the channel during the back gate etching. Once the back gate is defined, it is isolated by nitride and the second set of spacers is removed, to perform the silicuration of the source and drain access. The metallic source and drain in TiN / W are then deposited.

Although this technology is very advanced, considering the choice of high-k dielectrics, metallic gates, source and drain areas, the dimension of the back gate is

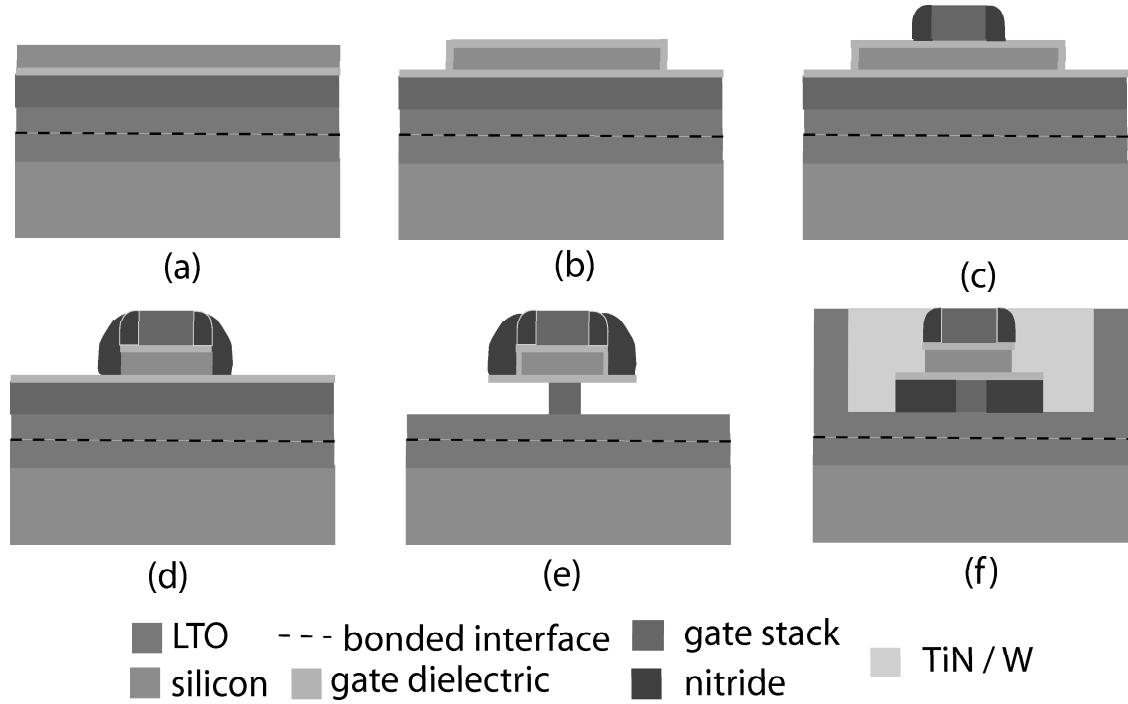


Figure 1.19: Process flow of self-aligned double gate MOSFET with metallic source and drain. (a) back gate stack definition, flip and bond and grinding, (b) active zone definition, (c) front gate processing and nitride spacers formation, (d) channel length definition and nitride spacers formation, (e) back gate definition, (f) nitride isolation of the back gate and metallic source and drain deposition [66].

controlled by the etching time during its definition. It is therefore difficult to obtain the same dimension for the Back and front gates [66]. Transistors with a gate length of 70 nm have however been fabricated and measured.

Improvement to the alignment process have been proposed by Widiez [66]. The etching of the front and back gate is performed simultaneously (Fig. 1.20).

The polysilicon from the gate stack TiN / polysilicon is here replace by poly SiGe. Once the stack, back gate / silicon channel / front gate has been realized by film report and deposition, it is etched by RIE until the BOX defining thus the channel length and the source and drain extension. The definition of the gate dimension is done by etching simultaneously the front and back gates. The polysilicon gate has been replaced by poly SiGe in order to be able to etch the gate material without attacking the silicon of the channel. The metallic layer and semiconductor layer of the gate stack are etched separately. A very low etch rate ensure a good control of the gate dimension. No transistors issues from this improved process have been

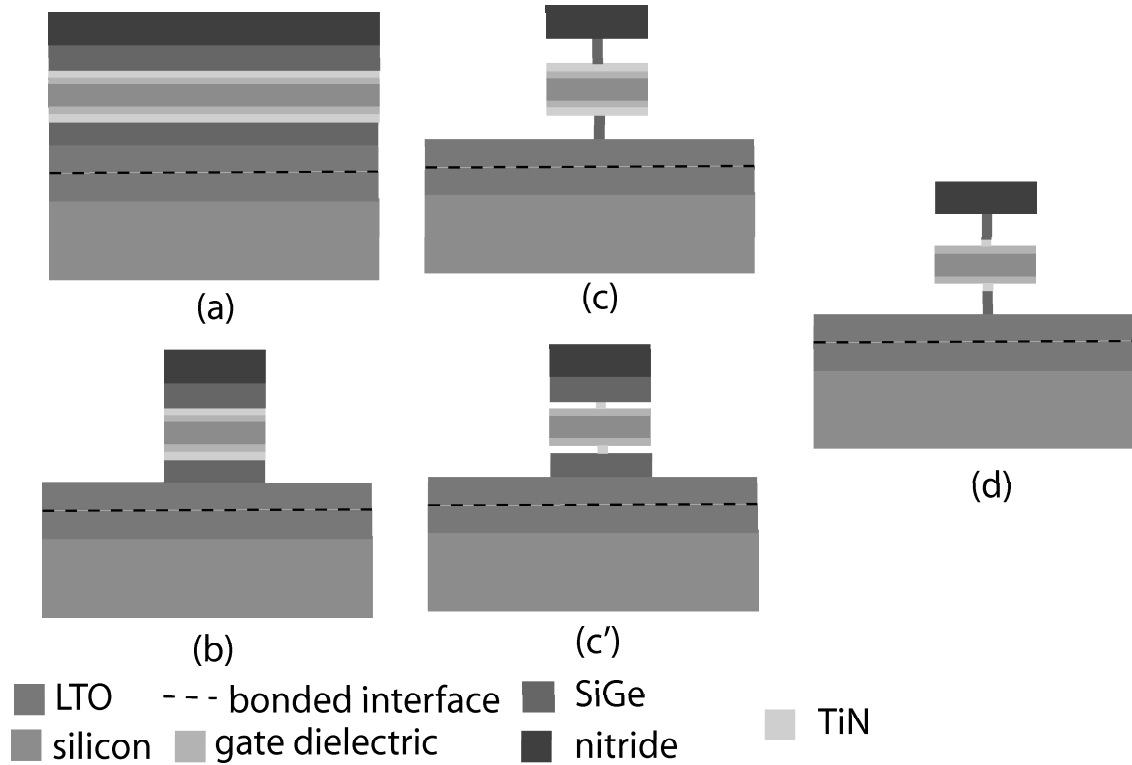


Figure 1.20: Improvement of the Back and front gates definition. (a) back gate stack / silicon channel / front gate stack definition, (b) RIE of the whole stack defining the front and back gate and the source and drain extension, (c) isotropic etching of the poly SiGe, (c') isotropic etching of the TiN, (d) gate size definition by isotropic etching of the remaining gate material [66].

demonstrated yet.

1.1.4.3 Conclusion

The process flows from the previous Section presented devices that have been realized. In these devices, either the channel or the source and drain areas had to be regrown. The regrowth of the channel by epitaxy or recrystallization is a source of defects in the silicon. Furthermore the architecture for which the channel is regrown does not offer the possibility to build spacers in an easy way, yielding thus large capacitances between the source and drain areas.

When regrowing the source and drain areas, if the front and back gate are not processed simultaneously, it is not easy to process the both gates with the same dimensions. Moreover regrowing the source and drain areas can be a source of increased source and drain resistance. Table 1.1 and 1.2 summarizes the main char-

acteristics of the process fabrication of self-aligned double gate transistors described above.

Process type	Pros	Cons	L_g achieved
MILC [57]	• Easy to scale down	• Metal contamination • Large source and drain parasitic capacitances • Poor active Si quality	350 nm
Tunnel epi-taxi [59]	• No metal contamination	• Large source and drain parasitic capacitances • Two wafer bonding steps • Poor active Si quality • Filling of the back gate cavity • Bulk contact	660 nm
Selective epi-taxi [61]	• No metal contamination • Reduced source and drain parasitic capacitances thanks to spacers	• Poor active Si quality • Filling of the back gate cavity	400 nm

Table 1.1: Main characteristics of the self-aligned process flow for the DG MOS. Processes with regrown active Si film.

The process presented by Widiez is the most promising of all the proposed solutions. The architecture includes spacers to reduces the source and drain parasitic capacitances, the silicon channel is made of crystalline silicon and the front and back gate have the same dimension. However, the control of the gate dimension is

Process type	Pros	Cons	L_g achieved
Taraschi [62]	• Reduced source and drain parasitic capacitances thanks to spacers • Crystalline active Si • No filling of the back gate • Same front and back gates size	• regrow of the source and drain extension	not fabricated
PAGODA [63]	• Crystalline active Si • Reduced source and drain parasitic capacitances thanks to spacers	• Back gate size defined by the wet etching time • Respective size of the front and back gates	125 nm
Deleonibus [65]	• Crystalline active Si • Reduced source and drain parasitic capacitances thanks to spacers	• Back gate size defined by the etching time • Respective size of the front and back gates	70 nm
Widiez [66]	• Crystalline active Si • Reduced source and drain parasitic capacitances thanks to spacers • Same front and back gate size	• gate size defined by the etching time	not fabricated

Table 1.2: Main characteristics of the self-aligned process flow for the DG MOS. Processes with crystalline active Si film.

done by varying the etch time during the gate definition, which may cause some fluctuation in the gate size.

We proposed three different process flow in which we also have the advantages of the structure proposed by Widiez but where the gate size is defined with more accuracy thanks to an etch stop or to a localized sacrificial zone.

1.2 *New self-aligned process defined by ion implantation*

We showed in the previous Section that fabrication of double gate transistors faces many challenges:

- Alignment of the front and back gates
- Respective size of the front and back gate
- Need of spacers between the gates and the source and drain areas
- Integrity of the active silicon film.

A process where the both gates could be defined simultaneously or at least defined by etching with the same precision would be ideal. If these process could preserve the integrity of the silicon from the active area (no channel or source and drain to regrow) the spacer definition could be done easily.

We present in the following Section three processes for fabrication of self-aligned planar double gate transistors in which the active area silicon film integrity is preserved. The milestone of these processes is the definition of one gate imprint by ion implantation using the other gate (or a dummy gate) as implantation mask. The imprint created by ion implantation consists in modifying the etching properties of the implanted material. One can thus define a sacrificial zone or etch stop zone. We named this technique *definition of buried mask by ion implantation*. This concept of buried mask defined by ion implantation is the main achievement of this PhD thesis. This concept will be intensively discussed in Chap. 2 and 3.

1.2.1 *Back gate definition by selective etching of implanted BOX*

In the *GAA* and *Bonding of pre-patterned cavities* processes, the back gate is formed in a cavity present in the buried oxide of an SOI wafer [37]. The drawback of these processes was that the alignment of the front and back gate had to be achieved by photolithography. We proposed here also to form the back gate cavity in the buried oxide, but to define this cavity self-aligned with the front gate.

As would be seen in Sec. 2.4.1, selective etching of the implanted oxide can be achieved in VHF. This effect is the keypoint of our process proposal. Oxide is grown on a SOI wafer, so that the silicon film is embedded between two oxide films. A implantation is performed in the top and bottom oxide layer through a negative mask of the gate. Two cavities can be then defined in the top and bottom oxide by selective etching. These cavities define thus the front and back gates. Fig. 1.21 details all the process steps to achieve the fabrication of a self-aligned planar double gate MOS transistor.

- (a) Starting wafer

The starting wafer is a conventional SOI wafer with a 400 nm thick BOX and 150 nm silicon. The BOX must be thick enough, as the back gate and its isolation toward the substrate will be built inside.

- (b) Oxidation

The SOI film is oxidized to produce a thin silicon active film and a thick oxide layer in which the front gate will be defined.

- (c) Hard mask formation and back gate buried mask definition

The front and back gates are defined by a buried mask in the top oxide and in the BOX. This buried mask is based on the etch rate enhancement of implanted oxide. This point is discussed in Sec. 2.4.1. As the implantation dose and energy required to modify the oxide etch rate is very high, a polysilicon mask is used for the implantation, instead of a photoresist mask which could be destroyed. A thin nitride layer serves as etch stop when defining by RIE the gate mask into the polysilicon layer. LTO spacers are added to compensate the lateral scattering of the species during the definition of the buried mask in the BOX by implantation. Silicon is the foreseen specie to be implanted as it would leave the active silicon film uncontaminated.

- (d) Front gate buried mask definition

As the implantation energy for the front gate buried mask is lower than for the back gate buried mask, the lateral scattering of the species during implantation

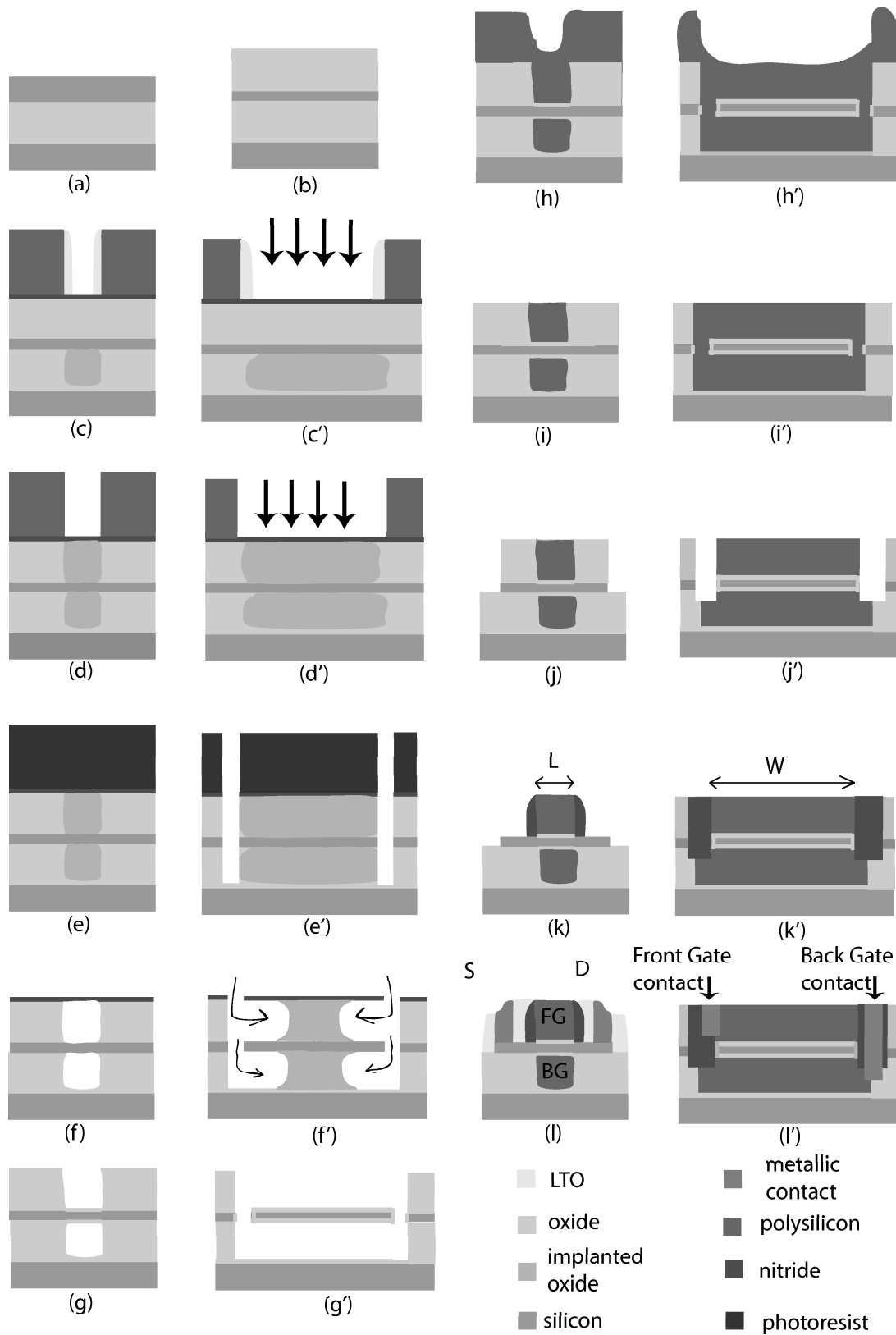


Figure 1.21: Process flow of a self-aligned double gate MOSFET by VHF revelation of a buried cavity [67]. (x) presents a cross-sectional lateral view and (x') a cross-sectional longitudinal view.

is lower, so the spacers are removed before the second implantation at a lower energy.

- (e) Buried mask access definition

Once the implantations have been performed, the hard mask is removed. Trenches are then opened by RIE through the whole stack: nitride / top oxide / SOI film / BOX, at the edge of the W of the transistor in order to access the implanted top oxide and BOX.

- (f) Buried mask revelation

VHF etching is performed under the form of short cycles etching / rinsing as would be described in Sec.3.2.

- (g) Top nitride film removal and gate oxidation

The nitride film is removed by RIE rather than by wet etching in order to avoid stiction of the silicon membrane on the BOX. The gate oxide is grown.

- (h) Gate polysilicon deposition

The gate polysilicon is deposited by LPCVD.

- (i) CMP

The polysilicon is planarized by CMP until the top oxide is reached.

- (j) Active zone deninition

The active zone (channel + source and drain areas) are defined by RIE.

- (k) Gates isolation and spacer formation

The front and back gates are isolated from each other by LPCVD nitride deposition. The oxide in which the front gate was embedded is removed. This operation can be done thanks to an almost infinite selective RIE of oxide toward silicon. The plasma of this selective etching is composed of CF_4 and H_2 . The etching mechanism will be detailed in the Appendix C. Nitride spacers are formed around the front gate.

- (1) Contact formation

LTO is deposited on the source and drain areas, contacts holes are opened, and the metallic contacts are formed. The two gates are connected independently. One hole is therefore opened in the nitride isolating trench in order to reach the buried polysilicon gate, the second one is opened directly in the top polysilicon.

This process is relatively simple and cost effective. No wafer bonding is required. The starting wafer is a common SOI wafer, and the process is fully compatible with a standard CMOS process. The definition of the cavity in the BOX in which the back gate would later sit is done thanks to a positive buried mask in oxide. The buried mask consists into creating a sacrificial zone in oxide. The etch rate enhancement of oxide thanks to ion implantation is studied in Chap. 2 and the revelation of cavities in oxide is studied in Chap. 3. The only difference with classical technology is the back gate definition, for which VHF etching is needed. However, the VHF etching is fully CMOS compatible so introduction of this technique in the process flow might not be a big issue.

One problem that could face this technique, is that the revelation of narrow and long cavities might not be very easy. A second problem is, likely to the *Bonding of pre-patterned cavities* process, that the filling of the back gate cavity which might not be possible for narrow and long cavities and could thus limit the W/L ratio of the fabricated transistors [37].

The following process gets rid of the first problem.

1.2.2 Front gate definition thanks to a negative buried mask in recrystallized Si- α

The previous process created an imprint in a buried layer aligned with a structure on the surface using ion implantation. We will also define by ion implantation an imprint, aligned on a surface structure, in a buried layer but reveal this imprint after transfer on a handle wafer of the mark of the implantation mask and the buried imprint. The revelation can thus be done on a blanket wafer and not in a cavity. The material used as buried mask is here recrystallized Si- α . The implantation of boron into silicon reduces the silicon etch rate in TMAH and can thus allow the

fabrication of negative buried mask into silicon, polysilicon and recrystallized Si- α . The physics of the etch rate reduction is studied in Chap. 2 and the revelation of negative buried mask in polysilicon is studied in Chap. 3.

The starting wafer is like a SOI wafer in which the BOX would include a buried recrystallized Si- α layer. A dummy gate formed on the top silicon serves as implantation mask to create the imprint into the buried recrystallized Si- α layer. The dummy gate is covered by LTO, which is then planarized by CMP. The dummy gate is removed and the processed wafer with pre-patterned cavities aligned on the buried imprints is flipped and bonded to an handle wafer. After CMP and grinding the buried imprint is revealed. This yields two self-aligned cavities apart from a silicon film. The boron imprint in recrystallized Si- α is revealed by TMAH etching, which has the properties to etch only the undoped silicon. This etching selectivity mechanism is explained in Sec. 2.4.2 Fig. 1.22 details the process flow of this novel proposal.

- (a) & (b) Starting wafer

The starting wafer is like an SOI wafer in which a recrystallized Si- α layer would be embedded in the BOX. This stack is realized by wafer bonding and deposition. A SOI wafer is first oxidized. Si- α is then deposited and recrystallized by RTA during 15 s at 950 °C. The deposition of Si- α instead of polysilicon ensures a smaller rms surface roughness, which is a critical parameter for bonding. This critical point is discussed in Appendix A.1. The processed SOI wafer is bonded to an oxidized bulk wafer. The optimization of the bonding parameters is described in Appendix A.2. The bulk silicon and the BOX from the SOI wafer are then removed by grinding and CMP. The starting wafer is then composed of the following stack: Si bulk / oxide / recrystallized Si- α / oxide / crystalline silicon.

- (c) Dummy gate definition

A nitride dummy gate is formed on the top silicon film, which has been protected by a screen oxide.

- (d) Buried mask definition

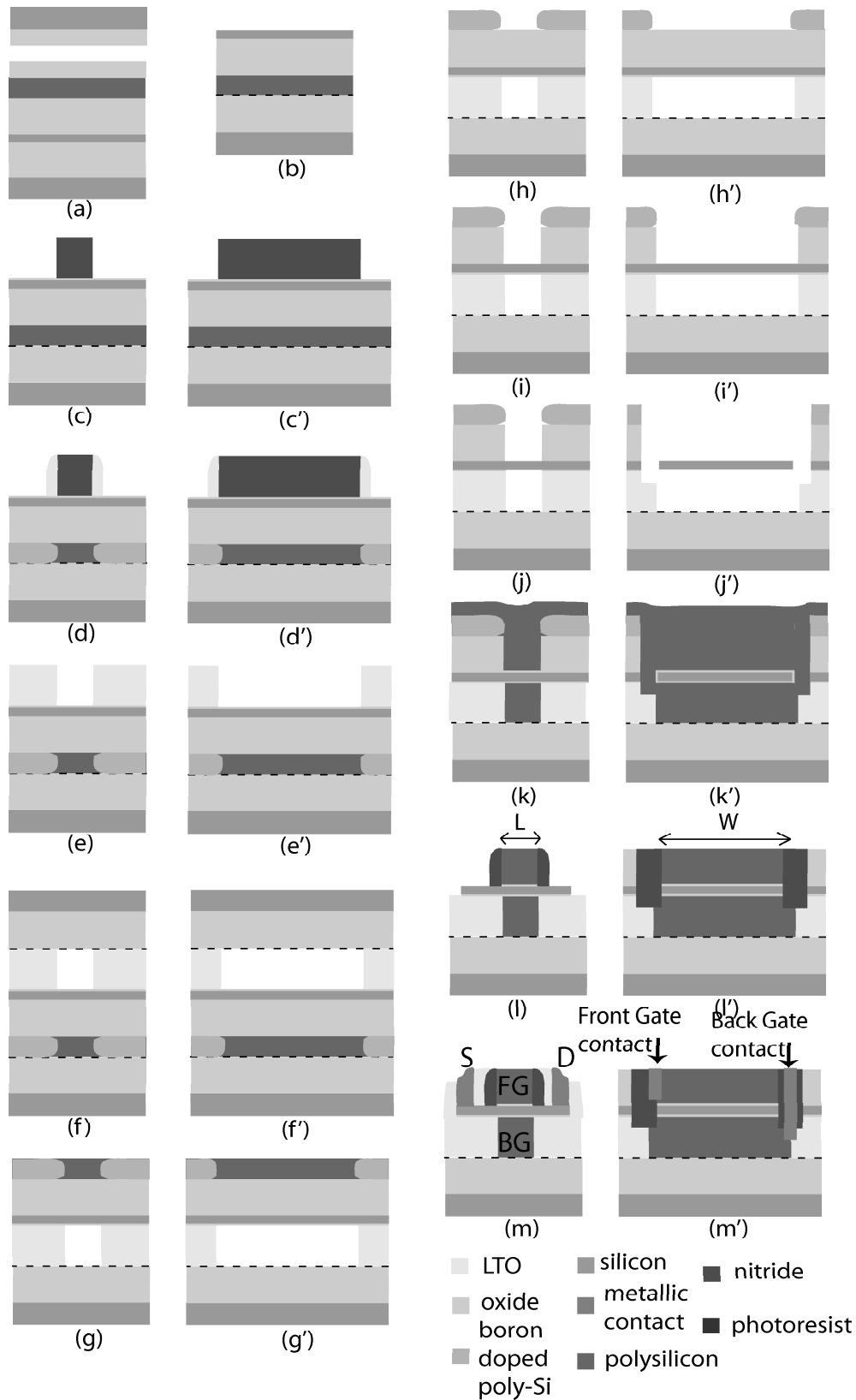


Figure 1.22: Process flow of a self-aligned double gate MOSFET by revelation of a negative buried mask in recrystallized Si- α [68],[69]. (x) presents a cross-sectional lateral view and (x') a cross-sectional longitudinal view.

LTO spacers are added to the dummy gate and the buried mask is defined by boron implantation. The spacers compensate the lateral scattering of the boron during implantation. The spacer thickness is calculated using the simulation software ATHENA.

- (e) LTO deposition / CMP and dummy gate removal

LTO is deposited and planarized by CMP, using the nitride as stopping layer. The nitride dummy gate is then removed by wet etching in ortho-phosphoric acid.

- (f) Bonding to a handle wafer

The wafer is then bonded to an oxidized handle wafer.

- (g) Grinding and CMP.

The bulk and BOX of the handle wafer are removed by grinding and CMP. The top layer is now the recrystallized Si- α layer in which the buried mask has been defined by boron implantation.

- (h) Buried mask revelation

The buried mask is revealed by TMAH etching according to the technique described in Sec. 2.4.2. The boron doped recrystallized Si- α remains.

- (i) Front gate pattern definition

The remaining recrystallized Si- α serves as mask for the definition of the front gate pattern defined in the oxide layer by RIE. CF_4/H_2 based plasma ensures an almost infinite selectivity between oxide and silicon. The etching mechanism of this plasma will be detailed in the Appendix C.

- (j) At the edge of the W of the transistor trenches are realized in the silicon film to reach the back gate cavity.

- (k) Gate oxidation and polysilicon deposition

Once the active silicon film has been reach and is surrounded by two cavities defining the future gates, the gate oxide is grown and the gate polysilicon is deposited.

- (l) Active zone definition

A CMP step planarizes the gate polysilicon and removes the recrystallized Si- α . The active zone is then defined by RIE. Spacers are added to the gate, and the front and back gate are isolated from each other.

- (m) Contact formation

LTO is deposited on the source and drain areas, contacts holes are opened, and the metallic contacts are formed. The two gates are connected independently. One hole is therefore opened in the nitride isolating trench in order to reach the buried polysilicon gate, the second one is opened directly in the top polysilicon.

Compared to the process where one of the gates was defined by selective etching of implanted oxide, this process offers the possibility to define gates of any size and W/L ratio for the back gate cavity. Indeed the revelation of the buried mask being done on a blanket surface, any kind of structure can be revealed. The buried mask material is in this case recrystallized Si- α . The etching selectivity is brought by the boron concentration introduced by ion implantation.

One drawback of this method is the filling of the back gate cavity, which might make impossible the fabrication of transistors with a large W or a narrow L. The second disadvantage of this method is the possible contamination of the source and drain regions during the boron implantation of the buried mask. Although the oxide layer between the active silicon film and the buried recrystallized Si- α film makes that the peak of boron concentration would be quite deep, the boron concentration will not be negligible in the top silicon film. The p-type doping can be compensated by phosphorous or arsenic implantation in the source and drain areas, but a too high concentration of impurities might degrades the mobility. Another issue of this process is the wafer bonding of the processed wafers on the handle wafer which has been oxidized or on which LTO has been deposited. A too high stress of the multilayers deposited on the wafers might induce a wafer curvature which could avoid the bonding. Low stress oxide is therefore needed. Methods for reducing the stress have been developed and will be detailed in Appendix B.

Although this method solved the problem of the back gate cavity dimension, it does not solve the problem of the filling of the back gate cavity. The following

section presents a process solution where this problem of cavity filling is solved.

1.2.3 Front Gate definition thanks to a positive buried mask in recrystallized Si- α

The use of a negative buried mask in recrystallized Si- α from Sec. 1.2.2 causes boron contamination in the source and drain areas. An alternative method could be to define the back gate by implanting with boron the gate area and remove by TMAH etching the recrystallized Si- α covering the source and drain area. It would unfortunately not work as defining the back gate by implantation would cause high boron doping in the channel. However this idea of having the back gate stack in place and to remove the gate material on the source and drain areas would offer the possibility of building transistor with any W/L ratio and getting rid of the filling of the back gate cavity. This could be achieved if one can define the gate by implantation of n- or p-type species through the source and drain areas in a buried recrystallized Si- α layer and reveal the implanted zone with a positive etching solution. The remaining recrystallized Si- α would thus be used as gate material. This solution would also solve the problem of the source and drain contamination if one could implant indifferently n- or p-type species. A HNA based solution that will be described in Sec. 2.4.3, etches selectively the n- or p-doped silicon so is used for this positive revelation of the implanted imprint in recrystallized Si- α . Fig. 1.2.3 presents the process flow of this method.

- (a) & (b) Starting wafer

The starting wafer is a stack composed of: bulk Si / BOX / gate polysilicon / gate oxide / active silicon film / gate oxide / gate polysilicon. This stack is realized by several steps of deposition and wafer bonding. The gate oxide is grown on an SOI wafer and the gate polysilicon is deposited on top of it. The polysilicon used is a Si- α recrystallized by RTA in order to have small grains and a low surface roughness. This low surface roughness allows the bonding of the processed wafer with an oxidized handle wafer (Appendix A.1 and A.2). The bulk and BOX of the SOI wafer are then removed by grinding and CMP. Once the crystalline silicon film is reached a new gate oxide is grown and the

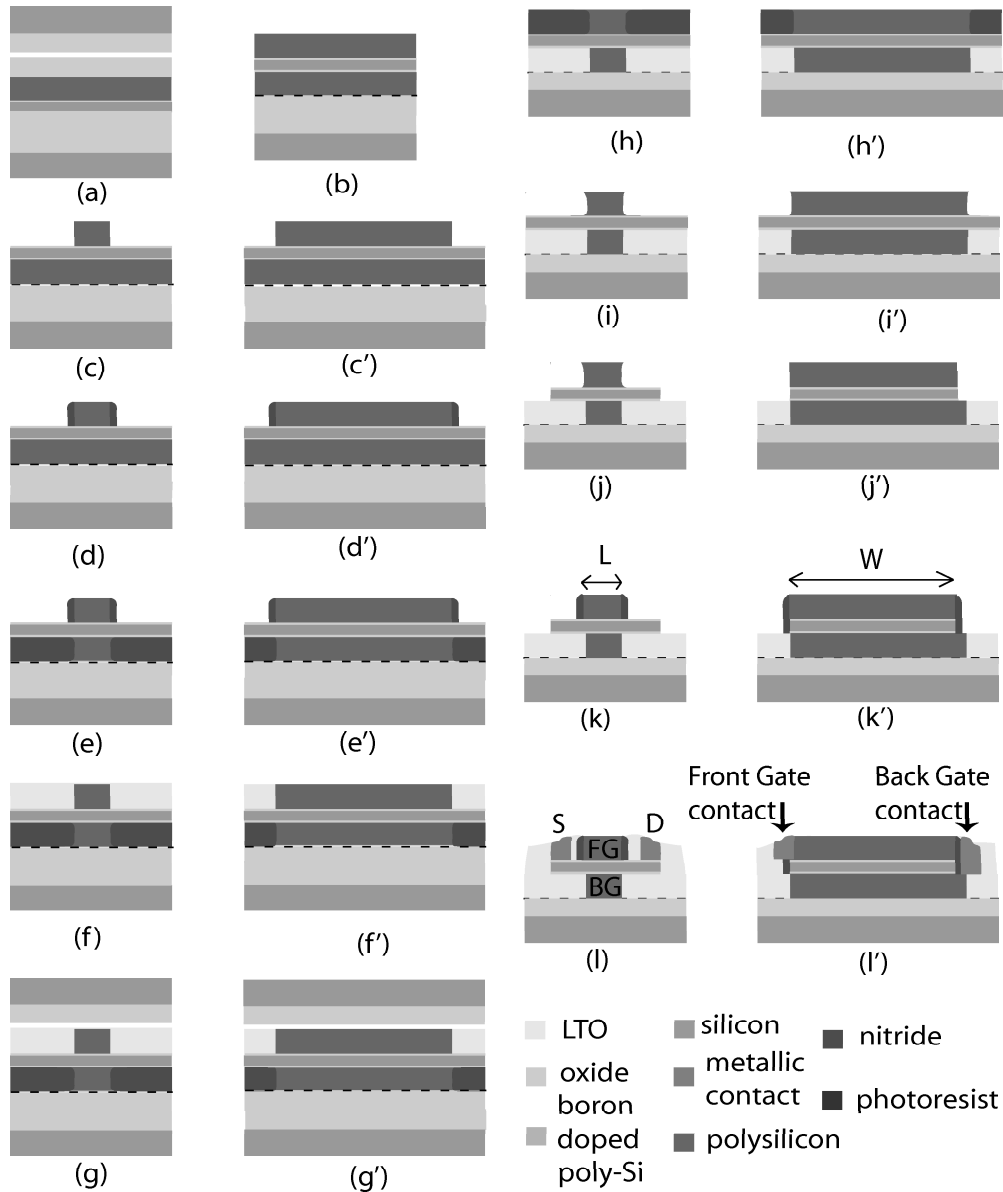


Figure 1.23: Process flow of a self-aligned double gate MOSFET by revelation of a positive buried mask in polysilicon [70]. (x) presents a cross-sectional lateral view and (x') a cross-sectional longitudinal view.

polysilicon gate (recrystallized Si- α) is deposited.

- (c) Gate definition

The future back gate is defined by RIE in the top recrystallized Si- α film. The etching of the polysilicon is done by RIE. The etch stop layer is the gate oxide. A specific RIE recipe with sensitive end point detection has therefore been developed. This point will be discussed in Appendix D

- (d) Spacers deposition

Nitride spacers are formed by LPCVD deposition and RIE.

- (e) Buried mask implantation

n- or p-type dopants (corresponding to the type of the transistor) are implanted through the source and drain areas to define an undoped zone (the future front gate) in the buried recrystallized Si- α layer aligned with the future back gate. The spacers compensate the lateral scattering of the implanted species during ion implantation. The undoped zone has thus the same width as the future back gate. A RTA is needed after the implantation to activate the implanted species.

- (f) LTO deposition and CMP.

The spacers are removed by wet etching in ortho-phosphoric acid. LTO is deposited and planarized by CMP.

- (g) Flip and bond

The wafer is then bonded to an oxidized handle wafer.

- (h) Grinding and CMP

The bulk silicon of the starting wafer is removed by grinding and CMP. The oxide layer is removed by wet etching to access the buried recrystallized Si- α in which the buried mask of the front gate has been implanted.

- (i) HNA revelation

The buried mask is revealed in HNA. The etching is done following the techniques exposed in Sec. 2.4.3 and Sec. 3.3.2.

- (j) Active zone definition

The active zone is defined by RIE.

- (k) Spacer definition

The gate spacers are formed. Nitride spacers are also formed at the edge of the transistor width to isolate the back gate from the front gate.

- (1) Contact formation

LTO is deposited on the source and drain areas, contacts holes are opened, and the metallic contacts are formed. The two gates are connected independently. One hole is therefore opened in the nitride isolating trench in order to reach the buried polysilicon gate, the second one is opened directly in the top polysilicon.

This process has to face the same problem of PECVD oxide bonding than the previous process. However in this case, the back gate is not made by the filling of a cavity like in the process using the revelation of a buried mask in oxide or a negative buried mask in polysilicon. There is thus no limitation on the gate W/L ratio. The use of either n-type or p-type doping for the buried mask creation avoids the source and drain contamination as the species used for the buried mask implantation can be chosen in function of the transistor type to be the same as the source and drain doping.

1.2.4 Conclusion

This three processes distinguish themselves from what have already been published because no silicon regrowth is required, neither for the source and drain area or for the channel area.

The Table 1.3 summarizes the advantages and drawbacks for each of the process proposals.

The common point of these three processes is the alignment of the front and back gate thank to a buried mask created by ion implantation. The buried mask consists into creating a sacrificial or etch stop zone in a buried layer. The use of ion implantation to define the buried mask, allows its self-alignment with the implantation mask on the surface wafer. The buried mask revelation is based on the etch rate modification of the buried layer induced by ion implantation. This major innovation makes our three process proposal original as it allow the creation of a self-aligned planar double gate transistors from which the active silicon film does not need to be regrown. An other advantage of this technique lies in the revelation of the buried mask which is performed by selective etching of the implanted or unimplanted zone. The accuracy with which the respective size of the two gates

Process type	Pros	Cons
Positive buried mask in oxide	• No wafer bonding required • Simple process • No channel contamination	• Buried mask revelation in cavity • Filling of the back gate cavity
Negative buried mask in recrystallized Si- α	• Buried mask revelation on surface	• Boron contamination of the source and drain areas • Two wafer bonding steps • Filling of the back gate cavity
Positive buried mask in recrystallized Si- α	• Buried mask implantation used for the source and drain doping • Buried mask revelation on surface	• Two wafer bonding steps

Table 1.3: Pros and cons of our process proposals.

can be defined is thus correlated to the etching selectivity, which is a improvement compare to the method proposed by Wong and Widiez, where the back gate size was defined by the wet etching time of the back gate [63], [66].

The main achievement of this PhD thesis was to fully characterize and explain the principle of etch rate modification by ion implantation and its application to buried mask creation. Chapter 2 deals with physics of ion implantation and etch rate modification induced by ion implantation. Chapter 3 demonstrates the revelation of buried cavity and buried structures defined by ion implantation.

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CHAPTER 2

ETCH RATE MODIFICATION BY ION IMPLANTATION

2.1 *Introduction*

The common point between the process proposals for self-aligned planar double gate presented in Sec. 1.2 is that one of the gate dimension is defined by implantation of a buried mask, using the other gate (or a dummy gate) as implantation mask.

The concept of buried mask is that ion implantation changes the properties of the target material, and that this change in material properties could influence the reactivity of the implanted material with some etching solutions.

The first part of this chapter will thus make a brief review of the ion implantation technique and theory. The impact of ion implantation on the target material will then be presented.

The second part of the chapter will present the simulation tools that have been used to simulate the ion implantation and its impact on the target material.

The third part of this chapter will then focus on the etch rate modification of silicon and oxide. The etch rate modification mechanisms are based on the use of three different type of impact that implantation causes to the target material. The following etch rate modification mechanism will be studied.

- Increased reactivity of oxide in HF due to covalent bond breaking during implantation.
- Decreased reactivity of polysilicon in TMAH due to internal tensile stress caused by the addition of atoms of smaller atomic radius to the lattice.
- Increased reactivity of polysilicon in HNA due to free carrier brought by n- or p-type doping.

2.2 Ion implantation. Technology and theory.

2.2.1 Ion implantation technology

Ion implantation is a material engineering process by which ions of determined charge and mass of a material can be implanted into another solid at a given energy, thereby changing the physical properties of the solid. The first patent in ion implantation has been deposited in the late 50's in the US [1]. A few years later in 62, Alväger and Hansen fabricated the first semiconductor diode in which the doping species were implanted [2]. Since that time, ion implantation has become the main method for doping semiconductors but its application domains have also been extended from tool steel toughening to hardening of prosthetic devices [3],[4]. We investigate in this work the effect of implantation on the etch rate of the most popular materials in silicon-based devices, i.e. silicon and silicon dioxide.

To perform an implantation a focused ion beam of a pure specie is accelerated toward the surface target at a given energy. The specie to implant is either under gaseous state or vaporised from a solid source in an oven. The species are then ionized in an arc chamber, by collisions with electrons and other excited molecules or ions. The ions created in the plasma are focused by an electric and magnetic field lens to avoid ion loss into the wall of the beam line and to ensure that the ion beam reaches the wafer in a well defined focus. The plasma created in the arc chamber contains any type of ions and contaminants in any charge state. The desired ion to implant is thus selected by a mass spectrometer. When a particle of mass m and charge q moves with a velocity v into an magnetic field B , the Lorentz forces make the ions following a curved path with a radius of curvature R depending on the ratio m/q according to Eq. 2.1.

$$\frac{m}{q} = \frac{R^2 * B^2}{v^2} \quad (2.1)$$

A initial beam containing various particle species can thereby be split into several single species beam with different beam directions, so that a small aperture placed behind the analyzing magnet can select the desired specie. The single particle beam is accelerated to the desired energy before reaching the wafer. The final kinetic energy E of the ions depends on the extraction voltage V_{ext} , the accelerating voltage

V_{acc} and of the ion charge state q according to Eq. 2.2:

$$E = q * (V_{ext} + V_{acc}) \quad (2.2)$$

Due to the fact that the area covered by the ion beam is typically some cm^2 , the beam has to be scanned over the entire surface wafer to ensure an uniform implantation for the whole wafer. Electrostatic or magnetic beam scanning, wafer mechanical scanning or spinning or a combination of these techniques is commonly used. Although electrostatic and magnetic beam scanning are technically less complicated than mechanical scanning, they induce a small tilt in the beam angle, which changes the implantation profile in the case of crystalline material and could cause non uniform doping. The sample holder can be tilted, so that the ion beam is not perpendicular to the surface. This functionality is of interest in the case of crystalline material in order to get an implantation profile similar to the one obtained in amorphous materials. Fig. 2.1 describes the schematic of an implanter.

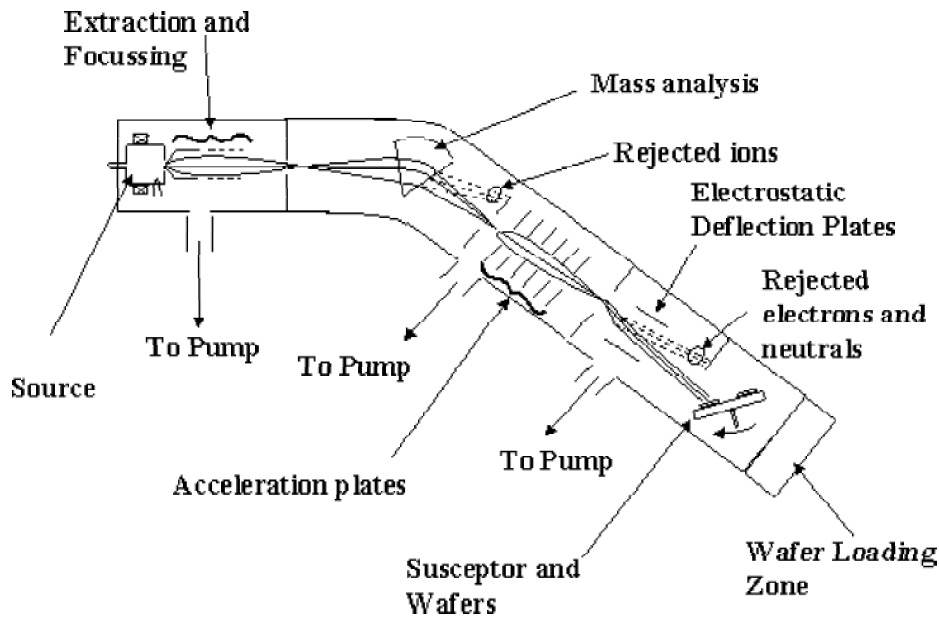


Figure 2.1: Schematic of an implanter [5].

The total amount of ions implanted in the target is called the dose ϕ and is easily measured, knowing the charge state of the implanted species q , by integrating the current I flowing through the sample of surface A during the implantation time t .

It is given in atoms per cm^2 according to Eq. 2.3.

$$\phi = \frac{\int I(t)dt}{A * q} \quad (2.3)$$

Typical ion energies are in the range of 10 to 500 keV. Below 10 keV the ions penetrate only a few nanometers in the target and results in very little damage to the target, which is not of interest in semiconductor doping. Above 500 keV, the resulting are very high and the dispersion of the implanted species in the target is very broad.

2.2.2 *Physic of implantation*

When an ion penetrates the target with an energy in keV range it transfers its energy to the target atoms through collisions. The ions trajectory is deflected due to collisions with the target atoms. The binding energy of the target atoms is typically in the 15 eV range, thereby target atoms can also be displaced. The final point of the ion trajectory is reached when the kinetic energy of the particle reaches the thermal energy which is of the order of 35 meV. There are two main mechanisms for ion energy loss [6]:

- the electronic energy loss, which is an inelastic process is the energy exchanged with the electron sea of the target S_e ,
- the nuclear energy loss, which is an elastic process is the energy exchanged through collision with the target nuclei S_n .

It is summarized as Eq. 2.4:

$$\frac{dE}{dx} = S_n(E) + S_e(E) \quad (2.4)$$

It is of importance to understand each of these mechanisms to evaluate their impact on the target material and their relative importance in function of the mass and energy of the implanted specie.

The electronic energy loss, S_e , is modeled by the interaction between a particle and a density averaged free electron gas. Lindhard calculated the electronic energy loss in function of the incident ion velocity and atomic number, the plasma density

of the target and the atomic number of the target atoms [7]. Numerical resolution of his calculation shows that for ion energies lower than 25 keV per atomic mass unit (amu), the electronic stopping power varies linearly with the ion velocity. The standard implantation performed in microelectronics processing is within this range of energy.

The nuclear energy loss, S_n , is modeled by the interaction of a charged particle with the nuclei of a solid and is described by a series of classical scattering processes. The analytical resolution is done assuming that only two particles (the ion and one target nucleus) are involved in the scattering process. This is called the binary collision approximation, which reduces the multi particles problem to a classical elastic two particles problem which is characterized by the conservation of energy and momentum. For calculation simplification the resolution is done in the center of the mass of the system. Modeling this scattering process necessitates to take into account the electrostatic Coulomb interaction potential between the ion and the target. This potential is however screened by the electron sea. Ziegler, Biersack and Littmark have performed potential calculations for a wide range of particle pairs taking into account the screening due to the electron sea [8]. They assumed solid state charge distributions for both particles, which were constructed by using a Hartree-Fock-Slater method [9]. Thanks to their modeling of the screening potential, the two body problem can be solved, and the energy transferred to the nuclei can be calculated. Numerical calculation of the energy lost through the collision with the nuclei shows that it is proportional to the incident ion energy for energies less than 1 keV/amu. Above 1 keV/amu, the nuclear deposited energies decreases slowly when increasing the incident ion energy.

The energy loss mechanism through collision with the nuclei is responsible for damage creation. This aspect is described in the following Section.

2.2.3 *Implantation damage*

An ion which penetrates into a target constantly loses energy through interactions with the electron sea. It may go many atomic layers until it suffers a collision with the target atom. A collision with a target atom induces a transfer of momentum and thus a change in incident ion direction. If the target is a crystalline material,

due to the periodical position of the target atoms, some crystal directions are more dense in atoms. Fig. 2.2 shows a modeling of crystalline silicon seen from the (110) and the (100) directions.

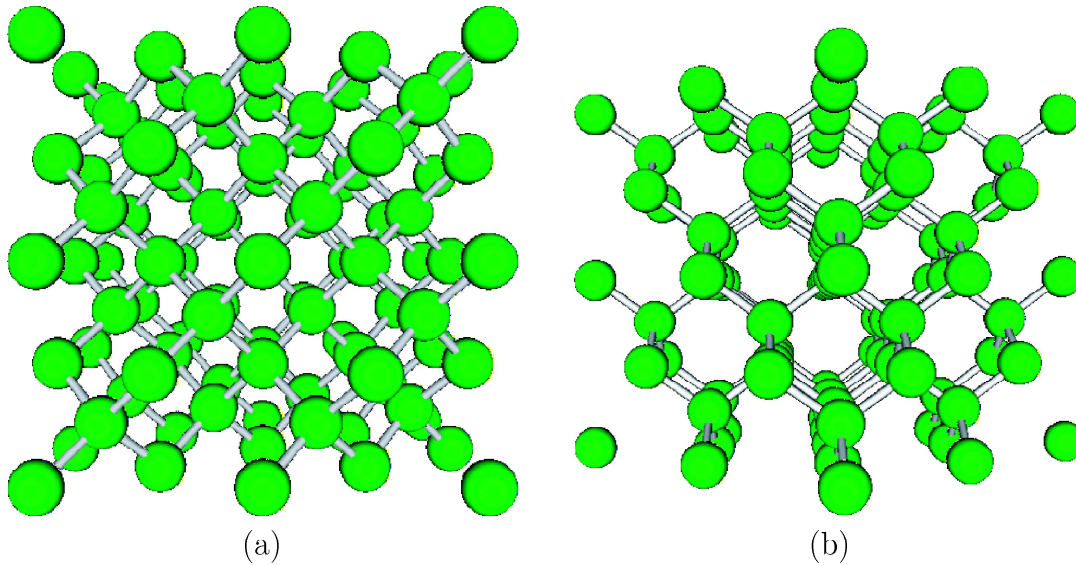


Figure 2.2: Modeling of crystalline silicon seen from (a) the (100) direction and (b) the (110) direction.

It is clearly seen that incident ions with a trajectory parallel to the (110) direction will suffer less collisions than the ones arriving parallel to the (100) direction. The incident ions with a trajectory parallel to the (110) direction will thus suffer less change in directions than the ones with a trajectory parallel to the (100) directions. They will thus rest deeper into the material. This effect is called channeling effect and has to be taken into account when performing implantation in crystalline material as it broadens the implanted range. This effect does not occur in amorphous materials as the atoms have a random spatial distribution. As seen in the previous section, a collision with the nuclei of the target atoms is an elastic collision between an incident ion of atomic number Z_1 and initial energy E_1 and a struck nucleus of atomic number Z_2 . The energy E_2 is transferred to the target ion. The energy needed to remove the ion of its site is called the displacement energy E_d . If the incident ion energy E_1 is larger than E_d , the typical displacement energy from 10 to 25 eV and if E_2 is higher than the binding energy from the ions to its site, E_b , the target atom can be removed of its site. The energy E_2 of the atom Z_2 is reduced by E_b before it undergoes another collision. If the energy of the recoil atom is lower than E_d , it will vibrate until it releases its energy under the form

of a phonon, responsible of the thermal heating of the target during implantation. Once the energy from the recoil atom or the incoming ion has decreased to reach the value of thermal energy, the trajectory of the ion or the recoil ends and they rest on site. The empty site left behind a recoil atom is called a vacancy. Replacement collision reduces the number of vacancies. If a moving atom strikes a stationary target atom and transfers more than its displacement energy to it and if the initial atom, after the collision, does not have enough energy to move onwards, then it can rest at the site of the atom it struck. If the incoming atom is the same element than the target atom, it is called a replacement collision and no defect is created. This effect contributes to a reduction of 30% of the vacancy number. When the replacing atom is from another type than the target atom, it is called a substitutional impurity. It means that in the case of a crystalline target, it occupies a site within a lattice site and forms covalent binding with the neighbor atoms. This type of defect is of major importance in microelectronics as the doping arise from the presence in the crystal lattice of atoms with a number of valence electrons different from the one of the lattice atoms. If an atom ends its course between two lattice site, it is called an interstitial. The displacement can be seen as the sum of the vacancies and the replacement collisions. The vacancies equal the number of interstitials. A large number of vacancies and interstitials can locally avoid the channeling effect by destroying locally the periodical arrangement of the atoms. This effect is sometimes used in implantation process technology to perform shallow implantations. If the number of generated vacancies and interstitials is very high a crystalline material undergoes a phase transition to an amorphous state where neither long range nor short range order of the atoms can be found. Amorphization is damagable in semiconductor processing as the semiconducting properties arise from the crystalline structure of the material. To summarize, ion implantations can create the following kind of defects:

- vacancies;
- interstitials;
- substitution atoms;
- amorphization and atoms displacements;

- heating of the target.

However, in microelectronics, the ion implantation is used to doped the semiconductors by introducing foreign atoms in the lattice and not to damage the crystalline target. The following section deals with lattice reconstruction.

2.2.4 *Thermal treatment*

As seen in the previous section, ion implantation can severely damage the lattice of the implanted target. The amorphization of the target can be useful to reduce the channeling effect when performing shallow implantation. The amorphization of silicon wafers is done by implanting silicon which does not contaminate the silicon substrate. High implantation current can also heat the implanted substrate by creation of phonons and recrystallize locally the target material [10]. However, in the standard implantation conditions in microelectronic processing such implantation currents are not reached and the target is amorphous after implantation. Moreover, the purpose of implantation is doping the semiconducting materials, which means introducing impurities at substitutional sites in a crystal lattice in order to make them electrically active.

Therefore, an annealing is performed after ion implantation to recover long range order of the target atoms and to include the impurities at substitutional sites. The outer electronic shells electrons of the impurities share their electron with the neighbor atoms of the lattice when placed at substitutional sites and form covalent binding. When the impurity is from the third or fifth column from the Mendeleïv chart, there is, respectively, a default or an extra electron, which is shared with the other lattice site and can move over the whole lattice creating thus free carriers positively or negatively charged, respectively, holes or electrons.

The annealing being done at high temperature, the atoms acquire enough energy through thermal activation to change their position within the lattice. According to the first Fick's law, the ion flux $\vec{J}$ which is the number of atoms crossing the surface unit per unit of time is expressed as:

$$\vec{J} = -D\vec{\nabla}(C) \quad (2.5)$$

with D the diffusion coefficient, in $\text{atm}/\text{cm}^2\text{s}^{-1}$, and C the impurities concentration in atm/cm^3 , the doping species will migrate from high to low concentration zone. The diffusion coefficient depends on the type of doping species, the type of the host material, the temperature, the amount of defects in the lattice and on the dopant concentration. The diffusion coefficient integrates all the different mechanism occurring during diffusion. The following paragraph details the diffusion mechanisms [11].

2.2.4.1 Diffusion mechanisms

- Interstitial impurities

Small atoms such as Helium or Hydrogen and transition metals from the fourth line of the Mendeleïev chart like Titanium, Vanadium, Chromium, etc. cannot sit at substitutional sites in a silicon lattice. They thus only occupy interstitial sites. Diffusion occurs when the impurities jump from an interstitial site to another as illustrated in Fig. 2.3.

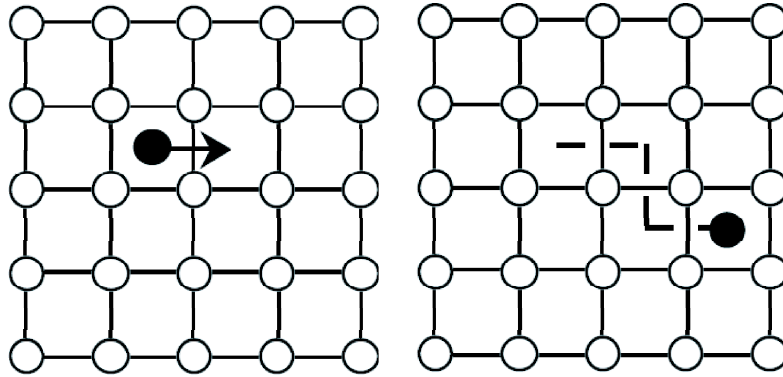


Figure 2.3: Diffusion of interstitial atoms.

In crystal the interstitial impurities can diffuse over long distances due to the abundance of interstitial sites, yielding very high diffusion coefficients. The species used for doping in microelectronics do not remain as interstitials in the lattice once annealing has been performed and diffuse via the mechanisms presented below.

- Substitutional impurities

Diffusion of substitutional atoms is possible only in the presence of lattice defects. These defects can either be self-interstitials or vacancy. Diffusion

assisted by vacancies is illustrated in Fig. 2.4.

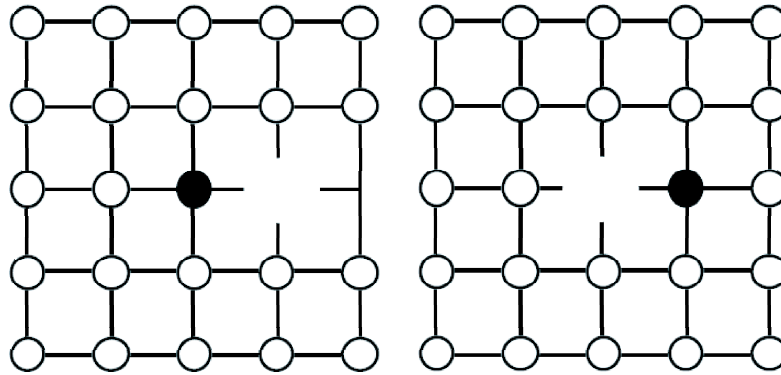


Figure 2.4: Diffusion of substitutional atoms assisted by vacancy.

To diffuse, the impurity must have a vacancy in his neighborhood and exchange its site with this vacancy. The vacancy exchanges then its site with a surrounding lattice atom. To diffuse further the impurity has to wait for another vacancy. It can happen that the binding energy between the impurity and the vacancy is rather high and that they diffuse together. This pair diffusion will be described later on.

Fig. 2.5 describes the diffusion mechanism assisted by the self-interstitials. In the silicon lattice, the self interstitials have the structure shown in (1): the interstitial is bound to the lattice. It is named a dissociated self-interstitial, it means that two silicon atoms share the same lattice site. When this self-interstitial comes in the neighborhood of a substitutional impurity, one of the silicon atom reacts with the impurity which then becomes interstitial (2), which is in fact a mixed dissociated interstitial and can then diffuse following the sequence of steps (3) and (4). The impurity can change many times of sites, and diffuse over long distances before dissociating. It can be seen as a pair of impurity self-interstitial diffusion.

- Dissociative mechanisms

Some impurities occupy preferentially a substitutional (where there are almost at rest) site but have a non negligible probability to sit at a interstitial site (with a very high diffusion coefficient). The effective diffusion coefficient from

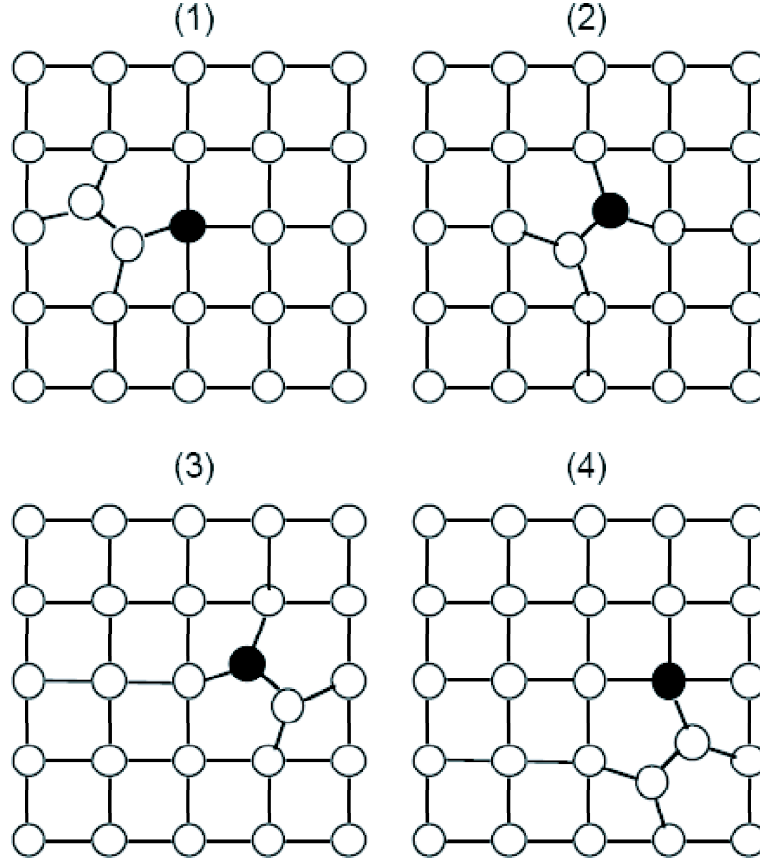


Figure 2.5: Diffusion of substitutional atoms assisted by self-interstitials.

which the value is intermediate between the one of interstitial and substitutional impurities is determined by the mechanism responsible for the impurity to go from one site to another. There are two main mechanisms. Fig. 2.6 describes the Frank-Turnbull mechanism in which a substitutional impurity is changed into an interstitial impurity thanks to the vacancies, as described in Eq. 2.6 [12].



with A_i and A_s impurities respectively interstitial and substitutional and V a vacancy.

Fig. 2.5 describes the diffusion mechanism assisted by the self-interstitials.

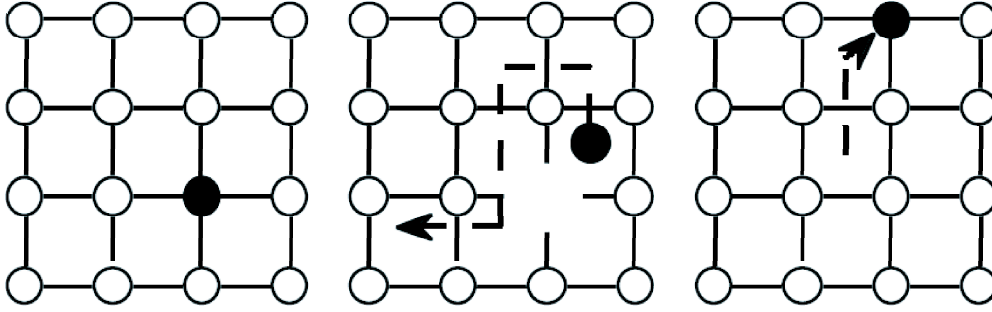


Figure 2.6: Diffusion via the Frank-Turnbull mechanism.

As the Franck-Turnbull mechanism was not very accurate in some experimental conditions, Gösele et *al.* proposed the kick-out mechanism described in Fig. 2.7 [13]. A self-interstitial can exchange its site with a substitutional impurity transforming thus the impurity in interstitial impurity. The impurity occupies a new substitutional site by the reverse reaction.



with Si_i and Si_s silicon, respectively, self-interstitial and substitutional and A_i and A_s impurities, respectively, interstitial and substitutional.

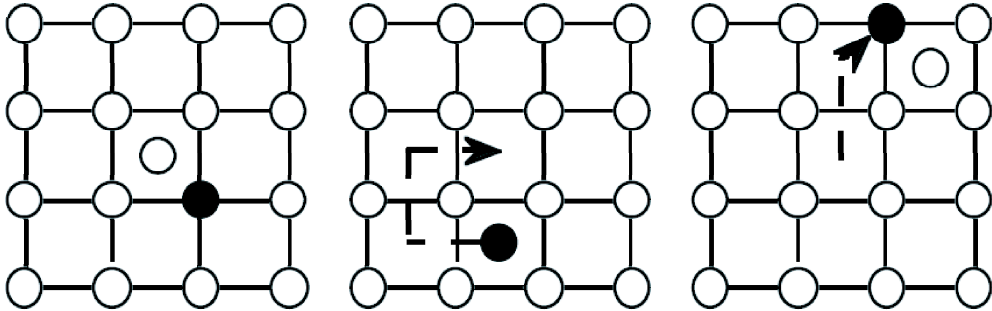


Figure 2.7: Diffusion via the Kick-out mechanism.

Annealing is performed at high temperature, in the range 700 to 1050°C. Long time annealing, from 10 min to 2 hours, presents the advantage of activating almost the whole amount of implanted ions but spreads the doping species over a wide range, which can be destructive when one performs shallow junction or nanometer scale transistors [14].

Rapid Thermal Annealing (RTA) is performed during 1 ms to 60 s. It is not as efficient as long time annealing to activate the implanted species but reduces the diffusion of the species [14]. However, the diffusion during a RTA is anomalously high when compared to the annealing time. Transient enhanced diffusion during RTA is described in the next section.

2.2.4.2 *Rapid Thermal annealing and transient enhanced diffusion*

Diffusion coefficient 10^3 to 10^4 times higher than usual are observed during RTA [15]. A closer look to the transient enhanced diffusion (TED) shows that the enhancement of the diffusion can be decomposed in three steps. An initial phase of ultra fast TED is followed by a plateau with near constant diffusion coefficient where the TED is still high but does not vary significantly up to a time where the TED drops to much smaller values, corresponding to those of classical diffusion. The time constant for the first step ranges between 2 s to 10^3 s at respective temperature of 800 °C and 600 °C. The time constant for the second step ranges from 10^2 s at 800°C to 10^6 s at 600°C [16]. The previous paragraph highlighted the role of the defects such as Frenkel pairs, which are interstitials and vacancies for diffusion of impurities. These defects are a consequence of the ion implantation and their concentration and space arrangement evolves during annealing with consequences on the diffusion of the impurities. A self-interstitial is not very stable. It strains the lattice due to its large size and has dangling bonds. The interstitials tend to cluster and bind to each other to form an interstitial chain which can measure up to a few nanometers, the so called $\{113\}$ rod defects. Fig. 2.8 shows a TEM picture of typical $\{113\}$ defects.

They minimize thus their energy. Self-interstitials diffuse rapidly over the lattice to form the $\{113\}$ defects that behave like an interstitial sink. The constant time for their formation is equivalent to the constant time of the first step of the TED. The self-interstitials contribute to the impurity diffusion during their displacement to form the $\{113\}$ clusters [18]. The second step of TED, where the enhanced diffusion is done at a constant rate corresponds to the dissolution of the $\{113\}$ clusters. The dissolution is done at constant rate and the released interstitials contribute to the diffusion of impurities. Once the clusters are dissolved, there is no extra interstitial and the diffusion coefficient gets back to its usual value.

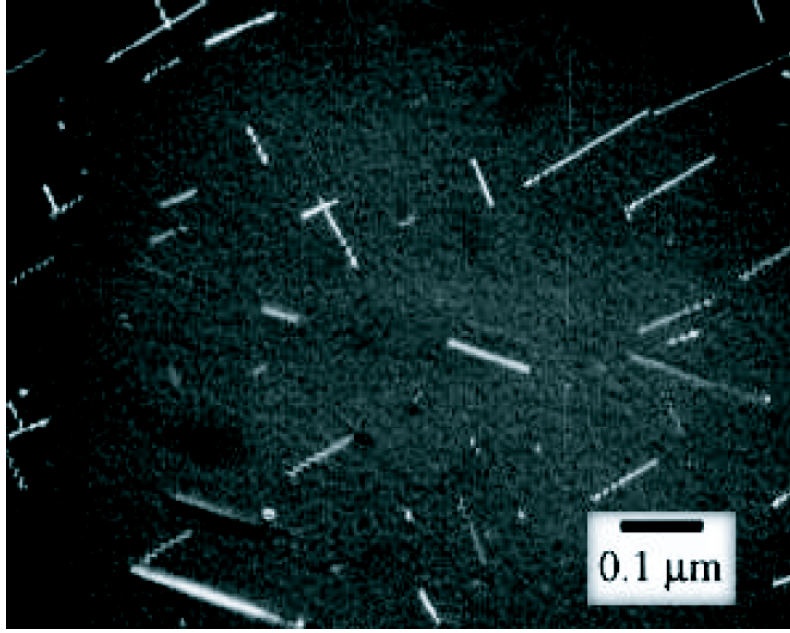


Figure 2.8: Micrograph of $\{311\}$ defects in silicon. Czochralski silicon implanted with $160 \text{ keV } 1 \times 10^{14} / \text{cm}^2 \text{ Si}^+$, annealed at $750 \text{ }^\circ\text{C}$ for 105 minutes [17].

2.2.5 Conclusion

We reviewed the ion implantation technology and physics. Ion implantation is done thanks to an implanter in energy ranges between 15 keV to 200 keV . The implanted specie loses its energy through constant deceleration in the electron sea (electronic energy loss) and through collisions with the nuclei (nuclear energy loss).

The collisions with the nuclei can displace the nuclei from their site and break the bond with the neighbor atoms. This creates, vacancies, interstitials, substitutional foreign atoms and amorphization of the target.

The target amorphized by implantation can be recrystallized by annealing. This high temperature step allows the implanted ions to take place at substitutional sites. The substitutional foreign atoms can thus share their excess or default electrons with the neighbor atoms.

The annealing is performed at high temperature. The annealing time can be on the hour order. In this case the lattice reconstruction is effective but diffusion occurs. RTA can also be done. The anneal time is comprised between ms and tens of s. The diffusion is assisted by the point defect (vacancies and interstitials) present in the crystal. The diffusion coefficient is several orders of magnitude higher in the case of RTA than for conventional annealing.

2.3 *Simulation of ion implantation*

In the previous section the physics of ion implantation has been briefly introduced, from the mechanism of ion energy loss along its trajectory within the target to the damage induced to the target and the thermal treatment used to minimize the impact of structural damage due to implantation.

As our goal is to create damage in oxide or to introduce substitutional atoms in the polysilicon lattice, we use simulation software to predict the effects of ion implantation. As performing simulation makes sense only if the limits of the simulator are known, we describe in the following the simulation of ion implantation.

A large number of software and freeware are available on the market, like ISE, ATHENA and SRIM [19]. ISE and ATHENA are able to simulate the whole fabrication process of microelectronic devices whether SRIM is dedicated only to ion implantation. There are two main approaches for the simulation of ion implantation.

- The first approach is based on the analytical description of reference SIMS profiles that have been measured for a wide range of ion energies, ion types, and targets materials;
- The second approach is based on Monte Carlo calculation of the ion trajectories. Thanks to the theory developed in the previous section, incident ions and recoil atom trajectories are calculated for each collision event.

The advantage of analytical simulation is the gain in calculation time but the accuracy becomes poor for multilayered and two dimensional structures but on the other hand Monte Carlo calculation is more accurate but time consuming. SRIM performs only physical calculation, on the other hand ATHENA and ISE perform both analytical and physical calculations.

2.3.1 *Analytical model*

The distribution of implanted ions can be described in the form of Eq. 2.8:

$$C(x) = \phi f(x) \tag{2.8}$$

where ϕ is the implantation dose defined in Section 2.2.1 and $f(x)$ a distribution function which is normalized according to Eq. 2.9:

$$\phi = \int_0^{\infty} C(x)dx \quad (2.9)$$

with $x=0$ at the surface.

The distribution function can be characterized by:

- the mean projected range R_p

$$R_p = \int_0^{\infty} x f(x)dx \quad (2.10)$$

- the standard deviation σ_p

$$\sigma_p^2 = \int_0^{\infty} (x - R_p)^2 f(x)dx \quad (2.11)$$

- the skewness γ

$$\gamma = \frac{\int_0^{\infty} (x - R_p)^3 f(x)dx}{\sigma_p^3} \quad (2.12)$$

- the kurtosis β

$$\beta = \frac{\int_0^{\infty} (x - R_p)^4 f(x)dx}{\sigma_p^4} \quad (2.13)$$

The implantation profile of any species in a simple material could at the first order be approximated by a Gaussian profile. Generally, the Gaussian distribution is inadequate because real profiles are asymmetrical in most cases. The simplest and most widely approved method for calculation of asymmetrical ion implantation profiles is the Pearson distribution. This function is used to obtain longitudinal implantation profiles. The Pearson function refers to a family of distribution curves that are solutions of Eq. 2.14.

$$\frac{df(x)}{dx} = \frac{(x - a)}{b_0 + b_1x + b_2x^2} f(x) \quad (2.14)$$

in which $f(x)$ is the distribution function. The constants a , b_0 , b_1 and b_2 are related to the moments of $f(x)$ given by Eq. 2.15 to Eq. 2.19.

$$a = -\frac{\gamma\sigma(\beta + 3)}{A} \quad (2.15)$$

$$b_0 = -\frac{\gamma^2(4\beta - 3\gamma^2)}{A} \quad (2.16)$$

$$b_1 = a \quad (2.17)$$

$$b_2 = -\frac{2\beta 3\gamma^2 - 6}{A} \quad (2.18)$$

$$A = 10\beta - 12\gamma^2 - 18 \quad (2.19)$$

where γ and β are the skewness and kurtosis, respectively. The tables contain the four moments R_p , σ_p , γ and β for Pearson distribution functions extracted from experimental SIMS implantation profiles made for a large variety of target materials, implanted ions and energy range.

Channeling effect can also analytically be modeled. A linear combination of two Pearson distributions is used according to Eq. 2.20. Instead of four parameters, five additional parameters are introduced. The first set of four moments describes the main part of the implanted distribution and the second set of Pearson moments describes the channeling tail and a proportionality factor r indicates the relative weight of the two curves.

$$f(x) = rf_a(x) + (1 - r)f_b(x) \quad (2.20)$$

f_a and f_b are independent Pearson functions with an individual set of parameters a , b_0 , b_1 , b_2 , while r is a proportionality coefficient.

2.3.2 *Physical model*

The analytical models described in the previous section give very good results when applied to ion implantation into simple planar structures (bare silicon or silicon covered with thin layer of other material). But for structures containing many non-planar layers (material regions) and for the cases which have not been studied yet experimentally, more sophisticated simulation models are required. The most flexi-

ble and universal approach to simulate ion implantation in non-standard conditions is the Monte Carlo Technique. This approach allows calculation of implantation profiles in an arbitrary structure with accuracy comparable to the accuracy of analytical models for a single layer structure. ATHENA contains two models for Monte-Carlo simulation of ion implantation: Amorphous Material Model and Crystalline Material Model. Both of them are based on the Binary Collision Approximation (BCA), but apply different approximations to the material structure and ion propagation through it. A beam of fast ions (energy range, approximately 50 eV/amu to 100 keV/amu) entering crystalline or amorphous solid is slowed down and scattered due to nuclear collisions and electronic interaction. Along its path, an individual projectile may create fast recoil atoms that can initiate collision cascades of moving target atoms. These atoms can either leave the surface (be sputtered) or deposited on a site different from their original one. Together with the projectiles being deposited in the substrate, this results in local compositional changes, damage creation and finally amorphization of the target. Depending on the crystal orientation and/or the direction of the beam, the implanted projectiles and the damage created by them has different spatial distribution. With even more higher fluency, these phenomena will cause collisional mixing in a layered substances, changes of the surface composition due to preferential sputtering, and the establishment of a stationary range profile of the implanted ions.

The paths of the individual moving particles and their collisions are modeled by means of the binary collision approximation for a crystalline, polycrystalline and amorphous substance, using a screened Coulomb potential for the nuclear collisions and a combination of local and nonlocal free-electron-gas approximation for the electronic energy loss. For each nuclear collision, the impact parameter and the Azimuthal Deflection Angle are determined according to the crystal structure using its translational symmetry. For amorphous materials, the impact parameter and the azimuthal deflection angle are determined from random numbers. A proper scaling is chosen so that each incident projectile (pseudoprojectile) represents an interval of implantation fluence. The creation of vacancy is not physically modeled in ATHENA. It assumes that the vacancy concentration is proportional to the number of implanted species, which is in contradiction with the literature which gives the

damage creation proportional to the square root of the dose ϕ or limited to a certain threshold [20],[21]. ATHENA models the amorphization probability of the struck lattice point according to Eq. 2.21:

$$f(r) = 1 - \exp \left[\frac{\Delta E(r)}{E_c} \right] \quad (2.21)$$

where $\Delta E(r)$ is the nuclear deposited energy at the considered impact point r and E_c the critical energy density, which represents the deposition energy per unit volume needed to amorphize the structure in the relevant volume. E_c follows an Arrhenius law according to Eq. 2.22

$$E_c(T) = E_{c0} \left\{ 1 - \exp \left[\frac{E_0 (T - T_\infty)}{2k_B T T_\infty} \right] \right\} \quad (2.22)$$

where E_{c0} is the activation energy, k_B the Boltzmann's constant, and T_∞ the temperature at and above which, the infinite dose is required for crystalline to amorphous transition. As this model is empirical and necessitates to tune E_{c0} and T_∞ , it might not gives good result in every range of dose, energy and might change in function of the type of implanted specie.

SRIM developed by Ziegler, is the most complete tool. Quick damage or fully cascade calculation can be performed. Atoms displacement, vacancy creation, electronic and nuclear energy loss, phonon energy dissipation can be calculated. Monte Carlo calculation are identical in principle to the one done in ATHENA, in the sense of calculating the trajectory of each ions ions and recoils atoms between every collisions, but the physical models used are more advanced concerning damage creation and dissipation of phonons. The disadvantage of SRIM is that it is not possible to calculate two dimensional profiles and that it does not take into account the crystalline structure of the target.

2.3.3 Comparison of analytical and physical models

The data tables used by ATHENA for analytical calculation of implantation are very accurate when they are simulating an implantation in exactly the same conditions than the reference implant of the sample on which the SIMS profile is included in the database. Table 2.1 indicates in which conditions of dose, energy, tilt and rotations

angles and for which species SIMS profiles have been made for implantation in (100) silicon. Analytical simulation for species within this range of implantation condition and species are very accurate because they are fitted on experimental SIMS profiles.

Ions	Energy (keV)	Dose (cm^{-2})	Tilt Angle ($^{\circ}$)	Rotation angle ($^{\circ}$)	Screen oxide ($\text{\AA}$)
B	1-100	10^{13} - 8×10^{15}	0-10	0-360	native - 500
BF_2	1-80	10^{13} - 8×10^{15}	0-10	0-360	native
P	12-200	10^{13} - 8×10^{15}	0-10	0-360	native
As	1-200	10^{13} - 8×10^{15}	0-10	0-360	native

Table 2.1: Range of validity of the Pearson model in ATHENA.

Fig.2.3.3 compares analytical and physical calculations of Boron implantation for the Single Pearson, Dual Pearson with Monte Carlo simulation from ATHENA and SRIM in bare silicon and in a polysilicon film. There are two analytical models, a Crystalline Material Model and the Amorphous Material Model. The Crystalline Material Model is combination of two Pearson distribution, while the amorphous material model describes the distribution of implanted ions by the way of a single Pearson distribution. There are three physical models, Monte Carlo calculations from SRIM, Crystalline and Amorphous Material Monte Carlo Models for ATHENA. SRIM and the Amorphous Material Model of Athena do not take into account the crystallographic properties of the target. The Crystalline Material Model from ATHENA takes into account the crystallographic properties of the implanted target and models thus the channeling effect.

For crystalline silicon the Dual Pearson model is assumed to be the most accurate as directly fitted on an experimental SIMS profile performed on a sample which has been implanted at the same dose and energy as the simulation. The single Pearson distribution neglects totally the channeling effects and compensates the broadening of the real distribution of the implanted species by a higher concentration at the mean projected range R_P .

The physical models which do not take the crystalline properties of the material

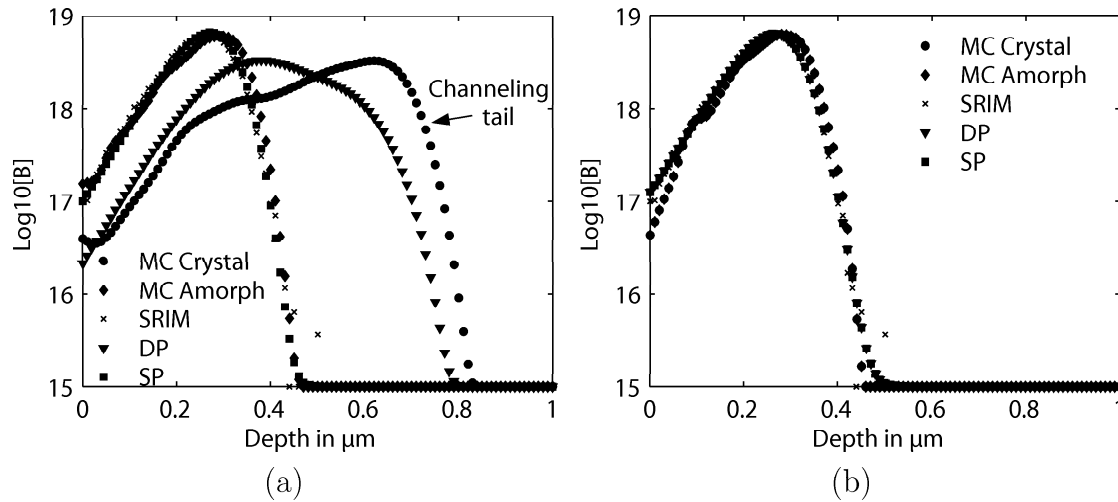


Figure 2.9: Simulation of Boron implantation at 75 keV and at a dose of 1×10^{14} atm/cm^2 and a tilt of 0° in (a) Si (100) and (b) polysilicon, both initially boron doped at 1×10^{15} atm/cm^3 with 5 different models. MC Crystal: Monte Carlo calculation of Crystalline Material Model from ATHENA, MC amorphous: Monte Carlo calculation of Crystalline Material Model from ATHENA, SRIM: Monte Carlo calculation using the SRIM code, SP: Single Pearson analytical model, DP: Double Pearson analytical model.

into account such as SRIM and Amorphous Material Model from ATHENA, underestimate the channeling effect. The distribution profile that they calculate is close to the one of a single Pearson analytical distribution. The physical Crystalline Material Model overestimates the channeling effect. This model takes into account the crystallographic properties of the target material, but during implantation, amorphization of the target occurs and the channeling effects decreases. For very high doses at the end of the implantation the target is amorphized and the implantation behaves like an implantation in an amorphous target. As described in Eq 2.21 and 2.22 the modeling of amorphization occurring during implantation is considered in ATHENA according to an empirical law. The parameters E_{c0} and T_∞ should be tuned to give more weight to amorphization during implantation.

In the case of polysilicon, there is no long range order in the position of the target atoms which are supposed to be randomly distributed. The three Monte Carlo models find thus the same result. The analytical description is done with a single Pearson distribution. The physical and analytical models perfectly fit.

Fig 2.10 compares the 5 models for the simulation of implantation in a SOI wafer. The crystalline silicon film thickness is 100 nm, the buried oxide thickness is 400

nm thick. Silicon dioxide being an amorphous material the 5 models give almost

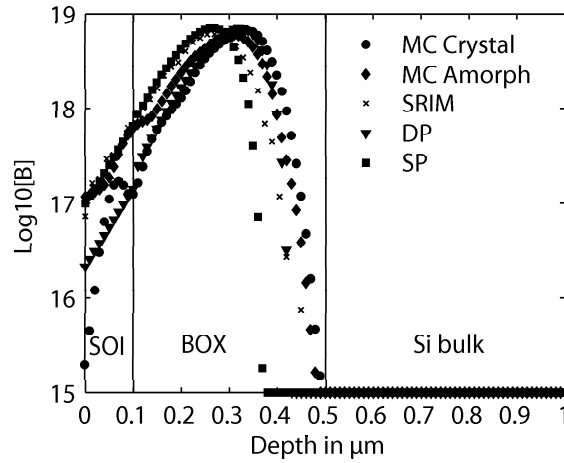


Figure 2.10: Simulation of Boron implantation at 75 keV and at a dose of 1×10^{14} atm/cm² and a tilt of 0° in a SOI film with 5 different models. MC Crystal: Monte Carlo calculation of Crystalline Material Model from ATHENA, MC amorphous: Monte Carlo calculation of Crystalline Material Model from ATHENA, SRIM: Monte Carlo calculation using the SRIM code, SP: Single Pearson analytical model, DP: Double Pearson analytical model.

the same result for implantation through the oxide film. The difference in final ion distribution arises from the channeling effect which is taken into account by the Monte Carlo Crystalline Material and the Dual Pearson models in the SOI film.

These 5 models differ in their degree of modeling which is of course directly linked to the computation time. Table 2.2 plots the simulation time needed for the simulation of the implantation from Fig. 2.10.

Model	SRIM	Monte Carlo Crystal	Monte Carlo Amorphous	Dual Pearson	Single Pearson
Computation time (s)	300	35	15	1.5	1.5

Table 2.2: Comparison of the computation time for the analytical and physical models.

In conclusion, the analytical models based on experimental SIMS profiles give good results for one dimensional simulations in the case of implantation conditions exactly similar to the one of the SIMS profile. Single Pearson models are used for amorphous materials and Double Pearson are used for crystalline materials. Multilayered and two dimensional structures have to be simulated with the Monte Carlo

models from ATHENA, as the analytical models do not give any physical calculation for the two dimensional profiles. The amorphous materials are sufficiently described by the Amorphous Material model in a shortest computation time. The main drawback of the Monte Carlo and analytical models from ATHENA is that they do not simulate the damage creation to the lattice. SRIM is the appropriate software for this kind of calculations, although it is not suitable for crystalline materials and two dimensional structures. The simulation tool and model must then be chosen in function of the kind of expected result.

2.4 Etch rate modification by ion implantation

The previous sections presented ion implantation, from physical model to numerical simulation. Three main consequences of ion implantation on the implanted material will focus our attention because of their impact on etch rate modification process:

- breaking of covalent bonds;
- modification of internal stress due to the presence of substitutional atoms;
- modification of semiconducting properties by doping.

The breaking of covalent bonds arises for every high dose implantation, and remains as long as the implanted sample has not been annealed. It can make the target material more reactive to some chemicals. It is the case of silicon dioxide which is etched faster in hydrofluoric after ion implantation.

Substitutional atoms occupy lattice site of the target atoms. As impurities are in very small proportion in the target material, the lattice parameter will remain the same as for undoped material. However, if the substitutional impurities do not have the same atomic radius than the lattice atoms, there is a tendency for the matrix to contract or to expand locally. However, the lattice restrain or to contract or to expand and it results in tensile or compressive stress. Tensile stress in boron doped silicon reduces the reactivity with Tetramethyl Ammonium Hydroxide (TMAH).

Doping of semiconductors moves the Fermi level towards the edge of the bandgap. It results under no bias conditions in a larger concentration of free carriers in the semiconductor. Some electrochemical reactions are possible only in the presence of

free carriers. Etch rate of silicon in a mixture of fluorhydric, acetic and nitric acids (HNA) is tremendously enhanced for doped silicon.

All of these three effects will be detailed in the following subsections, with a description of the etching mechanism and a description of the selectivities that can be reached.

2.4.1 Breaking of covalent bonds: Etching of implanted silicon dioxide

We develop in this section a highly selective etching of implanted oxide. Based on literature which mentions etch rate increase of implanted oxide, we characterize the impact of ion implantation with the nuclear deposited energy. We then improved the etching selectivity up to 200.

From mid 80's to 90's several research groups have published experimental results on etch rate modification of silicon dioxide by ion implantation [22],[23],[24]. As explained in the previous section ion implantation is responsible for destruction of the covalent binding between oxide and silicon atoms. The destruction of the covalent binding makes the oxide more reactive to HF etching and enhances the etch rate. The literature reports selectivity of 5 between implanted and unimplanted oxide [24]. We investigated this effect to get a better understanding of the phenomena and to improve the selectivity.

2.4.1.1 Etch rate increase in diluted HF due to bond breaking

3000 Å of thermal oxide were grown in wet ambient at 1000 °C on 3 inches p-type, (100) oriented silicon wafers. The oxide thickness was accurately measured by ellipsometry. A photolithography was done before the implantation defining implanted and unimplanted zones. Boron, Phosphorous, Argon and Arsenic were implanted at different energies and doses in the oxide layer through the photoresist mask. After implantation the resist was stripped by oxygen plasma the samples were cleaned in $\text{H}_2\text{O}_2/\text{H}_2\text{SO}_4$ solution and diced in 1 cm² pieces. Fig. 2.11 presents a schematic of the fabricated samples.

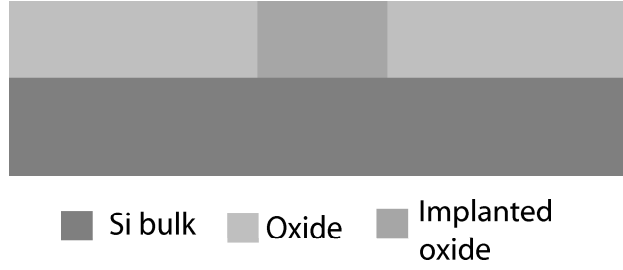


Figure 2.11: Schematic of the implanted oxide samples.

The 3000 Å thick oxide layer has been implanted by argon at an energy of 160 keV and a dose of 2×10^{14} atoms/cm². One sample has been annealed at 950°C during 30 minutes under a nitrogen flow of 1.5 l/min at atmospheric pressure. The etch rate in HF 3% was measured in function of the depth in the oxide layer measured from its top surface. Fig. 2.12(a) superposes the etching rate in function of oxide depth for unimplanted sample, implanted sample and annealed sample. Fig. 2.12(b) superposes the Ar concentration and the etch rate of the as implanted sample. The Ar concentration was calculated with the software SRIM. The wet HF etching was done in 3% HF solution diluted in DI water.

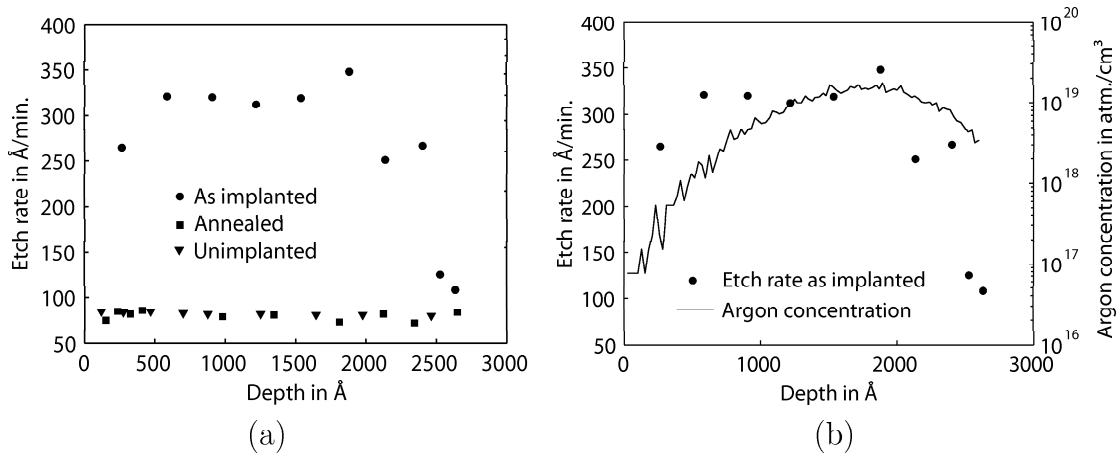


Figure 2.12: Etching in HF 3%. (a) Etch rate of as implanted oxide, annealed oxide and unimplanted oxide in function of depth. (b) Comparison between etch rate and argon concentration.

From the surface of the oxide layer to a depth of 2000 Å the etch rate has a constant value of 300 Å/min for the as implanted sample. From 2000 to 2600 Å, the etch rate drops abruptly to reach a value of 100 Å/min. The argon concentration, plotted in logarithmic scale, is roughly 1×10^{17} atm/cm³ close to the surface, and reaches a maximum of 1×10^{19} atm/cm³ around a depth of 1900 Å. From 2600 Å

the argon concentration is still rather high at a value of 2×10^{18} atm/cm³. It is thus clear that there is no direct correlation between the argon concentration and the etch rate modification. Hiraiwa *et al.* reported that the enhancement of the etch rate is due to the destruction of the Si-O bonds of the silicon dioxide [23]. Thermal annealing of implanted material leads to the reconstruction of the structure which has been damaged through implantation. The etch rate of the annealed sample is constant over the sample depth and moreover has the same value as the unimplanted sample. It proves that the etch rate enhancement of silicon dioxide depends on the destruction of the Si-O bonds.

2.4.1.2 Characterization of damage creation

As seen in the previous section when an ion penetrates a target it undergoes collisions with the atoms of the target until it loses its total amount of energy. Energy loss proceeds through collisions with the nuclei (elastic process) and with the electron shell (inelastic process) [25]. Energy loss through collisions with nuclei depends on ion energy while energy loss through collisions with electron shell depends on ion velocity. Thus electronic energy loss dominates the stopping of an implanted ion at high ion energies (higher than roughly 1 keV per atomic mass unit). However, at low ion energy, or when the ion has slowed down sufficiently, nuclear energy loss becomes significant. As the destruction of the Si-O bonds is due only to target nuclei displacement, we consider as relevant parameter only the nuclear energy loss. To calculate the nuclear energy loss we performed simulations using the SRIM [19] code. The total damage that suffers the target is characterized by the nuclear deposited energy E_n given by Eq. 2.23.

$$E_n = DS_n \quad (2.23)$$

where D is the implanted dose and S_n the nuclear energy loss defined in the previous section in Eq. 2.4.

We were able to simulate the nuclear energy loss per ion in function of the depth in the sample. Fig. 2.13 plots the nuclear deposited energy and the etch rate for as implanted and annealed samples in function of the depth into the silicon dioxide

layer.

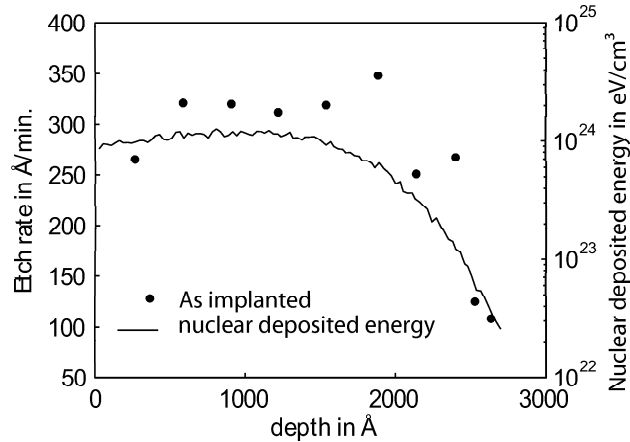


Figure 2.13: Etching in HF 3%. Etch rate of as implanted oxide versus the nuclear deposited energy.

The nuclear deposited energy has a constant value of 8×10^{23} eV/cm³ from the surface to a depth of 1600 Å and then decreases logarithmically. The nuclear deposited energy and the etch rate curves of the as implanted sample perfectly superpose to each other. This result demonstrates that the destruction of the Si-O bonds, characterized by the nuclear deposited energy is the mechanism responsible for the enhancement of the etching rate.

As the etch rate enhancement depends on the amount of damage created during implantation it is theoretically possible to implant any kind of ions to damage the silicon dioxide. Tests have been performed with the conventional ions used in the microelectronic industry, Boron, Phosphorous, Argon and Arsenic. As these ions do not have the same mass, their nuclear energy loss S_n will differ at constant projected range R_p . Indeed, when an ion penetrates a solid it is decelerated through the collisions with electrons and nuclei. For ion energies lower than 25 keV/amu, which is the case in the energy range we are dealing with, the electronic stopping power varies linearly with the ion velocity. Below 1 keV/amu, the electronic stopping power is negligible compared to the nuclear energy loss, but above 1 keV/amu almost all the energy is dissipated through collisions with the electrons. It means that damage creation will be more effective for heavy ions at a given energy or at relatively low energy for a given ion mass. However, at low energy heavy ions do not penetrate deeply into the substrate whereas light does. Fig. 2.14 plots the value of the nuclear deposited energy at the surface and the projected range versus ion energy for Boron,

Phosphorous, Argon and Arsenic.

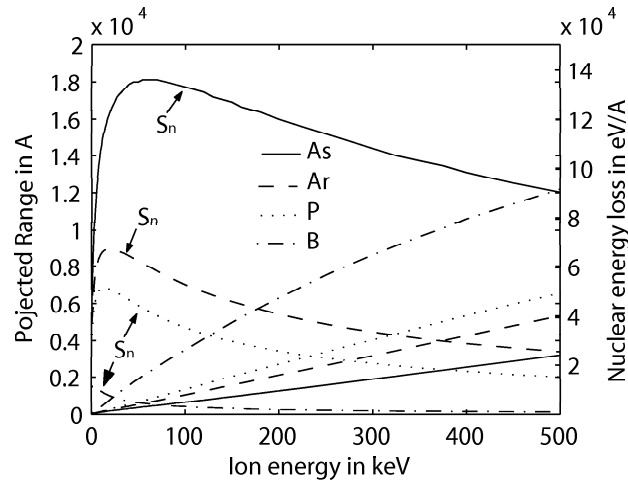


Figure 2.14: SRIM simulation of the Projected range and the nuclear energy loss versus ion energy for B, P, Ar and As implanted in silicon dioxide.

It appears clearly that although light ions penetrate deeply into the substrate, their contribution to surface damage is very small. Table 2.3 gives the value of the nuclear energy loss at a given maximum of the nuclear energy loss.

Specie	Energy in keV	R_p in Å	depth of maximal S_n in Å	maximal S_n in eV/Å
B	60	2240	1800	10.3
P	160	2173	1800	43
Ar	220	2350	1800	58
As	340	2215	1800	123

Table 2.3: SRIM simulations of R_p and S_n at Energies such that the peak in S_n occurs at the same depth for Boron, Phosphorous, Argon and Arsenic.

If one wants to use heavier ions making use of their higher nuclear energy loss, one has to increase drastically the energy to damage the target over the same depth. On the other hand, making use of light ions has to be compensated by an increased dose. A trade-off has to be found between the dose and the couple ion mass / ion energy. The limitation in energy of the implanter is most of the time the determining factor. It is of interest to note that the projected range is deeper than the maximum of nuclear energy loss. This results from the fact that the ions lose their energy before getting to rest.

As at UCL our EATON implanter is limited in energy to a value of 160 keV,

implantations of Boron, Phosphorous, Argon and Arsenic were thus performed in order to test the etch rate enhancement of oxide through implantation of any species. The implantations were done at two different energies to ensure a constant nuclear deposited energy in function of the depth. The implantation conditions are given in Table 2.4

Specie	Energy in keV	total dose in atm/cm ²
B	23% @ 20 keV	1.8 ¹³ atm/cm ² to 1.8 ¹⁷ atm/cm ²
	77% @ 90 keV	
P	16% @ 50 keV	4 ¹² atm/cm ² to 4 ¹⁶ atm/cm ²
	84% @ 150 keV	
Ar	18% @ 50 keV	1.9 ¹² atm/cm ² to 1.9 ¹⁶ atm/cm ²
	82% @ 150 keV	
As	100% @ 150 keV	7.7 ¹¹ atm/cm ² to 7.7 ¹⁵ atm/cm ²

Table 2.4: Implantation conditions for Boron, Phosphorous, Argon and Arsenic in silicon dioxide.

The Fig. 2.15 plots the nuclear energy loss in function of the depth for the four implants describes in table 2.4.

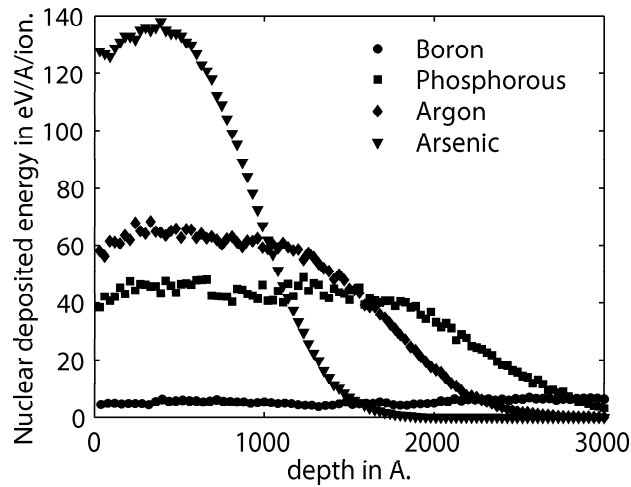


Figure 2.15: SRIM simulation of nuclear energy loss versus depth for B, P, Ar and As implanted in silicon dioxide.

Thanks to these simulations it is possible to calculate the nuclear deposited energy in function of depth. The etch rate is then measured in function of the depth to be correlated to the nuclear deposited energy. Fig 2.16 plots the etch rate of oxide in HF 3% in function of the nuclear deposited energy for different implanted species.

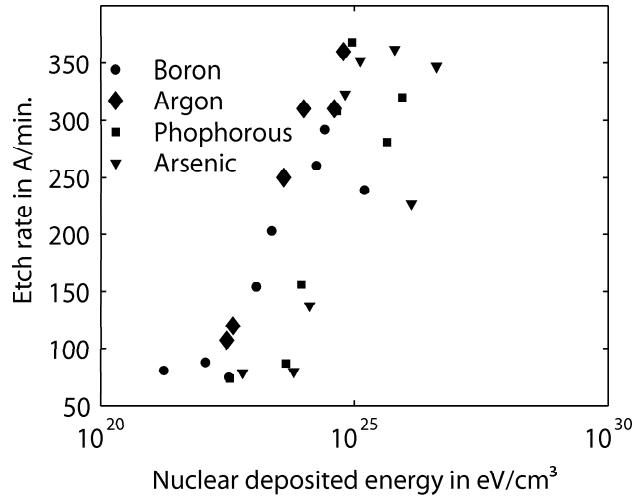


Figure 2.16: Etch rate of B, P, Ar and As implanted in silicon dioxide in HF 3% in function of the nuclear deposited energy.

All of the measured etch rates presented in the graph are for points taken in the depth range where the nuclear deposited energy is constant. Fig 2.16 confirms that the nuclear deposited energy is the main factor for etch rate modification, and that the type of implanted species has a limited influence on the etch rate. A nuclear deposited energy lower than 1×10^{23} eV/cm³ does not change the etch rate of oxide in HF 3%, i.e. 80 Å/min. Above 3×10^{24} eV/cm³, the etch rate saturates at an average value of 320 Å/min. Garrido *et al.* have shown that not more than 15.5% of the Si-O bonds can be broken [26]. Indeed, they demonstrated that above a certain concentration of nuclear deposited energy a steady state occurs between formation and breaking of Si-O bonds. However the dispersion of the points from Fig. 2.16 is large. This dispersion can be attributed to the error measurement of the etched thickness and to the fact that simulation of the damage does not take into account the fluence of the ion implantation, which has an impact on the amount of defects created into the target [27]. Moreover our implanter being quite old, the implantation current cannot be fixed to a chosen value from one implantation to another. In order to decrease the implantation time, high doses implantation were processed at high current. The wafer holder was cooled to -25 °C during implantation but as the wafer is not tightly bonded to the holder due to the presence of a joint, the heat brought by the implantation cannot be evacuated efficiently and the sample heats up. Fig. 2.17 shows the photoresist after a high dose implantation done in one pass. The photoresist is totally damaged after this high dose implantation, which

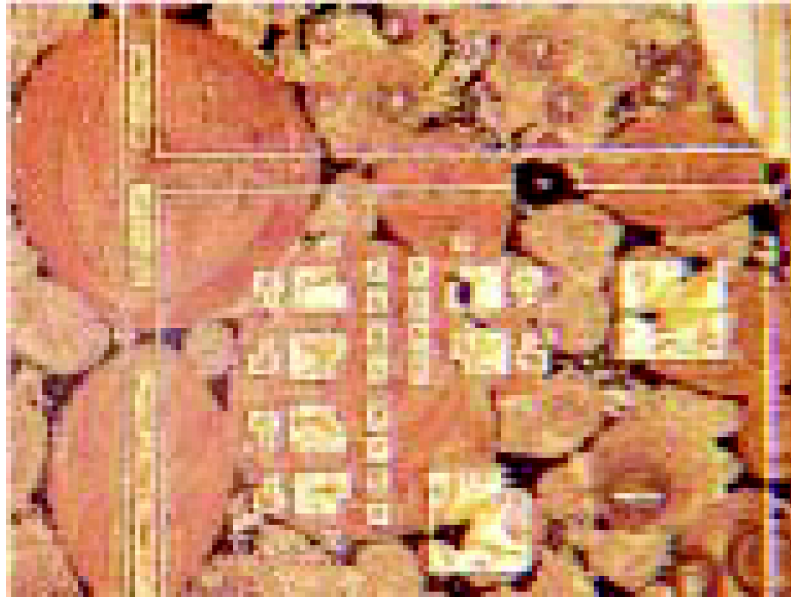


Figure 2.17: Optical microscopy of the wafer after an 170 keV phosphorous implantation at a dose of 2×10^{15} . atm/cm^3 . The photoresist mask is damaged.

means that the temperature of the wafer increased during implantation. To avoid photoresist destruction the high dose implantation were done in several time, in order for the wafer to cool down between the implantations.

Although the impact of the ion fluence on the damage creation has not been extensively studied, but as the heating of the wafer during implantation affects the damage creation during implantation, the impact of RTA on the etching selectivity has been measured [28].

Fig. 2.18 shows the evolution of the etching selectivity in function of the anneal temperature. The annealing was performed by RTA during 1 min. The etch rate was measured in BHF, solution in which the etching selectivity of as implanted sample is 2. Below a RTA temperature of 60 s at 400 °C, the etching selectivity between implanted and unimplanted oxide does not vary. Above this threshold it linearly decreases when increasing the temperature. This results let us suppose that the high implantation current needed to implant the sample and the subsequent heating of the wafers could be responsible for the dispersion observed in the measurement from Fig. 2.16

We can conclude from this subsection that the destruction of the bonds due to implantation is responsible for the enhancement of the oxide etch rate in HF solution. In a 3% HF concentrated solution a selectivity of 4 can be reached between implanted

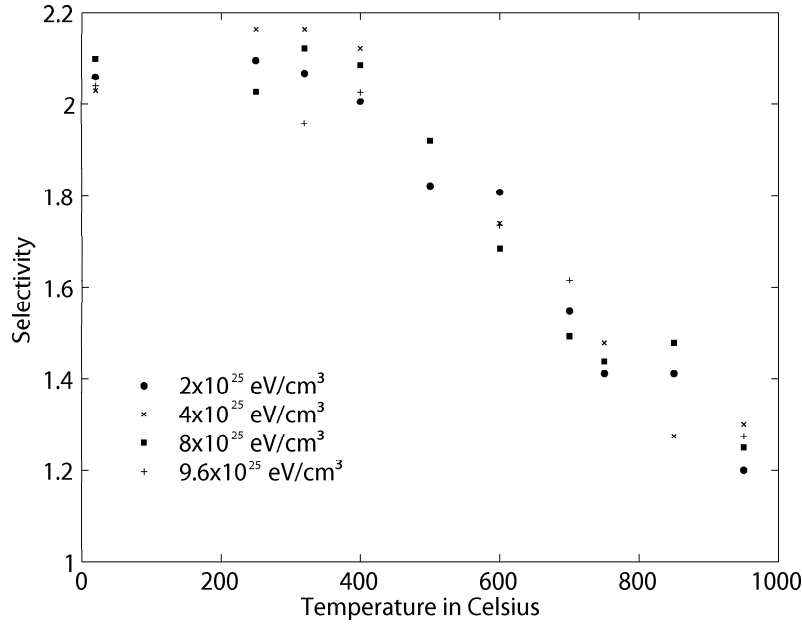


Figure 2.18: Etching selectivity in BHF in function of the RTA temperature. Etch rate of as implanted oxide versus the nuclear deposited energy.

and unimplanted silicon dioxide layer.

2.4.1.3 Improved Selectivity

Although the etch rate modification of silicon dioxide in hydrofluoric acid and the understanding of the physical mechanism driving the enhanced etch rate are of scientific interest, a selectivity of 4 is too low to be of any interest in microelectronic processing and could yield process fluctuation due to the weak control of the oxide etch rate. We put therefore an effort into increasing the etching selectivity by etching the sample in vapor HF [29].

The vapor HF etching was performed on a GEMETEC PAD-Fume (Fig. 2.19), commercially available system for wafer cleaning that was adapted according to custom specifications to enable stiction-free surface micromachining. The gas flow (nitrogen bubbling through a 49% HF solution) was 1 l/min and the temperature was 38°C.

Etching steps were performed during time periods of two or five minutes, depending on the etch rate of the implanted oxide. Fig. 2.20 plots the etch rate in function of the nuclear deposited energy for the boron and phosphorous implanted samples.

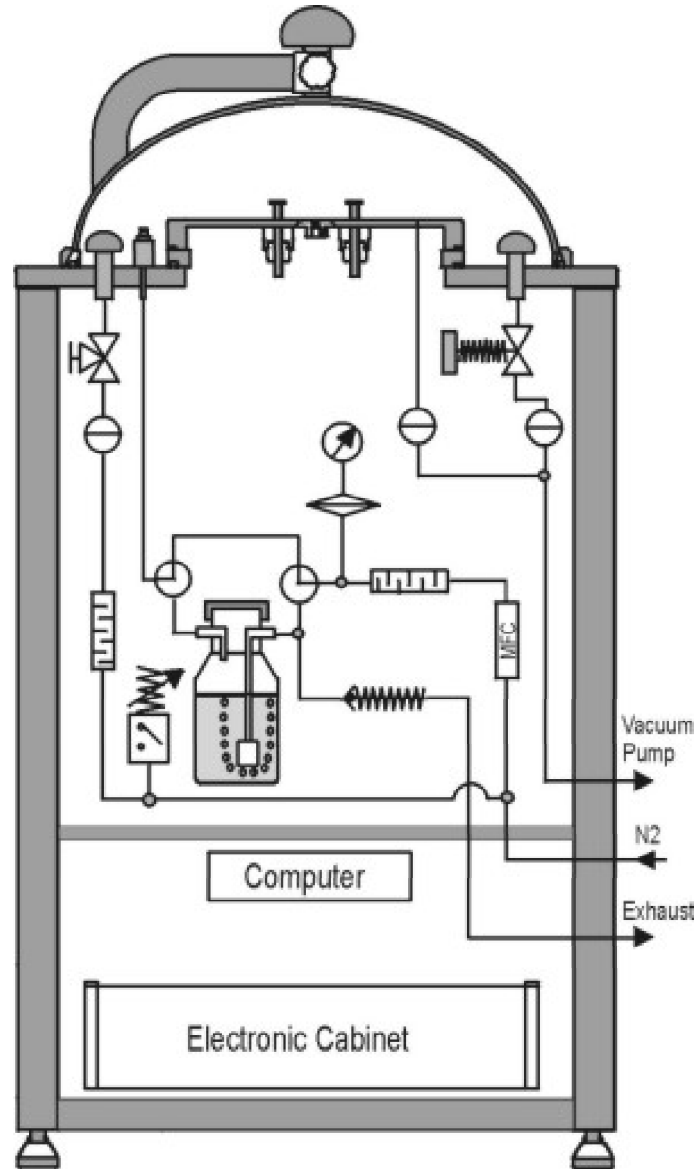


Figure 2.19: Schematic of the HF-vapor equipment [30].

The increase in etch rate occurs for the same concentration of nuclear deposited energy as in the case of the wet etching, but the etching selectivity between implanted and unimplanted oxide which was around 4 in the case of wet etching is in the range of 200 for vapor HF etching. The great etching selectivity difference between liquid and vapor HF can be easily explained knowing the etching mechanism of SiO_2 by HF. The etching of silicon dioxide in vapor HF has been well described in several

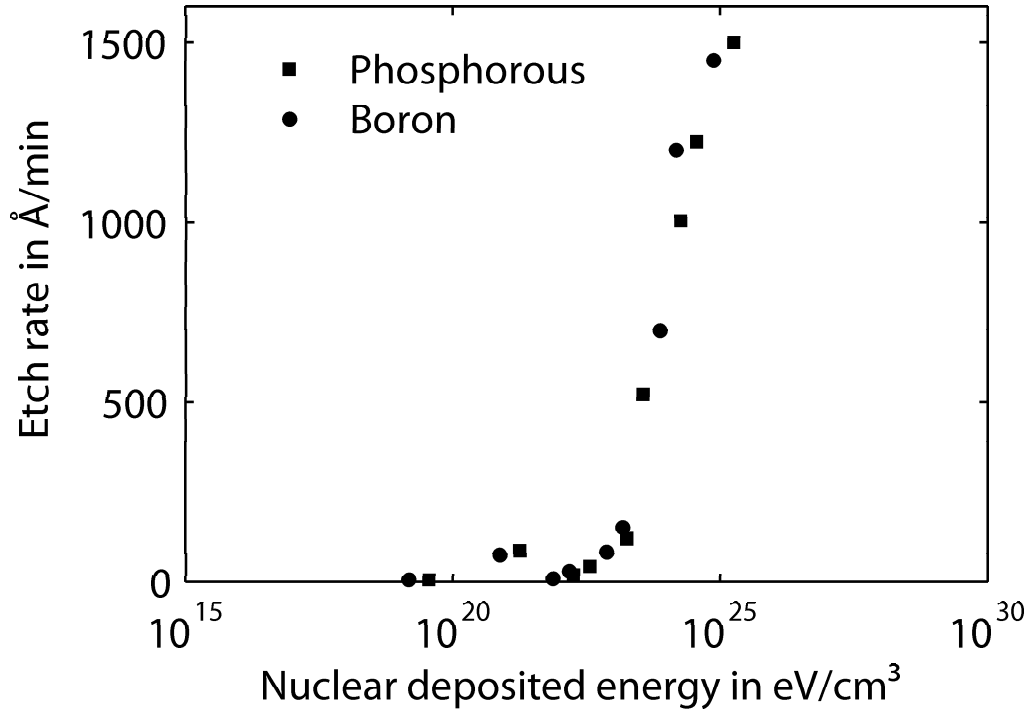
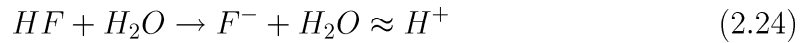


Figure 2.20: Etch rate of B and P implanted in silicon dioxide in VHF in function of the nuclear deposited energy.

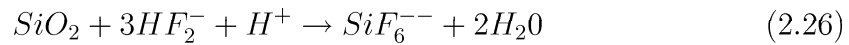
publications [31],[32],[33]. Water plays a key role in the etching. Its presence is necessary to trigger the reaction. First of all, HF is decomposed into a H^+ ion and a F^- ion thanks to H_2O molecule:



The fluorine ion binds to HF:



HF_2^- is the ion responsible for the oxide etching:

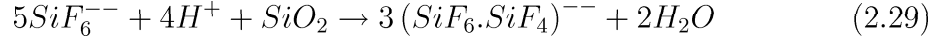


The reaction produces water and fluosilicic acid. The fluosilicic acid undergoes the following reaction:



SiF₄ evaporates and HF is re-used by the reaction.

Fluosilicic acid can also attack the oxide following the reaction:



However, SiF₆⁻⁻ is easily recombined in presence of H⁺ ions into H₂SiF₆ so that Eq. 2.29 is of minor importance in the etching of silicon dioxide.

As described above, in vapor HF the etching mechanism needs water to initiate the reaction. Condensation has to occur on the wafer surface for starting the reaction. Once the reaction has started, water is produced by the reaction and immediately re-used for a new reaction cycle enhancing thus the etch rate by avalanche effect. The etch rate will strongly depend on the amount of water produced by the etching. In the case of the wet etching, the quantity of water as product of the reaction is negligible in comparison to the water quantity of the solution and immediately dissolved and therefore does not influence the kinetic of the reaction. The etch rate mainly depends on the HF, HF₂⁻ and broken bonds concentration, but not on the reaction byproducts. In the case of vapor etching, water is the limiting factor of the reaction kinetic. Water from the 49% HF solution condensates on the surface and initiate the reaction but after a transition step the main origin of the water is from reaction byproducts. The avalanche effect will thus be multiplied by the higher reactivity of the oxide due to the presence of broken bonds and the fact that more water is produced in the damaged zone than in the non implanted oxide. Selectivity of 200 can thus be achieved.

2.4.1.4 Conclusion

The etch rate increase of oxide through damage creation due to implantation has been verified in diluted HF for various implanted species. The parameter which

controls the etch rate is the nuclear deposited energy, E_n which depends on the atoms of the target, the mass and the dose of the implanted ions. For a nuclear deposited energy lower than 1×10^{23} eV/cm³, the etch rate is not modified and for a nuclear deposited energy larger than 3×10^{24} eV/cm³, the etch rate reaches its maximum value. Light or heavy ions can both be implanted. Heavy ions will have a shallow penetration while the light ions will penetrate deeper in the film. To reach the same level of nuclear deposited energy, higher dose has to be considered for light ions as their nuclear energy loss is lower than for heavy ions. The use of vapor HF etching instead of diluted HF increases the selectivity from 4 to 200. The dissolution of silicon dioxide in HF is an auto catalytic reaction which only needs water to be initiated. In vapor HF etching, the water produced by the reaction will be preponderant compare to the total amount of water taking part to the reaction yielding to an avalanche effect and a drastic increase of the etch rate. This very high selectivity opens very promising applications such as buried mask patterning in oxide and definition of sacrificial layers which will be presented in Sec. 3.2.

2.4.2 Modification of internal stress: Etch stop properties of boron doped silicon

TMAH etching is a widely used etching solution in silicon micromachining. The etch stop properties of boron doped silicon are also known. Thanks to an extensive bibliography the anisotropic property of TMAH etching and the etch stop properties of boron doped silicon are explained. We then characterize the etch stop property of boron doped polysilicon in several TMAH solutions.

Boron doped silicon is nowadays widely used in MEMS micro machining as etch stop layer for etching in alkaline Si etching solutions such as Tetramethylammonium hydroxide (TMAH), Potassium hydroxyde (KOH) and Ethylenediamine pyrocatechol (EDP) [34],[35],[36]. Selectivity of 40 between doped and undoped silicon is achieved in TMAH solution [37]. The mechanism suspected for etch rate decrease of boron doped silicon is the tensile stress induced in the silicon lattice by substitutional boron atoms, since boron atoms present a smaller atomic radius compared to silicon atoms [38],[39],[40]. Boron doping can be done by ion implantation or diffu-

sion. In the case of implantation, an annealing has to be done in order to activate the boron atoms, by filling a substitutional sites. The RTA mechanism necessary to move the boron atoms at substitutional sites and the consequences of the induced strain are described in the following paragraphs.

2.4.2.1 *Boron: from implantation to substitutional site*

When crystalline silicon is implanted with boron, immobile dopant interstitial complexes are observed after moderate thermal treatments [41]. These boron complexes are commonly referred to as boron-interstitial clusters (BICs). The BICs have an average size of 2 nm. Several models involving reactions between boron and silicon interstitials to form BICs have been proposed [42], [43]. The exact path of the evolution is not known, but generally the final precipitate is believed to be a SiB_3 complex as predicted by the silicon-boron phase diagram [44]. BICs cannot be directly observed by TEM, however, the formation of BICs reduces the formation of $\{311\}$ defects. Law and Jones observed this by noting the reduction in trapped silicon interstitials in $\{311\}$ defects in the presence of boron [45]. Sztucki *et al.* and Bisognin *et al.* have shown that the presence of BICs induces a compressive strain to the lattice [46],[47]. However, the BICs dissolve during RTA and contribute to the TED through the same mechanism than the $\{113\}$ rod defects [48]. The boron atoms originating from the BICs take place at substitutional sites.

2.4.2.2 *Stress induced by substitutional boron*

The boron atom are much smaller than silicon with a radius of 0.88 Å versus 1.17 Å for silicon. As the smaller boron atoms displaces the silicon atoms there is a tendency for the lattice to contract locally as illustrated in Fig. 2.21,[49],[50],[51]. Si - B bonds are shorter than Si - Si bonds and one single boron atom can exert a 0.0141 Å lattice contraction per atomic percentage of boron in silicon at room temperature [52]. At high concentrations significant strain values can result due to a lattice mismatch between the silicon substrate and the boron. The strain ϵ can be assumed to be proportional to the boron proportion C_p , as follows [53], [54], [55]:

$$\epsilon = \beta * C_p \quad (2.30)$$

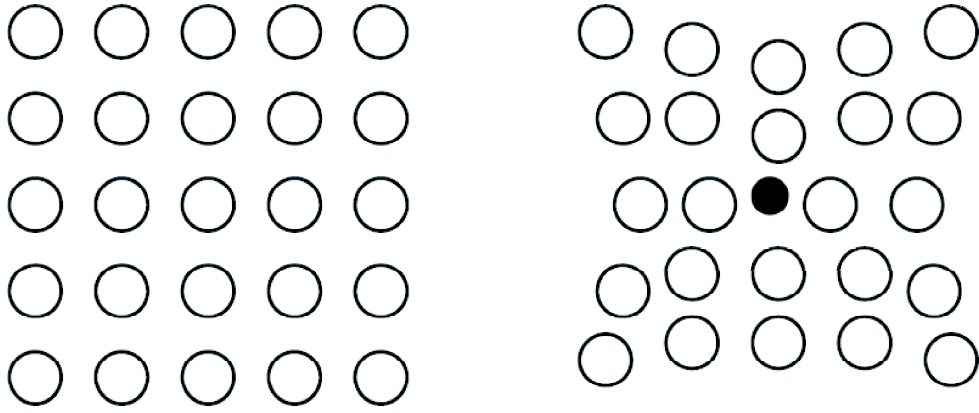


Figure 2.21: Lattice contraction from Boron

with β the lattice contraction coefficient defined as:

$$\beta = \frac{r_{Si} - r_B}{r_{Si}} \quad (2.31)$$

with r_{Si} and r_B the atomic radii of, respectively, the silicon and boron atoms. Eq. 2.31 assumes a linear model and adopts the convention that a tensile strain and stress are defined as positive. The boron proportion C_p is defined as the ratio of the boron concentration over the silicon concentration, which is for crystalline silicon of 5×10^{22} atm/cm³. This β value is in agreement with that determined by Horn [52] and nearly twice as much as the value reported by Pearson and Bardeen [56] which was measured on polysilicon, where grain boundary segregation of boron is expected. The weak effect of boron on polysilicon strain has to be pointed out and will be detailed in the future section. The stress distribution σ in the p⁺ layer can be assumed as biaxial and expressed as:

$$\sigma_{xx} = \sigma_{zz} = \sigma \quad (2.32)$$

$$\sigma_{yy} = 0 \quad (2.33)$$

with the surface wafer parallel to the x - z plane and normal to the y axis.

According to Timoshenko and Goodier and Prussin, for non symmetrical, *i.e.* one side diffusion, the stress $\sigma(y)$ caused by boron diffusion at depth y is given

by [57],[54]:

$$\sigma(y) = \frac{\beta E}{(1 - \nu)} \left[C_p(y) - \frac{1}{t} \int_0^t C_p(y') dy' - \frac{12(y - 0.5t)}{t^3} \int_0^t C_p(y') (y' - 0.5t) dy' \right] \quad (2.34)$$

where E and ν are respectively the Young modulus and the Poisson coefficient of the silicon and t the wafer thickness. The last term of Eq. 2.34 gives the stress release by buckling of the wafer, while the second term on the right hand side of the equation defines the position of the neutral plane $[\sigma(y) = 0]$. Since the thickness of the diffused layer is quite small compared to the wafer thickness, those two terms have only minor contributions to the stress distribution in the p^+ silicon layer. Therefore, the elastic stress $\sigma(y) = 0$ in the p^+ layer is basically the first term of the right side in Eq. 2.34. The numerical solution of this equation using for $C_p(y)$ the boron concentration profile obtained after implantation and annealing indicates that the p^+ layer is always under tensile stress, while the compressive stress in the region has very low boron concentration. It should be noted that the stress calculation proposed in Eq. 2.34 is based on the assumption that the stress is a pure elastic one, *i.e.*, no dislocation is introduced in the layer.

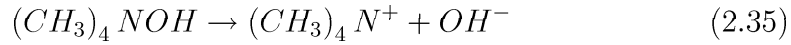
Ning *et al.* showed that under high temperature anneal dislocations are generated at the surface where dislocations semi-loops can nucleate and propagate down to the low stress region [58]. The dislocations release the strain energy. Oxidation of doped silicon has also an impact on stress [59]. The oxide grown creates a compressive stress and might also create dislocations due to the extra thermal budget necessary to perform the oxidation.

2.4.2.3 TMAH etching chemistry

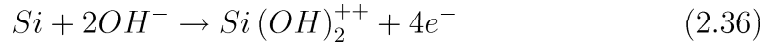
All common alkaline silicon etchants exhibit anisotropic etching properties and an etch rate reduction at high boron doping. However, potassium hydroxide (KOH) causes potassium contamination, which can strongly affect the behavior of the microelectronics devices, ethylenediamine pyrocatechol (EDP) has the drawback of being highly toxic and carcinogenic, which causes manipulation and environmental problems [60]. Tetramethylammonium hydroxide (TMAH) is also toxic but has

been chosen to perform anisotropic etching because of its etching selectivity toward aluminum when adding ammonium persulfate and silicon powder to the etching solution [61],[62],[63],[64],[65]. The generally accepted silicon etching process in TMAH starts with the diffusion of the reactant molecules to the silicon surface which then adsorb on to the silicon surface leading to the occurrence of the surface reaction. The final step in the etching process would be the desorption of the reaction products and dissolution of the desorbed products into the solution. The reaction that represents TMAH etching of silicon can be decomposed in the following steps [66],[67],[68],[69],[70]:

- Dissociation of TMAH to form hydroxyl ions responsible for silicon etching.

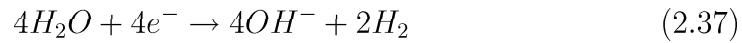


- Binding of hydroxyl ions on the unpaired electrons of the silicon surface dangling bond through the Helmholtz layer. The ion ionization energy is weak (near 0.35 eV) and thus this reaction occurs very rapidly.

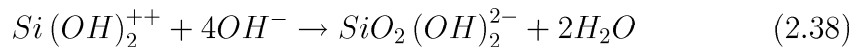


The four electrons are absorbed in the conduction band.

- Hydrogen reduction and formation of OH^- by reverse injection of electrons from the conduction band.

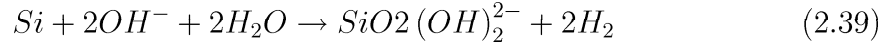


- Binding of the $Si(OH)_2^{++}$ compound with hydroxyl ions and removal of the Si complex. The activation energy for this step is higher as the Si-Si bonds between the Si complex and the Si bulk have to be broken.



$SiO_2(OH)_2^{2-}$ is a water soluble silicate complex.

The etching of TMAH can be resumed by the overall reaction:



It can be seen from Eq. 2.39 that the presence of water will enhance the etch rate as long as enough hydroxyl ions are produced by TMAH dissociation. Thong *et al.* reported that silicon etch rate increases with TMAH concentration to reach its maximum at 5% TMAH in aqueous solution [71]. The etch rate decreases then when increasing further the concentration. Below 5% TMAH the small amount of OH^- limits the reaction at the step described in Eq. 2.36. Above 5% the reaction is limited by the small amount of water which is necessary to reduce hydrogen as shown in Eq. 2.37. Etch rate increases with temperature, following an Arrhenius law. At room temperature no etching is observed. No etching is performed above 90 °C, as the concentration would change due to evaporation.

2.4.2.4 TMAH etching selectivity: Anisotropic etching

One of the main property of alkaline solutions is the anisotropic etching of silicon [72]. The (111) plane of the face cubic centered diamond structure is etched most slowly than any other crystal plane. Therefore the (111) plane is seen as an etch stop boundary which extend completely through the interior of the crystal. The ability to stop the etching on a specific (111) plane depends on the orientation of the (111) crystallographic planes with respect to the etch surface as well as the two-dimensional pattern of the surface etch mask as drawn in Fig. 2.22.

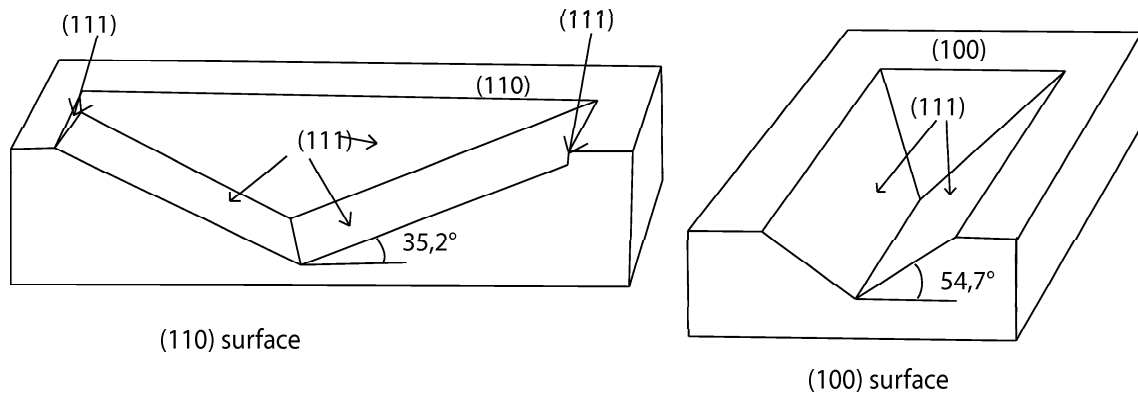


Figure 2.22: Anisotropic etching of silicon in TMAH. Etching stops on (111) plans.

Shikida *et al.*, have measured the etch rate and activation energy in function of the different crystal planes for etching in TMAH 20 wt.% at 80 °C [73],[74],[75],[76]. Table 2.5 gives the etch rates, the etch selectivity with respect to the (100) plane and the activation energy.

Orientation	Etch rate in $\mu\text{m}/\text{min}$	Etching ratio (ijk)/ (111)	Activation energy in eV
100	0.603	37	0.62
110	1.114	68	0.60
221	1.142	69	0.57
320	1.211	73	0.67
111	0.017	1	0.69

Table 2.5: Dependence of the etch rate and activation energy for silicon etching on the crystallographic orientation. Etching in TMAH 20 wt.% at 80°C [73],[74],[75],[76].

The best selectivity is to be found between the plan (320) and (111). However, in microelectronics the standard wafers present a (100) surface with a flat parallel to the (110) plan therefore those two planes are mostly used as etching direction.

The etching dependence on the crystal orientation is not fully understood yet. The literature does not agree on the activation energy for each crystallographic orientation. Steinland *et al.* found activation energy for the (100), (110) and (111) planes, respectively, 0.56, 0.50 and 0.54 eV in TMAH 25% [77]. Those values are lower than those of Shikida *et al.* although the etch rate decreases when increasing the TMAH concentration. This effect is probably due to the stirring of the solution in the experiment done by Steinland *et al.* However, it is difficult to draw a conclusion for the dependence of the etch rate on the crystallographic orientation from the activation energy. Indeed, the planes (221) and (320) have a similar etch rate but their activation energy differs from 0.10 eV. On the other hand, the (320) and (111) plane have a similar activation energy but the etching selectivity is 73 between these two planes.

Bernstein *et al.* calculated the surface energy of unrelaxed (111) and (100) surfaces [78]. They found using the density functional theory a surface energy of 2.5 eV for the unrelaxed (100) surface and 1.56 eV for the unrelaxed (111) surface. The surface energy characterizes the difference in energy from the bulk state (very

stable) to the surface state. The higher the surface energy is the most reactive will be the surface. This energetic approach is in agreement with the experimentally observed etch rates.

Camon *et al.* proposed an atomistic explanation of the anisotropic etching of TMAH [66],[67],[79]. They explained the anisotropy by the increased crystal packing density on the (111) planes and shielding of back bonds. As seen in the previous section, the etching can be decomposed in two steps:

- binding of the hydroxide ion to the unpaired electrons of the surface dangling bonds through the Helmholtz layer. The ionization energy of this surface state is weak and thus this reaction occurs rapidly.
- breaking of the Si-Si back bonds which proceed by electron transfer into the conduction band and successive binding of hydroxide ions which weaken the back bonds' strength. This event is thermally activated.

The difference in etch rate for the three main crystal orientations can be intuitively explained as follow.

- For the (100) plane (Fig. 2.23), the surface atoms have two dangling bonds and two bonds with bulk atoms (which have four bonds). Thus two bonds have to be broken to remove an atom.

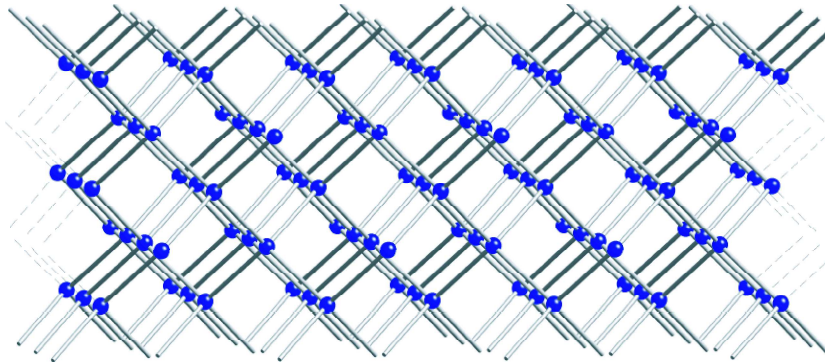


Figure 2.23: Model of the (100) Si surface. The surface atoms have two dangling bonds.

- For the (111) plane (Fig. 2.24), which corresponds to the lowest etch rate, the surface atoms have one dangling bond and three bonds with bulk atoms

(which have four bonds). Thus three bonds have to be broken to remove one atom from the etched surface.

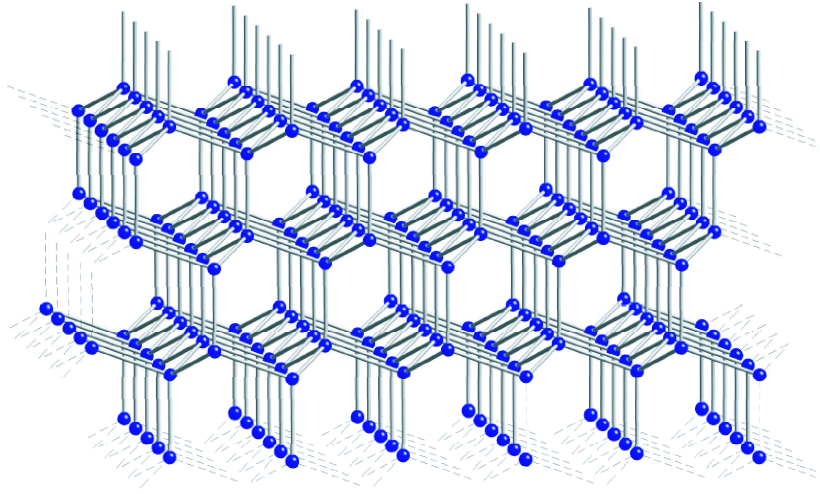


Figure 2.24: Model of the (111) Si surface. The surface atoms have one dangling bonds.

- For the (110) plane (Fig. 2.25), the atoms at the surface have one dangling bond, two bonds with other surface atoms (which have only three bonds) and one bond with a bulk atom (which has four bounds). In this case three bonds also have to be broken, but two of them are connected to three bound atoms instead of four bond atoms as in the case as in the (111) plane. These two bonds are certainly weaker.

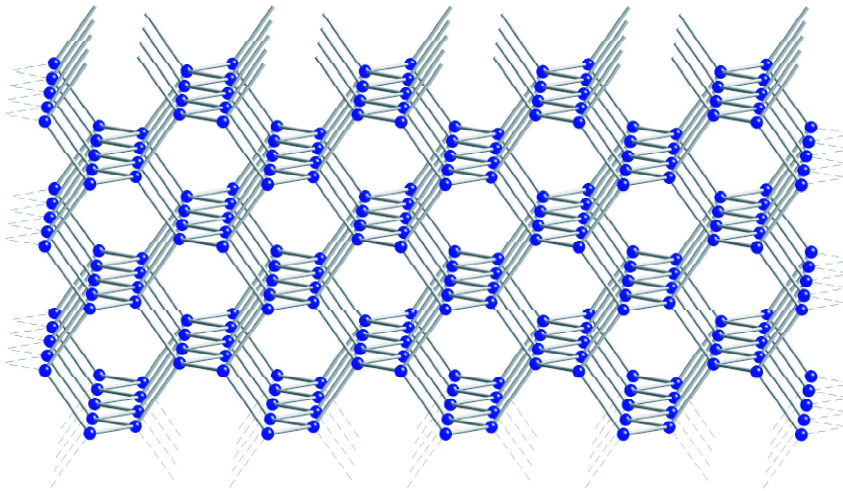


Figure 2.25: Model of the (110) Si surface. The surface atoms have one dangling bonds, two bonds with other surface atoms and one bond with a bulk atom.

The etching of polysilicon is macroscopically isotropic. Indeed, the polysilicon grains are randomly distributed in the space. They thus always present a crystallographic plane which is etched by TMAH.

2.4.2.5 TMAH etching selectivity: Aluminum masking

In order to use TMAH etching as compatible step with our standard CMOS process, selective TMAH etching toward aluminium has been achieved [80].

Excellent results were obtained using optimized chemical passivation of aluminum surface through addition of silicon powder in the etching solution [81]. Dissolved silicon in solution forms aluminosilicates on the metal which are less soluble than the aluminum oxide that would otherwise form at the metal surface. Introduction of silicates also decreases the pH of the solution and therefore lowers the etch rate and work to provide aluminum passivation. Experiments showed that dissolved silicon needed to passivate aluminum increases linearly with the etchant concentration. Since it is undesirable to dissolve excessive amounts of silicon in the etching solution, lower TMAH concentrations are preferable. Therefore, a TMAH 5% solution was used at a working temperature of 80°C with 16g/l of Si powder required to passivate aluminum. Silicic acid ($\text{Si}(\text{OH})_4$) could be added to TMAH as an alternative source of silicates [62]. It is a low density powder and the volume necessary is quite large. Therefore, it is not easy to manipulate and make the solution opaque. The silicon powder has a much higher surface area and dissolves very rapidly but foaming and excessive bubbling of the solution occurs during the dissolution due to the large amount of hydrogen gas generated during this process. To prevent the foaming over the edge of the etch bath, it is necessary to dissolve the silicon at lower temperature (about 50°C). After dissolution, the solution is quite transparent with some not harmful precipitates. The main drawback of this technique is that TMAH solution with low pH produces more rough etched silicon surfaces. The etched areas are covered with hillocks due to the formation of bubbles on the etched surface which temporarily masks the silicon surface. Redeposition of insoluble etch products on the surface also contributes to mask silicon. Initially the number of pyramids at the surface is small, but as etching continues new pyramids are formed and begin to superimpose over previous hillocks. These pyramids significantly reduce the etch rate

in (100) direction because they expose slowly etching crystal (111) planes. They are finally aesthetics. To reduce surface roughness, ammonium persulfate (APS, $(\text{NH}_4)_2\text{S}_2\text{O}_8$) as oxidizer is added, in powder shape, into silicon doped TMAH solution to reduce oxygen production [63], [64], [65]. It does not contain alkaline ions and is therefore CMOS compatible. The required amount is only 5 grams per liter of solution but it is rapidly consumed (after about 45 min) in the reaction with silicon. Therefore, this amount is added every 45 minutes when the precipitate is completely dissolved. The addition of excess persulfate is not critical regarding the silicon etching rate. TMAH etching solutions with dissolved silicon, with and without added oxidizers, can only be used for several 3 hours etches. The pH of the solution slowly drops over time, until the etch rate diminishes to unusable levels. This decrease in pH is likely due to silicate saturation of the etching solution. The low cost of the solution and ease of disposal make it feasible to use a fresh solution to finish etching if necessary.

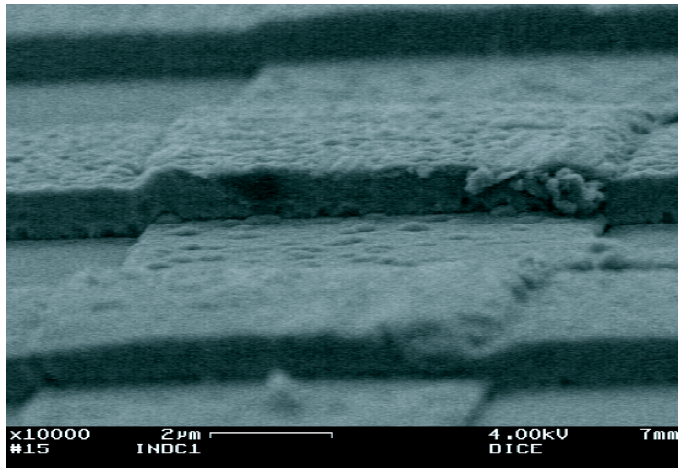


Figure 2.26: SEM picture of 2 aluminum lines crossing a polysilicon line covered by a silicon oxide layer. The SEM photo has been taken after 3 hours etching in a TMAH based solution (+APS and Si powder).

Reasonable etching rates ($1.2 \mu\text{m}/\text{min}$) have been obtained in TMAH doped with silicon in combination with persulfate. No deterioration of the aluminum interconnections has been observed as shown in Fig. 2.26 after an etching time of approximately 3 hours.

2.4.2.6 TMAH etching selectivity: Boron etch stop layer

As briefly introduced before, alkaline solutions exhibit a decrease in etch rate for boron doped silicon. Etching rates were measured on silicon and polysilicon for boron concentration varying between 1×10^{17} and 4×10^{20} atm/cm^3 in 20% and 25% concentrated TMAH solutions as whole as in the previously described aluminum selective TMAH solution.

The etching tests were performed at 80°C . Temperature was controlled by a thermometer connected to a regulator. To avoid changes in concentration of the solution during the experiment, a water cooled reflux condenser was used. The polysilicon sample was a $2.5 \mu\text{m}$ film deposited on a thermally oxidized silicon wafer. Boron implantation through a thin thermal oxide had been done to dope the sample.

The silicon sample was simply a bulk wafer which had been implanted with boron through a thin thermal oxide. Homogeneous concentration of boron through the whole thickness of the polysilicon film and over the first μm of the silicon substrate had been achieved thanks to a 5 hours diffusion under nitrogen flow at 1100°C . The thin thermal oxide avoided boron release in the ambient atmosphere during diffusion. The depth of even boron concentration in silicon had been simulated with the software ATHENA. The boron concentration in polysilicon was simply calculated as the dose divided by the thickness. Table 2.6 summarizes the boron implantation doses and the corresponding boron concentration in the silicon and polysilicon samples.

The etching was performed after opening windows in the masking thermal oxide. In order to get an accurate measurement of the etch rate, the etching had to be performed in the range of constant boron concentration.

The etch rate was deduced from a profilometry measurement of the step between the mask and the polysilicon or silicon surface before and after TMAH etching. The etching time varies between 2 and 12 min depending on the etch rate of the sample.

Fig. 2.27(a) presents the etch rate of silicon and polysilicon in function of the boron concentration in a 25% TMAH solution at 80°C . Fig. 2.27(b) plots the selectivity. Lowly doped silicon and polysilicon are etched at respective rates of 2700 and 5000 $\text{\AA}/\text{min}$. A selectivity of 0.1 for the etch rate is achieved at a boron concentration of 8×10^{19} atm/cm^3 for silicon and polysilicon. For higher boron concentration,

Boron im- plantation dose in atm/cm ² at 120 keV	Boron con- centration in atm/cm ³ in polysilicon	Boron con- centration in atm/cm ³ in silicon	Range of con- stant Boron concentration in silicon in μm
7×10^{14}	2.8×10^{18}	5×10^{18}	0.5
1.5×10^{15}	6×10^{18}	8.5×10^{18}	0.7
2.2×10^{15}	8.8×10^{18}	1.3×10^{19}	0.7
4×10^{15}	1.6×10^{19}	2×10^{19}	0.7
7×10^{15}	2.8×10^{19}	3.1×10^{19}	0.7
1×10^{16}	4×10^{19}	4.2×10^{19}	0.8
1.5×10^{16}	6×10^{19}	5×10^{19}	1
2.2×10^{16}	8.8×10^{19}	6.6×10^{19}	1.2
4×10^{16}	1.6×10^{20}	1×10^{20}	1.5
7×10^{16}	2.8×10^{20}	1.6×10^{20}	1.8
1×10^{17}	4×10^{20}	2×10^{20}	2

Table 2.6: Implantation dose and corresponding doping concentration for polysilicon and silicon samples. In the case of crystalline silicon the range of constant concentration is also indicated.

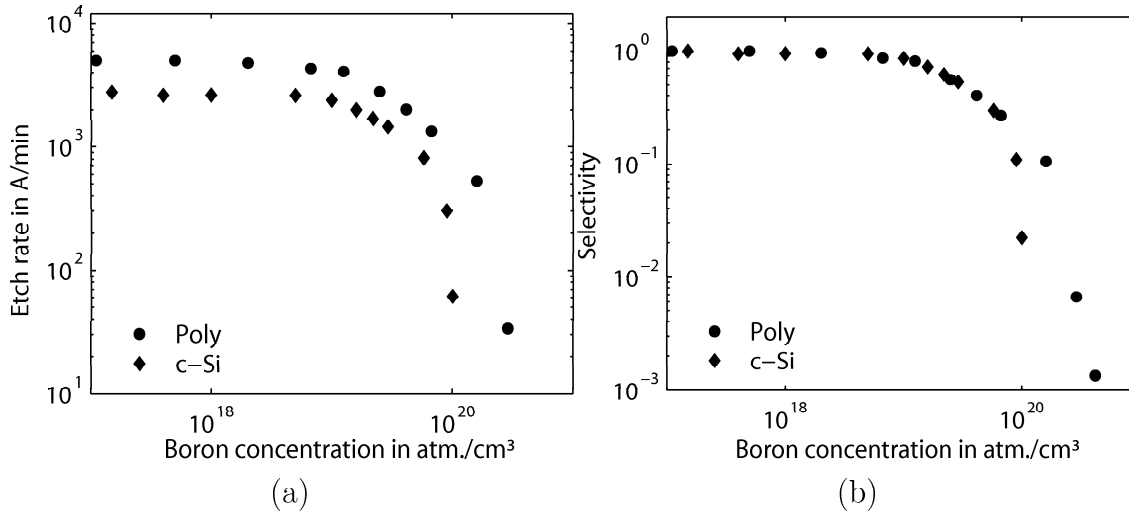


Figure 2.27: Etch rate (a) and selectivity (b) of silicon and polysilicon in 25% TMAH at 80 °C.

the etching selectivity reaches 0.02 at a boron concentration of 1×10^{20} atm/cm³ for silicon and 0.001 for polysilicon at a boron concentration of 4×10^{20} atm/cm³. Above a concentration threshold of 1×10^{20} atm/cm³, at a given boron concentration the etching selectivity is closer to zero for silicon than for polysilicon. The etching rate of polysilicon is always higher than the one of crystalline silicon.

Fig. 2.28(a) presents the etch rate of silicon and polysilicon in function of the boron concentration in a 20% TMAH solution at 80 °C. Fig. 2.28(b) plots the

selectivity. The etch rate of lowly doped polysilicon and silicon are respectively

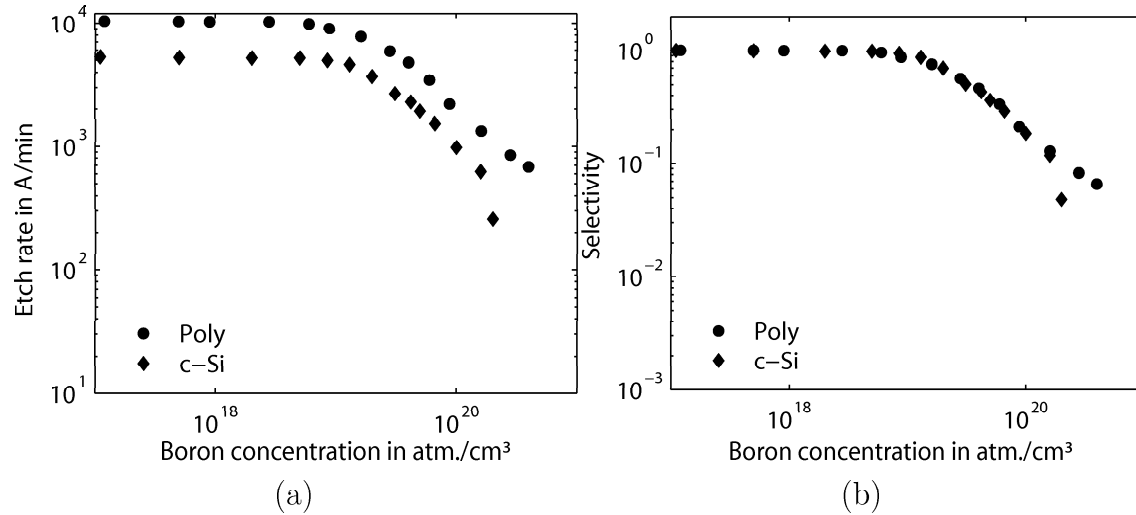


Figure 2.28: Etch rate (a) and selectivity (b) of silicon and polysilicon in 20% TMAH at 80 °C.

10300 Å/min and 5300 Å/min. An etching selectivity of 0.1 is achieved at a boron concentration of 2×10^{20} atm/cm³. Above this boron concentration, at a given boron concentration the etch-stop effect is more efficient for silicon than for polysilicon. The polysilicon etch rate is almost twice as the one of crystalline silicon and that for any boron concentration. The lowest selectivity reached is 0.05 for crystalline silicon at a boron concentration of 2×10^{20} atm/cm³.

Fig. 2.29(a) presents the etch rate of silicon and polysilicon in function of the boron concentration in the TMAH solution selective to aluminum (5% TMAH, 16 g/l of powder silicon and 5 g/l of APS) at 80 °C. Fig. 2.29(b) plots the selectivity. The etch rate of undoped polysilicon and silicon are respectively 5100 and 3100 Å/min. An etching selectivity of 0.1 is achieved at a boron concentration of 1×10^{20} atm/cm³ for crystalline silicon and at a boron concentration of 2×10^{20} atm/cm³ for polysilicon. Above this boron concentration, at a given boron concentration the etch-stop effect is more efficient for silicon than for polysilicon. The polysilicon etch rate is almost twice as the one of crystalline silicon and that for any boron concentration. The lowest selectivity reached is 0.01 for crystalline silicon at a boron concentration of 2×10^{20} atm/cm³.

All of these TMAH based solutions exhibit an etch rate reduction for highly boron doped samples. This effect which is now often used in MEMS fabrication and bulk micromachining is not fully understood yet. As seen in Eq. 2.37 during etching

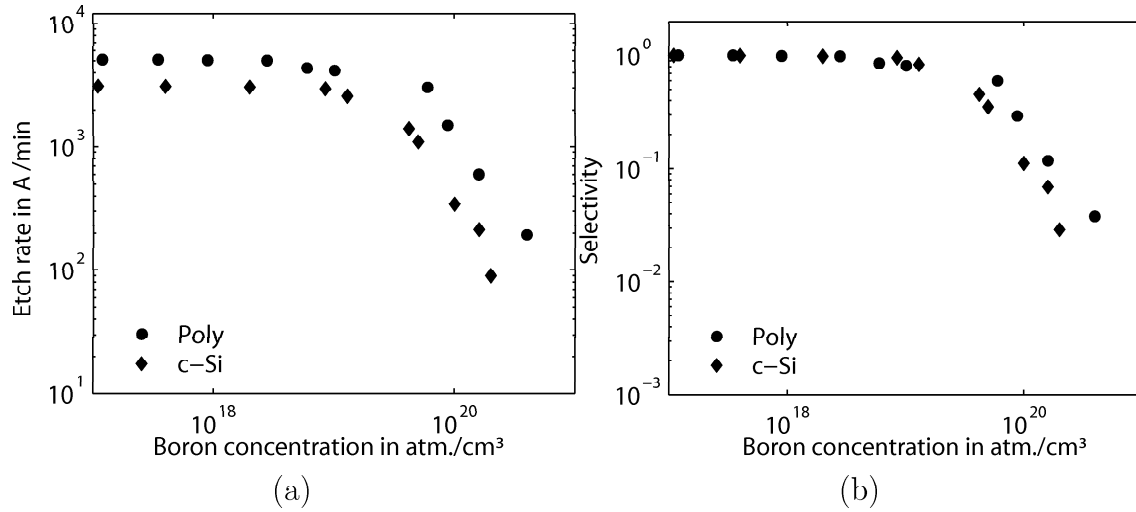


Figure 2.29: Etch rate (a) and selectivity (b) of silicon and polysilicon in aluminum selective TMAH (APS + Si powder) at 80 °C.

of silicon by TMAH, four electrons from the conduction band are emitted by reverse injection and contributes to hydrogen reduction and formation of OH^- ions. It has been thought that for highly p doped silicon those electrons would be trapped by holes, and that the reaction would stop. However, this hypothesis does not explain the etch stop property of highly n doped silicon that have been reported by Palik *et al.* [82]. Moreover Thong *et al.* have shown that illumination does not have any impact on the silicon etch rate in TMAH, confirming thus that the electrons from the conduction band do not influence the etch rate [71].

The most complete explanation of the p^{++} doped silicon etching selectivity is the strain induced to the silicon lattice by the substitutional boron atoms which have a smaller size than the silicon atoms. As shown in the previous section, introduction of boron in the silicon induces a tensile stress. Decarli *et al.* demonstrate the evidence of the influence of stress on TMAH etching of silicon [38]. They induced stress in the etched silicon via the use of a stressed masking material. They then measured the etch rate of silicon in the (111) and (100) directions. In the presence of tensile masking film, the etch rate increases and the anisotropic ratio, defined as the ratio between the etch rate in the (111) direction and the etch rate in the (100) direction, decreases. Inversely, in the presence of a compressive masking material, the etch rates decrease and the anisotropic ratio increases. As a tensile (respectively compressive) masking material induces a compressive (respectively tensile) stress in the underlying silicon, the tensile stress can indeed be seen as responsible for the

etch rate reduction of silicon in TMAH.

Our measurements show that for any TMAH based etching solutions the etch rate of polysilicon is always higher than the one of silicon. The selectivity of undoped silicon versus doped silicon is equivalent to the one of undoped polysilicon versus doped polysilicon at relatively low boron concentration. At higher concentration, the polysilicon has to be more doped than silicon to reach the same selectivity, in other words, p^{++} silicon is a more efficient etch stop than p^{++} polysilicon. The presence of grain boundaries in polysilicon explains this difference in etching behavior between silicon and polysilicon. The grain boundaries are preferential sites for etching of TMAH explaining thus the higher etch rate. Ning *et al.* have shown that the strain induced in silicon by substitutional boron atoms could be calculated by Eq. 2.30 where the strain ϵ is linked to the boron concentration via a proportionality coefficient β [53]. Horn *et al.* have measured this β coefficient for silicon and they found a value validating the theory of Eq. 2.31 [52]. Bardeen *et al.* found for polysilicon a value for β half of the one found by Horn *et al.* for silicon [56]. The lower boron contribution to strain for polysilicon than for silicon is explained by the boron trapped in the grain boundaries and by the constraints relaxation as well. This explains the highest boron concentration required for polysilicon to reach the same etching selectivity than for crystalline silicon.

Fig. 2.30 and Fig. 2.31 plot the etch rates and selectivity for the three different solutions for silicon and polysilicon. A lower TMAH concentration yields higher

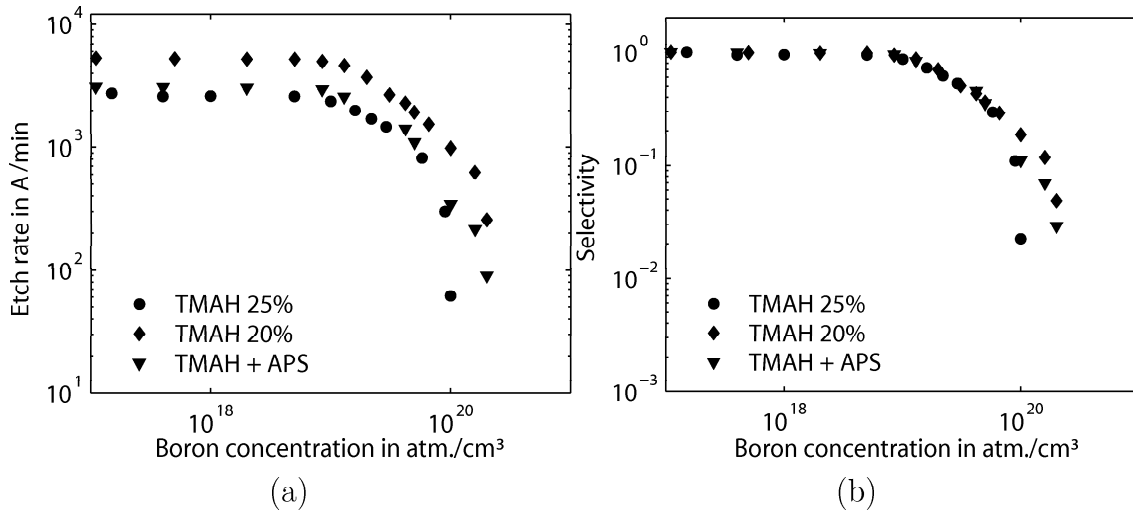


Figure 2.30: Etch rate (a) and selectivity (b) of silicon in Aluminum selective (APS + Si powder), 20% and 25% TMAH at 80 °C.

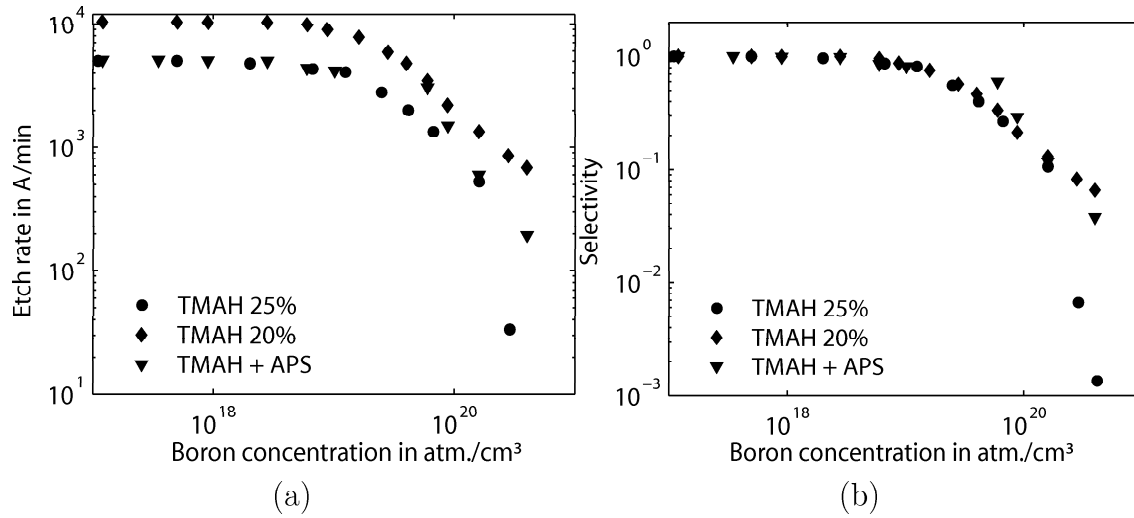


Figure 2.31: Etch rate (a) and selectivity (b) of polysilicon in aluminum selective (APS + Si powder), 20% and 25% TMAH at 80 °C.

etch rates, for both silicon and polysilicon, as confirmed by the literature, and the TMAH etching mechanism described from Eq. 2.35 to Eq. 2.39 which shows that above a threshold TMAH concentration of 5%, the etching is limited by the water concentration [71]. The aluminum selective etching solution has the slowest etch rate although its 5% TMAH concentration. The 16 g/l of silicon added to the solution partially neutralize the TMAH and decrease thus the etch rate compared to a 5% TMAH solution.

There is no difference in etching selectivity between the three solutions. The slope of the selectivity curve is higher for crystalline silicon than for polysilicon. The highest selectivity is reached for polysilicon etched in a 25% TMAH solution.

Etch stop layer can thus be defined in both crystalline and polycrystalline silicon. The main difference between crystalline and polycrystalline silicon etching, is the respective anisotropic and isotropic property of the etching. The range over which the etch stop layer can be defined depends on the technique used to dope the silicon or polysilicon. High energy implantation combined with a long annealing time at high temperature can diffuse the boron over a range of around 5 μm in crystalline silicon. In polysilicon, the diffusion is faster due to the presence of grain joints, but the thicknesses of the polysilicon films does not usually exceeds a few μm due to the deposition techniques. Solid source diffusion can also be used but is less efficient to get thick etch stop layer, because a boron silicate glass forms on the surface during diffusion, which then acts as a screen layer for the new incoming doping atoms.

Furthermore ion implantation allows to introduce the doping species deeply in the material.

Fig. 2.32 and Fig. 2.33 illustrates the difference in etching profile between crystalline and polycrystalline silicon.

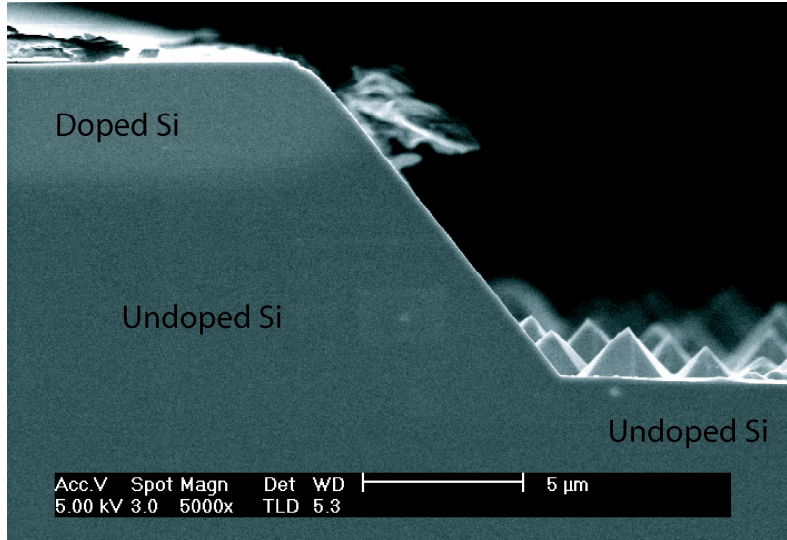


Figure 2.32: Anisotropic etching of crystalline silicon. The silicon wafer has been doped by implantation through a photoresist mask to pattern doped and undoped zones. After TMAH etching the implanted silicon acts as an etch mask. In the unimplanted zone, the etching stops on the (111) plane making thus a angle of 54.7° with the surface. The doped zone in the silicon appears brighter than the undoped bulk silicon [83]. In the p^{++} silicon, the boron atoms are negatively ionized and form a negatively charged zone which re-emits the secondary electrons easily than the undoped bulk silicon.

2.4.2.7 Conclusion

Etch rate decrease of boron doped silicon and polysilicon has been measured in function of the boron concentration in a 20% and 25% TMAH solutions and in a solution selective to aluminum in which APS and silicon powder were added to a 5% TMAH solution. Increasing the TMAH concentration of the solution decreases the etch rate but allows to reach larger ratio between etch rate of undoped and doped material. The decrease of the etch rate of one order of magnitude is achieved for a boron concentration of $1 \times 10^{20} \text{ atm/cm}^3$. Best selectivities have been measured in the range of 0.01 for silicon for boron concentration of $2 \times 10^{20} \text{ atm/cm}^3$ and of 0.001 for polysilicon for boron concentration of $4 \times 10^{20} \text{ atm/cm}^3$. A TMAH based solution

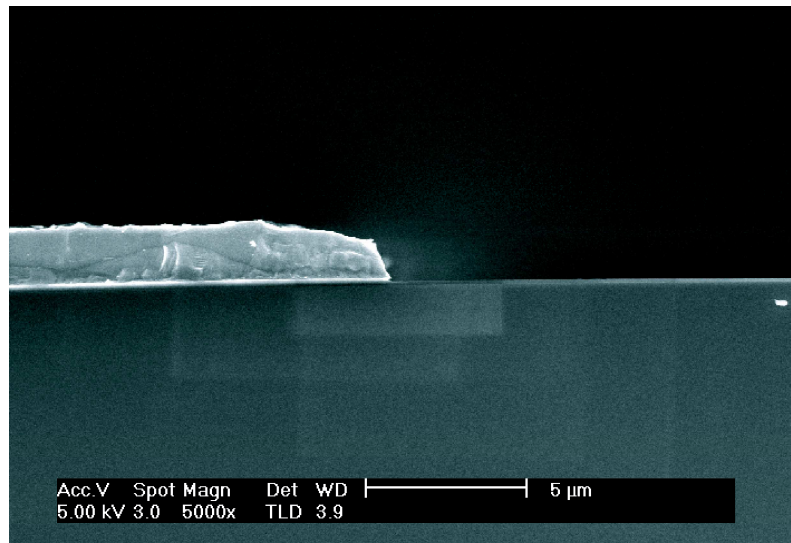


Figure 2.33: Isotropic etching of polysilicon. The 25000 Å polysilicon film was doped by implantation through a photoresist mask to pattern doped and undoped zones. After TMAH etching the undoped silicon is totally removed whether the doped silicon remains. The slope of the etched wall has the typical shape of an isotropically etched layer.

selective to aluminum has shown selectivities between doped and undoped silicon comparable to the one obtained for diluted TMAH.

A complete literature review explains the etch rate reduction of doped silicon in TMAH due to the tensile stress induced by the boron which has a smaller atomic radius than silicon and which occupy substitutional sites in the silicon lattice. This is confirmed by the better etch stop efficiency of a silicon boron doped layer compared to a polysilicon layer doped at the same boron concentration, knowing that the stress due to substitutional boron is lower in polysilicon than in crystalline silicon.

The advantage of polysilicon compared to crystalline silicon in TMAH etching is the isotropic character of the etching.

This effect of boron doping on the TMAH etch rate of silicon and polysilicon combined with the isotropic property of the polysilicon etching makes polysilicon a good candidate for the creation of etch stop layers. Ion implantation allows doping below the surface and makes the creation of a buried etch stop layer and buried mask possible. It will be demonstrated in Sec. 3.3.

2.4.3 *Modification of semiconductor doping: Increased etch rate of p- and n-doped silicon and polysilicon in HNA*

The two previous section studied the modification of etch rate of oxide and silicon due to the consequence of ion implantation such as bond breaking and stress induced due to substitutional atoms of smaller size than the lattice atoms, respectively. This last section of the chapter presents the etch rate modification due to the modification of the semiconducting properties of silicon or polysilicon doped by ion implantation.

Doping of silicon consists in replacing silicon lattice atoms by elements of the third or fifth column of the Mendeleïev chart at a substitutional site in the silicon lattice. Silicon belongs to the fourth column of the Mendeleïev chart and has thus four electrons on its outer electronic shell. The elements from the third and fifth columns have three and five electrons on the outer shell, respectively. The atoms must have eight electrons on the outer shell in order to be in a stable state. As the silicon atoms have only four electrons on their outer electronic shell, they must share their electrons with the neighbor atoms to reach the stable state. If the neighbor atom is a doping impurity which has an electron in default or in excess, it will get to a ionized state and capture or release an electron in the lattice. An element from the third column of the Mendeleïv chart is called an acceptor because it captures an electron from the lattice. Respectively, an impurity from the fifth column is called a donor as it release an electron in the lattice. This excess or lack (called hole) of electron is able to move freely within the lattice and is called a free carriers. It modifies the electrical properties of the silicon. The amount of holes or electrons in a semiconductor at equilibrium conditions is characterized by the Fermi level [84]. The Fermi level lies within the bandgap and gives the energy level for which the Fermi Dirac distribution function has a value of $\frac{1}{2}$. The Fermi Dirac distribution is given in Eq. 2.40:

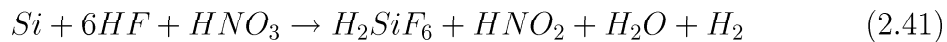
$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}} \quad (2.40)$$

The Fermi Dirac distribution function $f(E)$ gives the probability that an available energy state E will be occupied by an electron at the temperature T . k is the Boltzmann constant. In undoped semiconductors the Fermi level E_F lies in the middle of the bandgap. In the n type (respectively p type) semiconductors the

Fermi level lies close to the conduction (respectively valence) band yielding a large concentration of electrons (respectively holes) in the conduction band. The ability to modify the nature and the amount of the free carriers in silicon is the milestone of microelectronics, without which the fabrication of pn junctions, bipolar transistors and MOSFET would not be possible. Although the main application of silicon doping is the fabrication of active devices, it can also influence the reactivity of silicon to some chemicals.

2.4.3.1 Etching mechanism of silicon in HNA

Schwartz and Robbins have extensively studied the hydrofluoric / nitric acid (HF/HNO₃) based silicon etching solution which has the property to etch the doped silicon up to 150 times faster than the undoped silicon [85],[86],[87],[88],[89]. This etch rate variation can only be understood by taking a close look to the etching mechanism of silicon in the HF/HNO₃ system [68]. A popular solution used is a mix of HF, HNO₃ and acetic acid. This solution is often denominated as HNA. The etching mechanism described below can be seen as an oxidation of the silicon by the nitric acid followed by dissolution of the oxide by the hydrofluoric acid. The overall reaction is:



The schematic in Fig. 2.34 synthesizes the overall redox reaction of silicon in HNA.

Etching occurs via a redox reaction. Silicon is first oxidized by the nitric acid and then dissolved by the hydrofluoric acid that acts as a complexing agent. Points on the silicon surface randomly become oxidation or reduction sites. Each point on the surface becomes both an anode and a cathode site over time. Silicon is promoted to a higher oxidation state at an anodic site which supplies positive charges in the form of holes:



N₂O issue from nitric acid dissociation is simultaneously reduced at a cathode

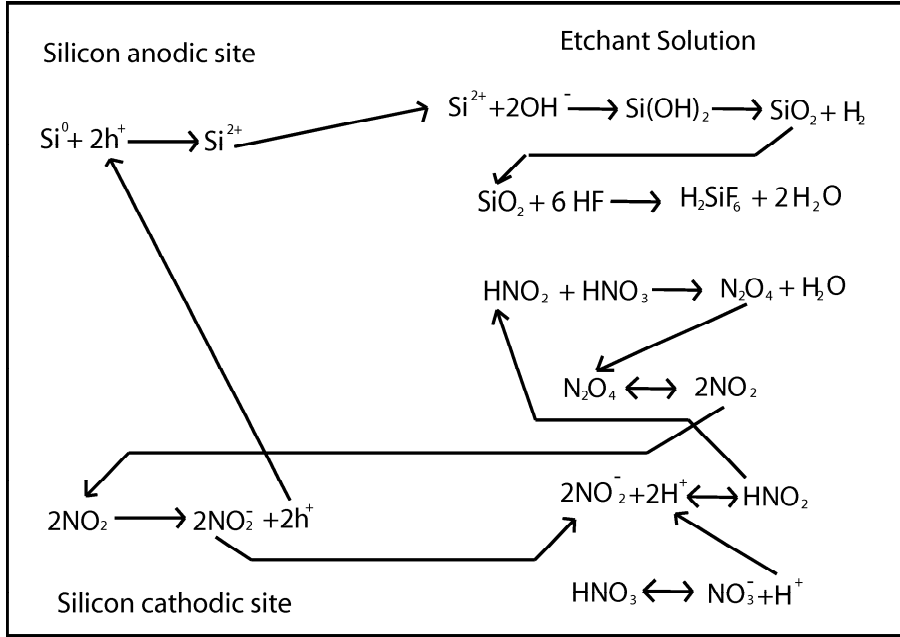
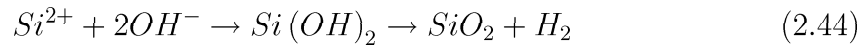


Figure 2.34: Etching mechanism of silicon in HNA.

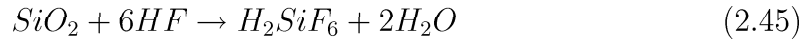
site and produces free holes which are then used at an anodic site (Eq. 2.42):



The Si^{2+} combines with OH^- to form SiO_2 :



The SiO_2 is then dissolved by HF to form a water soluble complex of H_2SiF_6 :



The nitric acid has a complex dissociation mechanism. Deprotonation of nitric acid occurs:

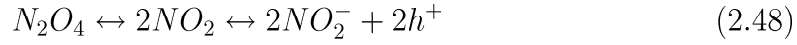


Holes and HNO_2 are produced by an autocatalytic cycle:



The hole responsible for the excitation of silicon as described in Eq. 2.42 origi-

nates from the dissociation of N_2O_4 :



The proton generated during the dissociation of HNO_3 (Eq. 2.46) is re-used for the formation of $HN0_2$:



N_2O is effectively the oxidizer of silicon. Its reduction supplies holes for the oxidation of the silicon. HNO_2 is regenerated by the auto catalytic reaction. The oxidizing power of the etching is set by the amount of undissociated HNO_3 . The acetic acid acts as a diluent. It is preferred to water because of its better wetability of the silicon surface.

The etch rate of silicon by HNA is limited by the oxidation rate of silicon by the nitric acid and by the dissolution rate of oxide by the hydrofluoric acid. Oxidation of silicon is enhanced if the silicon is in an excited state. In n-type doped silicon the majority free carriers are electrons. The electrons on the surface will behave like a cathodic site they will thus enhance the reaction from Eq. 2.48. In a p-type doped silicon the holes will enhance the reaction from Eq. 2.43 creating thus a lot of cathodic sites. For the both types of doping the silicon oxidation rate by nitric acid will be enhanced by the presence of the free carriers.

The composition of the solution has also an impact on the etching mechanism and kinetics. Fig. 2.35 plots the iso etch rate curves, and details the etching mechanism for four regions of solution composition [87], [88].

- Region 1

For high HF concentrations, contours are parallel to the lines of constant HNO_3 , therefore the etch rate is controlled by HNO_3 in this region. However, the oxidation of silicon by the nitric acid starts only if the nitric acid was dissociated by its auto-catalytic process according to Eq. 2.46 - 2.49. The reaction will start in presence of catalyst under the form of NO_2 or at excited silicon states which can be due to doping or to surface defects. Any stirring of the reaction may dissipate the catalyst and quench the reaction. Etching in

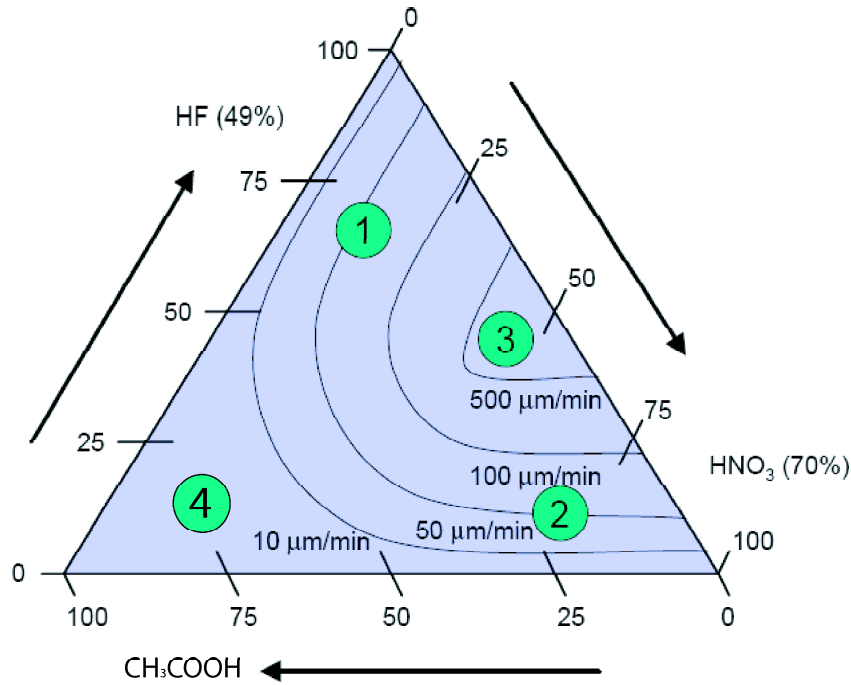


Figure 2.35: Curves of constant silicon etch rate in function of etchant composition in the 49% HF, 70 % HNO₃ and 99 % CH₃COOH [87], [88].

this region is dependent on the etch rate which is increased by surface defects and excited states due to the free carriers from the semiconductor. Selective etching can occur in this composition range.

- Region 2

For high HNO₃ concentrations, contours are parallel to the lines of constant HF, therefore the etch rate is controlled by HF in this region. The whole silicon surface is covered by an oxide film. The more reactive center may begin to etch first but they soon become covered with an oxide layer. The oxide protects the reactive center from excessive oxidation while the remainder of the surfaces catches up. This result is a smoother etched surface as when the limiting factor for the etching is nitric acid. As the etching is limited by the dissolution of the oxide and not by its formation, there is for this composition range no selective etching between doped and undoped areas, as well as between damaged and undamaged areas.

- Region 3

Initially not very sensitive to the amount of acetic acid, then the etch rate falls

sharply for 1:1 HF:HNO₃ ratios. As the etch rate is extremely high it is not of any practical use for microelectronic processing.

- Region 4

The concentration in HF and HNO₃ is very low, then the etch rate falls and becomes erratic with respect to small changes in composition [88].

Our goal is to achieve selective etching of doped regions at a relatively low etch rate, as the usual thicknesses of polysilicon films in micromachining rarely exceed the micrometer range. The literature reports different solution compositions which present a selective behavior between doped and undoped silicon. Kurt presents a HNA solution of composition 1 HF : 3 HNO₃ : 8 CH₃COOH, called HNA [1:3:8] (Region 4), which is supposed to etch silicon with a doping n or p higher than 1x10¹⁷ atm/cm³ 150 times faster than undoped silicon [89]. Schwartz and Robbins propose a p⁺ etching solution selective to n doped and undoped silicon of composition 1 HF : 8 HNO₃ : 1 CH₃COOH, called HNA [1:8:1] (Region 2), and a p and n etching solution selective to undoped silicon of composition 1 HF : 1 HNO₃ : 2 CH₃COOH, called HNA [1:1:2] (between Region 1, 2 and 4) [88].

HNA [1:3:8] and HNA [1:1:2] solutions were studied in detail because of their etch rate enhancement for both n and p doping and their relatively low etch rate. HNA [1:8:1] solution was not tested because of its too high etch rate according to Fig. 2.35. The two solutions were tested on doped polysilicon instead of silicon since our motivation is the fabrication of a buried mask in a polysilicon layer. The etching was tested on thin and thick polysilicon films. The thin polysilicon films were processed as follow: a 3000 Å polysilicon film was deposited by LPCVD on an oxidized silicon wafer. The polysilicon was then thermally oxidized to create a 1000 Å oxide film used as screen oxide for the implantation step. A photolithographic step defined zones to be implanted either with boron, phosphorous or arsenic to create p- and n-type doped samples at concentrations varying between 1x10¹⁵ and 1x10¹⁹ atm/cm³. The purpose of the screen oxide is to set the R_p of the implanted doping profile as close as possible from the polysilicon surface. In the case of Arsenic implantation the screen oxide thickness was reduced to 100 Å in order to adapt the implantation energy to the capacity of our implanter and the photoresist implanta-

tion mask was replaced by a nitride mask in which windows were opened by RIE. Fig. 2.36 shows a schematic cross section of the samples.

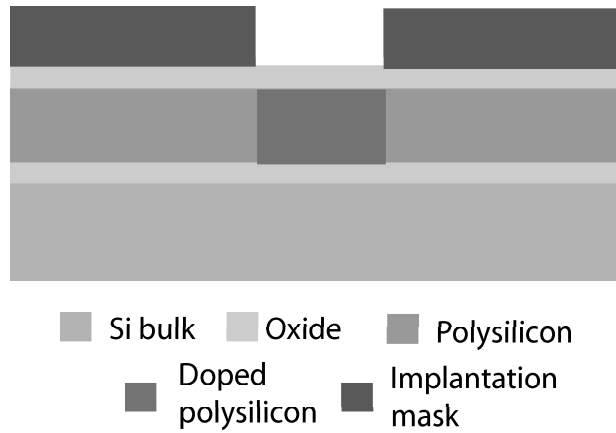


Figure 2.36: Schematic of the samples.

The sample were doped by implantation followed by a rapid thermal annealing of 15 s at 950 °C under nitrogen flow. Table 2.7 gives the implantation energy, the dose range and the corresponding energy range for each implanted species.

Doping specie	Implantation energy in keV	Dose range in atm/cm ²
B	70	1.6x10 ¹⁰ to 1.6x10 ¹⁴
P	150	2x10 ¹⁰ to 1.6x10 ¹⁴
As	180	1x10 ¹⁰ to 1x10 ¹⁴

Table 2.7: Implantation dose and energy of the thin polysilicon film samples etched in HNA [1:3:8].

The processing of the thick polysilicon films differs from the previous one by the thickness of the polysilicon film, 25000 Å instead of 3000 Å and the anneal method. The wafers were implanted with boron and arsenic through a 200 Å screen oxide at the energies and doses given in Table 2.8.

Doping specie	Implantation energy in keV	Dose range in atm/cm ²	Concentration range in atm/cm ³
B	150	1x10 ¹³ to 4x10 ¹⁵	5x10 ¹⁶ to 2x10 ¹⁹
As	150	1x10 ¹³ to 4x10 ¹⁵	5x10 ¹⁶ to 2x10 ¹⁹

Table 2.8: Implantation dose and energy of the thick polysilicon film samples etched in HNA [1:1:2].

A 500 Å LPCVD nitride film was deposited before a 2 hours diffusion at 1050 °C to avoid outdiffusion of the implanted species during the long time annealing. This annealing ensured a constant doping concentration through the whole thickness of the polysilicon film. After diffusion openings were made in the nitride protective film thanks to a photolithographic step and a RIE. Fig. 2.37 presents a schematic of the fabricated sample.

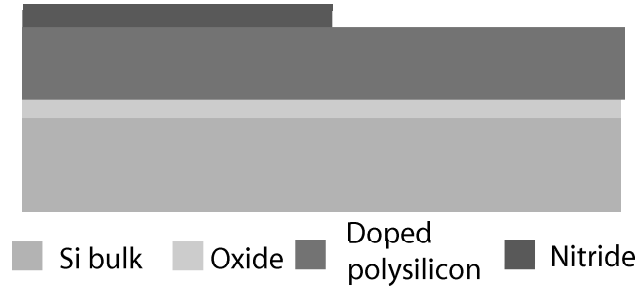


Figure 2.37: Schematic of the sample.

2.4.3.2 Autocatalytic reaction

The first tests were made in the HNA [1:3:8] solution on the thin polysilicon films. Fig. 2.38 shows arsenic doped samples at a concentration of 1×10^{16} atm/cm³ after 3 min etching.

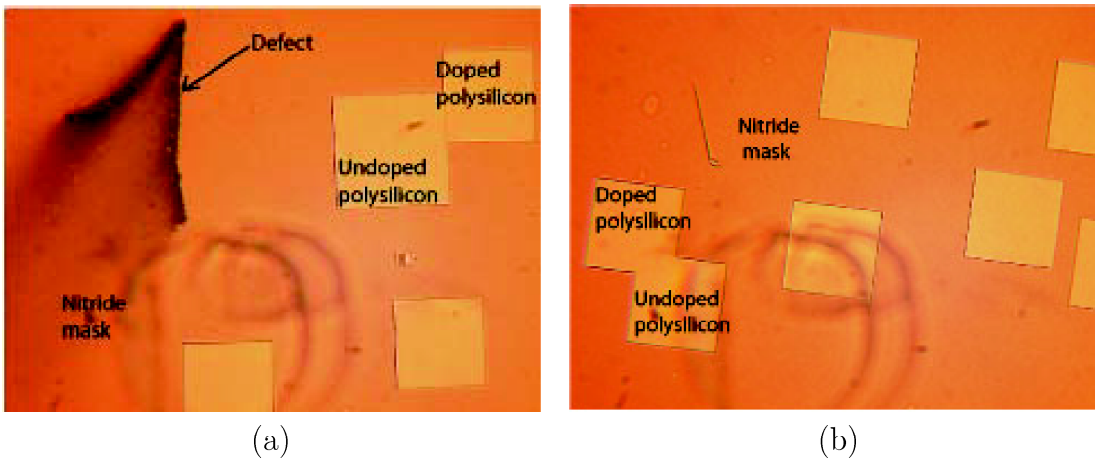


Figure 2.38: Optical microscopy of arsenic lowly doped samples after 3 min etching in 1 HF : 3 HNO₃ : 8 CH₃COOH. Windows are opened in the nitride mask on implanted and unimplanted areas. (a) Cracks in the surface. (b) Defects free surface.

The sample which has been scratched with a diamond is strongly attacked while the defects free sample is not attacked at all. The undoped and doped areas that were

in contact with HNA are not attacked. It is due to the low doping concentration and to the lack of defects on the surface. This proves that surface defects are preferential points for etching.

Fig. 2.39 shows an arsenic doped sample at a concentration of $5 \times 10^{18} \text{ atm/cm}^3$ after 3 min etching in the same solution. The undoped area is not etched, while in

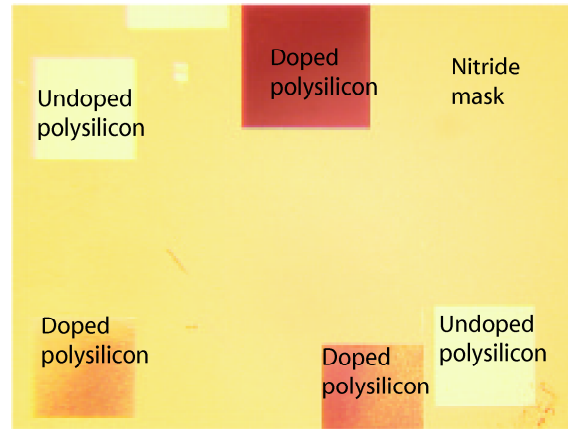


Figure 2.39: Highly doped arsenic sample after 3 min etching in HNA [1:3:8]

the doped area the etching seems to propagate from one corner of the doped zone to the rest of the doped zone. This result shows that during the etching nitric acid which is dissociated via an autocatalytic cycle needs the reaction byproducts of its dissociation to sustain further reaction. Therefore the etching propagates from one site to the neighbor sites.

Fig. 2.40 shows etching of highly doped boron sample after HNA etching. The samples were dipped in the solution until etching occurred.

The sample (a) was dipped in BHF before HNA etching to remove the screen oxide, whether the sample (b) was etched with its screen oxide. Sample (a) was dipped in the solution during 8 min before any etching of the doped areas could be observed. For the sample (b) 15 s. were sufficient to etch the doped areas. In the case of sample (b), the etching was initiated by etching of the screen oxide by HF. During the dissolution of oxide by HF, protons are exchanged (Eq. 2.24 and 2.26). They could contribute to the nitric acid dissociation (Eq. 2.49) and initiate the autocatalytic reaction of silicon oxidation by nitric acid.

Fig. 2.38, 2.39 and 2.40 have shown that HNA etching of silicon can easily start at points defects on the silicon surface and that once the reaction starts, the auto-

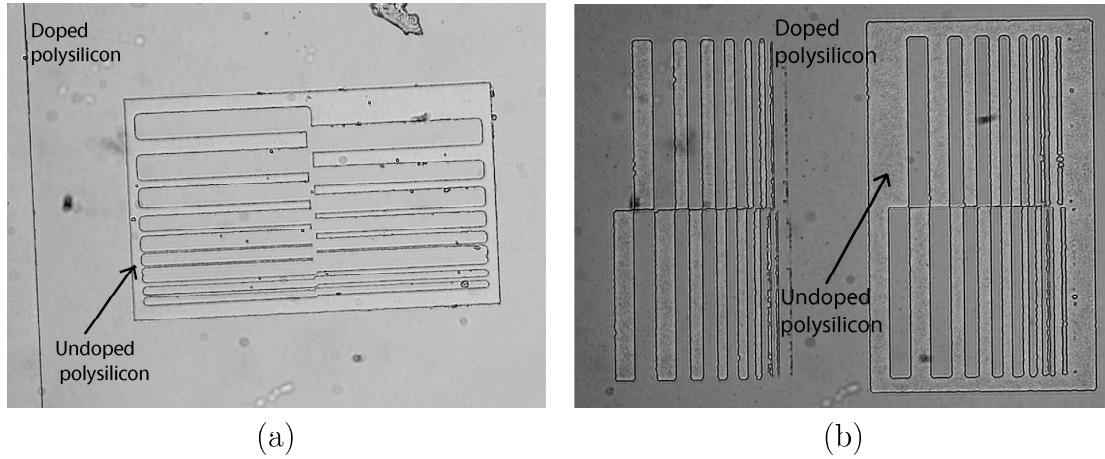


Figure 2.40: Optical microscopy of boron doped samples at a concentration of 8×10^{19} atoms./cm³. after etching in HNA [1:3:8]. (a) no oxide present before etching (b) screen oxide present before etching.

catalytic cycle of nitric acid dissociation allows the reaction to propagate through the neighbor sites of the starting point.

The drawback of the HNA [1:3:8] solution is that the start of the reaction is unpredictable on defect free surfaces. We attempted to solve this problem by adding 1 gr/l of Si powder in the HNA solution and by stirring the solution during 5 min and letting then the solution at rest during 5 min after stirring. The etching was then performed in the HNA [1:3:8] without stirring once the silicon powder was dissolved. This method of aging the solution gives better results in terms of etching reproducibility. However, it requires to prepare a new solution for each etching and the lifetime of the solution is limited, which makes the HNA [1:3:8] not friendly to use.

The HNA [1:1:2] was tested on the thick polysilicon films. Undoped samples were dipped in the solution for time periods varying from 15 s to 1 min.

Table 2.9 gives the etched thickness of the polysilicon film and the corresponding etch rate in function of the etching time.

Fig. 2.41 shows the cross section of the undoped samples for four different etching time. The samples were dipped into the solution without any stirring of the solution and rinsed in de-ionized water.

The evolution of the calculated etch rate in function of the etching time clearly demonstrates the autocatalytic behavior of the reaction. After 15 s in the HNA [1:1:2] 985 Å are etched. 5 s later i.e. for 20 s etching time, the etched thickness has

Etching time in s	Etched thickness in Å	Etch rate in Å/min
15	985	3940
20	7169	21507
30	13900	27800
60	27500	≥ 55000

Table 2.9: Etch rate in function of the etching time for undoped polysilicon etched in HNA [1:1:2] without stirring.

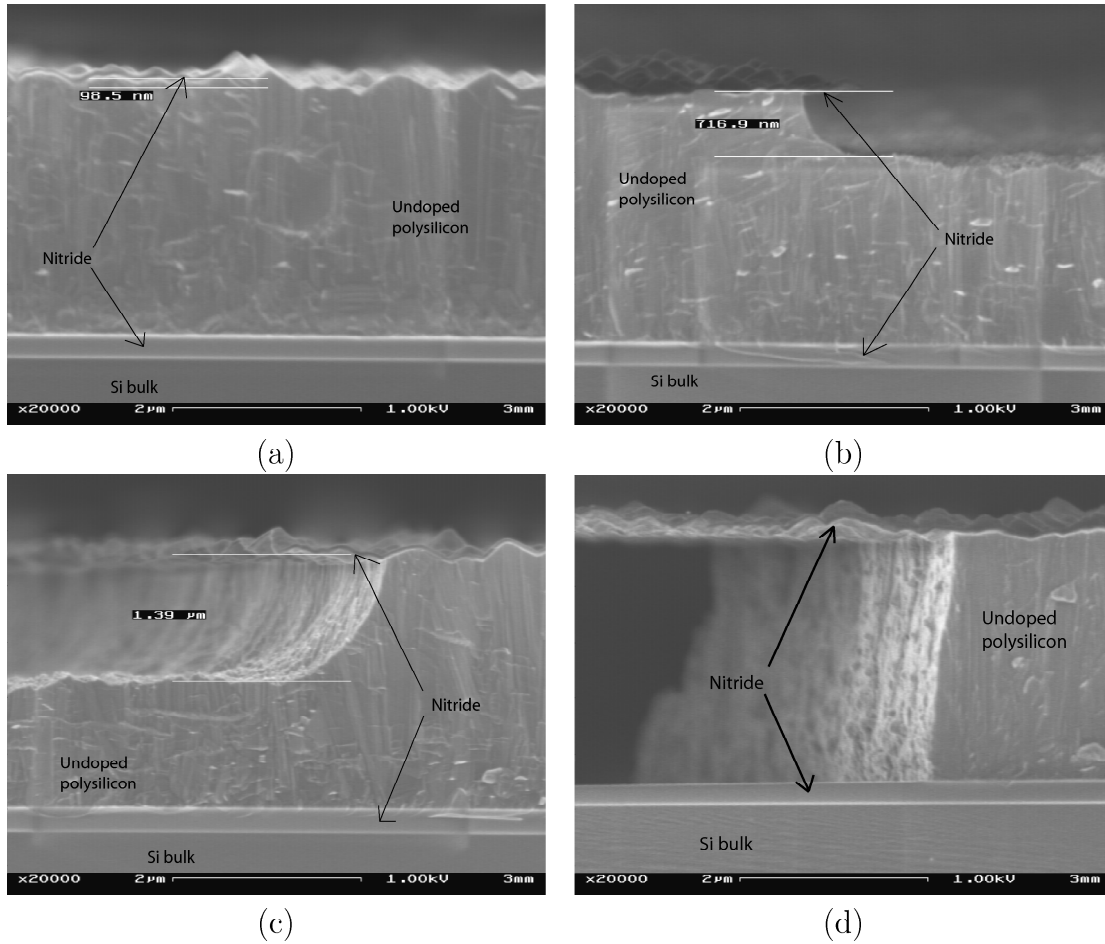


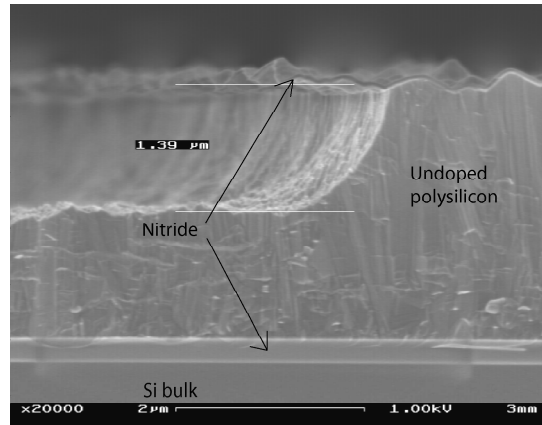
Figure 2.41: SEM cross section of undoped polysilicon film after etching in HNA [1:1:2] without stirring for (a) 15 s, (b) 20 s, (c) 30 s and (d) 1 min etching times.

been multiplied by a factor of 7, to reach 7169 Å, when the time was only increased of 33 %. The reaction needs defects on the surface to start. Once the reaction has started, it produces HNO_2 (Eq. 2.41), which is then re-used for the dissociation of HNO_3 (Eq. 2.47). The more silicon has reacted, the more HNO_2 is present in the solution which increases the oxidation rate of silicon by nitric acid. The reaction byproducts increase the oxidation rate of silicon in the vicinity of the starting point.

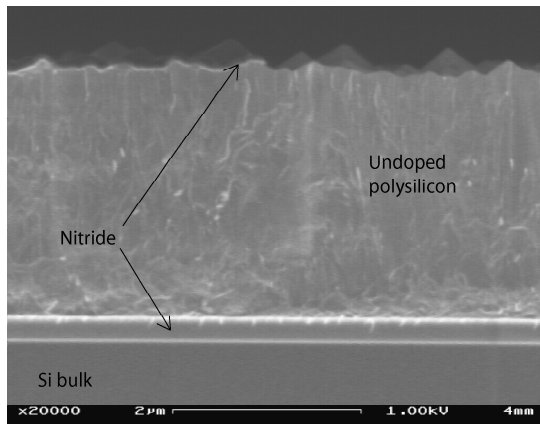
Therefore, the etching of polysilicon seems to propagate on the wafer surface, as previously seen in Fig. 2.39.

Our goal being to achieve selective etching between doped and undoped zones we need to decrease the etching in the undoped area, or at least to reduce the etch rate variation in function of the etching time. The etch rate acceleration being a consequence of the reaction byproducts presence, a way to decrease the etch rate is to move away from the etched site the reaction byproducts immediately after their formation. This can be done by vigorous stirring of the solution.

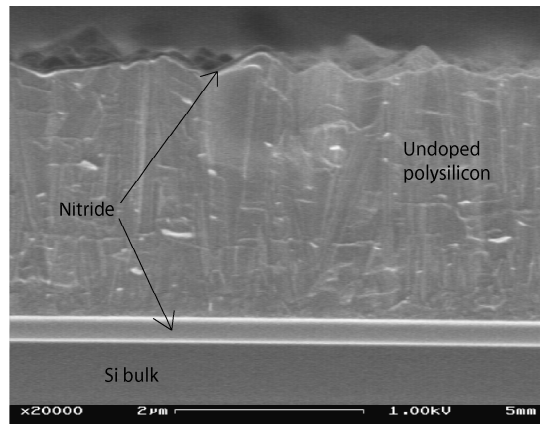
Fig. 2.42 shows the undoped sample dipped in HNA [1:1:2] during 30 s for various agitation conditions. In ultrasonic bath or when stirring the solution, no etching of



(a)



(b)



(c)

Figure 2.42: SEM cross section of undoped polysilicon film after 30 s etching in HNA [1:1:2]. (a) no stirring, (b) stirring, (c) ultra-sonic bath.

the undoped polysilicon occurs as the reaction byproducts are immediately dissolved.

An undoped sample was held 2 min in HNA [1:1:2] with stirring and ultrasonic

agitation without being attacked. Undoped polysilicon can thus be considered as an etch stop with respect to doped silicon which is highly reactive to HNA. The next section details the etch rate in function of the doping level.

2.4.3.3 Etching selectivity in function of the doping level

The previous section showed the autocatalytic behavior of the HNA etching system and presented a method to reduce the spontaneous etching of undoped polysilicon. We will now characterize the etch rate in function of the doping levels of polysilicon.

Etch rate in function of the doping has been measured on arsenic and boron doped samples in HNA [1:1:2]. Fig. 2.43 plots the etched polysilicon thickness after 15 s etching with and without stirring for various doping level of arsenic and boron.

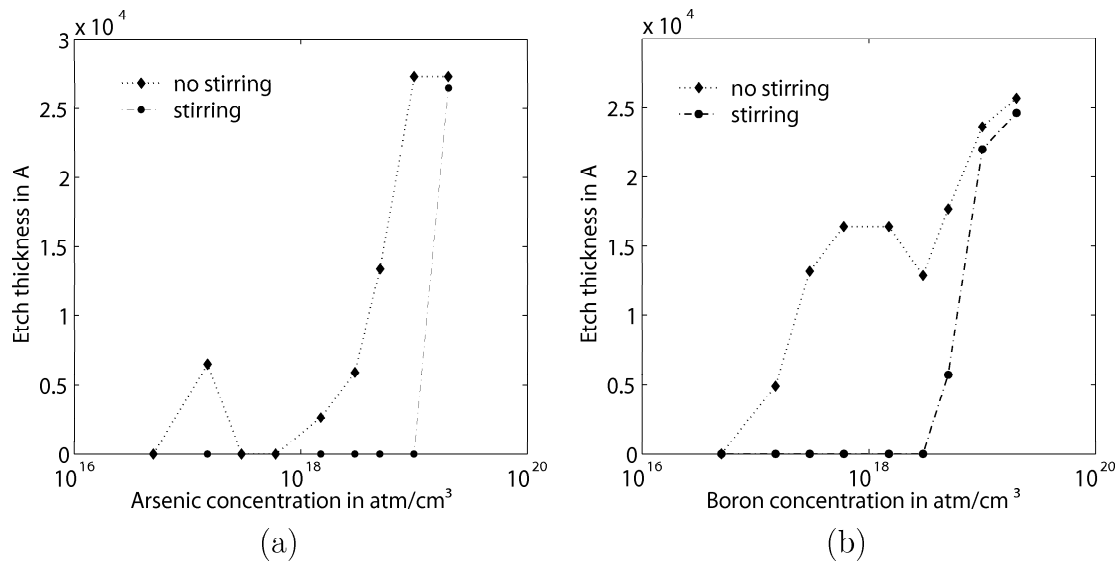


Figure 2.43: Etched polysilicon thickness after 15 s etching in HNA [1:1:2] in function of the doping level. (a) Arsenic doped samples, (b) Boron doped samples.

Without any stirring, increasing the doping increases the etch rate, but the reaction is not properly controlled, as can be seen in the plot for the arsenic doped sample, where a lowly doped sample has been etched when samples with higher doping have not been etched at all. The plot of the boron doped sample reveals also the unpredictable character of the etching. Highly doped samples can be etched at a slower etch rate than samples of lower doping. The highly doped samples where etched completely. We can therefore only conclude that, as $26000 \text{ \AA}$ have been etched in 15 s, the etch rate for sample doped with boron or arsenic at a concentration higher than $2 \times 10^{19} \text{ atm/cm}^3$ is higher or equal to $10.4 \text{ }\mu\text{m/min}$.

When stirring the solution, no etching occurs when increasing the doping concentration until the etch rate suddenly reaches high values. Stirring the solution reduces the chance for the reaction to start and destroys the autocatalytic character of the etching. Below a doping threshold no etching occurs because the density of silicon excited states is too low. Every attempt to start the etching from such excited states on the polysilicon surface is counterbalanced by the immediate dissolution of the reaction products that could sustain the reaction. Above a certain doping threshold, the density of excited silicon atoms at the surface becomes high enough to start the reaction and to produce more reaction byproducts than the stirring can dissolve. The etching can thus continue by a sort of avalanche effect. The selectivity between doped and undoped silicon is thus increased.

Fig. 2.44 compares the etched polysilicon thickness for arsenic and boron doped samples in HNA [1:1:2] without stirring. The rapid etching reaction of doped polysil-

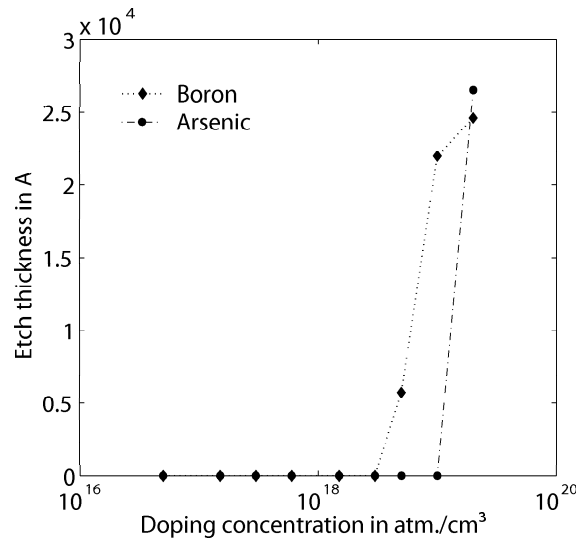


Figure 2.44: Etched silicon thickness in function of the doping concentration for arsenic and boron doped samples.

icon occurs at lower doping level for boron than for arsenic concentration. The whole thickness of the film is etched when the doping concentration reaches 1×10^{19} atm/cm³ for boron while a concentration in arsenic of 2×10^{19} atm/cm³ is required to etch the whole polysilicon film. Doping concentrations half of these threshold concentrations do not show any etching at all. Due to the very high value of the etch rate which is higher than $10 \mu\text{m}/\text{min}$, it is impossible to characterize accurately the etch rate. No progressive change in etch rate is observed in function of the doping.

It seems that once the reaction has started it is extremely violent and etches the silicon at very high rate. A small diminution of the doping concentration causes the etch rate to vanish abruptly. The difference in doping threshold between arsenic and boron doped samples has not been investigated but the literature reports that the selectivity might be slightly different for n- or p-type doped silicon [88]. However, as the change in etch rate is so abrupt in function of the doping concentration, the main parameter for selective etching of doped silicon or polysilicon is the concentration threshold above which etching occurs.

2.4.3.4 Conclusion

The HNA etching system has been described. Its complexity and its autocatalytic character makes it very difficult to control. HNA [1:1:2] yields higher etch rate than HNA [1:3:8] but the etching in HNA [1:1:2] is more reproducible than in HNA [1:3:8]. Etching in an ultrasonic bath or by stirring the solution reduces the erratic start of the etching reaction. As the etch rate is extremely high for doped polysilicon it has not been determined accurately but can be assumed to be larger than 10 $\mu\text{m}/\text{min}$ for highly doped polysilicon. The behavior of the etch rate in function of the polysilicon is binary. Below a doping threshold which lies between 1×10^{19} and $2 \times 10^{19} \text{ atm}/\text{cm}^3$, no etching occurs. Above this threshold etching occurs at a rate larger than 10 $\mu\text{m}/\text{min}$. This original etching behavior allows the possibility to use doped polysilicon or silicon as sacrificial layer while undoped polysilicon could be used as etch stop layer. This etching is highly selective to silicon nitride but present unfortunately a poor selectivity to silicon dioxide.

2.5 Conclusion

This chapter described the etch rate modification of common microelectronics materials by ion implantation. A brief review on ion implantation physics described the phenomena occurring during ion implantation. The incoming atoms suffer collisions with the target atoms. The energy lost through the collisions with the nuclei of the target characterizes the damage made to the target, such as covalent bond breaking and amorphization in the case of a crystalline target. Once the implanted atom is

at rest, it can, after an annealing, take place at a substitutional site on the target lattice. Substitutional atoms in crystalline lattice can stress the host lattice if there is a mismatch between the atomic radii of the implanted and the target atoms. In the case of a semiconductor as target material, the substitutional atoms can be a source of free carriers and dope the semiconductor. These three effects:

- bond breaking,
- stress induced,
- semiconductor doping,

can drastically change the etch rate of silicon dioxide, silicon and polysilicon.

Implanted silicon dioxide presents a highest reactivity to HF due to the covalent bonds broken during ion implantation. Etching selectivity of 200 can be achieved between unimplanted and implanted oxide when etched in VHF. Any species can be implanted to damage the silicon dioxide, as long as no anneal reconstruct the broken bonds. The damage creation is characterized by the nuclear deposited energy.

Silicon or polysilicon doped with boron suffers an induced tensile stress which reduces their reactivity to TMAH. Etching selectivity of 100 can easily be achieved between implanted and unimplanted polysilicon. The difference between crystalline and polycrystalline silicon etching in TMAH is the loss of the anisotropic character of the etching for the polycrystalline material.

Doped silicon or polysilicon increases tremendously its etch rate in HNA. Doping of n or p type can indifferently be used. Etch rate larger than 10 $\mu\text{m}/\text{min}$ can be achieved for doped polysilicon.

Table 2.10 summarizes the etching characteristics of the three selective etching method presented in this chapter.

Etching in VHF and HNA are autocatalytic reactions, which means that any start of the etching sustains further etching. Therefore, very high etching selectivity between material that have been modified by ion implantation to be more reactive to the etching solution and unimplanted material can be achieved. The drawback of the autocatalytic reaction is that they can propagate to the neighbor unimplanted area if one does not worry about the evacuation of the reaction by-products that serve as catalysts for the reaction.

Etching solution	VHF	HNA [1:1:2]	TMAH 25%
Etched material	oxide	polysilicon	polysilicon
Etching mechanism	Damage	n or p-type doping	Tensile stress induced by substitutional boron
Etch rate unimplanted	7Å/min	-	5000 Å/min
Etch rate implanted	1500 Å/min	10 μm/min	500 Å/min
Selectivity threshold	1×10^{23} - 3×10^{23} eV/cm ³	9×10^{18} - 2×10^{19} atm/cm ³	8×10^{19} - 1×10^{20} atm/cm ³
Remarks	Autocatalytic reaction. Etch rate linked to the amount of water condensed on the surface	Autocatalytic reaction. Etch rate linked to the amount of dissociated HNO ₃ on the surface	Reaction non catalytic

Table 2.10: Main characteristics of the selective etching induced by ion implantation.

These three techniques of etch rate modification by ion implantation allow to define sacrificial or etch stop zones within a layer of the same material. Ion implantation at high energy leads to important properties changes of a buried layer at depth in the micron range. However in this chapter, the change in etch rate was measured on the whole wafer surface. The fabrication process of the planar double gate described in Sec. 1.2 requires the revelation of structure with a size in the range of a typical transistor gate length, some tens of nm. Due to our limitation in photolithographic equipment we investigated in the following chapter the possibility to reveal structure with a minimal size in the micrometer range. Chap. 3 investigates thus the limitation of the revelation of narrow structure in polysilicon and narrow cavities in oxide.

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CHAPTER 3

BURIED MASK REVELATION

3.1 *Introduction*

The previous chapter described the etch rate modification of oxide, silicon and polysilicon by ion implantation. Implanted oxide is etched 200 time faster than unimplanted oxide in VHF. Doped polysilicon n or p-type is etched at etch rate larger than $10\text{ }\mu\text{m}/\text{min}$ in HNA when undoped polysilicon can be dipped 2 min in HNA without being attacked. The etch rate of boron doped polysilicon was reduced by a factor of 100 when etched in TMAH. These etch rate modifications are the result of the intrinsic properties changes of oxide or silicon by ion implantation. One property of ion implantation is that the depth at which the intrinsic properties of the target will be modified depends on the implantation energy. These techniques allow thus the creation of the buried mask needed for the fabrication of self-aligned planar double gate transistors as described in Sec. 1.2.

The three Sections of this Chapter will qualify the revelation of buried mask made thanks to the use of each of the three selective etching methods developed in Chap. 2. Conclusion would be drawn concerning the feasibility of the self-aligned planar double gate transistors thanks to this technique.

The technique will also be extended to some other applications.

3.2 *Positive buried mask in oxide*

The process described in Sec. 1.2.1 needs selective etching of implanted oxide to reveal a cavity in the BOX and in a top oxide of a SOI wafer. We study in the first part of this Section the influence of the process parameters on the etching selectivity and follow then in the second part with the development of buried masks.

We tested the revelation of buried cavities by implanting phosphorous in the BOX of an SOI wafer. The SOI and BOX were, respectively 100, and 400 nm thick. Phosphorous was chosen for the good compromise it offers between the high nuclear

energy loss it induces and the depth over which damages can be created without implanting at too high energies. Boron could have been used to create damages at higher depth but the required implanted dose to create enough damages is quite high. Phosphorous was thus implanted at 170 keV at a dose of 4×10^{16} atm/cm³. The corresponding nuclear deposited energy was thus 1.5×10^{26} eV/cm³. Windows were then opened in the SOI film by RIE to reach the BOX. Fig. 3.1 describes the samples used to qualify the buried mask.

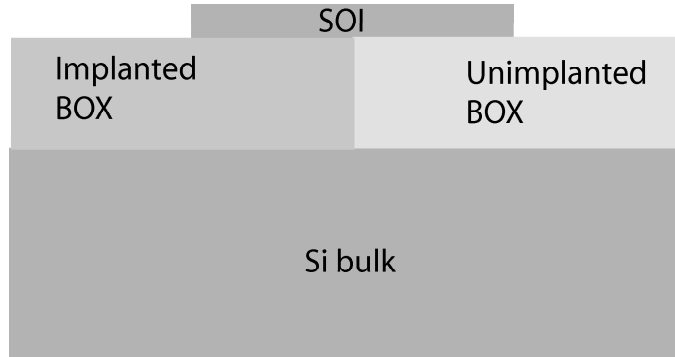


Figure 3.1: Schematic of the test structure.

The underetch was then measured in the unimplanted and implanted zones in function of the process parameters. The first chapter emphasized on the autocatalytic character of the reaction and on the role of water. The amount of water is a key parameter controlling the etch rate of the reaction. Varying temperature and etching time affect the water amount presents on the wafer surface and can thus modify the etch rate and the etching selectivity.

The first Section presents the impact of the process parameters on the etching selectivity like temperature, etching time, geometry effects and proposes solutions to maximize the selectivity.

The second Section demonstrate the cavity revelation.

3.2.1 Influence of the process conditions on the etching selectivity

3.2.1.1 Temperature

In VHF, water which is a reaction byproduct and catalyst can condensate on the surface, enhancing thus the etch rate. The balance between condensation and evap-

oration of water is strongly dependent on the temperature. Etching tests have been performed during 4 min at temperatures varying between 40.5 and 52.2 °C. Table 3.1 summarizes the underetch in implanted and unimplanted areas in function of the temperature.

Etching temperature in °C	Underetch unimplanted oxide in nm	Underetch implanted oxide in nm
40.5	421	1520
47.5	163	767
52.2	-	159

Table 3.1: Under etch in implanted and unimplanted zones after 4 min VHF etching at various temperature.

It appears clearly that increasing the temperature decreases the etch rate in the implanted area. At low temperature water condensates on the wafer surface enhancing thus the reaction between oxide and HF. The underetch is 10 times larger at 40.5 °C than at 52.2 °C.

In the unimplanted areas the underetch is not measurable at 52.2 °C and increases when temperature decreases. The underetch in the unimplanted area is linked to the effect of temperature but SEM picture of the cross section of sample after etching shows that geometrical effects of the window opened in the SOI layer also contribute to the underetch in the unimplanted layer.

Fig. 3.2 presents SEM cross section of the unimplanted and implanted areas after 4 min etching in VHF.

In the case of etched implanted oxide, at 40.5 and 47.5 °C, (Fig.3.2 (b) and (d)), the BOX is totally etched and the etching front is vertical. At 52.2 °C, the BOX was locally attacked, at the edge of the SOI film. The same effect is observed for the underetch of the unimplanted samples etched at 40.5 and 47.5 °C. The BOX is etched only in the vicinity of the SOI film edge. Fig. 3.3 presents a tilted view of this enhanced etching of the BOX close to the edge of the silicon film. This effect may be explained by the geometry at the edge of the SOI film. The RIE used to open the window in the SOI film did not stop on the BOX surface but etched also the half of the BOX thickness giving rise to a square angle in the oxide. The water produced by the etching at this angle in the oxide has more chance to recondensate

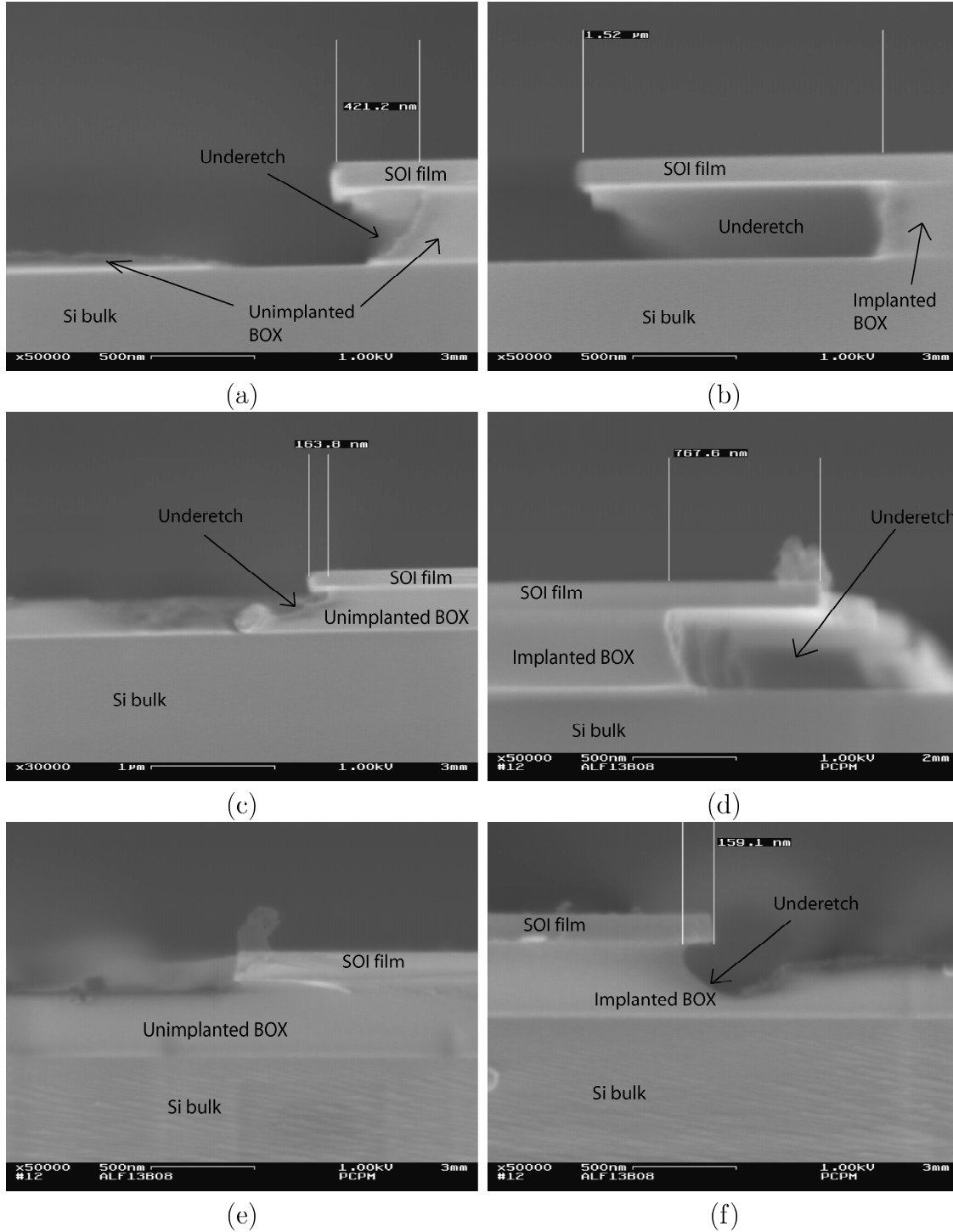


Figure 3.2: SEM cross section of the (a), (c), (e) implanted and (b), (d),(f) unimplanted samples after 4 min. VHF etching at (a),(b) 40.5 °C, (c),(d) 47.5 °C and (e),(f) 52.2 °C.

on the vertical oxide surface after evaporation, as explained in Fig. 3.4, yielding thus new reaction between oxide and HF. This is probably the source of this particular enhanced etching close to the SOI film edge.

The impact of temperature on the etching is a decrease of the etch rate of the

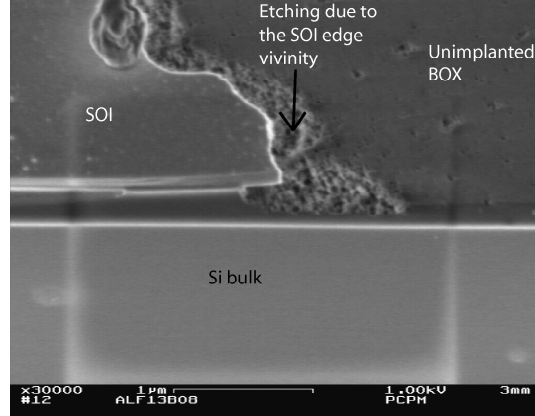


Figure 3.3: Unimplanted area after 4 min. VHF at 47.5 °C.

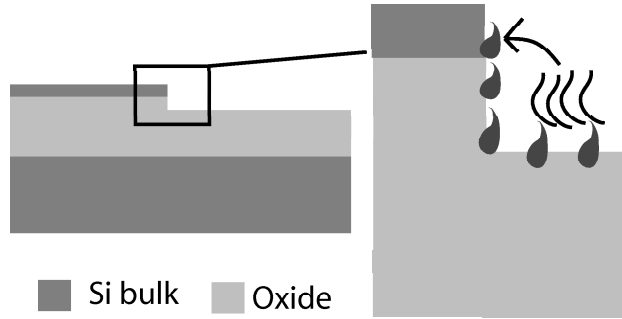


Figure 3.4: Recondensation at the edge of the Si film.

implanted area, accompanied by a decrease of the underetch in the unimplanted area yielding an increase of the etching selectivity. The temperature is therefore a parameter which influences etch rate and etching selectivity.

3.2.1.2 Etching time

The previous paragraph put into evidence the impact of the temperature on the amount of water presents on the surface. As etching produces water, if the evaporation rate is smaller than the condensation and production rate, the water will accumulate at the surface increasing thus the etch rate. The underetch has thus also been measured for various etching time. Fig. 3.5 plots the underetch in the implanted and unimplanted areas in function of the etching time. The underetch in the unimplanted area shows variation independent of the etching time for etching time shorter than 5 min. It increases then slightly to reach roughly 750 nm after 10 min etching. The underetch in the unimplanted area increases drastically after 5

min etching. More relevant parameters than underetch for micromachining are etch

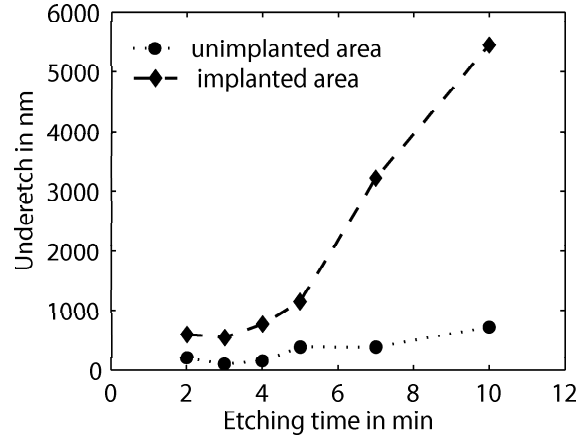


Figure 3.5: Underetch in the implanted and unimplanted areas in function of the etching time. The VHF etching was performed at 47.5 °C.

rate and etching selectivity. Fig. 3.6 plots the etch rate and etching selectivity in function of etching time. The etch rate is higher for two minutes etching than for

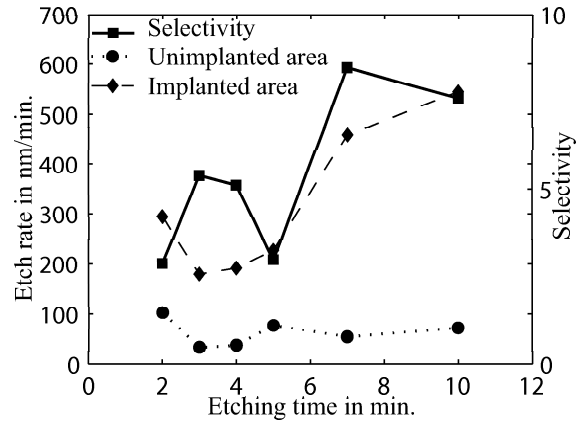


Figure 3.6: Etch rate in the implanted and unimplanted areas and etching selectivity in function of the etching time. The VHF etching was performed at 47.5 °C.

three minutes. This can be attributed to the water condensed on the wafer during the storage of the wafer before etching. Witvrouw et *al.* showed that the pre-heat time preceding the VHF etching can influence the etch rate for short etching times due to the presence of condensed water on the sample surface [1]. Fig. 3.7 and shows cross section of the samples in the implanted and unimplanted areas for different etching times. The etch rate of the unimplanted oxide is quite constant with respect to etching time. The etch rate of the underetch in the unimplanted area is quite stable, although difficult to estimate due to the geometrical effect described in

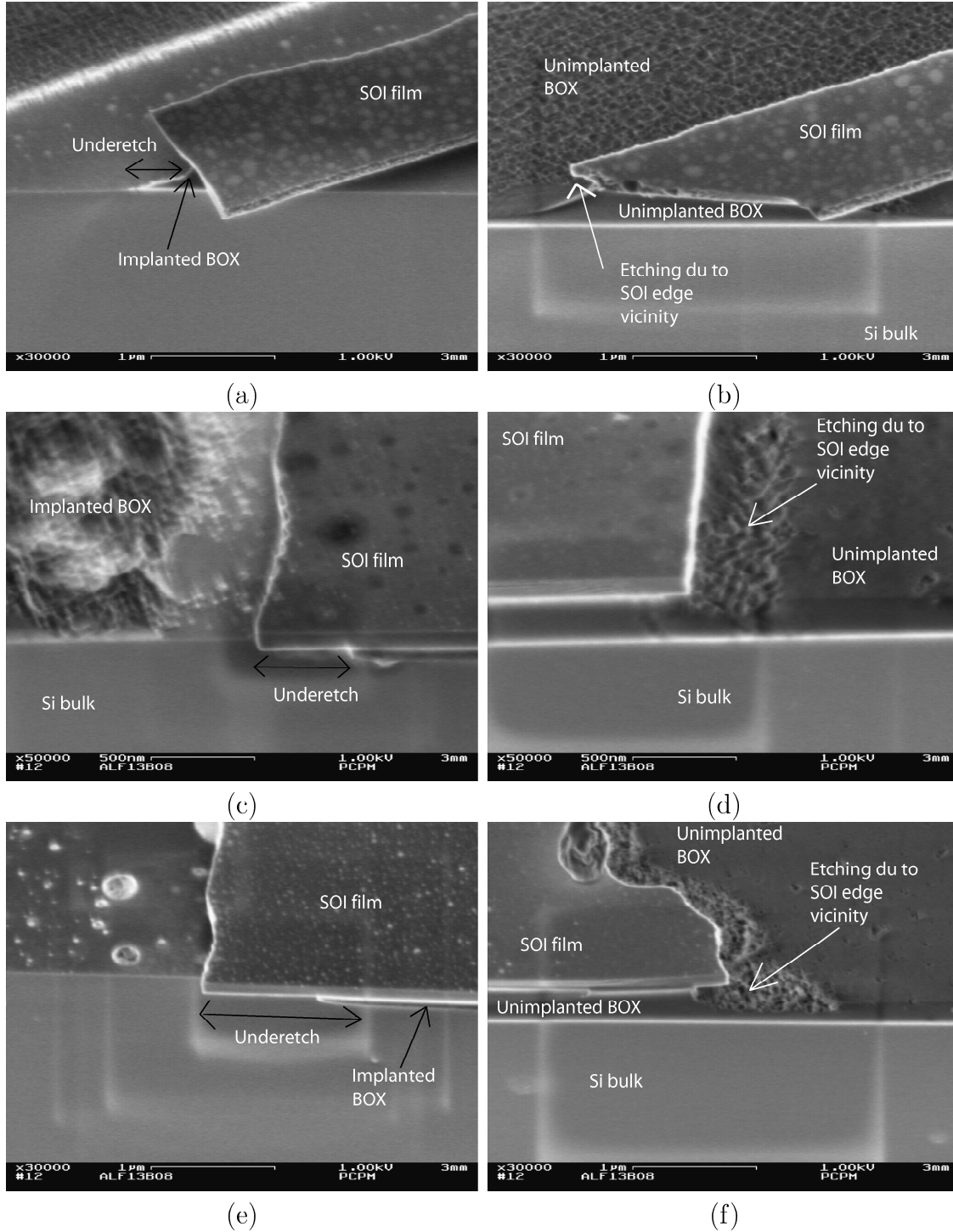


Figure 3.7: SEM cross section of the (a), (c), (e) implanted and (b), (d),(f) unimplanted samples after VHF etching at 47.5 °C during (a),(b) 2 min, (c),(d) 3 min and (e),(f) 4 min.

Fig. 3.3. The etch rate in the implanted area is larger than in the unimplanted area but increases drastically after 5 min etching enhancing thus the selectivity. The accumulation of water issue from the reaction in the implanted area which are etched faster and produced thus more water is responsible for this etch rate increase after

5 min. The Etching selectivity shows two regimes.

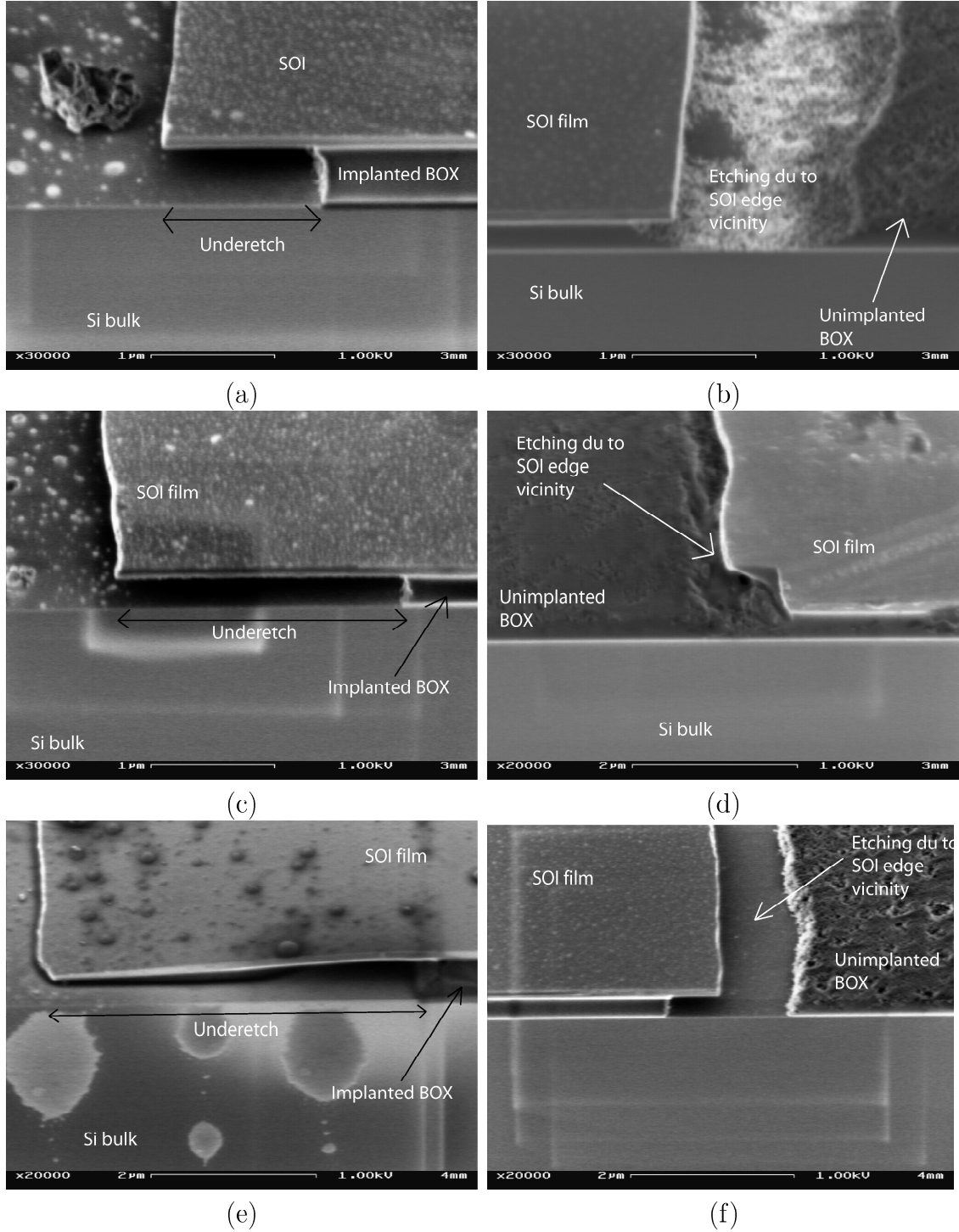


Figure 3.8: SEM cross section of the (a), (c), (e) implanted and (b), (d),(f) unimplanted samples after VHF etching at 47.5 °C during (a),(b) 5 min, (c),(d) 7 min and (e),(f) 10 min.

For etching times shorter than 5 min, the selectivity ranges between 3 and 5. Above 5 min, the selectivity is around 10 for the underetch rate between implanted and unimplanted areas. However, for too long etching time the selectivity tends to

decrease due to water accumulation on the unimplanted areas.

The SEM cross sections for the wafer etched during a short time show enhanced etching at the edge of the silicon mask. This effect is even more pronounced for longer etching time, as shown in Fig. 3.8. After 10 minutes in VHF the etching of unimplanted oxide combined with the edge effect yields unacceptable results due to the excessive underetch in the unimplanted area. The accumulation of water causes local enhancement of the oxide etch rate, independently on the damages created into the oxide. This water accumulation can be amplified by the structure shape. The following paragraph details the impact of the structure shape and its associated proximity effect.

3.2.1.3 Proximity effect

The etching temperature and time influence the etch rate of implanted and unimplanted oxide by modifying the amount of condensed water on surface. The shape of the etched structure can also influence the water condensation. As shown in Fig. 3.3, water preferably condensates at an edge of the structure and enhances thus the etch rate.

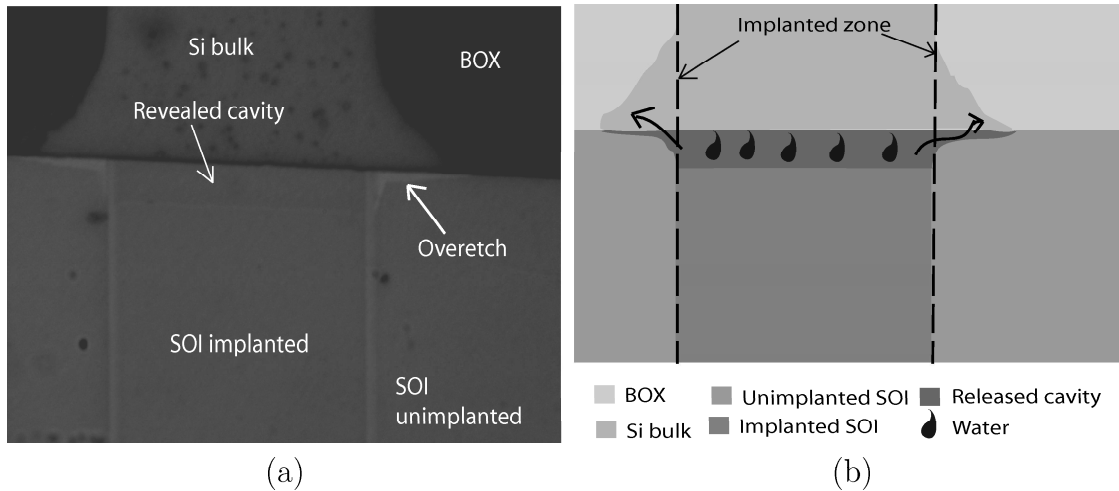


Figure 3.9: (a) Optical microscopy of a revealed cavity. (b) Schematic of a revealed cavity.

In the case of a buried layer etching, the water vapor will have to escape at one of the end of the masking film. The water concentration will thus be higher close to the structure boundaries. Fig. 3.9 illustrates that the exhaust of the water through the cavity entrance recondensate close to the entrance and at the boundaries of the

cavities yielding thus an etching of the unimplanted oxide, under the SOI film and on the uncovered unimplanted BOX. Fig. 3.10 shows a SEM picture of the etching propagation to the unimplanted oxide when revealing a buried cavity.

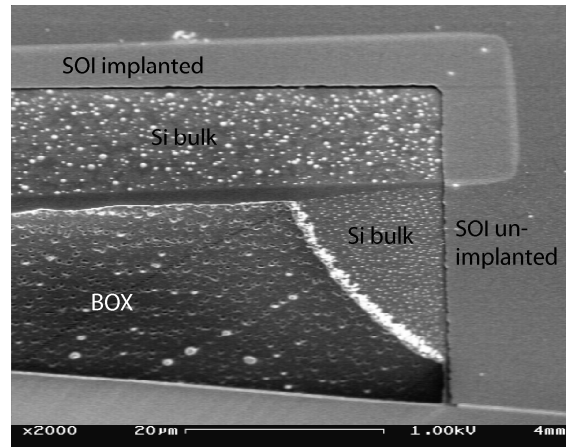


Figure 3.10: SEM tilted view of the revealed buried mask. The VHF etching was performed at 47.5 °C during 10 min.

The etching propagation is clearly enhanced in the vicinity of a released membrane. A typical V-shaped underetch occurs in the unimplanted area close to the boundary of the SOI film due to the water vapor flowing out from the etched cavity.

Selective etching of implanted silicon dioxide presented in the previous chapter had shown a selectivity of 200 when a top oxide film was etched. This very high selectivity is not to be found when etching a buried cavity. Decreasing the temperature increases the etch rate but decreases the etching selectivity. Inversely increasing the temperature decreases the etch rate but increases the etching selectivity. As in MEMS micromachining the typical dimension of buried sacrificial layer to release is on the order of the tens of micrometers, etching at high temperature would not be possible for the release of large structures. Increasing the etching time to compensate the low etch rate also decreases the selectivity due to the accumulation of water in any angular shape, which increases the etch rate in the unimplanted areas. Moreover, during the etching of the buried sacrificial oxide layer, the water produced by the etching is confined between the bulk silicon and the top SOI layer. This enhances the etch rate at the etch front but produces V-shape at the edge of the SOI film, where the water vapor flows out. The difficulty of the VHF selective etching of implanted oxide is that water, which is a reaction byproduct is catalyst of the reaction. We have to find process conditions, mainly etching time and temperature

for which evaporation rate of water is larger than the condensation and the water production rate on the unimplanted oxide but lower than the water production rate on the implanted oxide. Under these conditions etching will occur in the implanted areas and not in the unimplanted ones. Unfortunately in the case of buried cavities the confinement of produced water enhances the etch rate and propagates the etching to unimplanted regions. Too long etching times cause also water accumulation and decreases the etching selectivity. The following section presents a solution to maintain the etching selectivity while long underetch is required.

3.2.1.4 Etch - Rinsing Cycles

The control of the water amount over the oxide surface is a critical parameter allowing to achieve a high etching selectivity between implanted and unimplanted zones. A default of water will stop the etching, an excess of water will decrease the selectivity, therefore the process parameters such as time and temperature are critical. It has been also shown that for too long etching time the water accumulates on the surface and decreases thus the etching selectivity. To maintain the selectivity at a high level, it is necessary to avoid water accumulation. Etching is therefore performed according to the following cycle:

- VHF etching step
- N₂ rinsing step

Etching occurs during the VHF step while the accumulated water is removed during the N₂ rinsing step. Thanks to this method, one avoids water accumulation, which was responsible for the etching selectivity deterioration. Fig. 3.11 shows an optical top view of the sample after a cycling etching. The SOI film is released only in the implanted area. The underetch is limited in the unimplanted area. The etching does not propagate from the implanted areas to the unimplanted ones, the boundary between implanted and unimplanted area is sharp. No typical V-shape as in Fig. 3.9 and 3.10 is observed when performing etching-rinsing cycles. Fig. 3.12 plots the SEM cross section of an oxidized SOI wafer which has been implanted in order to create damages in the top oxide and in the buried oxide.

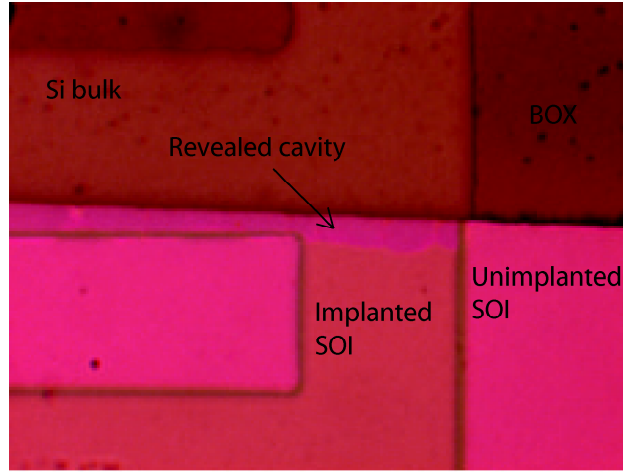


Figure 3.11: Optical microscopy top view of the revealed buried mask. 60 cycles of 1 min VHF 2 min N₂ rinsing performed at 40.2 °C.

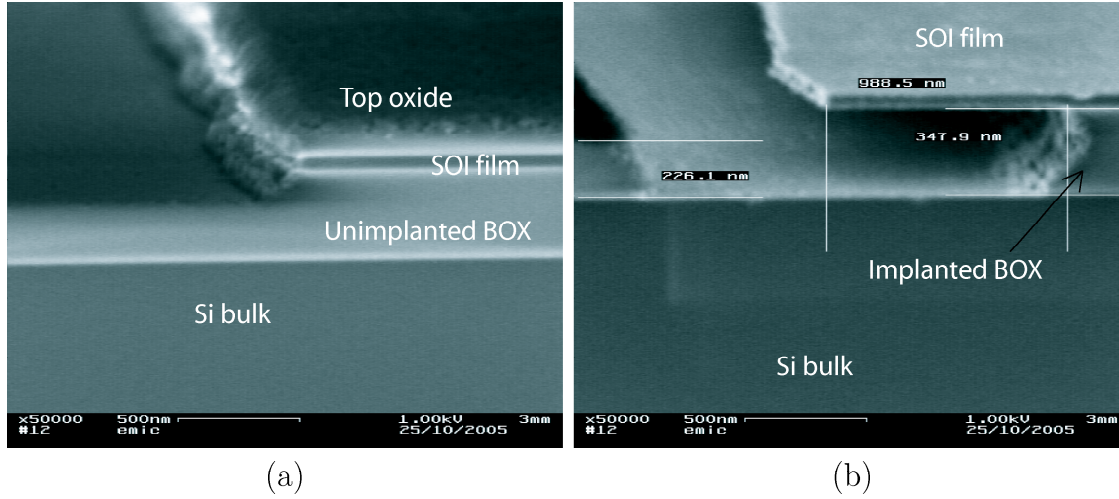


Figure 3.12: SEM cross section of the (a) unimplanted and (b) implanted samples after 15 cycles of 2 min. VHF etching and 3 min. N₂ rinsing at 40.2 °C.

After a cycling etching at 40.2 °C, the underetch is negligible in the unimplanted area and reaches roughly 1 μm in the implanted area. This result shows that VHF etching is very sensitive to the process conditions. The selectivity can be maintained at high values by tuning the process cycling times very accurately. Indeed, doubling the cycling etching time can strongly affect the etching selectivity. Fig. 3.13 shows the same sample than in Fig. 3.12 but for a double cycling etching time. The etching selectivity is lost. The total etching time is identical than in the case of Fig. 3.12. The etch rate in the unimplanted area is larger and the selectivity is poorer. This confirms that the etching time is a very sensitive parameter and that etching-rinsing cycle principle has to be considered in order to achieve good selectivity.

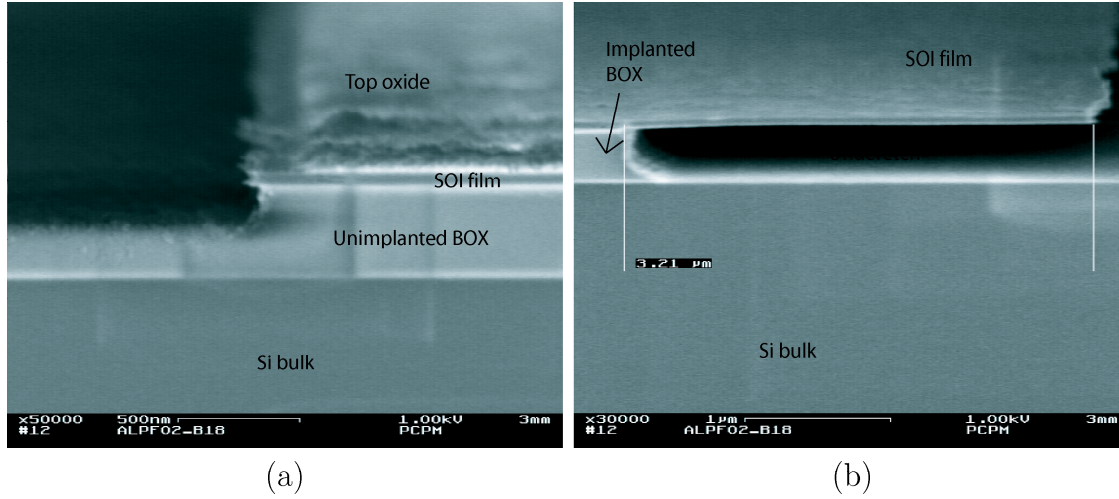


Figure 3.13: SEM cross section of the (a) unimplanted and (b) implanted samples after 7 cycles of 4 min. VHF etching and 5 min. N₂ rinsing at 40.2 °C.

3.2.1.5 Conclusion

The influence of temperature and etching time on etching rate and selectivity have been characterized. From these results we can concluded that the etching has to be performed under cycles of VHF etching directly followed by a N₂ rinsing in order to evacuate the accumulated water which is responsible for the selectivity degradation. Unfortunately, all these tests performed on 1 cm² samples are not valid any more on three inches wafers. Indeed the VHF etch rate decreases with the wafer size [1] and varies with the density of structures to be etched. The cycling time and temperature have then to be re-calibrated for each new design of structure to reveal. Although this inconvenient, the revelation of buried cavities in oxide thanks to selective etching of damaged silicon dioxide is a new technique allowing a broad field of applications.

3.2.2 Definition of the buried structures

As shown in the previous paragraph revelation of buried mask and cavities in silicon dioxide is highly sensitive to the process conditions. The use of short etching steps followed by rinsing steps allows the release of SOI membranes only in the area where the BOX is implanted. Although the good results obtained in term of etching selectivity it has been shown that the shape of the implanted zone could affect the shape of the released membrane (Fig. 3.9 and 3.10). In the previous section, the released membranes had a dimension in the range of hundred of microns and the

aperture in the membrane allowing the penetration of VHF into the cavity was also on the same size order. Such membranes are of interest in MEMS applications but as seen in the Sec. 1.2.1, self-aligned planar double gate fabrication requires the fabrication of cavities in the same size order as a transistor gate. This section will thus investigate the feasibility of cavity release for which the section of the aperture through which the VHF can enter the cavity is a few microns wide for a few hundreds nanometers high and over length of a few tens microns.

3.2.2.1 *Sample fabrication*

The idea being to demonstrate that the top bottom gates of a double gate transistor could be defined in oxide by ion implantation . We thus tried to reveal a cavity in a buried oxide film aligned on a trench in a surface oxide film. For cost reason oxidized bulk wafers on which polysilicon was deposited by LPCVD were used instead of SOI wafers. The polysilicon film was supposed to model the SOI film, in which the transistor channel would be built. The top and bottom oxide films were 100 nm thick. The top oxide film was made by thermal oxidation of the polysilicon film. The remaining polysilicon thickness after oxidation was 50 nm.

The zones to be implanted were defined by photolithography. The implantation mask was a dark field with apertures under the form of lines from which the width varied from 1 to 10 μm and length varying from 3 to 100 μm . The buried mask was defined by phosphorous implantation in two steps. The first implantation was performed at 170 keV and at a dose of $3.5 \times 10^{16} \text{ atm/cm}^3$. A second implantation was done at lower energy, 50 keV, and at a dose of $5 \times 10^{15} \text{ atm/cm}^3$ to create the same damage concentration in the top oxide as in the bottom oxide. The final nuclear deposited energy was $1.5 \times 10^{26} \text{ eV/cm}^3$ in the implanted areas according to SRIM simulations (Fig. 3.14).

Fig. 3.15 shows a schematic of the sample fabrication used for the following experiments.

Although we tried to minimize the damages to the photoresist mask by doing the high dose implantation in 10 times, it was nevertheless a bit destroyed after implantation as can be seen in Fig. 3.16 (a), but some parts on the wafer are still unaffected by the photoresist destruction and can be used as test samples (Fig. 3.16

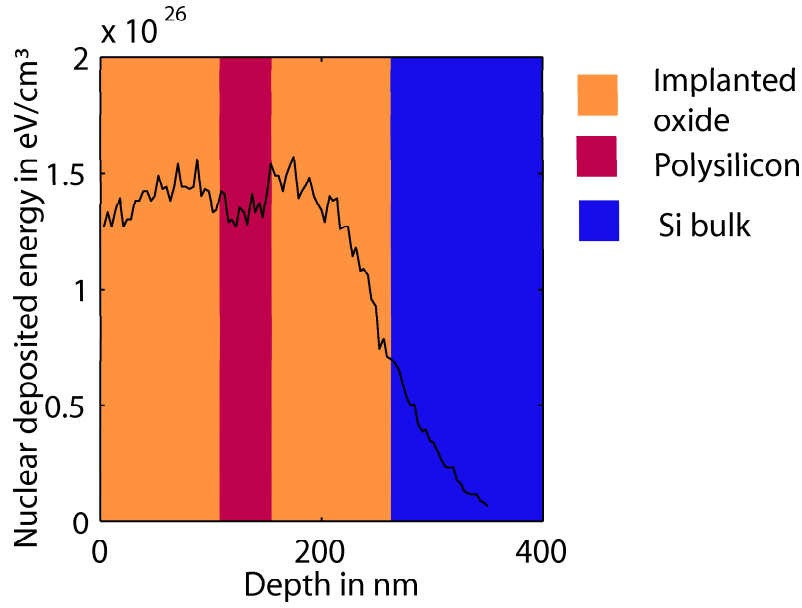


Figure 3.14: SRIM simulation of the nuclear deposited energy in the oxide / poly / oxide stack after the phosphorous implantation at 170 and 50 keV and at respective doses of 3.5×10^{16} and 5×10^{15} atm/cm^3 .

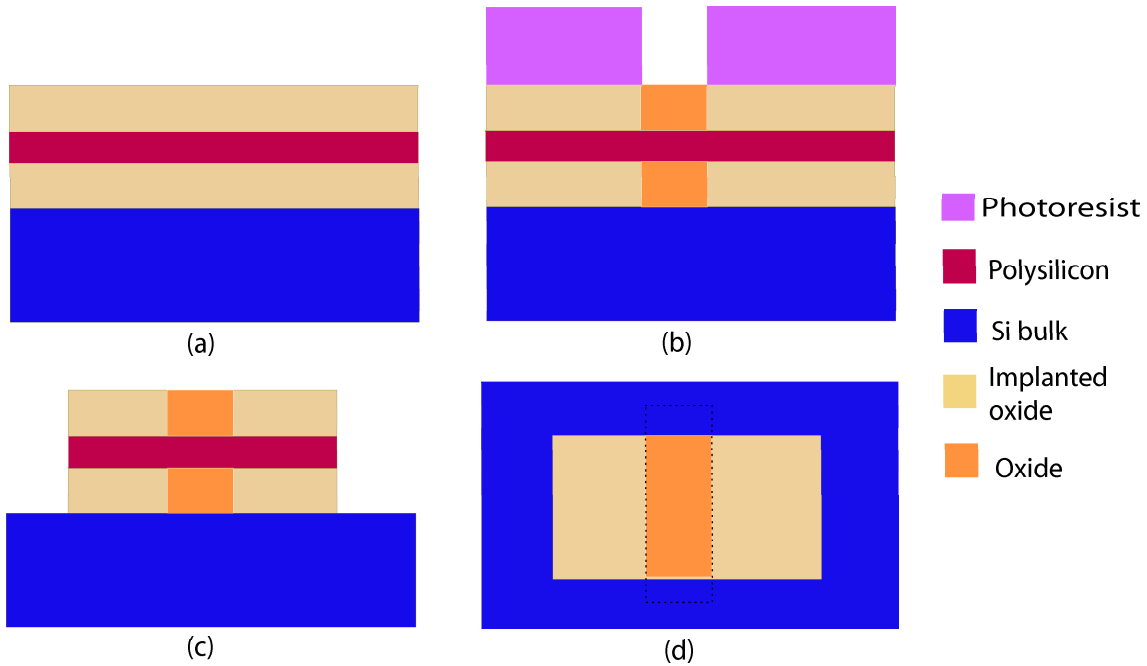


Figure 3.15: Schematic of the sample fabrication. (a) the polysilicon deposited on the oxidized bulk wafer is oxidized, (b) the buried mask is defined by ion implantation, (c) access to the bottom oxide is defined by a mesa process, (d) top view of the final sample.

(b)).

After the buried mask and the top oxide implantations, another photolithography was performed to define the access to the bottom oxide layer in order to be able to

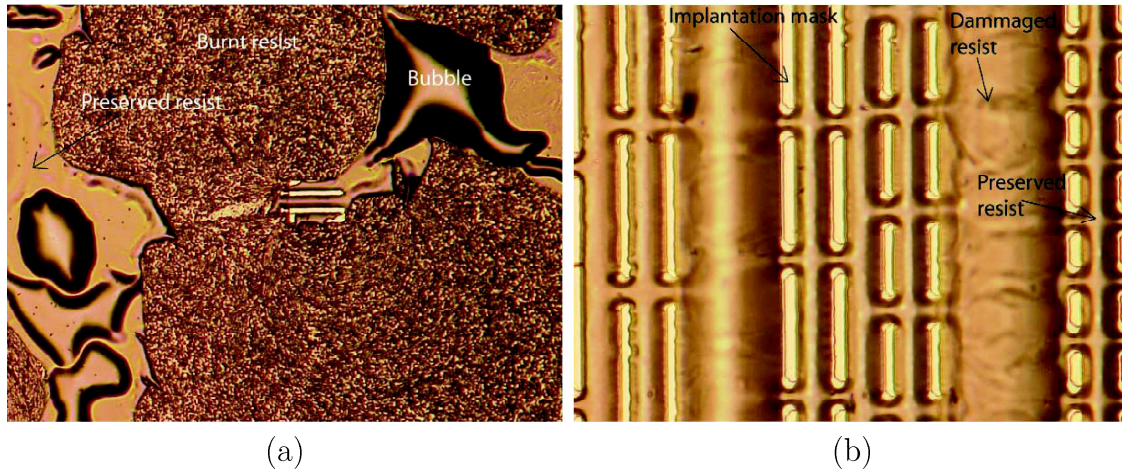


Figure 3.16: Optical microscopy of the photoresist mask after implantation. The mask was partially destroyed (a), but some test structures were preserved (b).

reveal the buried mask. The mask used was a light field defining mesa around the implanted area. The two oxide layers and the polysilicon layers were etched by RIE. After photoresist removal in oxygen plasma, and cleaning in smoking nitric acid it can be observed that the wafer were partially damaged due to the poor resistance of the resist to implantation, but still as shown in Fig. 3.17 some parts of the sample can be used for experiments.



Figure 3.17: Optical microscopy of the sample surface after photoresist removal. The dark zones are the one that were protected by the photoresist mask. The light zones are the one where the resist was destructed.

3.2.2.2 Buried cavity revelation

Based on the results presented in Sec. 3.2.1, we performed our experiments on 1 cm^2 samples with the following process conditions: VHF etching time of 1 min, 2 min of N_2 rinsing, fixed temperature of 38°C , and various number of etching rinsing cycles were considered.

Fig. 3.18 shows the cavity revelation as a function of the cycles number for $20 \mu\text{m}$ wide cavities. The cavity length was known from the structure layout and then used as a reference for further measurement on the structure.

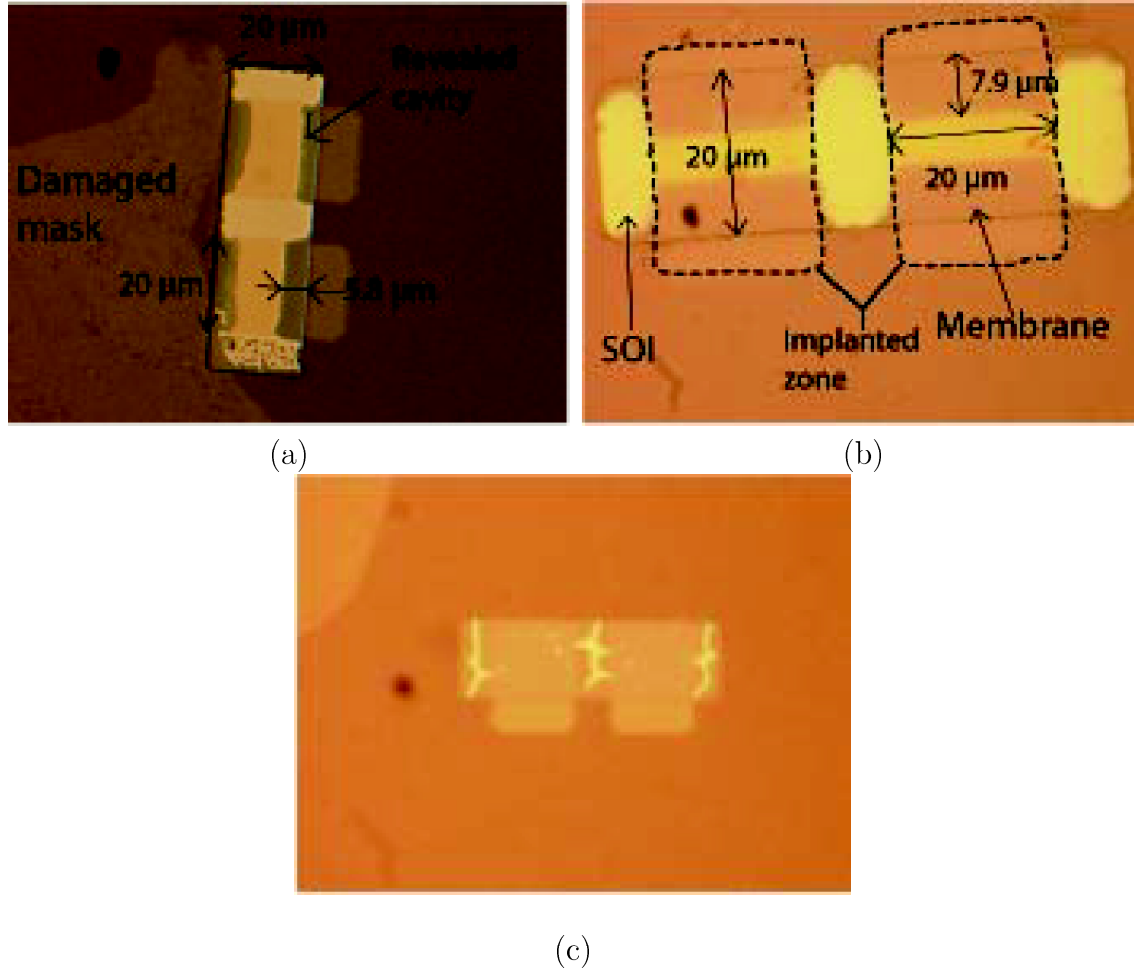


Figure 3.18: Samples after (a) 60, (b) 120 and (c) 180 cycles of 1 min VHF etching and 2 min N_2 rinsing.

The cavity revealed had a width of $20 \mu\text{m}$ and a length of $20 \mu\text{m}$. As the opening were on the both sides of the cavity, we measured the revealed length only from one side. After the first 60 cycles the revealed length of the cavity was $5.8 \mu\text{m}$ and the

selectivity between doped and undoped zone was very good. After 120 cycles the revealed length was $7.9\ \mu\text{m}$, but the selectivity was poorer than for shorter etching time. After 180 cycles, the membrane was totally removed but the unimplanted areas were also strongly attacked. During the first 60 cycles 96 nm were etched per cycles in average. During the following 120 cycles, only 35 nm were etched per cycles in average. This decrease of the etch rate with the etching time is due to the small height of the cavity (200 nm) which is an obstacle for gases penetration. The deeper the etch front penetrates into the cavity, the more time it requires for N_2 to rinse the etch front and for HF to replace N_2 after rinsing.

Fig. 3.19 shows the cavity revelation as a function of the cycles number for narrower cavities.

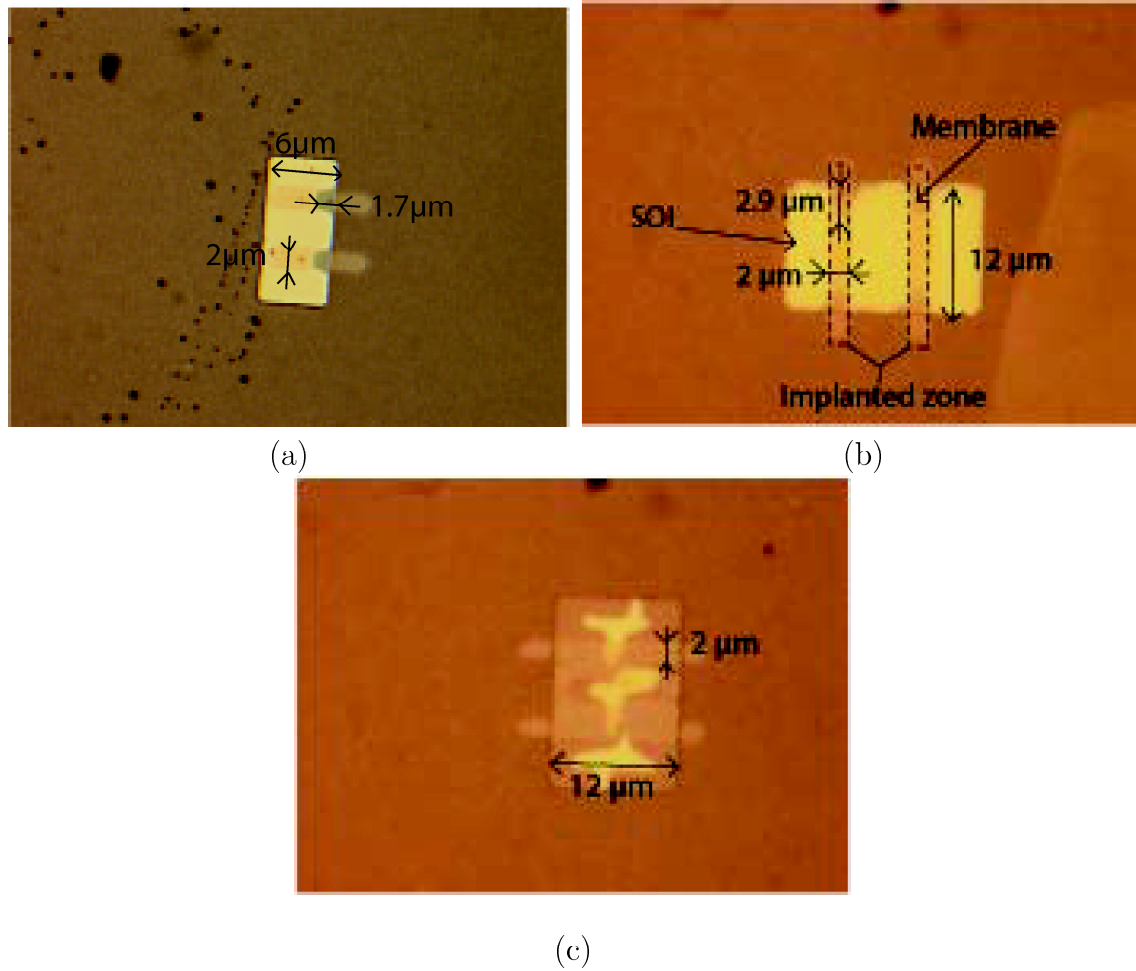


Figure 3.19: Samples after (a) 60, (b) 120 and (c) 180 cycles of 1 min VHF etching and 2 min N_2 rinsing.

The etched structures were 2 μm wide. The etched length into cavities was 1.7 μm after 60 cycles and 2.9 μm after 120 cycles. After 180 cycles, the unimplanted oxide was attacked and the selectivity was lost. As for the large structures the average etch rate per cycle tends to decrease with the length of the cavity. After 60 cycles the average etch rate is 28 nm/cycle and decreases to 20 nm/cycle after 120 cycles. These values are smaller than for larger cavities which can be explained by the smaller section of the cavity. Furthermore for smaller cavities the average etch rate per cycle decreases of 30 % as it was decreasing of 70 % when etching 120 cycles instead of 60. This lower decrease of the average etch rate is due to the smallest cavity length of the narrow cavities.

Fig. 3.18 and 3.19 show that although the etching selectivity can be maintained with cycling etching it decreases after too many etching cycles. 120 cycles seems to be an acceptable values of cycles that can be performed. It is thus possible to keep a fairly good selectivity and to reveal cavities. The maximal length of the cavities that are possible to reveal depends on their width. For 20 μm wide cavities, it can be deduced from Fig. 3.18 (b) that cavities of 20 μm wide and 16 μm long could be revealed at the condition that the etching is performed from the both extremities of the cavity. 2 μm wide cavities can be revealed if their length does not exceed 6 μm , according to Fig. 3.19 (b). Fig. 3.20 shows optical views of entirely revealed cavities of different sizes.

It can be concluded from Fig. 3.18 and 3.20 that the revelation of buried cavities, when revealed from the both sides, is possible if the cavities dimensions does not exceed some geometrical specifications. Narrow cavities, i.e. having a width smaller than 4 μm can have a length 2 to 3 times larger than the width. For small cavity width, increasing the cavity width increases the maximal cavity length, as it increases the section through which the VHF penetrates into the cavity.

The width of the revealed cavity is larger than the implantation mask width. The 2 μm wide implantation mask yields a 3.1 μm wide cavity. The 3 μm wide implantation mask yields a 3.9 μm wide cavity in the case of the 6 μm long cavity and a 3.3 to 5 μm wide cavity in the case of the 9 μm cavity. This is partly due to the lateral scattering of the implanted ions during the implantation and to the overetch to unimplanted areas. Unfortunately, as the SRIM software is able to calculate

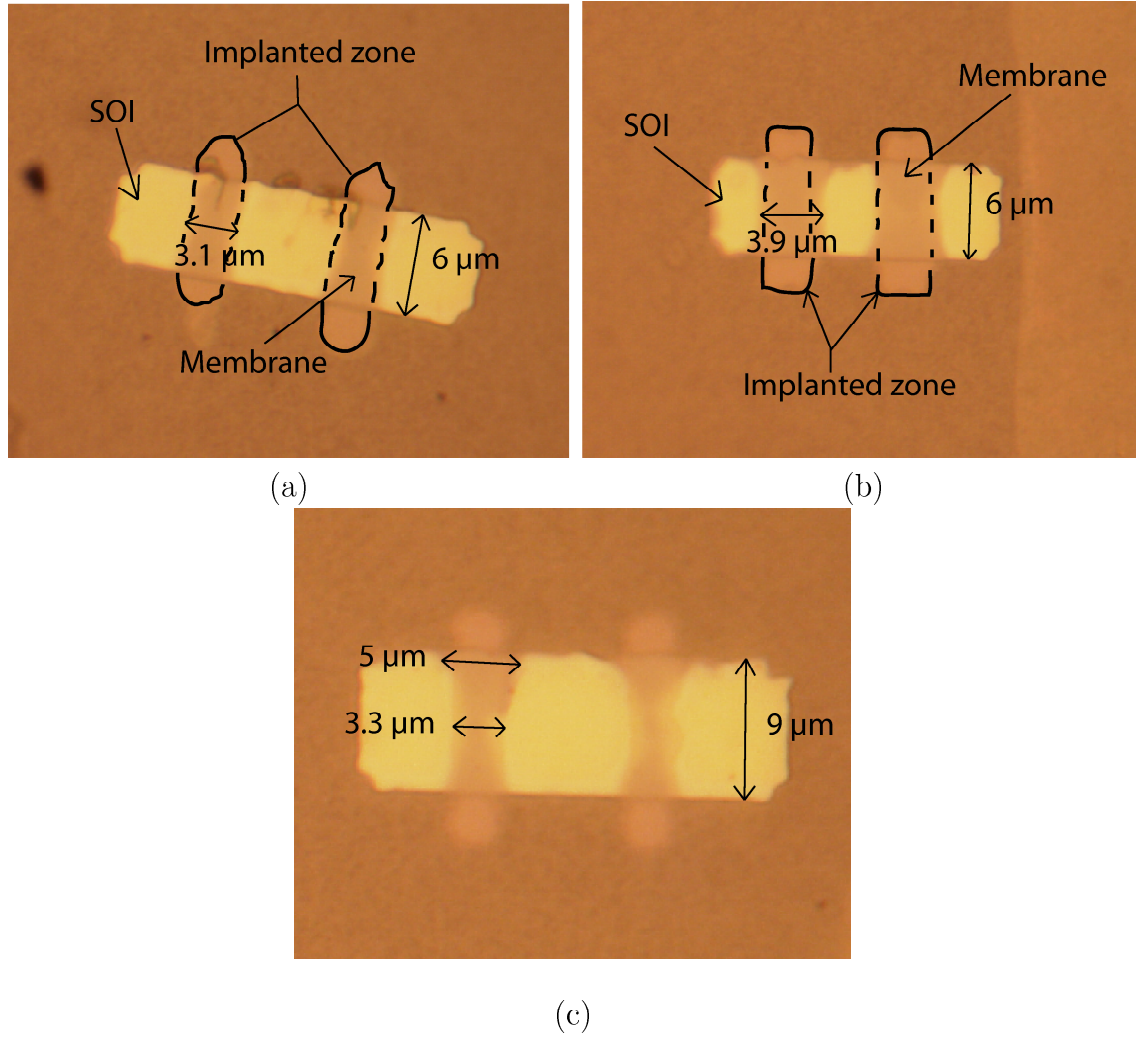


Figure 3.20: Samples after 120 cycles of 1 min VHF etching and 2 min N_2 rinsing. The implantation mask for the buried mask definition were respectively (a) $2 \times 6 \mu\text{m}^2$, (b) $3 \times 6 \mu\text{m}^2$ and (c) $3 \times 9 \mu\text{m}^2$.

the nuclear deposited energy only in one direction, we are unable to calculate the amount of nuclear deposited energy which scatters under the mask and therefore to predict the real size of the buried mask. The effect of etching propagation to unimplanted areas is clearly seen in Fig. 3.20 (c), where the cavity width is larger at the beginning of the cavity than at middle. For larger cavities, with a width in the $20 \mu\text{m}$ range, the maximal length is 75 % of the cavity width. For so large cavities, the limiting factor to the gases penetration is the height of the cavity, which was in our case 200 nm.

We have now demonstrated the feasibility of buried cavity revelation. The maximal size of the cavity revelation is unfortunately limited, as whole as the length

which depends on the cavity width. Due to the observation method which has been done by optical microscopy it was not possible to determine with a high accuracy the width of the revealed cavity and to compare it precisely with the implantation mask size. Moreover, optical microscopy does not bring any information on the vertical wall definition of the cavity. SEM imaging was therefore performed on sample from Fig. 3.20 (c) and is shown in Fig. 3.21.

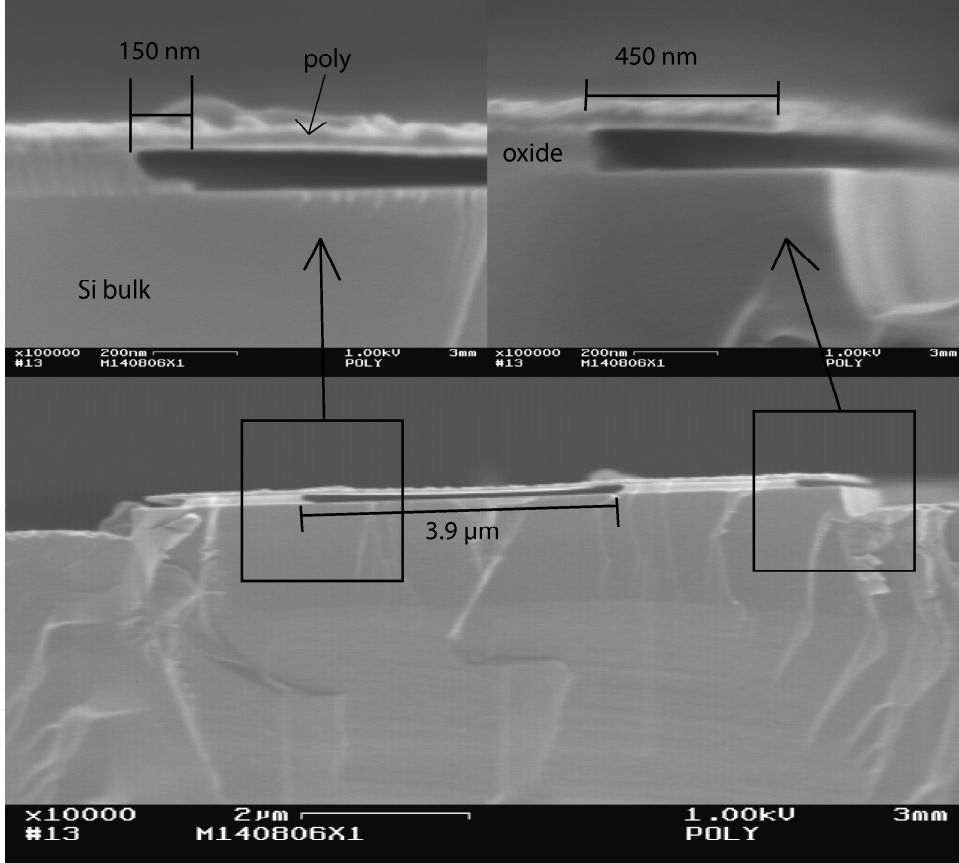


Figure 3.21: SEM cross section in the lateral direction of a revealed cavity after 120 cycles of 1 min VHF etching and 2 min N₂ rinsing. The implantation mask was 3 μm wide.

A limited underetch of 450 nm is observed in the unimplanted area, at the edge of the mesa. The vertical walls are defined with an accuracy of 150 nm. This can be attributed to the implantation which was not done at high enough energy. Although the fairly good cavity definition, we have to mention that the 200 nm thick top oxide layer was totally etched, which is coherent with the 450 nm underetch observed in the unimplanted areas. We conclude that the revelation of a buried cavity can be done, but as it needs an important number etching-rinsing cycles, a buried mask in a directly exposed oxide can not be revealed at the same time. Therefore the

process presented in Sec. 1.2.1 consists into revealing two self-aligned cavities rather than a buried mask aligned on a cavity.

3.2.2.3 Conclusion

Buried cavity revelation has been demonstrated. The ratio length over width of the cavities that can be revealed does not exceed 3 for narrow cavities with width in the 3 μm range. For larger cavities the ratio length over width decreases, to reach 0.75. The limitation of the cavity revelation length is due to the cross section of the cavity. For narrow cavities the cavity width is the limiting factor while it is the cavity thickness for wide cavities. The cross section of the cavities limits the VHF penetration into the cavity and the ability to rinse with N_2 . This effect becomes of importance when the revealed length is important. The etch rate per cycle therefore decreases with the revealed length.

In the case of the GAA process, the cavity was a square of $3 \times 3 \mu\text{m}^2$ [36]. Our process is an improvement because the W/L ratio can be larger than 1. Compared to the process developed by Chung, although we avoid a wafer bonding step, we cannot achieve a W/L ratio of 10 that was achieved [37].

Our results seems thus not to be scalable to narrow and long cavities revelation, and thus not of much interest for self-aligned planar double gate fabrication. However it can be used in fabrication of μm scale devices if one wants to reveal cavities from which the width is equal to the length. Nanometer scale devices could however be fabricated if the cavity width is very large compare to the cavity length, in other words, if the etch front is large but the underetch length small.

Although the revelation of buried mask in oxide on surface thin films has not been fully characterized, it is a promising method as the selectivity is maximal in theses conditions.

Potential applications of the selective etching of implanted oxide will be presented in the last paragraph of this chapter.

3.3 Buried mask in polysilicon

The previous section showed that it is possible to create buried cavities in silicon dioxide using the etch rate modification of silicon dioxide by ion implantation. In this section we describe the creation of positive and negative buried masks into polysilicon using the etch rate enhancement of n- or p-type doped polysilicon when etched in HNA and the etch rate reduction of boron doped polysilicon when etched in TMAH. We will also demonstrate that the revelation of buried cavities is unfortunately not possible.

A positive buried mask consists in reproducing in a buried layer the structure of the photoresist mask, i.e. removing the polysilicon in the zone where there was no resist on the surface. A negative buried mask consists in reproducing in a buried layer the inverse of the structure of the photoresist mask, i.e. removing the polysilicon at the zone where there was resist on the surface. In other words the implanted areas will behave respectively, as sacrificial material in the case of positive mask and as etch stop material in the case of negative mask (Fig. 3.22).

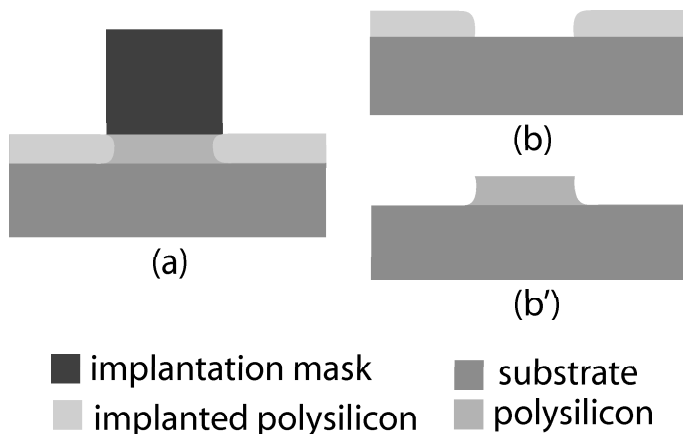


Figure 3.22: Comparison between negative and positive buried mask. (a) Implantation mask, (b) negative buried mask, (b') positive buried mask.

Our goal is to realize small structures using positive and negative buried mask in polysilicon.

3.3.1 Sample fabrication

The samples used to demonstrate the feasibility of buried mask in polysilicon were based on the similar architecture than the one used in section 3.2.2.1. The following

films were deposited on a bulk silicon wafer by LPCVD: 3000 Å nitride / 2000 Å polysilicon / 1000 Å nitride / 2000 Å polysilicon and 500 Å nitride. The purpose of the bottom nitride film is to separate the polysilicon layer in which the buried mask will be implanted from the bulk silicon. The top nitride layer was used as a screen layer during dopant implantation. Fig. 3.23 shows the schematic of the samples used for positive and negative mask revelation in HNA. n- or p- type doping both influence the polysilicon etch rate in HNA but as boron is lighter than phosphorous or arsenic, it penetrates deeper into the polysilicon at a given implantation energy. Moreover, boron doping of polysilicon induces tensile stress which decreases the etch rate of polysilicon in TMAH. Boron was therefore chosen as specie to be implanted into polysilicon, as the implanted area could be revealed in both HNA and TMAH. The photolithographic mask used to define the area to be implanted was a dark field. In the case of the positive buried mask implantation, the use of a positive photoresist yields small apertures in the photoresist spin-coated on the wafer. A negative photoresist was used to define narrow lines of resist for the negative buried mask implantation.

The implantation was done in three steps:

- 8×10^{15} atm/cm³ at 140 keV,
- 5×10^{15} atm/cm³ at 45 keV,
- 2×10^{15} atm/cm³ at 15 keV.

This implantation made at various doses and energies ensured a constant doping concentration in the top and bottom polysilicon film of 4×10^{20} atm/cm³. The doses and energies were calculated using the ATHENA software (Fig. 3.24).

The implantation photoresist mask was also used to etch away by RIE the top nitride film after implantation, in order to have a physical mark of the implanted zone. The mesa was defined by a second photolithography followed by a RIE to reach the bottom nitride film. The obtained sample had the same architecture than the one used to demonstrate the feasibility of buried cavities in oxide. The oxide layer are here replaced by polysilicon and the polysilicon is replaced by nitride. In the case of the buried mask in oxide the damage created by implantation were responsible for the etch rate modification so any thermal budget was to avoid after

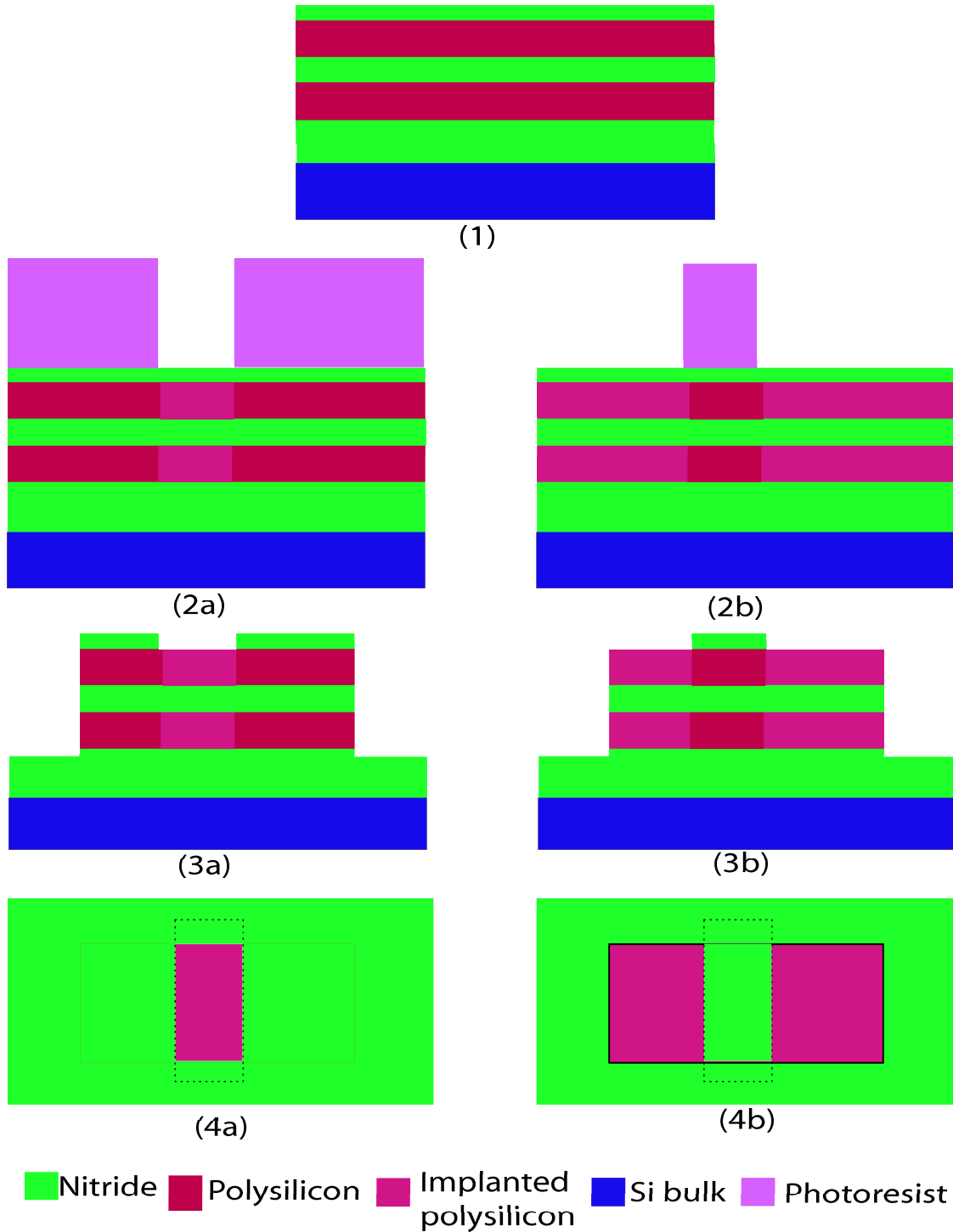


Figure 3.23: Schematic of the sample fabrication. (1) the stack of nitride and polysilicon films is deposited by LPCVD, the (2a) positive and (2b) negative buried mask are defined by ion implantation, (3a and 3b) access to the bottom polysilicon is defined by a mesa process, (4a and 4b) top view of the final samples.

ion implantation. For negative and positive buried mask revelation the physical effects used in the selective etching are respectively, tensile stress induced by boron in polysilicon and doping of polysilicon. In both cases the boron atoms need to occupy

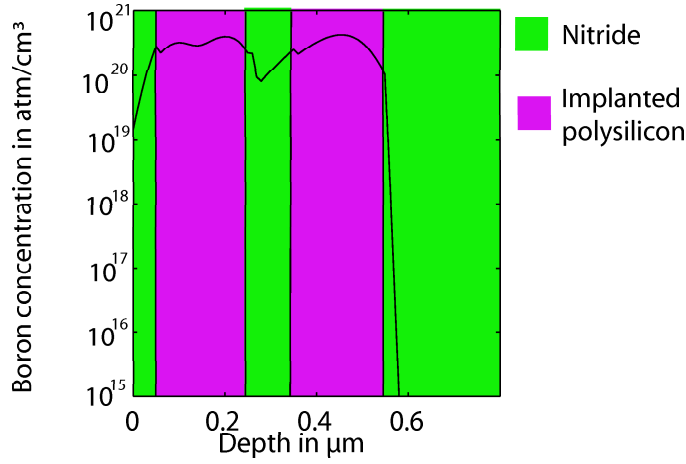


Figure 3.24: ATHENA simulation of the Boron implantation at 140, 45 and 15 keV at respective doses of 8×10^{15} , 5×10^{15} and 2×10^{15} atm/cm^3 . The simulation was done with the SVDP model.

substitutional sites on the lattice in order to induce stress and to be electrically active. After implantation the polysilicon is amorphized therefore a RTA is needed to recrystallize the implanted polysilicon and place the boron atoms at substitutional sites in order for them to be electrically active. The RTA was performed during 15 s at a temperature of 950 °C under a nitrogen flow of 2 l/min.

3.3.2 Positive buried mask in polysilicon

The Chapter 2 showed that a highly selective etching of doped polysilicon could be achieved in HNA [1:1:2] when performing the etching in a stirred solution under ultrasonic environment.

3.3.2.1 Attempt to reveal a buried cavity

In our first experiment we tried to reveal a cavity in the bottom polysilicon layer self-aligned with a trench in the top polysilicon layer as it has been done in oxide in section 3.2. The wafers were diced in 1 cm^2 samples and dipped in HNA for time varying between 30 s to 2 min. The solution was in an ultrasonic bath and stirred with a magnet. Fig. 3.25 shows the samples after etching for various etching time.

Etching of doped zones occurs, but propagates to the undoped zones. It has been shown in Sec. 2.4.3 that the etching of polysilicon in HNA is an autocatalytic reaction. The byproducts issue from nitric acid dissociation subsequent to silicon

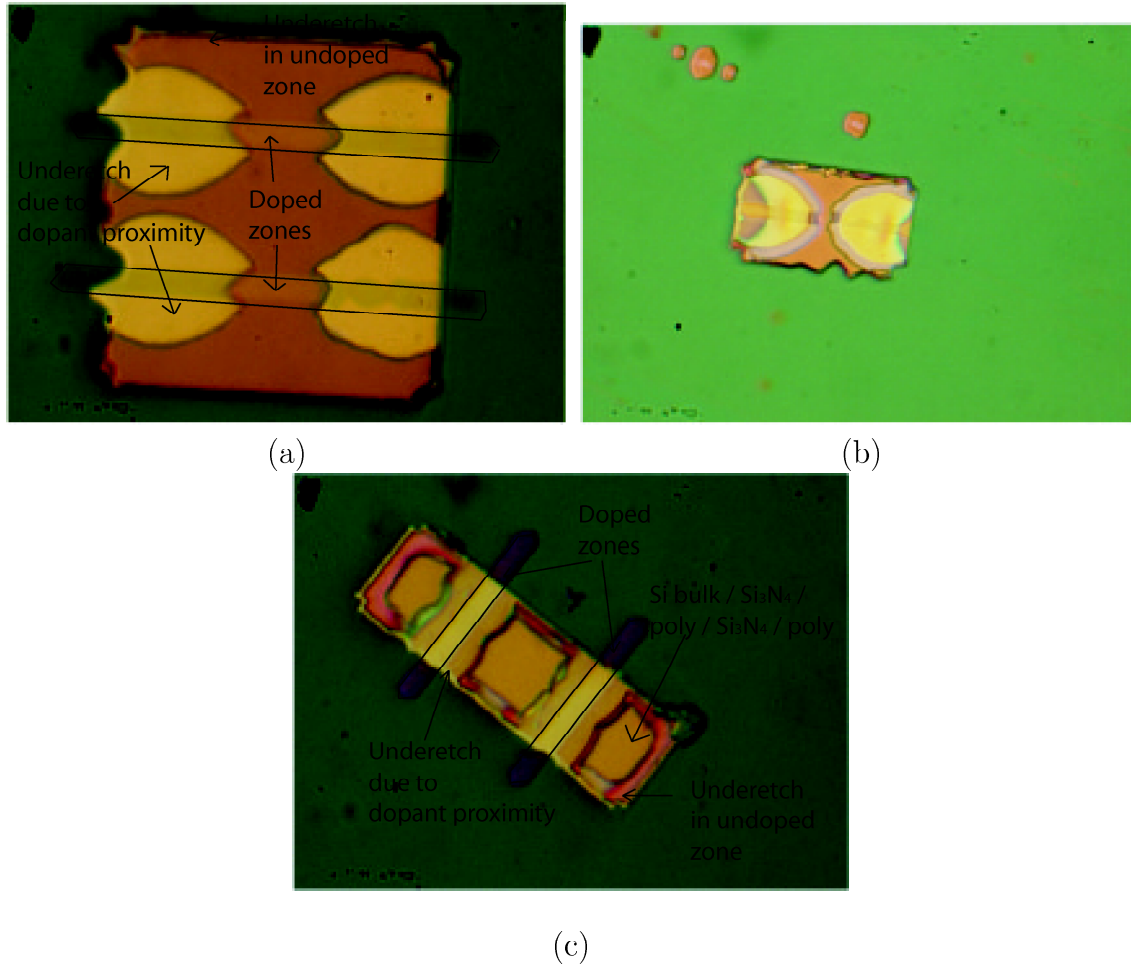


Figure 3.25: Samples after (a) 30 s, (b) 1 min and (c) 2 min etching in stirred HNA[1:1:2] in ultrasonic bath.

oxidation by nitric acid serve as catalyst for oxidation of silicon by nitric acid. It implies that once the reaction has started it continues. Washing out the surface of these catalysts stops the oxidation of silicon by nitric acid, except if the silicon presents atoms in excited states, which is the case for doped silicon and in the presence of defects. Ultrasonic bath and solution stirring have proved to be good method to remove the catalysts from the reaction sites, which yield highly selective etching of doped silicon versus undoped silicon. However, this method was developed on surface silicon. In the case of the sample from Fig. 3.25, as the etching is done in a cavity, the stirring of the solution is not efficient to remove the reaction byproducts from inside of the cavity. The ultrasounds certainly remove the reaction byproducts from the etch front but as they remain in the cavity they propagates the etching to the undoped area. It is also observed, for etching time of 2 min, that underetch

occurs in the undoped area. The polysilicon surface in contact with the solution has been etched by RIE, which might have created some defects yielding a higher reactivity to HNA and could thus explain the start of the reaction on the vertical wall of the mesa. Once the polysilicon film stack between the nitride layers has been attacked, a small cavity is formed and the removal of the etching byproducts is not very efficient, yielding further etching.

This experiment shows that it is unfortunately not possible to create buried cavity into polysilicon using the HNA selective etching of doped polysilicon versus undoped polysilicon because the removal of reaction byproducts, which are catalysts for the reaction, is not possible from the cavities, and one thus loses the etching selectivity.

3.3.2.2 *Revelation of a buried mask*

The previous section showed the impossibility to reveal buried cavity, however, as the selective etching in HNA of doped polysilicon works on surface material, it is possible to create a mask in a buried layer as illustrated in Fig 3.26.

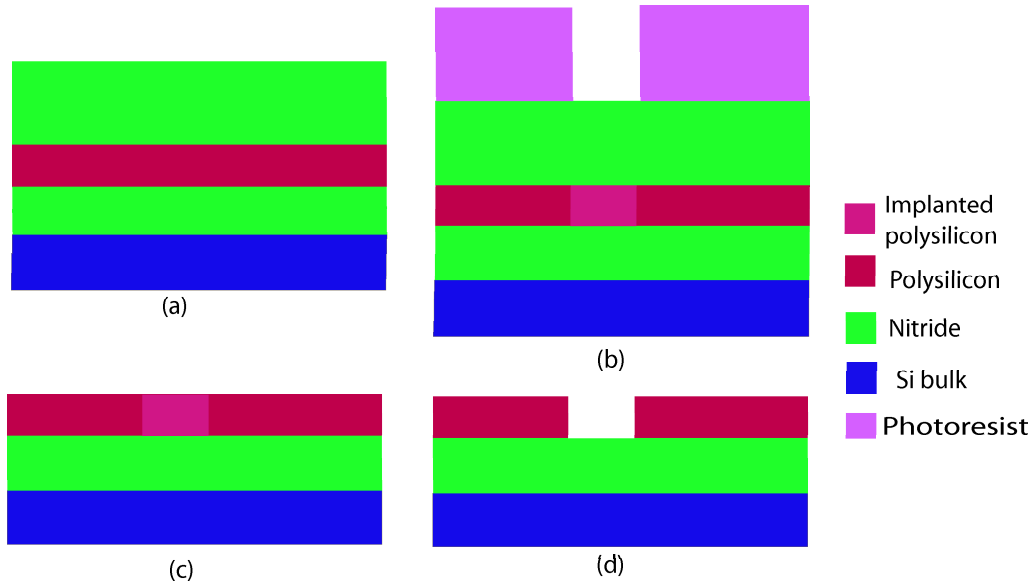


Figure 3.26: Example of buried mask revelation. (a) creation of a stack with a buried polysilicon layer, (b) implantation into the buried polysilicon layer, (c) removal of the top layer, (d) revelation of the doped area defined by implantation.

The samples from the previous experiment were thus used to demonstrate the revelation of buried mask. The nitride film covering the top polysilicon layer has

been removed after wet etching in H_3PO_4 at 174°C . The samples were then etched in HNA with stirring and ultrasound during 20 s. Optical microscopy have been done to investigate the quality of the revelation. Fig. 3.27 presents an optical view of the revealed structure.

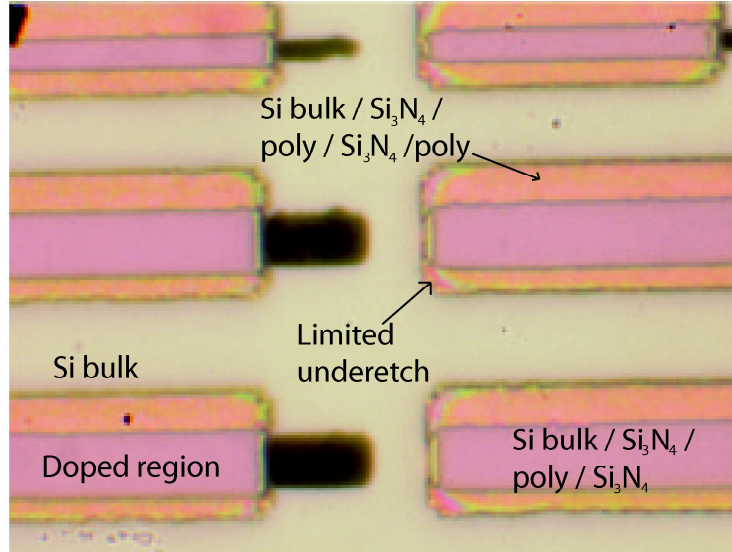


Figure 3.27: Sample revelation after 20 s in HNA. The etching was performed with stirring and ultrasound.

The doped polysilicon is totally removed and the selectivity between doped and undoped areas is preserved. The underetch in the undoped zone is limited to the edge of the structure. Fig. 3.28 shows optical microscopy of a quality test pattern and an array $1\ \mu\text{m}$ lines with an interspace of $1\ \mu\text{m}$.

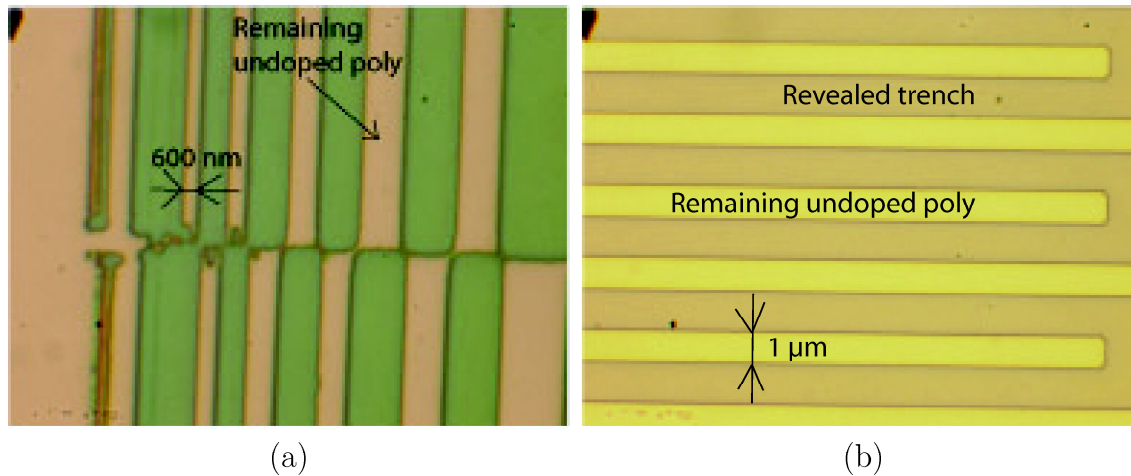


Figure 3.28: Optical microscopy of (a) the quality mark and of (b) an array of $1\ \mu\text{m}$ lines revealed after 20 s in HNA.

The narrowest lines from the quality test pattern are 600 nm wide. They are revealed although the quality of the photolithographic mask used for implantation was not optimal. SEM cross section of the revealed samples gives more informations on the profile of the revealed structures (Fig. 3.29).

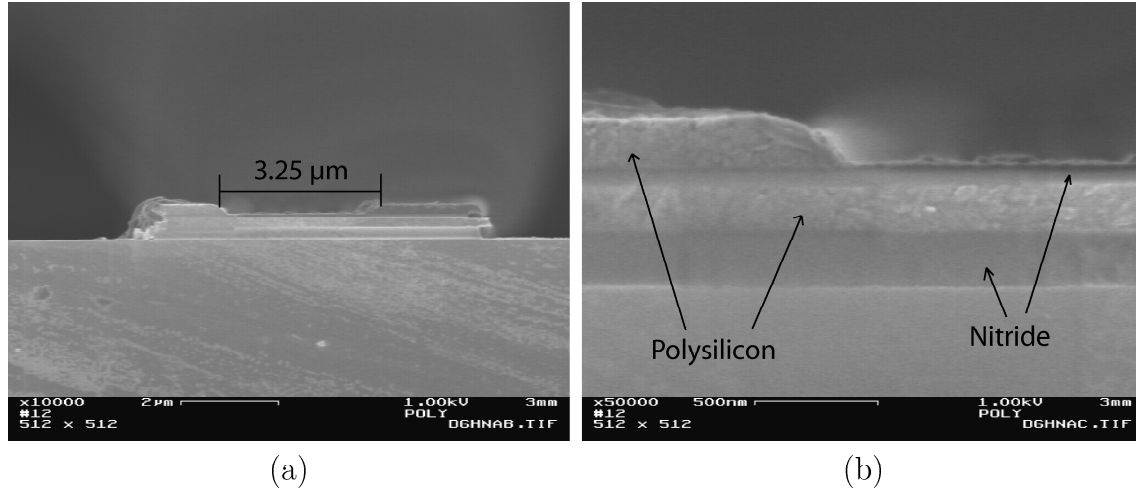


Figure 3.29: SEM cross section of the sample revealed in HNA during 20 s. (a) general view, (b) detail of the buried mask edge.

The aperture of the photolithographic mask used for implantation was 3 μm wide. The aperture of the buried mask is 3.25 μm at the top of the polysilicon layer (Fig. 3.29 (a)) and the walls of the buried mask are not perfectly vertical (Fig. 3.29 (b)). Underetch of the nitride films can be observed on the left hand side of Fig. 3.29 (a). It is a consequence of the top nitride film etching in orthophosphoric acid. The mask edge being not well defined with 20 s etching in HNA, the etching time was increased to 30 s in order to improve the buried mask definition (Fig. 3.30). Increasing the etching time yields a better definition of the mask walls. They are better defined but the size of the buried mask is larger than the photoresist mask used during implantation. It is due to the lateral scattering of the implanted ions under the implantation mask during ion implantation.

The simulation software ATHENA has been used to simulate, using the Monte Carlo algorithm, the lateral scattering of the implanted ions under the implantation mask. Fig. 3.31 plots the 2D simulation of the implantation at the edge of the mask. The implantation has been simulated for the doses and energy given in section 3.3.1. The tilt and twist were both null.

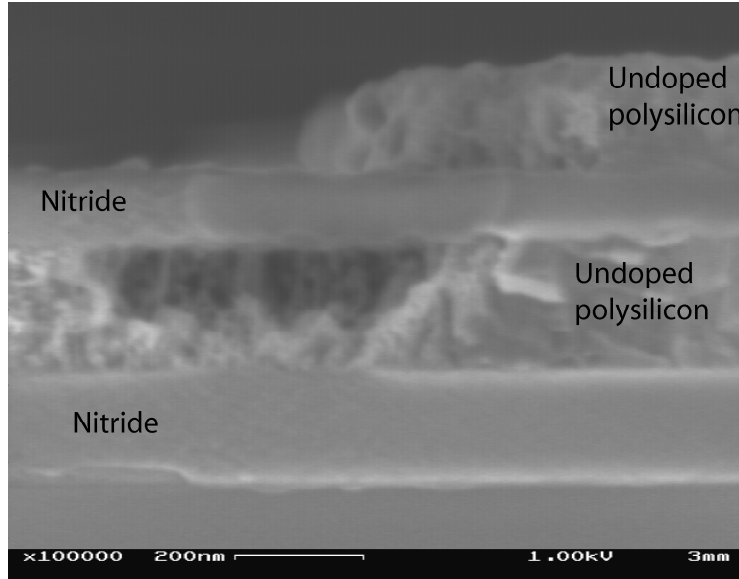


Figure 3.30: Sample revelation after 30 s in HNA. The etching was performed with stirring and ultrasound.

Boron concentrations higher than $2 \times 10^{19} \text{ atm/cm}^3$ are plotted in dark color, boron concentration lower than $1 \times 10^{19} \text{ atm/cm}^3$ are plotted in light color. These two limits of boron concentrations corresponds to the limit of selectivity for HNA etching between etched and unetched polysilicon. This way of plotting the boron concentration shows which part of the top polysilicon layer will be etched during the HNA etching. This simulation shows that the sacrificial layer penetrates 125 nm under the mask at a depth of 250 nm below the surface. Therefore the buried mask should be 250 nm larger than the implantation mask for a 200 nm thick layer lying 50 nm below the surface. Indeed implantation at higher depth requires a higher energy, for which the projected range R_p and the lateral range are larger. This enlargement of the buried mask compare to the photolithographic mask is observed in Fig. 3.29 (a), but also in Fig. 3.32 where one measures the remaining undoped polysilicon that was between two doped zones. The space between the two doped areas was $2.5 \mu\text{m}$. It remains here $2.23 \mu\text{m}$. Which corresponds roughly to the 125 nm that were etched on each side due to the lateral scattering of the boron under the mask. There is 20 nm difference between the measured buried mask size and its calculated value. This difference corresponds to the definition of the buried mask edge, which are defined with an accuracy in the 20 - 40 nm range.

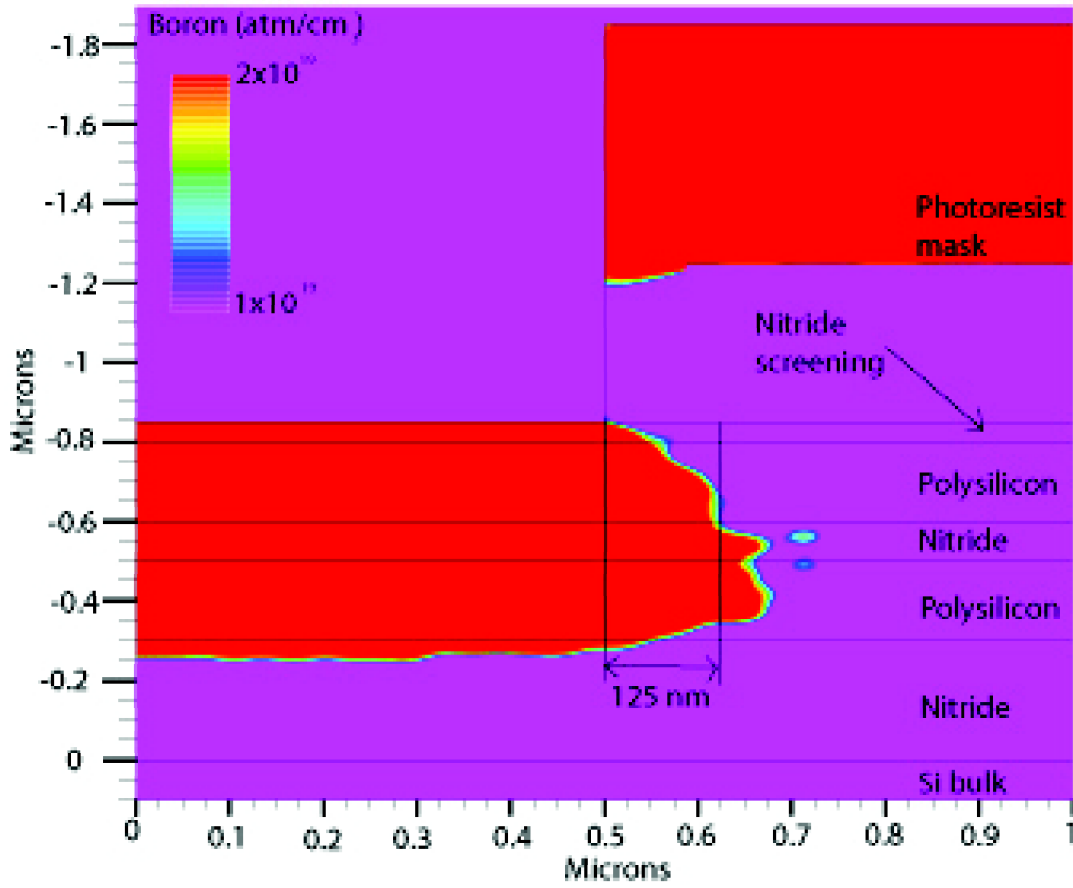


Figure 3.31: Monte Carlo simulation of the boron implantation done in three steps: 8×10^{15} atm/cm³ at 140 keV, 5×10^{15} atm/cm³ at 45 keV and 2×10^{15} atm/cm³ at 15 keV.

3.3.2.3 Conclusion

The revelation of positive buried mask in HNA is thus possible by defining doped zone with ion implantation. The difference in the calculated size of the structure, taking into account the lateral scattering of the doping species during ion implantation and the measured structure by SEM imaging is the the 40 to 80 nm range (twice the accuracy with which the edge is defined). This value might appear high but is partly due to the roughness of the vertical wall of the revealed structure, as can be seen in Fig. 3.29. The origin of this roughness arises from the implantation profile which is not straight in the shadow of the mask but presents some variation as can be seen in the simulated implantation profile from Fig. 3.31. Apart from the roughness of the vertical wall due to the implantation profile, it can be seen on Fig. 3.31 that the change in boron concentration from a value at which etching oc-

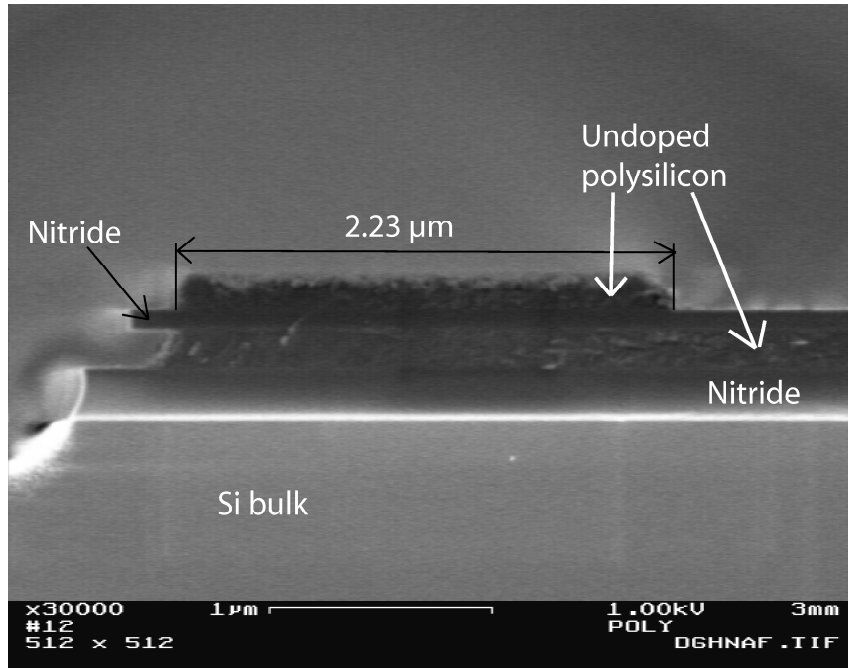


Figure 3.32: SEM cross section of a remaining undoped zone between two doped zones after 30 s in HNA with stirring and ultrasounds.

curs to a value at which no etching occurs (given in the graph from Fig. 2.44) is very abrupt and is done over a range of roughly 15 nm. This value is very low thanks to the very high selectivity of the etching. It might however be slightly underestimated as the diffusion during the RTA was not taken account during the simulation with ATHENA due to the lack of efficient simulation models.

3.3.3 Negative buried mask in polysilicon

The chapter 2.4.2 described the mechanism responsible for etch rate reduction of boron doped polysilicon in TMAH. We will demonstrate in this section, that it is possible to reveal negative buried mask in polysilicon.

3.3.3.1 Attempt to reveal a buried cavity

Revelation of a buried cavity in an oxide layer has been demonstrated in Sec. 3.2.2.2, but the Sec. 3.3.2 showed that it was not possible to reveal a cavity using a positive buried mask into polysilicon. This section shows that it is also unfortunately impossible to reveal a buried cavity using a negative buried mask into polysilicon. Fig. 3.33 shows a view of the negative buried mask sample presented in Fig. 3.23

after 9 min in a 10 % TMAH solution at 90 °C. It can be seen that no underetch

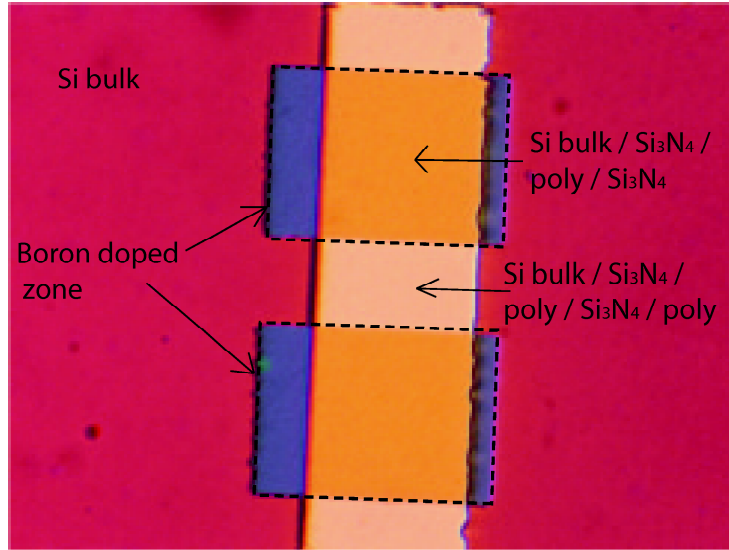


Figure 3.33: Optical microscopy of the sample after 9 min in 10 % TMAH at 90 °C.

occurred in the undoped area. A possible explanation is that according to Eq. 2.35 to 2.39 the etching of silicon in TMAH produces gaseous hydrogen, which is released under the form of bubbles. These bubbles stick on the surface for a short time until being released. The literature [2] shows that they are responsible for an increased roughness when etching silicon because they act as a mask when stuck on the surface. In the case of our samples, the etching might start and a small cavity might be formed, but then the produced H_2 gets trapped in the cavity and avoids any further etching. It has been tried to perform the etching in an ultrasonic bath, in order to release the trapped hydrogen, but it was not successful. Unfortunately revelation of buried cavity in polysilicon using a negative buried mask is not possible.

3.3.3.2 *Revelation of a negative buried mask*

Following the same experimental procedure as in section 3.3.2 we demonstrate here that although revelation of buried cavity is not possible, revelation with TMAH of negative buried mask is possible on a buried layer layer that has been implanted once the top layer is removed (Fig. 3.34) The top nitride from the samples from Fig. 3.23 was thus removed by wet etching in orthophosphoric acid at 174 °C. The samples were then revealed in 10% TMAH at 90 °C during 3 min. Fig. 3.35 shows a optical microscopy top views of the sample after TMAH revelation. The revealed

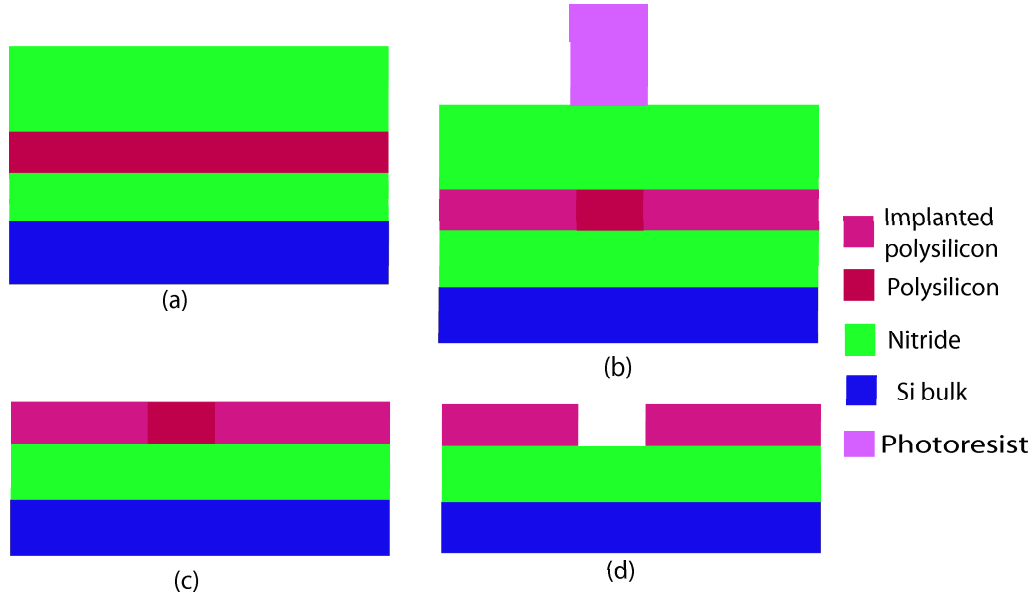


Figure 3.34: Example of buried mask revelation. (a) creation of a stack with a buried polysilicon layer, (b) implantation into the buried polysilicon layer, (c) removal of the top layer, (d) revelation of the doped area defined by implantation.

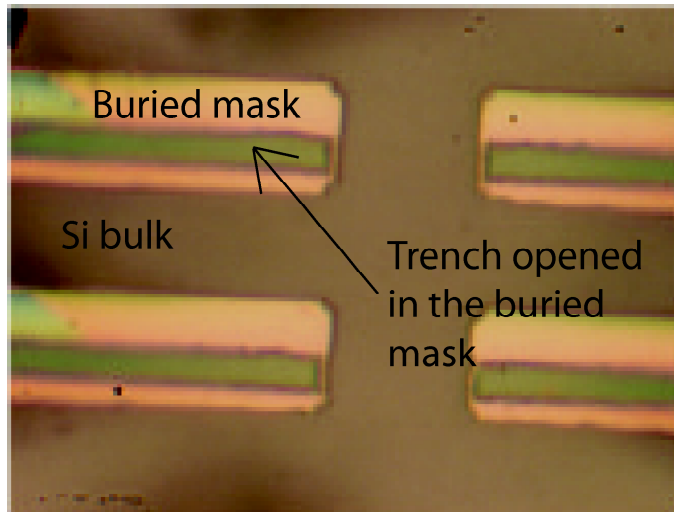


Figure 3.35: Optical microscopy of the negative buried mask after TMAH revelation.

trenches are $2\ \mu\text{m}$ wide and are well defined. Fig. 3.36 presents a SEM cross section of the revealed structure.

The roughness of the vertical walls is $70\ \text{nm}$. The narrowest section of the negative buried mask is $1.70\ \mu\text{m}$ and the widest section is $1.85\ \mu\text{m}$. The photoresist mask used for the ion implantation was $2\ \mu\text{m}$ wide. It is thus possible to define by ion implantation and revelation in TMAH a negative buried mask. The size of the buried mask is $300\ \text{nm}$ smaller than the implantation mask.

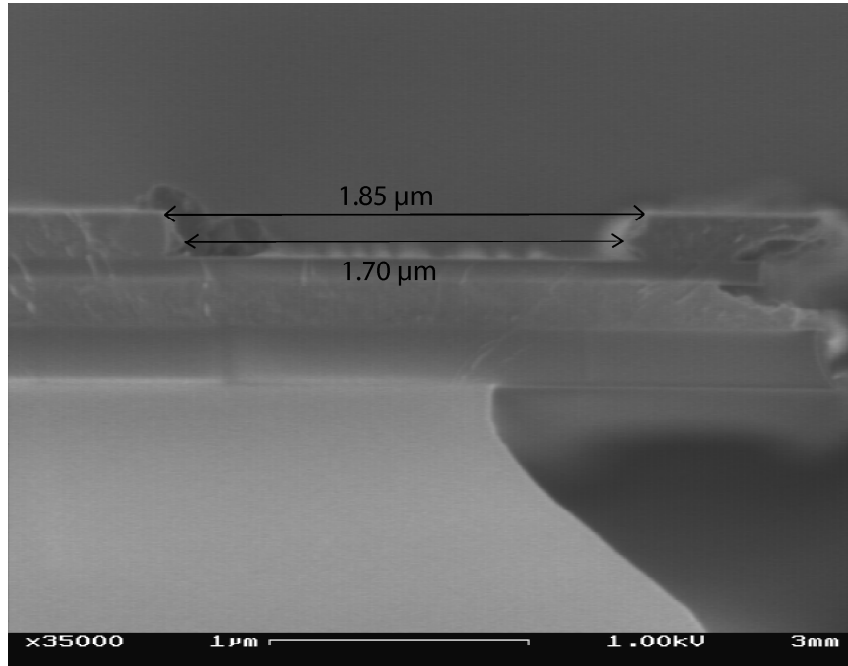


Figure 3.36: SEM cross section of a revealed negative buried mask in polysilicon.

An ATHENA Monte Carlo simulation of the ion implantation was performed to estimate the lateral dispersion of the doping species under the implantation mask. Sec. 2.4.2.6 shows that the etch rate of boron doped polysilicon starts to decrease for boron concentrations larger than $4 \times 10^{19} \text{ atm/cm}^3$. We therefore plotted in dark color the concentration larger than $5 \times 10^{19} \text{ atm/cm}^3$ and in light color the concentration lower than $4 \times 10^{19} \text{ atm/cm}^3$. The 2D simulation is shown in Fig 3.37:

It can be seen from the 2D simulation that the roughness observed on the vertical wall of the structure (Fig. 3.36) is not an artifact but arises from the dopant profile which also presents a small bump. Close to the surface, the boron penetration is limited to 50 nm, whether its maximal penetration is 120 nm deeper in the polysilicon layer. When comparing with Fig. 3.36 where the maximal width of the mask (which is close to the surface) was 150 nm smaller than the implantation mask and the minimum width was 300 nm smaller than the implantation mask, it means that the buried mask propagated from 75 nm under the implantation mask close to the surface and from 150 nm below the surface. It is comparable with our simulations where we observe respectively, 50 nm and 120 nm. This 25 to 30 nm difference in the comparison between lateral dispersion of the boron atoms and the buried mask size, can be attributed to the diffusion during the RTA which has not been simulated

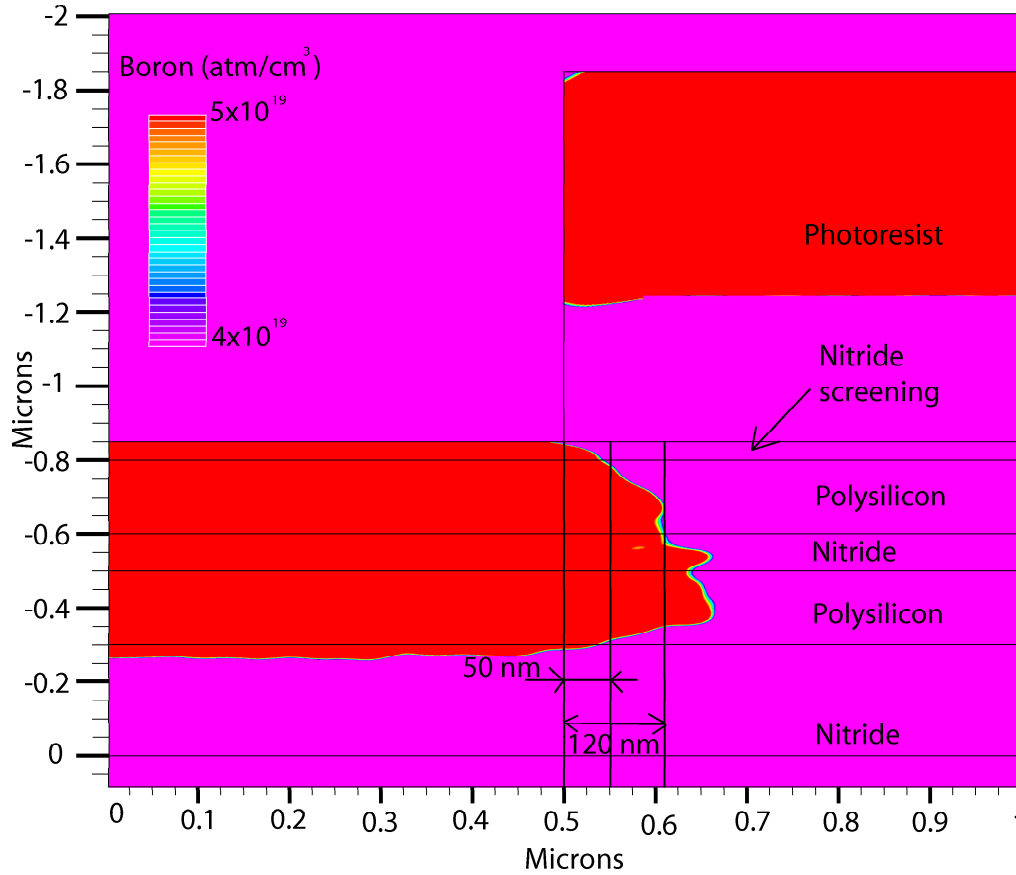


Figure 3.37: Monte Carlo simulation of the boron implantation done in three steps: $8 \times 10^{15} \text{ atm/cm}^3$ at 140 keV, $5 \times 10^{15} \text{ atm/cm}^3$ at 45 keV and $2 \times 10^{15} \text{ atm/cm}^3$ at 15 keV.

due to the lack of accurate models for RTA simulation. A other possible origin for this small difference is that the boron concentration have always been simulated and never measured by SIMS or SCM. We have therefore an uncertainty on the boron concentration for the etching selectivity curve, which combine with the uncertainty of the 2D simulation can give this small difference between the simulation and the picture.

3.3.3.3 Conclusion

We demonstrated that it is possible to create a negative buried mask into polysilicon using TMAH selective etching of undoped polysilicon. The creation of a buried cavity is unfortunately not achievable. As for the positive buried mask revealed in HNA, the negative buried mask revealed in TMAH has a narrower size than the implantation due to boron scattering under the implantation during implantation.

This difference in size and the roughness of the revealed buried mask wall can be partly attributed to the lateral scattering of the boron during ion implantation and also to the non vertical profile of the implanted boron concentration. Once taking this parameters into account thanks to simulation with ATHENA (Fig. 3.37), a difference of 25 to 30 nm between the calculated cavity and the measured revealed cavity remains. This difference can be attributed to the fact that the diffusion during RTA was not simulated due to the lack of effective model and also to the fact that the etching rate in function of the boron concentration presented in Fig. 2.31 does not vanish very abruptly.

3.3.4 Proposal to improve the definition of the polysilicon buried masks

The revelation of positive or negative buried mask gives good results in terms of etching selectivity but the size of the revealed buried structure does not fit with the size of the implantation mask. We propose in this section a method to overcome the lateral dispersion of the implanted ions by the use of spacer during ion implantation.

A trench in polysilicon revealed by buried mask implantation and selective etching is wider than the implantation mask in the case of a positive mask and narrower in the case of a negative mask. This effect is explained by the dispersion of the implanted ions under the implantation mask during the buried mask implantation. To counter balance the effect of the lateral scattering of the ions under the implantation mask during implantation, one could adjust the size of the implantation mask as a function of the buried mask depth, to take into account the effect of the lateral dispersion. The size of the mask would be extracted from 2D simulation of ion implantation. The drawback of this method is that the buried mask film thickness would depend on its depth, as the longitudinal straggling varies with the implantation depth and energy. Fig. 3.38 plots the projected range R_p , the longitudinal S_L and lateral S_l straggling versus the implantation energy for boron implantation into polysilicon. The projected range R_p characterizes the depth at which the boron concentration is maximal. The longitudinal straggling S_L and the lateral straggle S_l are, respectively the square root of the variance of the ion distribution at the depth

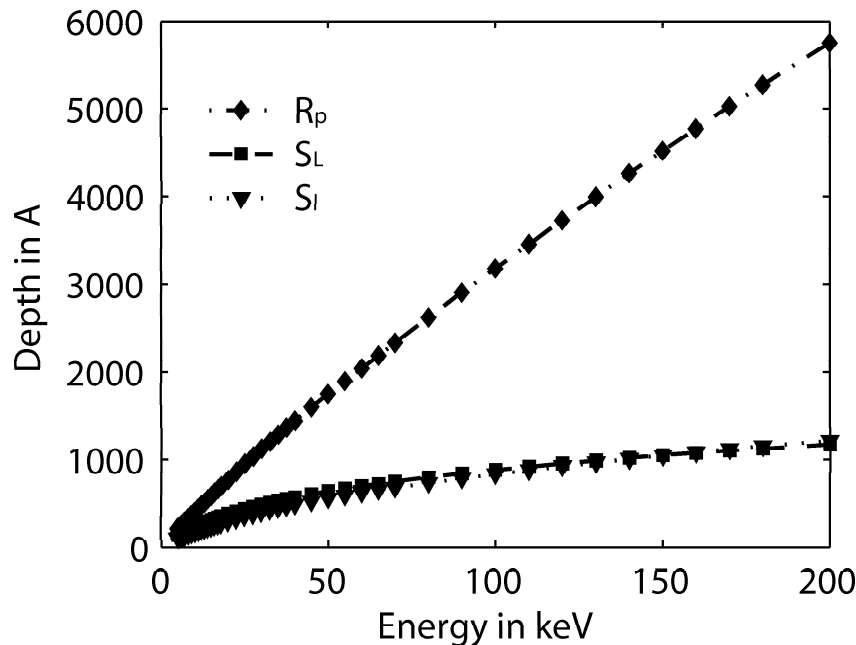


Figure 3.38: SRIM simulation of the projected range R_p , the longitudinal S_L and lateral S_l straggling versus the implantation energy for boron implantation into polysilicon.

of maximal concentration in respectively, the implantation direction and the perpendicular direction to the implantation direction. In other words, the projected range characterizes the depth of the buried mask, the longitudinal straggling the thickness of the buried mask and the lateral straggling the length of penetration of the buried mask under the implantation mask. It is of interest to note that the projected range increases at higher rate than the lateral and longitudinal straggling which are almost identical for implantation energies above 50 keV. Tuning the implantation mask size in order to get the desired buried mask size is not the ideal method as the buried mask would have a fix thickness depending on the implantation energy.

Another possibility would be to implant heavier species for which the lateral straggling is lower than for lighter species at equivalent R_p . Table 3.2 compares for the common doping species the longitudinal and lateral straggling for a projected range of 200 nm. Although increasing the ion mass could slightly reduce the lateral straggling, the energy has to be considerably increased to reach the same buried mask depth. Moreover, at high energy the amount of damages induced is very high and could be damageable to the structure, and special care should be taken during implantation to preserve the photoresist mask. At last, increasing the ion mass

Specie	Implantation energy in keV	Longitudinal straggling in Å	Lateral straggling in Å
B	60	701	622
P	155	640	501
As	325	525	409

Table 3.2: SRIM simulation of the longitudinal and lateral straggling and implantation energy for various species implanted in polysilicon at a projected range of 2000 Å.

does not solve the problem of the buried mask thickness linked to the implantation energy.

In order to get rid of the correlation between buried mask thickness and buried mask depth, the implantation can be done at different energies, as it has been done for the sample of Fig. 3.23, but with a change in the implantation mask size for each implantation energy. Implanting at different energies allows the creation of a thick buried mask, and changing the mask size during implantation allows to control the lateral dispersion of the doping species under the mask. As making a new photo lithography between each ion implantation would rise up the problem of photo lithography alignment, which is critical when the mask size has to be diminished off from 50 nm between two subsequent implantations, it has been thought to use a hard mask in nitride for example which would have the same size than the desired buried mask. The implantation mask size would then be varied by adding spacers to the buried mask. The spacers could be done by conformal LPCVD of amorphous silicon at 525 °C, which is a rather low temperature and would not contribute to dopants diffusion and followed by an anisotropic RIE of the deposited amorphous silicon. The advantage of this method is that the spacers allows modification of the implantation mask width and could be removed after implantation by HNA etching. A compromise has to be found between the quality of the buried mask definition and the number of cycles: spacer definition / implantation / spacer removal.

The sample of Fig. 3.23 has been used as model for new simulations in which the number of implantation steps has been increased and for which spacers were added during each implantation. Table 3.3 shows the implantations steps with associated dose, energy and spacer thickness that were used in the 2D simulation.

Implantation energy in keV	Dose in atm/cm ³	Spacer thickness in nm
200	5x10 ¹⁵	200
140	3.5x10 ¹⁵	190
61	3.4x10 ¹⁵	80
35	1.5x10 ¹⁵	80
22	1.2x10 ¹⁵	60

Table 3.3: Implantation doses, energies and associated spacer thicknesses.

This set of parameters was adjusted to create self aligned buried mask into the two polysilicon layers. Fig. 3.39 plots the boron concentration at each steps of the implantation steps.

Between each implantations the spacers are removed and replaced by new ones of other thickness. The high energy implantation is done at first, because if one would do the low energy implantation at first, the species would then be drag deeply into the structure during the high energy implantation. This implantation in five steps gives very good results in terms of buried mask alignment with the hard mask on the top surface, the spacers compensating the lateral scattering of the ions during implantation. Fig. 3.40 compares the obtained result with a sample on which the same implantations would have been performed without any spacer.

The lateral scattering of the boron in the first silicon layer is roughly 100 nm and reaches 300 nm in the bottom polysilicon layer. One can observe the lateral scattering due to each implantation. The technique using spacers during implantation is thus a very good method to create a buried mask of any thickness, aligned on the implantation mask. One point which might be critical for the spacer deposition is that the spacer has to be deposited with a conformal deposition. It is the case for the LPCVD, but they are usually performed at high temperature. Therefore the use of amorphous silicon is recommended as it is deposited at 525 °C, a temperature at which the diffusion is negligible. The diffusion models used by the software ATHENA are not accurate enough to simulate the diffusion of the boron if one would simulate the diffusion during the deposition of spacers at higher temperature.

3.3.4.1 Conclusion

We have shown that revelation of positive and negative buried mask in polysilicon was made possible thanks to ion implantation and revelation in HNA and TMAH.

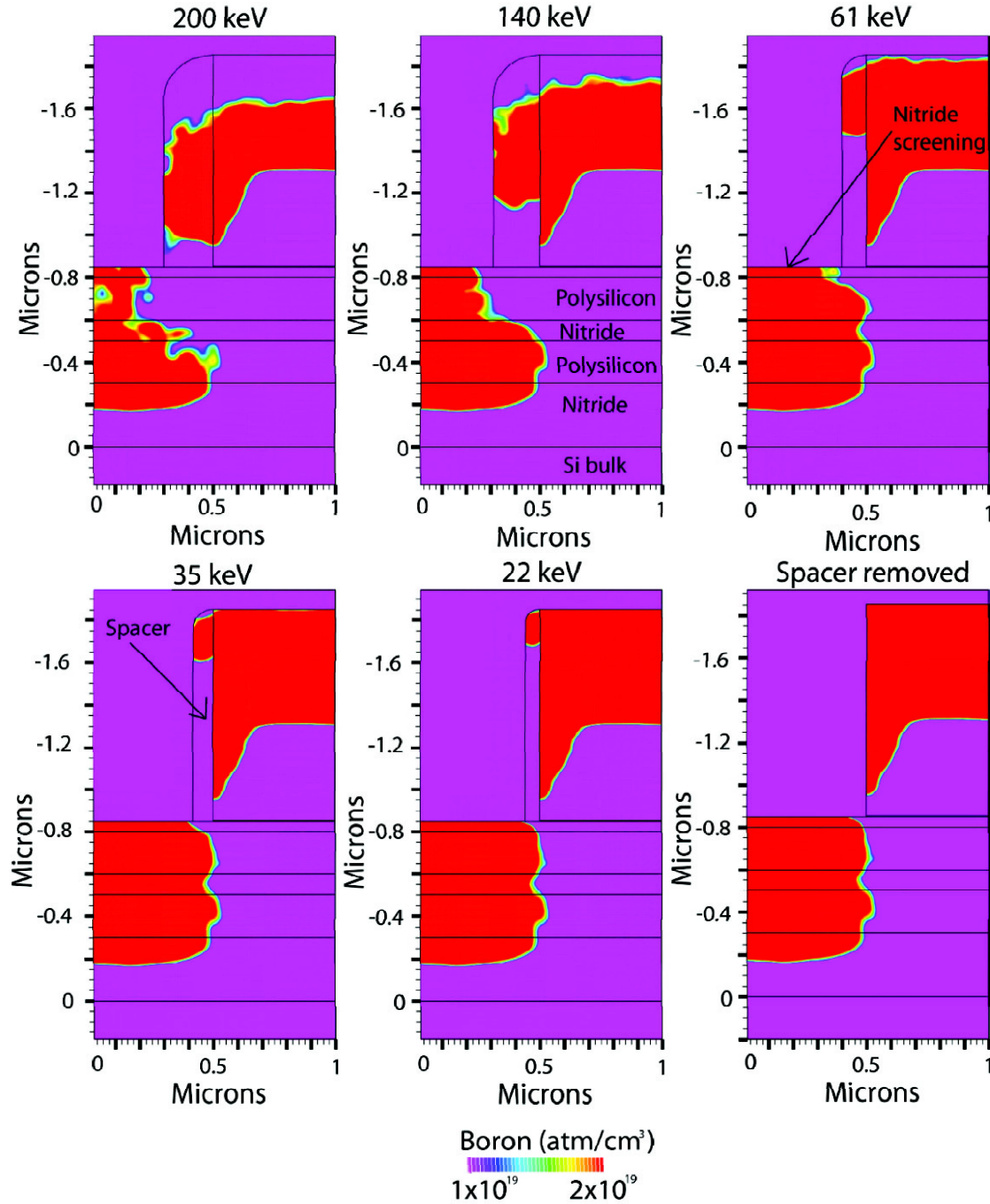


Figure 3.39: ATHENA 2D Monte Carlo simulation of the boron implantation for each steps of the ion implantation.

The edge of the buried mask was defined with an accuracy of respectively, 40 nm and 70 nm for the positive and negative buried mask. This poor accuracy is partly due to the roughness of the revealed vertical wall. This vertical wall roughness is due to the concentration of implanted species which presents variations at the edge of the buried mask. Sec. 3.3.4 showed that performing the ion implantation

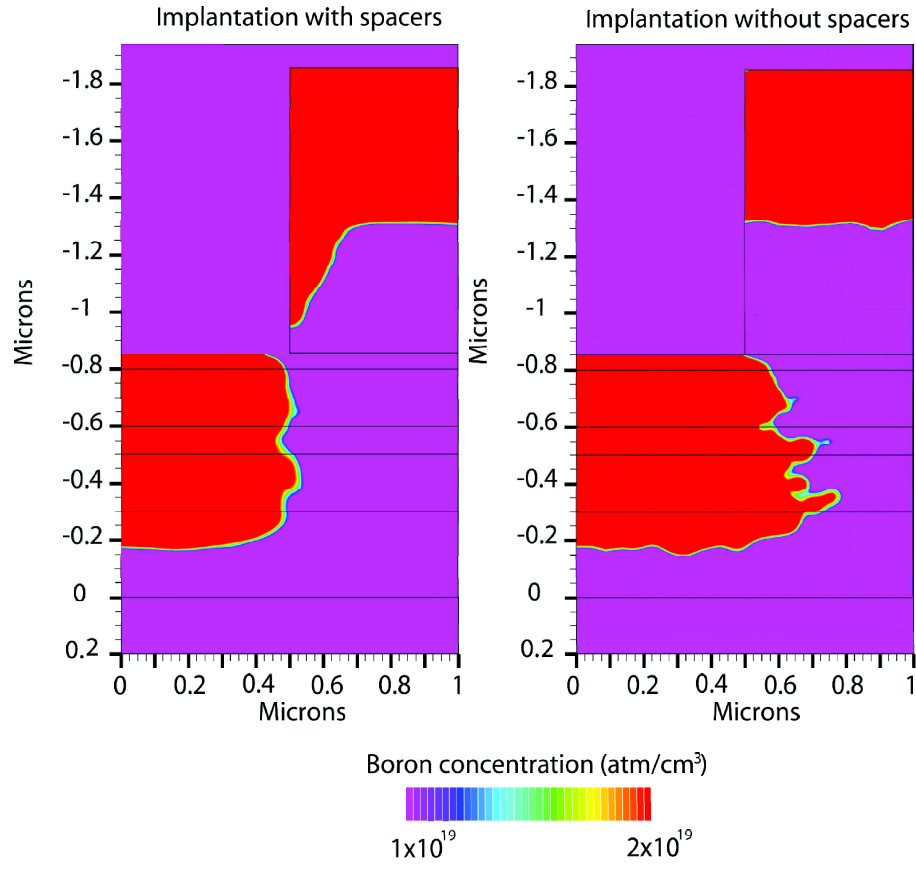


Figure 3.40: ATHENA 2D Monte Carlo simulation of the boron implantation for a sample with spacers during implantation and a sample without spacers.

at various energies and correcting the lateral scattering of the implanted species via the addition of spacers to the mask during ion implantation could give a buried mask with a very sharp profile, aligned with the edge of the implantation mask. This improvement to the buried mask definition thanks to a sharp definition of the implanted species concentration will avoid the surface roughness of the wall of the revealed buried mask. This reduction of the vertical wall roughness will allow the fabrication of buried mask with a better definition. One can expect to define the buried mask with an accuracy depending on the etching selectivity in function of the doping concentration and depending on the doping species gradient concentration at the mask edge. The Sec. 3.3.2 and Sec. 3.3.3 showed that the contribution of the concentration gradient and the etching selectivity to the accuracy of the definition were respectively 15 and 25 nm for the positive and negative buried mask. In the case of the positive buried mask revealed in HNA, the accuracy might be increased further as the doping threshold is very abrupt between etched and unetched polysilicon.

These fairly good accuracies make the process *Negative buried mask in recrystallized Si- α* , with an expected accuracy of 25 nm, similar in precision to the PAGODA process for which a gate length of 125 nm had been achieved. The *Positive buried mask in recrystallized Si- α* process, with a expected accuracy of 15 nm, could achieve smaller dimension than the PAGODA process and can compete with the process proposed by Widiez where although a gate length of 70 nm has been achieved, the gate size is controlled by the etching time. The etch stop property of the HNA and TMAH revelation makes the process more robust toward process fluctuations than controlling a dimension only with the etching time.

3.4 Conclusion

The chapter 2 showed that it was possible to modify the etch rate of silicon dioxide and polysilicon thanks to ions implantation and described the physics responsible for etch rate modification. This chapter showed that it was possible to create buried mask into silicon dioxide and polysilicon using etching selectivity between implanted and unimplanted material.

Etching of implanted oxide into a cavity presents a lower etching selectivity

between implanted and unimplanted oxide as etching on the wafer surface. This decrease in etching selectivity is due to the water produced by the reaction which condensate into the cavity and acts as catalyst for further etching of the unimplanted oxide. This problem is partly solved by performing the revelation under cycles of etching / rinsing. Thanks to this technique the revelation of narrow cavities of $9\text{ }\mu\text{m}$ long for a width down to $2\text{ }\mu\text{m}$ can be revealed. Large cavities are also possible to reveal but the ratio length over width is smaller than for narrower cavities. Cavities of $20\text{ }\mu\text{m} \times 18\text{ }\mu\text{m}$ should be possible to reveal. Revelation of self-aligned cavity should be investigated but is theoretically possible. Our initial goal was the creation of very narrow cavities that could be used for self-aligned planar double gate fabrication. As these devices are of interest for the 32 nm technology node, we must unfortunately conclude that our revelation technique is not adapted for the process that we proposed in Sec. 1.2.1.

However, although the revelation of cavities with a narrow etch front and a long length to reveal shows strong limitation, the revelation of cavities with a very large etch front but a very short length to reveal might be possible. Moreover the revelation of buried mask in implanted oxide is possible.

Although cavities in polysilicon are not possible to reveal neither with HNA or TMAH, positive and negative buried mask in polysilicon are possible to reveal with an accuracy of respectively 30 and 70 nm. This values could be decreased to respectively 15 and 25 nm when implanting the buried mask at various energies and compensating the lateral scattering of the implanted species by the addition of a spacer during ion implantation. The creation of positive and negative buried mask in polysilicon is thus a good technique for the fabrication of self-aligned planar double gate transistors.

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CHAPTER 4

CONCLUSION AND PERSPECTIVES

4.1 Conclusion

The constant increase in microprocessor performances has been made possible mostly thanks to the transistor dimension downscaling. To push further this downscaling, it is necessary to modify the type of materials used for MOSFETs fabrication (high- k dielectrics, metallic gate, strained silicon, germanium...) but also to change the transistor architecture. The multigates transistors seem to be the most promising solution to reach the semiconductor roadmap requirements. In this context, the motivation of this work was to explore new process solutions to build planar Double Gate MOS transistors based on new process steps.

After a brief introduction, we explain in the first Chapter the need for Double Gate MOS and review all the type of Double Gate transistors that have been fabricated, pointing out their advantages and weaknesses. The disadvantage of the FinFET, trigate, Π - and Ω -gate transistors is that the length of the transistor is limited by the thickness of silicon film. Multi-finger architectures must therefore be used to build transistors with any W/L ratio. However, the multi-finger structures are source of parasitic capacitances, which limits the high frequency performances of the transistor. The use of multi-finger architectures can be avoided with the planar double gate architecture. The most critical issue in planar Double Gate MOS fabrication is the alignment of the front and back gate. Self-aligned process have been proposed but the disadvantage of this techniques is that either the active silicon film or the source and drain areas have to be regrown by epitaxy or recrystallization. We proposed thus three different processes for which no silicon regrow is required and where the Front and Back Gates are self-aligned by definition of buried mask by ion implantation and thin film transfer. The demonstration of the feasibility of some

of the process steps common for the three proposed process such as wafer bonding, PECVD oxide quality and selective RIE is demonstrated in the Appendix.

The innovative concept of our process proposal being the creation of buried mask by ion implantation the following chapters of the thesis explain how to modify the etch rate of common materials by ion implantation and how buried mask can be defined in polysilicon and oxide.

The second Chapter reviews the physics of ion implantation and presents the simulation software used to simulate the ion implantation and its impact on the implanted material, such as damage creation and introduction of foreign atoms in the lattice if the target is recrystallized after implantation. These foreign atoms can dope the polysilicon by exchanging excess or lack of electron with the neighbor atoms. If the foreign atoms are smaller than the lattice atoms, stress is induced to the lattice.

The damages created in the oxide by ion implantation can increase its etch rate in VHF by a factor of 200. The reaction between SiO_2 and HF is an autocatalytic reaction with water as catalyst and reaction byproducts. Etching in VHF is highly selective as the etching cannot start until water has condensate on the surface. An etching temperature of 40 °C avoids the water to condensate on the surface but is too low to evaporate the large amount of water produced by the etching reaction on the implanted oxide which is more reactive with HF. This produced water sustains the reaction by acting as catalyst.

The stress induced by substitutional boron into polysilicon reduces by a factor close to 100 the etch rate of highly boron doped polysilicon in TMAH. Extensive bibliography had been done to understand the etch stop mechanism.

The n- or p-type highly doped polysilicon is etched at a rate of 10 $\mu\text{m}/\text{min}$ in HNA. The free carriers due to the doping put the surface silicon in excited state, which makes it more reactive to the nitric acid. The reaction of silicon and nitric acid is an autocatalytic reaction which oxidizes the silicon. The oxide is then dissolved by HF. This reaction can be stopped by removing the reactions byproducts, which are catalysts, from the surface, by performing the etching in ultrasonic bath. This etch stop method work only for undoped silicon, which ensure a very high

selectivity between doped and undoped polysilicon.

The third Chapter demonstrates that etch rate modification by ion implantation of silicon dioxide or polysilicon can be used to reveal buried pattern in polysilicon or cavities in oxide.

Cavities have thus been revealed in the BOX of an SOI wafer thanks to implantation of oxide and VHF revelation. Due to the auto-catalytic mechanism of oxide etching by HF, the cavity revelation is done under the form of cycles VHF etching / N_2 rinsing to maintain a high selectivity, otherwise the produced water condensates in the cavities and the selectivity is lost. Despite this original revelation method, very narrow cavities have not been revealed as the selectivity decreases as far as the etching is done deeply in the cavity. The narrowest revealed cavities were $3\text{ }\mu\text{m}$ wide for $9\text{ }\mu\text{m}$ long.

The revelation of etch stop zone by TMAH had demonstrated the possibility to reveal buried pattern with a definition of 70 nm. The revelation of buried cavities was unfortunately not possible. The TMAH etching producing gaseous H_2 , hydrogen bubbles form at the entrance of the cavity and block any circulation of OH^- ions, which stops the etching.

The revelation of the sacrificial zone with HNA had demonstrated the possibility to reveal the buried pattern with a definition of 40 nm. The revelation of buried cavities was unfortunately not possible, the selectivity between doped and undoped silicon being lost. Due to the narrow dimensions of the cavity, the etching byproducts cannot be removed from the etched cavity, even with the use of ultrasounds.

Better definition of the buried mask is made possible thanks to a multi step implantation performed at various energies combined with a lateral scattering compensation by the addition of spacers to the implantation mask. This sharper definition of the buried mask will increase the accuracy of the revealed structures to the expected values of 15 nm for HNA revelation and 25 nm for TMAH revelation. This makes thus our process proposals for self-aligned planar DG MOS fabrication competitive with the actual techniques such as PAGODA.

The concept of buried mask is a new technique that we developed in view of self-

aligned double gate fabrication. Our work shows that positive and negative buried mask in polysilicon could be used for fabrication of submicronic planar double gate MOSFETs if more work would be invested in characterizing the integration of all the process steps. Positive buried mask in oxide can not achieve small enough dimension to meet the requirement of our process. Our process *positive buried mask in oxide* is therefore not scalable to submicronic dimensions.

However this buried mask concept could be applied to many other field, mostly in MEMS fabrication.

This following Section will introduce some foreseen application of buried mask in oxide and polysilicon

4.2 Perspectives

4.2.1 Buried mask in oxide

We have shown in Sec. 3.2.2 that the revelation of narrow cavities was limited in length although Sec. 2.4 showed that very high selectivities could be achieved when revealing a buried mask on a surface film. We therefore extend the technique to the revelation of wide cavities with a very short underetch length.

This section presents potential application of buried mask in oxide.

4.2.1.1 Wave modulator

In the context of development of on chip interconnects, the top silicon of SOI wafers could be used as wave guide. Moselund *et al.* showed in 2D and 3D simulations that wave modulation could be obtained by embedding the silicon optical wave guide into a polysilicon gate [1]. Varying the gate bias changes the refractive index due to free carriers injection [2]. In their wave modulator proposal, the Si bar has a cross section of $340 \times 340 \text{ nm}^2$ and a length up to $10 \text{ }\mu\text{m}$ (Fig. 4.1)

Their work is only theoretical and does not include a process flow. Our selective etching of implanted oxide could be used to define the gate all around wave modulator starting from a SOI wafer.

Fig. 4.2 shows a schematic of a possible process flow for the fabrication.

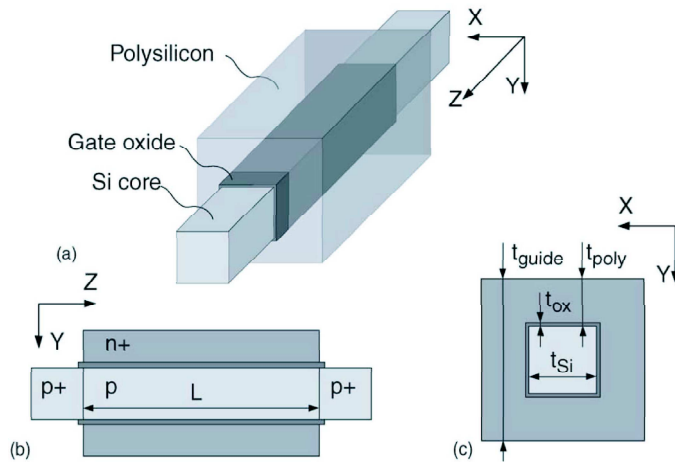


Figure 4.1: (a) schematic of the GAA wave modulator. (b) longitudinal cross section, (c) transversal cross section [1].

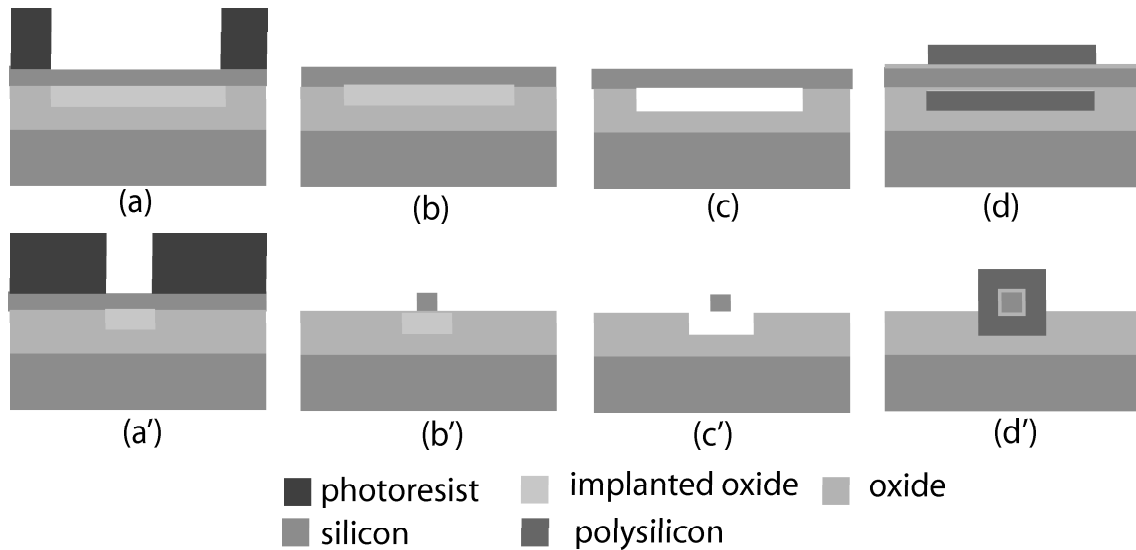


Figure 4.2: Schematic of the GAA wave modulator process flow. (x) presents a longitudinal cross section and (x') a transversal cross section. (a) buried mask definition in oxide, (b) wave guide definition, (c) buried mask revelation, (d) gate oxidation and polysilicon gate deposition [1].

The silicon film is used to fabricate the wave guide and the gate all around is embedded in the BOX. To get a sharp definition of the cavity in which the gate will be embedded, selective etching of implanted oxide is used. The buried mask is thus implanted through the whole silicon film. After the wave guide definition by RIE, the implanted oxide is etched in VHF, the gate oxide is grown and the polysilicon gate is deposited.

VHF revelation would be here possible thanks to the very short underetch length.

4.2.1.2 Quadruple gate MOSFET

π -gate transistors could easily be transformed into quadruple gate using selective etching of implanted oxide. The revelation of the buried structure would be identical to the one of the wave modulator, the only difference would lie on the smallest size of the silicon beam.

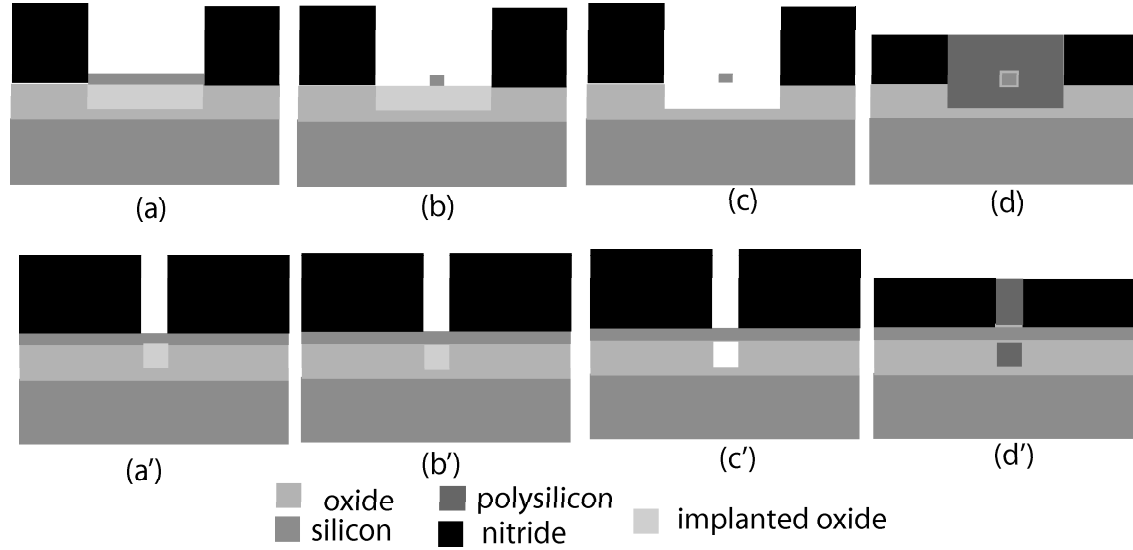


Figure 4.3: Schematic of the quadruple gate process flow. (x') presents a longitudinal cross section and (x) a transversal cross section. a) buried mask definition in oxide, (b) wave guide definition, (c) buried mask revelation, (d) gate oxidation and polysilicon gate deposition, CMP

The buried mask is first defined by implantation of silicon, using a nitride mask. The silicon nanowire is then defined by RIE. After revelation, the gate oxide is grown and the polysilicon gate is deposited. A CMP planarizes the polysilicon gate after deposition.

This process offers the advantage of being simple and cost effective.

4.2.1.3 Underetch reduction in MEMS release

When releasing a beam in MEMS micromachining, there is a systematic underetch corresponding to half of the largest width of the released beams (Fig. 4.4).

Implanting the zone to be released would avoid the underetch. This underetch reduction when performing beam release allows the fabrication of well anchored beams.

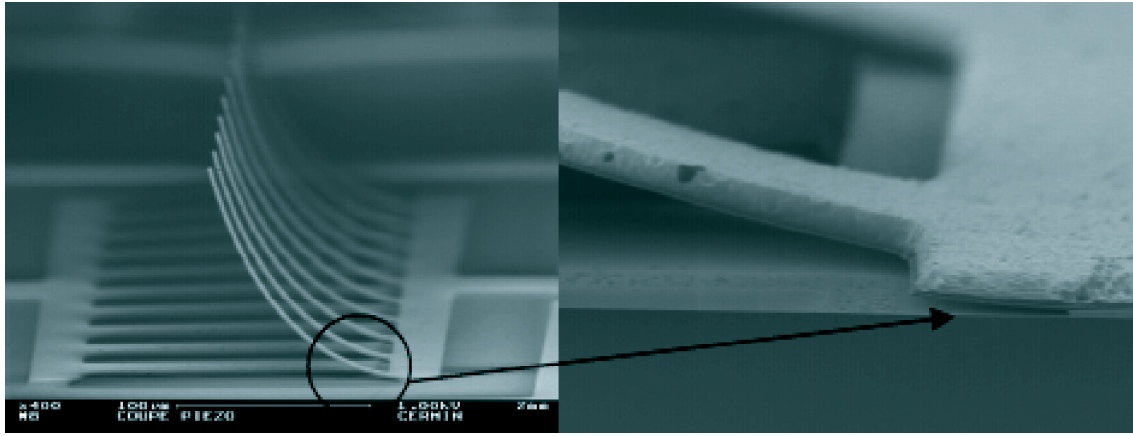


Figure 4.4: Underetch in MEMS release

4.2.2 *Buried mask in polysilicon*

Polysilicon offers the advantage that either positive or negative buried mask can be built in, depending on the type of doping species implanted and on the type of etching solution used for the revelation. As the buried mask formed in polysilicon cannot be revealed under a masking film, no cavity can be revealed. The revelation can be made only from a free surface. This buried mask technique gives the same result as a photolithographic step followed by a RIE. The depth of the revealed trench being fixed by the doping profile. However, compared to a photolithographic step and a RIE, the buried mask technique presents the advantage that the wafer can suffer other processing steps between the implantation and the revelation and that the implantation mask do not need to be present when performing the revelation. In other words, the buried mask technique allows the definition of a structure that can be stored in a layer until revelation. One can thus transfer the film in which the buried mask has been defined to a handle wafer before revelation. Moreover, if one conserve the implantation mask (which can be an hard mask) before transferring the film in which the buried mask has been imprinted one can obtain a buried mask self-aligned with the implantation mask. This technique allows thus the fabrication of the self-aligned planar double gate MOS according to the process proposals presented in Sec. 1.2.2 and 1.2.3.

The buried mask does not necessarily need to be revealed from the surface through which the implantation was performed. One can also perform the revelation by etching the back side of the film in which the buried has been implanted.

The etching of the buried mask from the back side can be made possible if one remove the bulk below the buried mask film to create a membrane. The buried mask can then be revealed on the back side of a membrane.

The technique allows thus the definition of structures on the back side of a membrane which would have not been possible with a photolithographic step followed by a RIE. The next section will study potential application of this technique.

4.2.2.1 Advanced sensors

Laconte presented in its PhD thesis new flow sensors fabricated on silicon membrane [3]. The flow sensor is composed of two thermocouples and of one micro heater. The temperature sensors are placed upstream and downstream of the micro heater. The measurement of the temperature difference between the upstream and downstream sensors is correlated to the gas flow. The Fig. 4.5 shows the structure of the flow sensor.

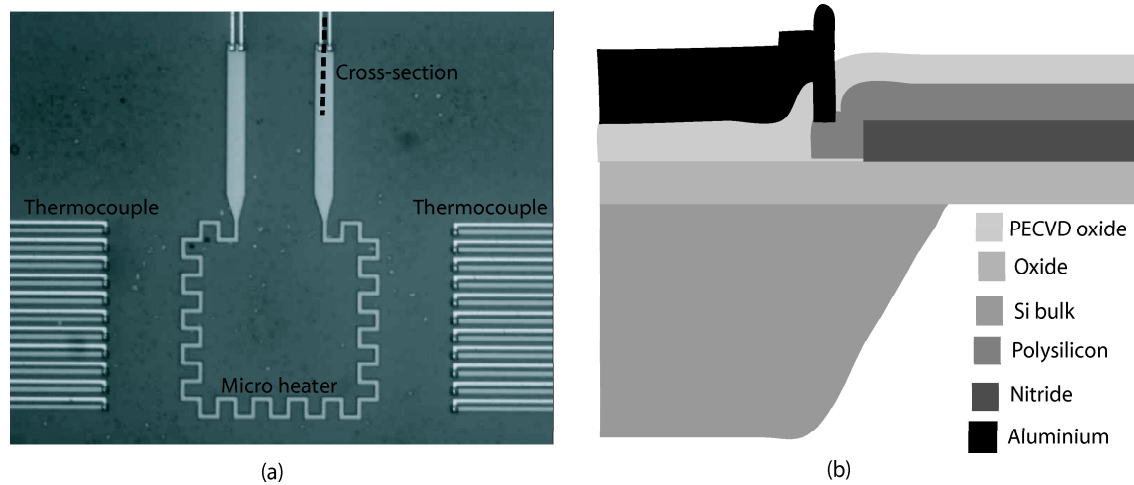


Figure 4.5: Close view of a flow sensor [3]. (a) SEM top view, (b) schematic cross section of the micro-heater.

The structure can be improved by transferring the heater on the back side of the membrane. A polysilicon layer could be inserted into the buried oxide of an SOI film by film report engineering, as shown in Sec. 1.2.2. The polysilicon serpentine forming the heater would be defined in this layer thanks to a negative buried mask revealed in TMAH. This would allow to use the free surface of the SOI film from the membrane for analog or digital purpose. Fig. 4.6 presents a schematic of the proposed new flow sensor.

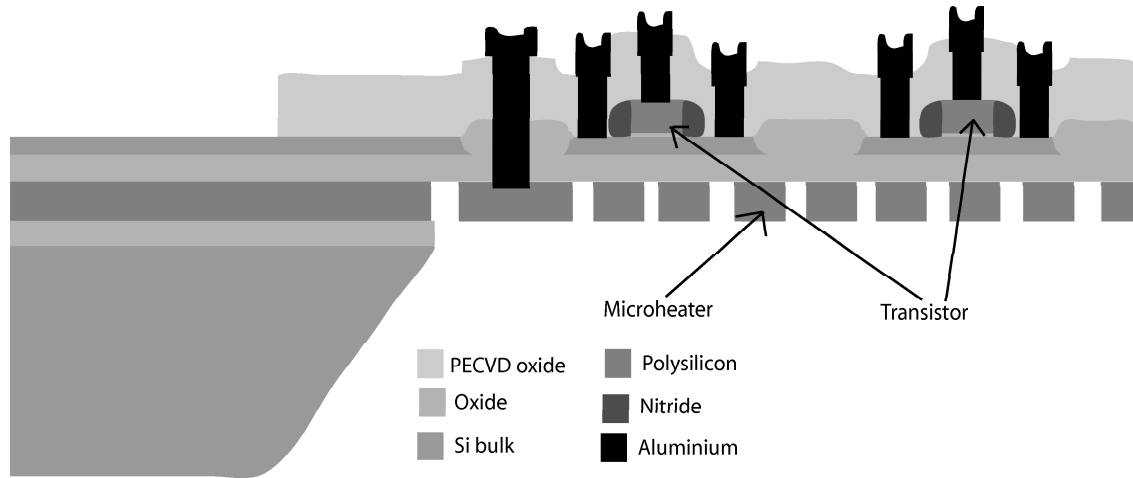


Figure 4.6: Schematic of a new flow sensor. The micro heater is below the membrane. Transistors are build on the SOI film of the membrane.

Placing the micro heater on the back side of the membrane frees space on the membrane surface that can be used to place some transistors.

Some gas sensors and calorimeters are also based on the same structure composed of a micro heater and a thermopile [4],[5]. A material which presents affinity with the detected chemical is coated on the membrane and serves as detector. The adsorbed chemical is characterized by the amount of heat necessary for its evaporation. The chemical adsorbed on the surface can also change the work function of the coated material and affects the V_t of a transistor lying under the coated material. Our method to design the heating element below the membrane is a way to reduce the device size.

4.2.2.2 Buried interconnect

The ability to create polysilicon lines on the back side of a membrane allows the fabrication of back side interconnects in polysilicon when building circuits on a membrane.

4.2.2.3 Embedded sensors

Bertholet *et al.* showed that it is possible to create a wafer with a buried aluminum layer [6]. One could thus fabricate the membrane presented in Fig. 4.7 thanks to wafer bonding engineering.

A buried mask could be defined in the underlying polysilicon film of the mem-

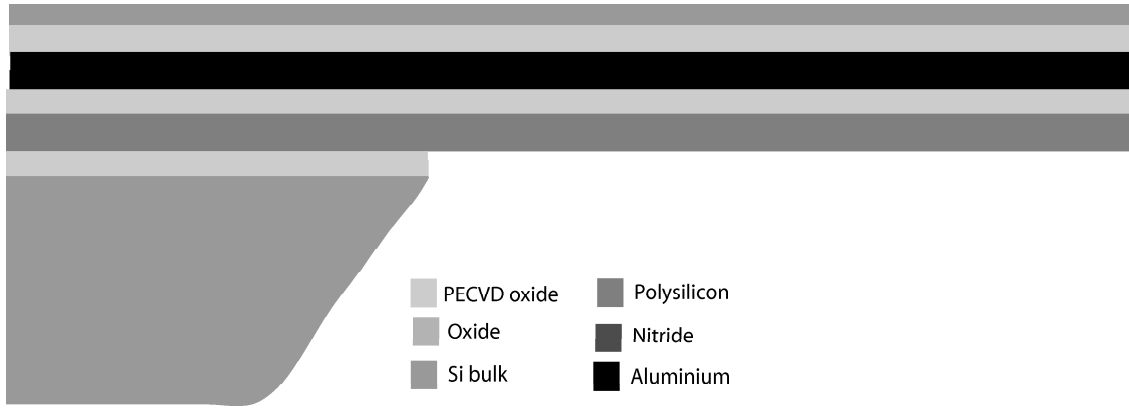


Figure 4.7: Membrane with an embedded aluminum layer.

brane by implantation through the whole stack defining thus a hard mask to etch by RIE the aluminum layer. DNA sensors based on interdigitated Al/ Al_2O_3 microelectrodes could thus be fabricated. Fig. 4.8 presents a schematic of the DNA sensor with the interdigitated electrodes on the back side of the membrane.

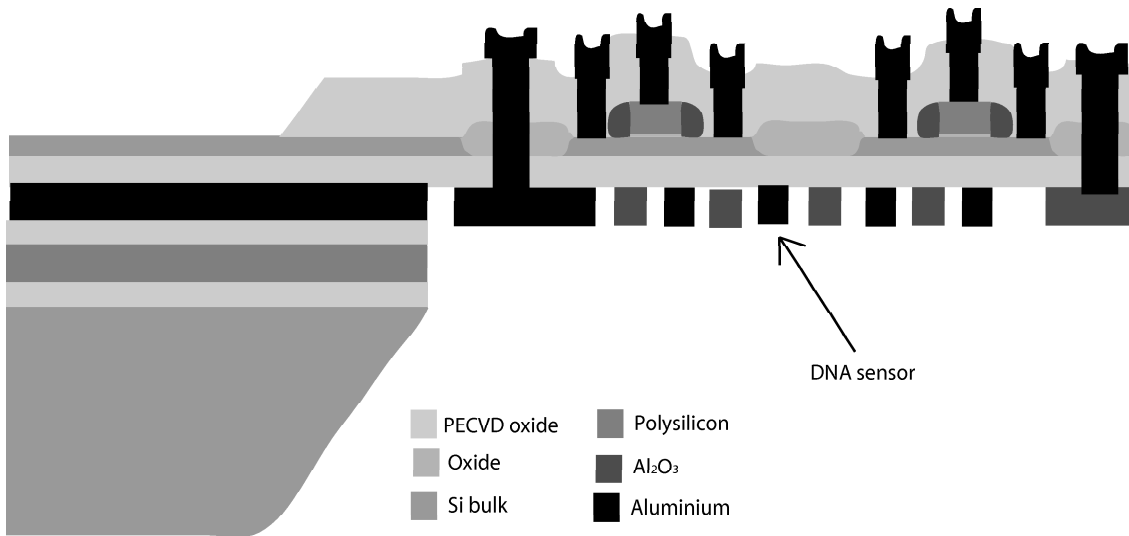


Figure 4.8: Schematic of a new DNA sensor. The interdigitated microelectrodes are below the membrane. Transistors are built on the SOI film of the membrane.

This would improve the design of such biosensors as developed by Moreno-Hagelsieb *et al.* [7],[8]. The sensor part could be in the cavity whether the analog circuit would lie on top of the membrane. This architecture would save silicon surface but also preserve the microelectronic part of the sensors from an aggressive environment.

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APPENDIX A

EXOTIC SOI WAFER

FABRICATION

A.1 Si- α or polysilicon

In both Sec. 1.2.2 and 1.2.3 the fabrication of the stating wafer requires the bonding of an oxidized handle wafer on a polysilicon layer. Preliminary tests showed that the bonding of one oxidized wafer with a wafer on which polysilicon was deposited was impossible. Indeed the too high surface roughness of the polysilicon is responsible of the unbondability [1]. Fig. A.1 shows a cross section of a polysilicon obtained by LPCVD at 625 °C.

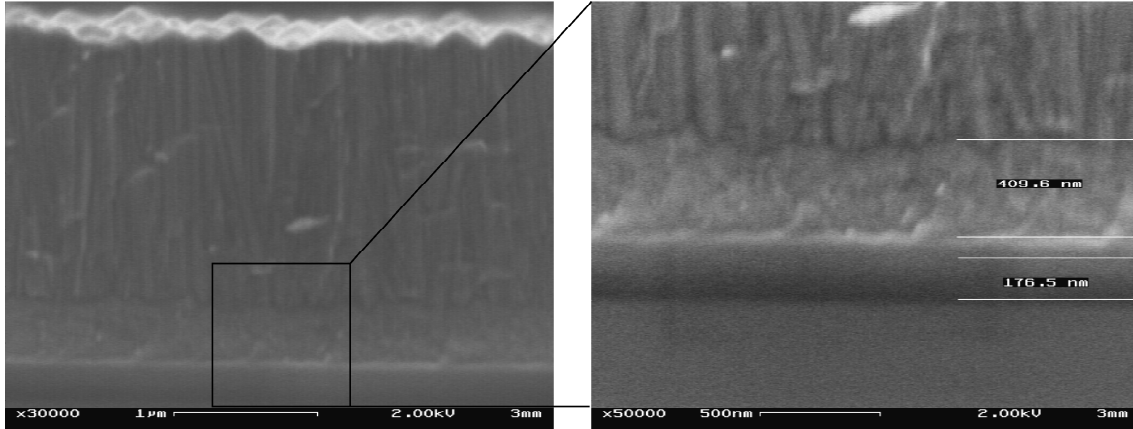


Figure A.1: Cross section of a LPCVD polysilicon film obtained at 625 °C.

The SEM cross section of a LPCVD polysilicon film is sufficient to show that the rms surface roughness is well above 5 Å, which is the maximal limit for wafer bonding [2]. This is confirmed by AFM measurements from Table A.1 [3].

Sample	RMS roughness (Å)	Hmax (Å)
Si- α	3.64	54
Recrystallized Si- α	3.7	31.4
Polysilicon	22.4	164

Table A.1: AFM measurement of the surface roughness

As the oxidation of the polysilicon increases the surface roughness, the polysilicon has been replaced by Si- α . As the polysilicon layer is used in the buried mask application for its crystalline properties (the etching selectivity of TMAH toward boron doped silicon is due to the stress induced in the lattice by the smaller boron atoms and the etching selectivity of HNA toward doped silicon is due to the free carriers, consequence of the presence of doping atoms at substitutional sites in the lattice), the Si- α must be recrystallized by RTA. The Fig. A.2 shows a cross section of a LPCVD Si- α obtained at 525 °C, before and after a 30 s RTA at 900 °C.

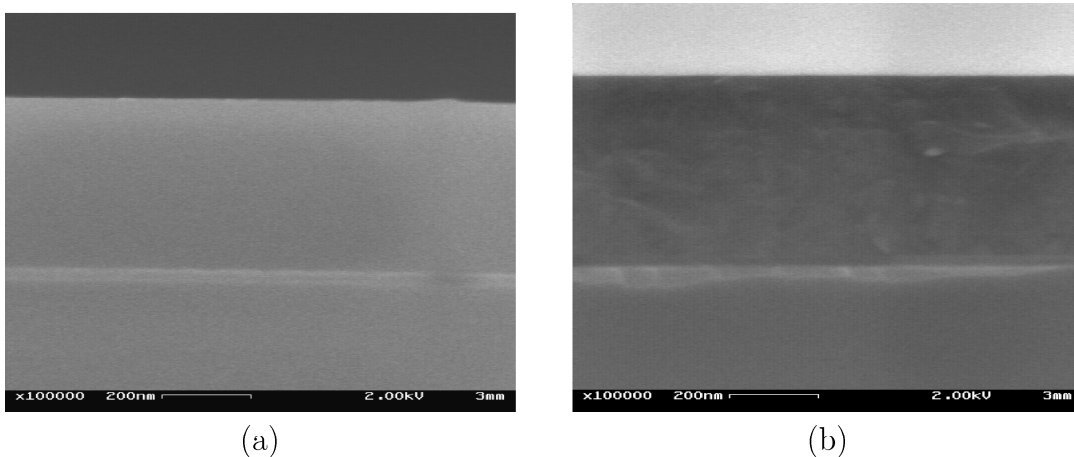


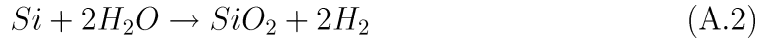
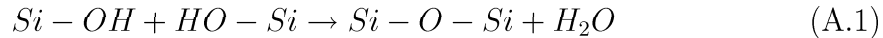
Figure A.2: SEM cross section of LPCVD Si- α obtained at 525 °C. (a) after deposition, (b) after 30 s RTA at 900 °C.

The surface of Si- α is smooth and without topography. The RTA creates grain in the recrystallized layer and reduces the rms surface roughness. Bonding has thus been made possible thanks to the use of recrystallized Si- α , as will be shown in the following Section.

A.2 *Bonding of recrystallized Si- α*

When two atomically smooth and clean surfaces are brought into intimate contact they adhere to each other via intermolecular forces such as van der Waals forces or hydrogen bonding. By temperature treatment or introducing some monolayers of appropriate molecules into the interlayer the bonding strength can be increased in such a way that it is comparable with the chemical bond and acts like a welding. Solids of almost any material combination may be joined through this room temperature technique. The adhesion of silicon to oxide is done through the presence

of -OH groups on the wafer surface. The chemical reaction occurring during wafer bonding can be decomposed in two steps according to Eq. A.1 and A.2 [4].



This effect is used for the fabrication of the starting wafers of the processes described in Sec. 1.2.2 and 1.2.3 where an oxidized bulk wafer has to be bonded to a wafer covered by a recrystallized Si- α layer.

Our first test was to bond an oxidized recrystallized Si- α wafer on an oxidized Si bulk wafer. This pair of wafers was impossible to bond. AFM measurement of the oxide grown from the recrystallized Si- α shows a rms surface roughness of 14 Å which avoids the wafer bonding.

The bonding of an oxidized Si bulk wafer was thus tested with a wafer on which Si- α was deposited and recrystallized. The characterization was limited to Infra-Red (IR) imaging.

The surface cleaning of the wafers before bonding has a drastic influence on the number of -OH groups presents on the surface and thus on the bonding quality [5],[6],[7]. We performed wafer bonding with different types of cleaning.

A.2.1 Influence of the cleaning.

Different methods of cleaning and activation were tested before wafer bonding:

- standard cleaning and rinser dryer,
- standard cleaning, rinser dryer and O₂ plasma activation,
- standard cleaning, rinser dryer, O₂ plasma activation and rinser dryer.

Fig. A.3 plots the IR images of the wafers after bonding in each of the described cleaning and activation conditions. This set of pictures is qualitatively representative of the results obtained on a batch of 6 bonded wafer pairs.

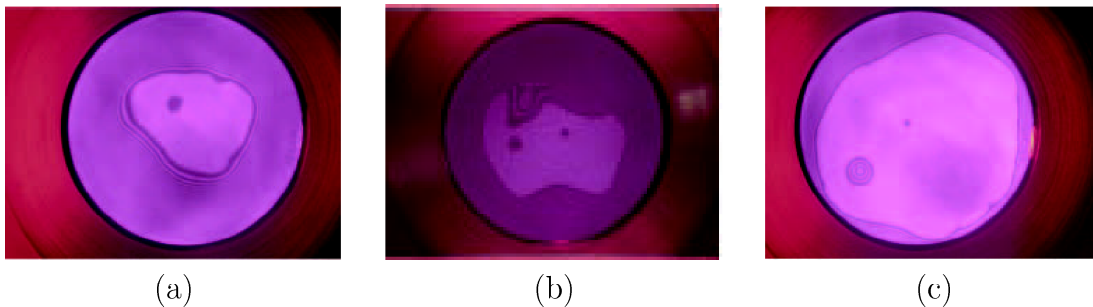


Figure A.3: IR imaging of the bonded wafers. (a) standard cleaning and rinser dryer, (b) standard cleaning, rinser dryer and O₂ plasma activation, (c) standard cleaning, rinser dryer, O₂ plasma activation and rinser dryer.

The bright areas are the bonded area and the interference fringes the unbonded area. The Newton rings are caused by interferences due to the air gap between the two wafers. The bonded area is maximal when the wafer are prepared in the following way: standard cleaning, rinser dryer, O₂ plasma activation and rinser dryer. This preparation method is the one chosen for the following experiments.

A.2.2 *Si- α recrystallization pre- or post-bonding*

The recrystallization was tested before and after wafer bonding. Fig. A.4 compares bonded wafers from which the Si- α was recrystallized before and after bonding.

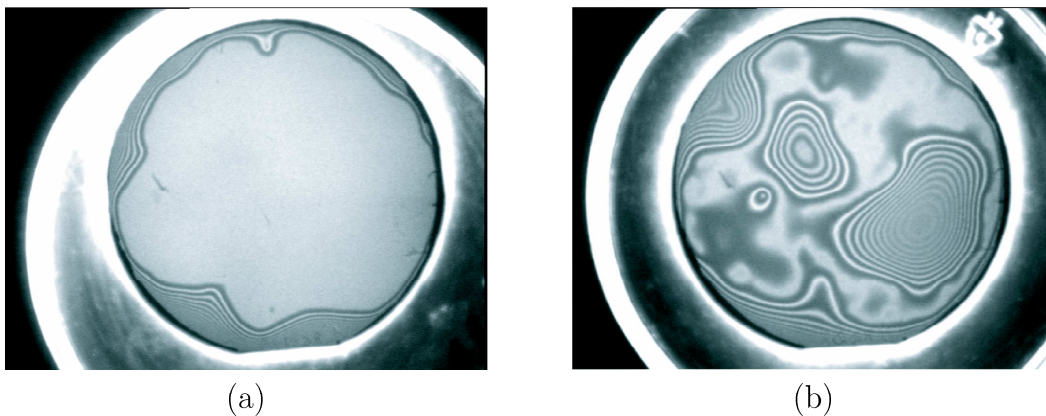


Figure A.4: IR imaging of bonded wafers. Si- α recrystallization (a) before bonding, (b) after bonding.

The wafer bonding is of fairly good quality when the recrystallization is done before the wafer bonding. The bonded interface is destroyed by the surface reconstruction that occurs during the Si- α recrystallization. In order to validate this hypothesis and to check the impact of RTA on the bonded surface, a RTA was

performed on a bonded pair of wafer from which the wafer covered by Si- α was recrystallized before wafer bonding. Fig. A.5 shows a IR imaging of this bonded pair.

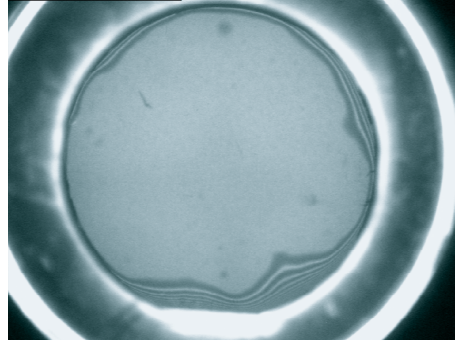


Figure A.5: IR imaging of bonded wafers after RTA. The Si- α has been recrystallized before bonding.

The bonded surface is increased after RTA. It confirms that recrystallization of the Si- α destroys the bonded interface and that the RTA has a positive impact on the bonding. This impact can be explained by the second step of the bonding reaction from Eq. A.2 where it can be seen that the H_2 formed during the bonding must out-diffuse.

Based on the experience that a post bonding thermal treatment could increase the bonding surface, other post bonding treatment were performed.

A.2.3 Post bonding treatment

We tried after bonding the following method to increase the bonded surfaces:

- ultra high vacuum,
- low temperature annealing,
- high temperature annealing,
- high pressure.

Ultra high vacuum

Fig. A.6 shows the bonded wafers after bonding and after 4 days at a pressure of 1.10^{-7} mTorr.

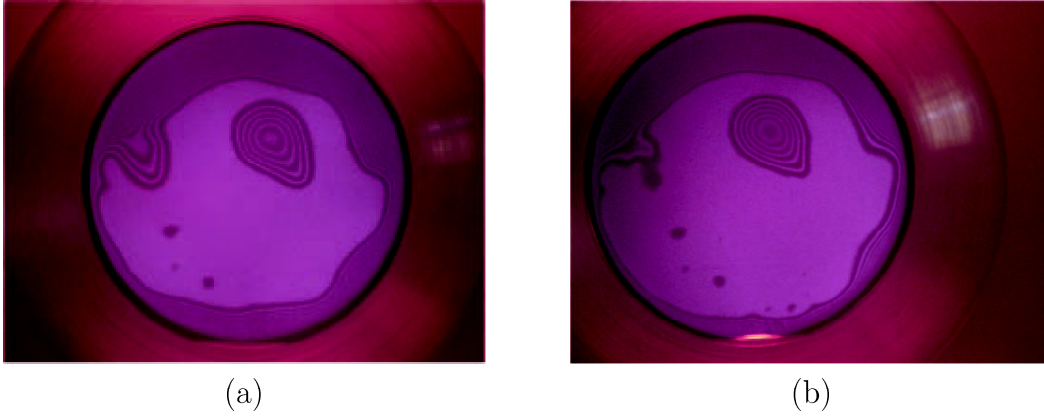


Figure A.6: IR imaging of bonded wafers. (a) before and (b) after 4 days at a pressure of 1.10^{-7} mTorr.

The presence of the wafer under low pressure conditions increases slightly the quality of the bonding. The out-diffusion of hydrogen might be enhanced.

Low temperature annealing

A low temperature annealing was also performed. The wafers were placed in a oven a $140\text{ }^{\circ}\text{C}$ under a nitrogen flow at atomic pressure during 12 hours. Fig. A.7 shows the wafers before and after annealing.

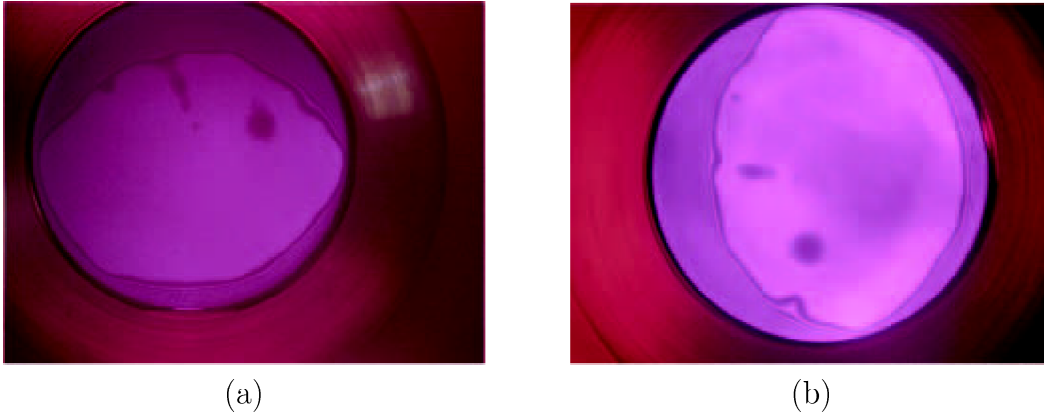


Figure A.7: IR imaging of bonded wafers. (a) before and (b) after annealing at $140\text{ }^{\circ}\text{C}$ during 12 hours.

The impact of a low temperature is limited.

High temperature annealing

An annealing at $1000\text{ }^{\circ}\text{C}$ was thus tested during 52 h (Fig. A.8).

The effect of a high temperature is very positive. Almost the whole surface of the wafer is bonded.

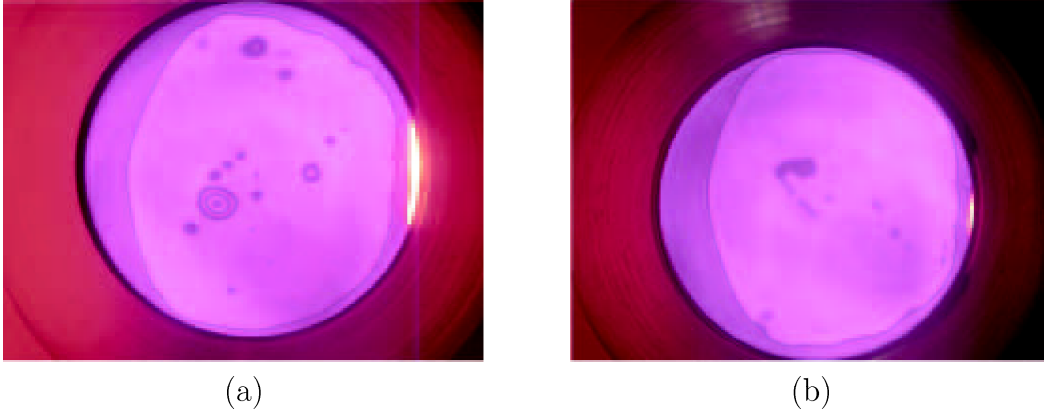


Figure A.8: IR imaging of bonded wafers. (a) before and (b) after annealing at 1000 °C during 52 hours.

High pressure

It was also tried to applied a pressure on the wafers after bonding (Fig. A.9). A nano-imprinter was used to apply a pressure of 60 bars at 260 °C during 10 min.

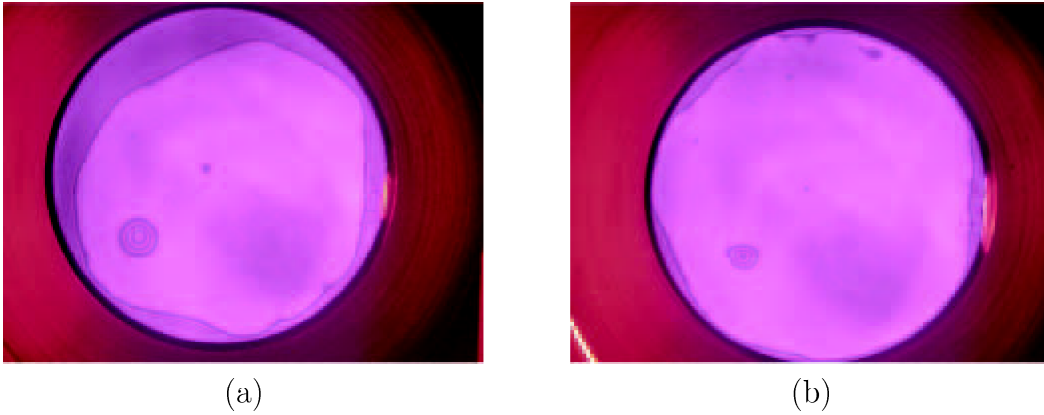


Figure A.9: IR imaging of bonded wafers. (a) before and (b) after a load of 60 bars at 60 °C during 10 min.

Applying a pressure on the bonded wafers increases of a significant manner the bonded surface. However this technique presents the risk of breaking the wafers if they were not perfectly aligned during the bonding.

A.2.4 conclusion

The bonding of a wafer covered by recrystallized Si- α and an oxidized bulk Si wafer is possible. The bonded surface can be maximized by choosing appropriate pre- and post-bonding conditions.

The proposed cleaning and activation method is the following:

- standard cleaning (RCA),
- rinser dryer
- O₂ plasma
- rinser dryer.

Once the bonding has been performed, the proposed post-bonding procedure is the following:

- 60 bars loading at 260 °C during 10 min,
- 5 h anneal at 1000 °C under nitrogen flow.

In order to prove the feasibility of the fabrication process of the starting wafers described in Sec. 1.2.2 and 1.2.3, the grinding and CMP of the SOI wafer should be characterized.

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APPENDIX B

STRESS RELEASE IN PECVD OXIDE

In the processes from Sec. 1.2.2 and 1.2.3, wafer bonding is not only required for the fabrication of the starting wafers, but also during the process, once the future Back Gate has been embedded in low thermal oxide. The addition of stressed multilayers on the initial substrate causes wafer bow, which can degrade the quality of the bonding to the handle wafer [1]. We investigate in this section the ways of minimizing the stress in the PECVD oxide by tuning the plasma parameters, such as pressure, total gas flow, gases ratio but also by the use of RTA after deposition.

B.1 Experimental procedure

Three inch diameter p-type (100) 380 μm thick bulk silicon wafers were used as substrates. The PECVD of silicon oxide was made in an OXFORD Plasmalab System 100 [2]. The size of the deposition chamber allows to process three wafers simultaneously. The chamber consists of a top electrode with high uniformity shower head gas inlet separated by substrate electrode heated and grounded. The frequency of the RF power generator applied to the top electrode is 13.56 MHz. Through the whole batch of experiment the pressure in the chamber was kept at 1 Torr and the substrate electrode temperature was also kept constant at 300°C. The two precursor gases used to form the silicon oxide were nitrous oxide (N_2O) and silane (SiH_4) diluted in nitrogen at a concentration of 5%. In the following, silane or SiH_4 stands for 5% of SiH_4 in 95% N_2 .

Variation range for the parameters were: from 200 sccm to 1050 sccm for the total flow rate, from 5 to 17 for the ratio $[\text{N}_2\text{O}]/[\text{SiH}_4]$, and from 30 W to 100 W for the RF power. The deposition time was 20 minutes, in order to get a film thickness between 10000 Å and 20000 Å, the deposition rate depending strongly on the deposition parameters.

An ADDAX RTA oven with a single 3 inch wafer chamber was used for the RTA. As observed by Carlos Dominguez *et al.* [3], the ambient gas during annealing does not have any impact on the effect of the RTA. Thus the atmosphere during RTA was pure nitrogen, with a flow rate of 4 l/min during the heating phase and a flow rate of 6 l/min during the cooling phase. The heating rate was 700 °C/s and the cooling was efficient enough to reach a temperature of 500 °C in less than 2 seconds after a heating at 950 °C. The temperature varied between 400 and 950 °C and the annealing time between 2 and 30 s.

We focused our study of the PECVD oxide into measuring the deposition rate, etch rate in BHF and stress. The stress and etch rate in BHF were measured before and after RTA.

The BHF used to characterize the etch rate was prepared in the following proportions: 87% NHF₄[40%], 13% HF[49%] in volume. The etching was performed at 20°C without shaking.

The film thickness was measured by spectroscopic ellipsometry. A mapping of the surface was performed to get a measure of the uniformity of the deposition.

The residual stress of the oxide layer was deduced by a measurement from the strain induced in the silicon substrate by the oxide layer deposition (change in wafer curvature). The wafer curvature before and after deposition was obtained using the Dektak profilometer over a distance of 50 mm. The profilometer gave the maximal bow h_{max} of the wafer surface over the length of the scan L (Fig.B.1).

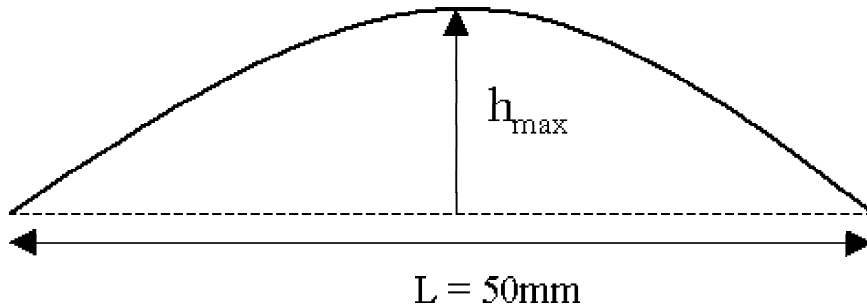


Figure B.1: Evaluation of the radius curvature by profilometer scan.

The curvature radius R is approximated by:

$$R = \frac{(L/2)^2}{2h_{max}} \quad (\text{B.1})$$

Once the strain is determined, the stress is easily calculated using the Hook's law for elastic deformation. If the film thickness is much lower than the wafer thickness, and the stress isotropically distributed through the cross section of the film, one can calculate the stress σ thanks to the Stoney equation (Eq. B.2) [4]:

$$\sigma = \frac{E}{6(1-\nu)} \cdot \frac{t_{sub}^2}{t_{film}} \cdot \left(\frac{1}{R_{post}} - \frac{1}{R_{pre}} \right) \quad (\text{B.2})$$

where σ is the stress in the thin film, E and ν , respectively the Young modulus and Poisson coefficient of the substrate, t_{sub} and t_{film} , respectively, the substrate and film thicknesses and R_{pre} and R_{post} respectively the curvature radius of the wafer before and after deposition. As the wafers do not have the same curvature radius before deposition (the h_{max} value can vary from 600 nm up to 15 μm), the curvature radius was measured before and after deposition on each wafer.

B.2 Impact of the gas flow

Firstly the total gas flow was varied from 200 sccm to 1050 sccm keeping all the other parameters constant (chamber pressure to 1 Torr, RF power to 100 W, table temperature to 300 °C, $[\text{N}_2\text{O}:\text{SiH}_4]=7$). All the interesting physical properties were measured before and after a RTA at 900 °C.

The wafers had a nice aspect after deposition; the film thickness was homogeneous over the whole wafer for total gas flow over 400 sccm. Below this value, the standard deviation of the measured thickness was 3%. This effect is due to the volume of our deposition chamber, which, allowing to process three wafers at a time, requires a minimum gas flow through the chamber to have an homogenous diffusion of the gases inside the chamber. The deposition rate increases linearly with the total gas flow, letting us assume that all the gases react and give rise to more oxide when more reactants are present (Fig. B.2).

The residual stress (Fig. B.3) and the etch rate (Fig. B.4) are strongly correlated.

Though a small increase in the etch rate pre- and post-annealing correlated to

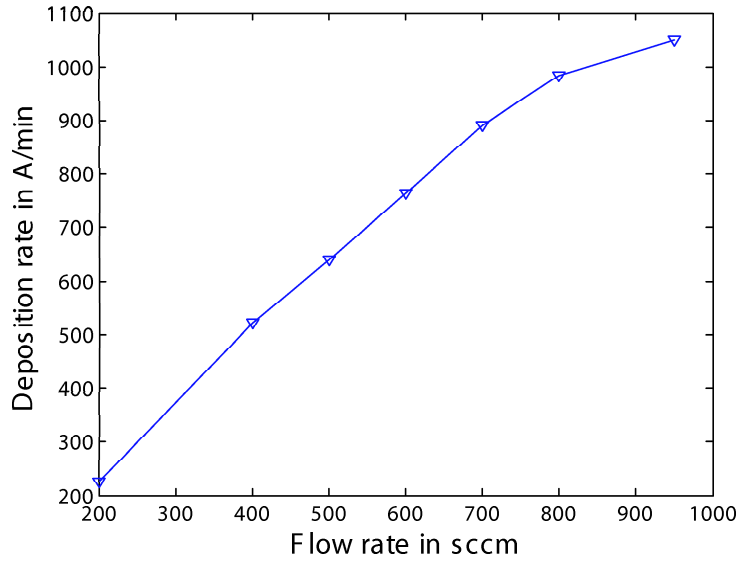


Figure B.2: Deposition rate in function of the total gas flow.

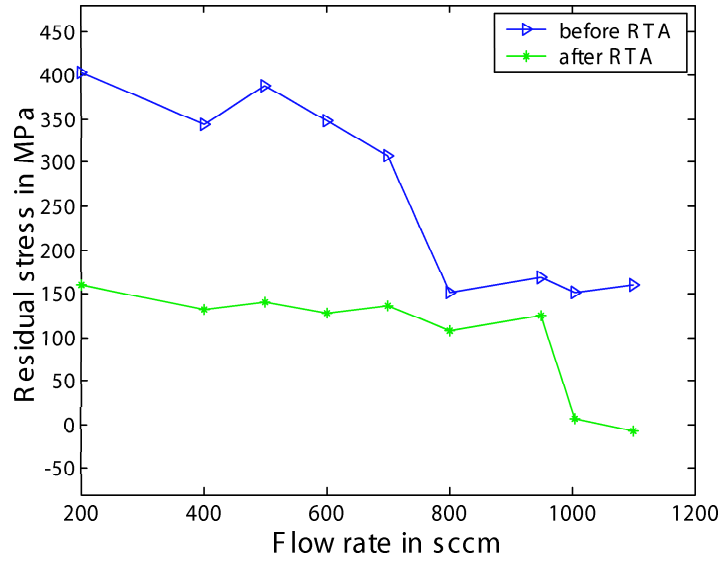


Figure B.3: Thin film stress in function of the total gas flow.

a slight decrease of the residual stress pre and post annealing when increasing the flow rate up till 700 sccm, the etch rate increases drastically when increasing the total flow rate above this value with a simultaneous drop in the residual stress. The RTA allows to keep an acceptable etch rate of 3000 Å/min at 800 sccm while having the residual stress considerably reduced from 180 to 128 MPa. Above this total gas flow, it is not possible any more to control the etch rate, the error bars on the graph indicating the non homogeneity of the etch rate. On the other hand the residual

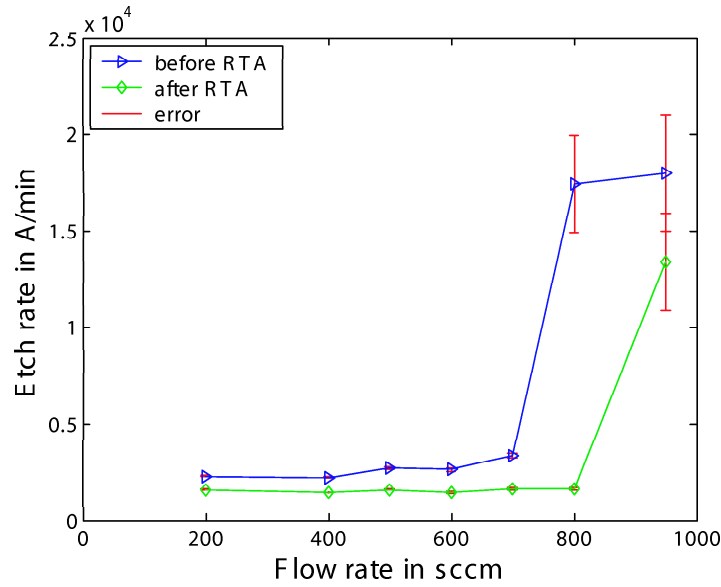


Figure B.4: BHF etch rate in function of the total gas flow.

stress in that case becomes null after RTA.

B.3 Impact of the RF power

The power was then varied from 30 to 100 W. Total gas flow was kept at 600 sccm, pressure at 1 Torr, $[N_2O]/[SiH_4]=7$ and the table temperature remained constant at 300 °C.

The deposited films have a homogenous thickness over the whole wafer, the measured value having a standard deviation around 0.7%. The deposition rate increases slightly with the power, but not of a significant manner, only 20% faster from 30 to 100 W (Fig. B.5).

Increasing the power does not give real advantage for the deposition rate.

Stress post deposition continuously decreases when the power decreases (Fig. B.6).

Previous studies showed that the quality of the PECVD film strongly depends on the ratio $\eta P/F$, where η is the gas dissociation efficiency, P the power and F the total gas flow [5]. A too low ratio will yield poor quality oxide with voids and nodules and weakly bonded atoms, whether a high ratio means that the energy transfer process is well matched to the presence of ion species and leading to a well bonded atoms in the deposited layer [6]. At small power, the atoms being weakly

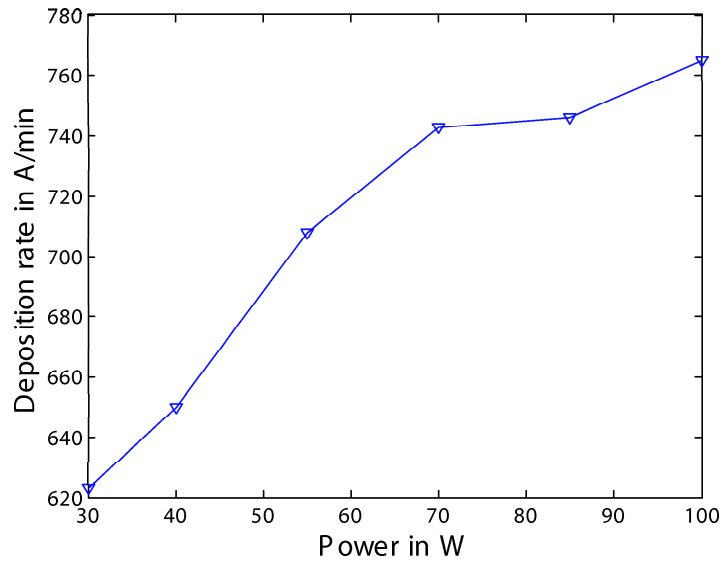


Figure B.5: Deposition rate in function of the RF power.

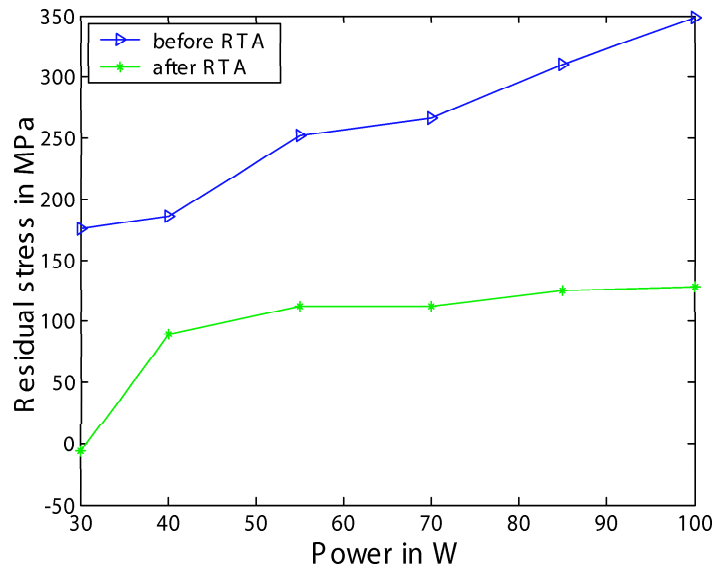


Figure B.6: Thin film stress in function of the RF power.

bonded in the silicon oxide layer, they relax the internal stress by forming voids. The RTA decreases always the stress by his effect of re-organization of the deposited layer. At higher power, the ionization of the precursor gases is more complete and the grown oxide does not have voids or particles. For a power of 30 W, the stress becomes null but the stress varies with the time. This point will be mentioned later on.

The etch rate decreases continuously when the power increases (Fig. B.7).

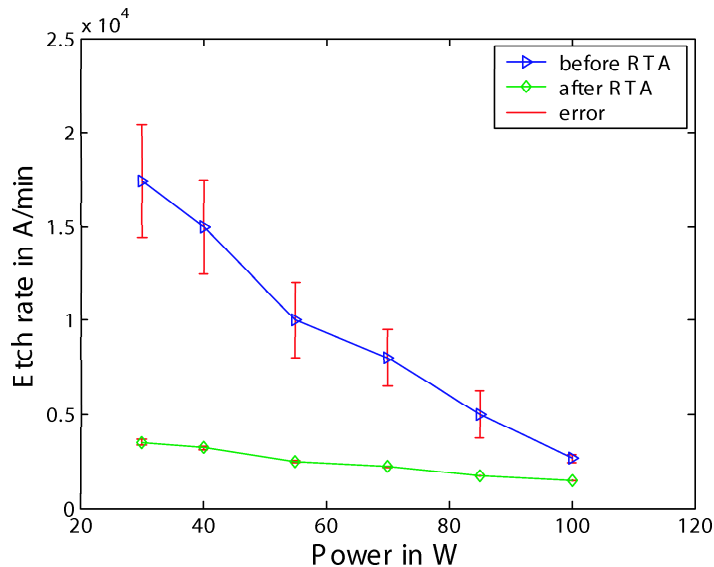


Figure B.7: Etch rate in function of the RF power.

For low power, the etching of the deposited film in BHF is totally non uniform, the etching rate being determined with an uncertainty of 5000 Å. The silicon oxide formed at low power has weakly bonded atoms, so easily etch by HF. The RTA decreases drastically and make homogeneous the etch rate. At low power, the etch rate after RTA is in the order of 4000 Å/min, which can be a handling value. The oxide deposited at 30 W seems to be a good candidate for bonding and passivation applications, except its temporal instability.

B.4 Impact of the $[N_2O]/[SiH_4]$ ratio.

The ratio of the two precursor gases $[N_2O]/[SiH_4]$ was varied from 5 to 17. Total gas flow was kept at 600 sccm, pressure at 1 Torr, power at 100 W and the table temperature remained constant at 300 °C.

The deposition rate increases when the SiH_4 partial pressure increases (Fig. B.8).

The limiting factor for oxide deposition rate is the quantity of Si ions presents in the plasma. However at high $[N_2O]/[SiH_4]$ ratio, more Si-O bonds are formed whether at low $[N_2O]/[SiH_4]$ ratio more Si-H bonds are formed [7],[8]. Although at small $[N_2O]/[SiH_4]$ ratio the deposition rate is high the oxide quality is poor as can be seen in Fig. B.9.

For too high silane concentration (below a gas ratio of 6), the etch rate increases

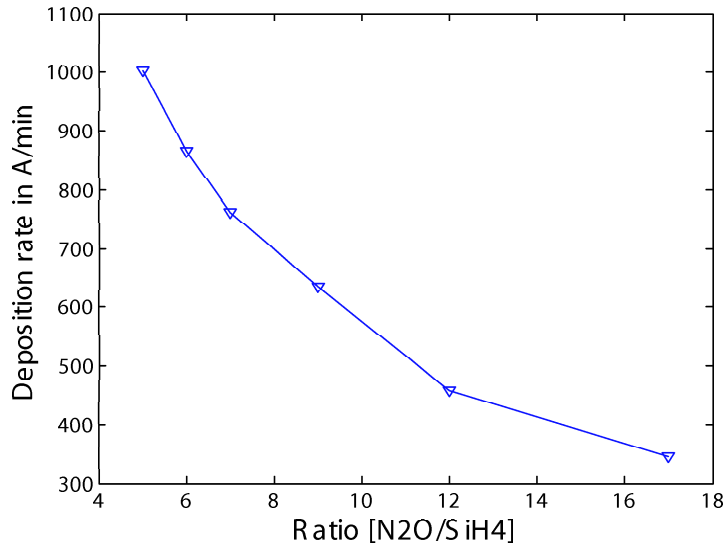


Figure B.8: Deposition rate in function of the $[\text{N}_2\text{O}]/[\text{SiH}_4]$ ratio.

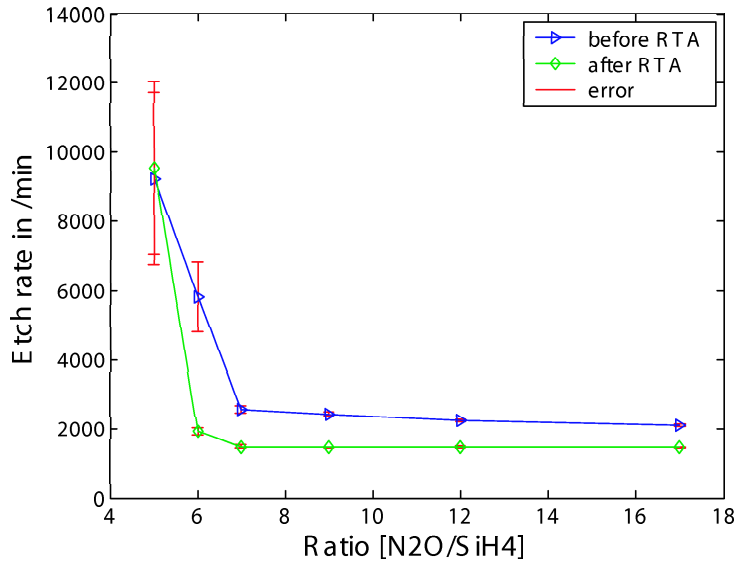


Figure B.9: Etch rate in function of the $[\text{N}_2\text{O}]/[\text{SiH}_4]$ ratio.

and is not homogeneous over the whole wafer surface. Not even RTA can increase the resistance of the deposited oxide to BHF. We observe conjointly with the etch rate increase a decrease of residual stress (Fig. B.10).

For Si-rich PECVD silicon oxide the bond reaction energy is lower than for stoichiometric silicon dioxide, explaining the higher reactivity with BHF [7]. As for the previous samples the RTA decreases the residual stress and the BHF etch rate. The mechanisms involved are the same as for the two previous batches of experiences. For a gas ratio of 6, the etch rate is brought back from 5000 to 2000

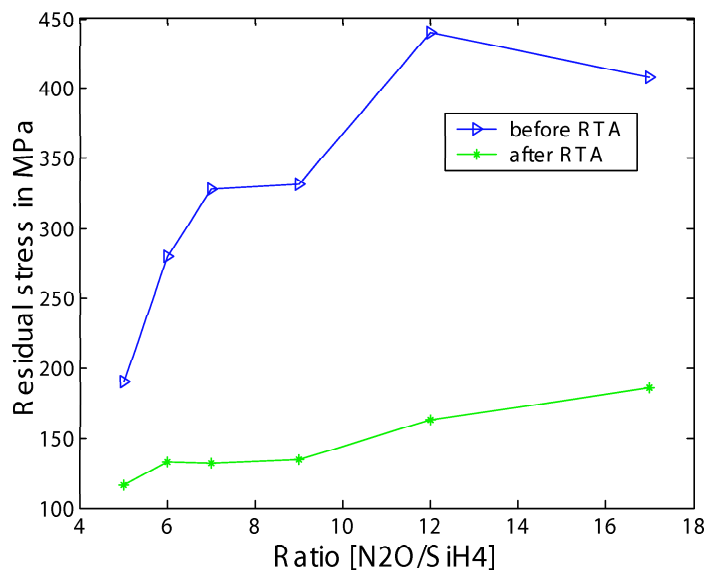


Figure B.10: Thin film stress in function of the $[\text{N}_2\text{O}]/[\text{SiH}_4]$ ratio.

$\text{\AA}/\text{min}$, which is an acceptable value to control oxide etching in a process. Null stress is not achieved by varying the gas ratio.

B.5 Impact of the RTA

Various RTA times and temperatures were tested on samples with an $1.5\ \mu\text{m}$ thick oxide layer. The experimental conditions for the deposition of this layer were: table temperature 300°C , RF power 100 W, total gas flow 600 sccm, ratio $[\text{N}_2\text{O}/\text{SiH}_4]=7$, chamber pressure 1 Torr. The RTA time was varied from 3 to 30 s (Fig. B.11) and compare with a conventional annealing of 30 min at 900°C in $1.5\ \text{l}/\text{min}\ \text{N}_2$. The RTA temperature was increased from 400 to 950°C (Fig. B.12). Etch rate and residual stress were then measured.

Below 500°C RTA has no impact on the deposited oxide. No reconstruction or impurities release occurs, as shown by the stability of the two measured parameters. As the temperature increases up till 950°C stress and etch rate are decreasing with the same behavior. The literature provides many explanations for this change in properties [9],[10]. The non stoichiometric $\text{SiO}_x\text{N}_y\text{H}_z$ film will release H and N atoms during the annealing and experiences the following network reaction:

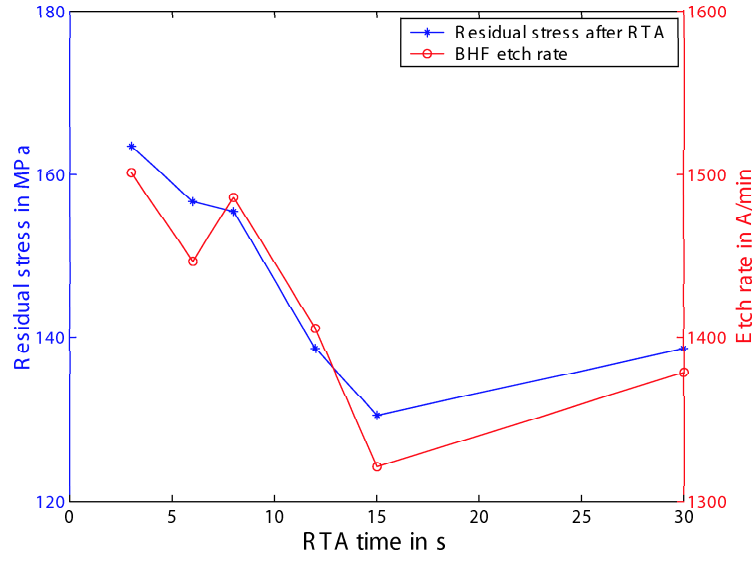


Figure B.11: Evolution of the thin film properties in function of the RTA time.

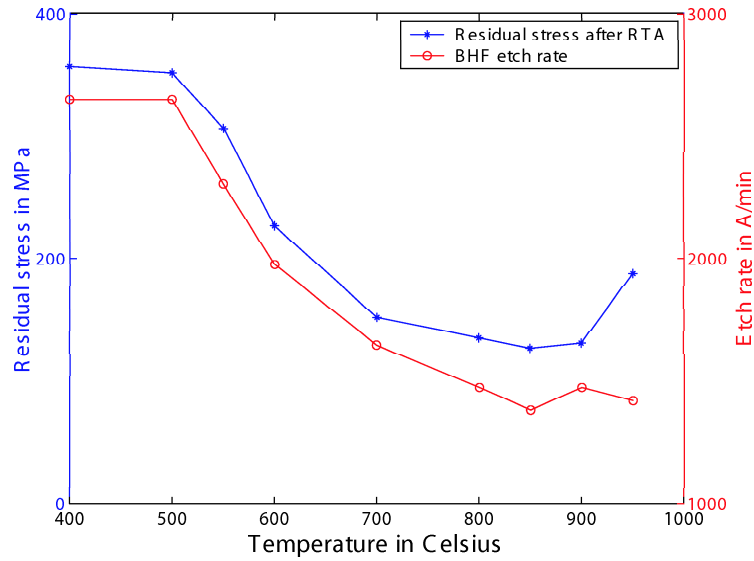


Figure B.12: Evolution of the thin film properties in function of the RTA temperature.

$$\text{SiO}_x \rightarrow \left(\frac{x}{2}\right) \text{SiO}_2 + \left(1 - \frac{x}{2}\right) \text{Si} \quad (\text{B.3})$$

Below 700 °C, H is released but the bonds Si-O do not suffer any re-arrangement. Above 700 °C re-organization of Si-O in SiO₂ occurs. In our experiences we did not measure the concentration of Si-H, Si-N, Si-O bonds, but we measured the macroscopic properties. A RTA of 900°C during 15 s seems to be enough to reach

the best properties that one can get for a given oxide. The etch rate and the residual stress do not change significantly above 900 °C. Although the measurements in Figure 15 are quite noisy, it appears that the RTA time has also an influence. The residual stress and the BHF etch rate reach their minimal value in 15 s, respectively 132 MPa and 1330 Å/min. Taking into account the measurement error, one can say that the etch rate and the residual stress do not vary any more above 15 s. After conventional furnace annealing (30 min. 900°C under nitrogen atmosphere) the residual stress reaches a value of 160 MPa and the BHF etch rate a value of 1290 Å/min. It appears clearly that RTA is the best method to anneal a PECVD oxide. The gain in etch rate reduction are similar to those get from conventional furnace annealing, the gain in stress reduction are even better and the thermal budget is fairly low and does not induce extra diffusion.

B.6 Quality of the PECVD oxide

B.6.1 Roughness and bondability

As the PECVD oxide will be bonded to a handle wafer, it is necessary to control its stress, and we demonstrated that it was possible to reduce the stress of the deposited thin film by choosing appropriate plasma conditions and by the use of RTA after deposition. However, reducing the wafer bow is not sufficient to perform a wafer bonding; the wafer surface must also be very smooth. AFM measurements have thus been made on several oxides before and after RTA. Table B.1 shows the roughness of several types of oxide. High and low stressed oxide have been measured.

The surface roughness is too high to perform a wafer bonding. A CMP step can be used to reduce the surface roughness, but we did not perform any experiment to check the feasibility of roughness reduction of PECVD oxide by CMP.

B.6.2 Stability over time

It has been observed that the residual stress in the thin film PECVD oxide increases with time after deposition. This effect is attributed to the water absorbed by the PECVD oxide once present in ambient [11].

Deposition conditions	RMS roughness before RTA in (Å)	Average roughness after RTA in (Å)
30 W, $[\text{N}_2\text{O}/\text{SiH}_4]=7$, 600 sccm (low stress oxide)	40.7	39.2
100 W, $[\text{N}_2\text{O}/\text{SiH}_4]=7$, 600 sccm (high stress oxide)	35.6	34.4
100 W, $[\text{N}_2\text{O}/\text{SiH}_4]=5$, 600 sccm (low stress oxide)	38.6	39.9
100 W, $[\text{N}_2\text{O}/\text{SiH}_4]=7$ 1050 sccm (low stress oxide)	45.2	53.6

Table B.1: AFM measurement of the surface roughness

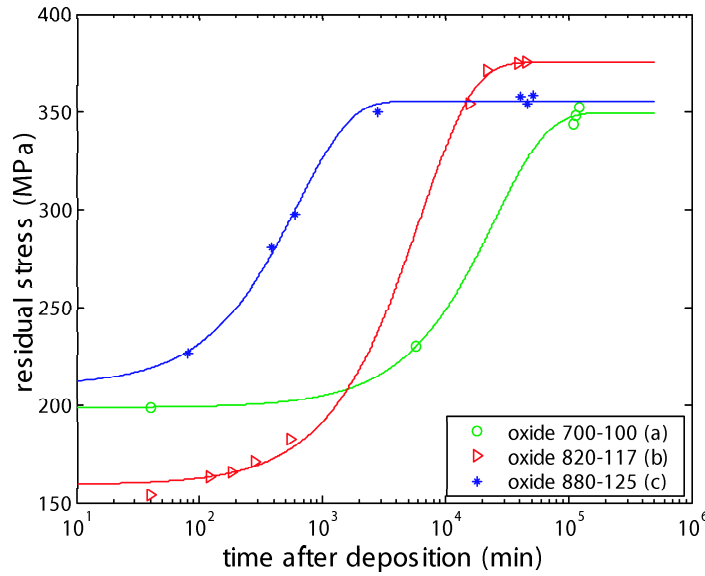


Figure B.13: Evolution of the thin film stress in function of the time after deposition. The oxide were deposited at 300 °C, 100 W RF power, (a) 700 sccm N_2O , 100 sccm SiH_4 , (b) 820 sccm N_2O , 117 sccm SiH_4 , (c) 880 sccm N_2O , 125 sccm SiH_4

This effect is more pronounced on low stress oxides (Fig.B.13). This property limits the choice of the PECVD oxide. Indeed, industrial applications cannot wait a long period until the oxide has stabilized.

B.6.3 Electrical properties

The PECVD oxide is supposed to surround the Back Gate. Its electrical properties must then be characterized. In order to check the electrical properties of the deposited PECVD oxide and the influence of RTA on its electrical properties, C-

V curves were performed on MOS capacitances [12]. The MOS capacitances were made on high resistivity silicon wafer to enhance the MOS capacitance effect. The deposited thickness of PECVD oxide was 4000 Å. The contact on the back side of the wafer was made of a 3000 Å thick layer of Al. The contact on the front side was made of a 1 μm thick layer of Al. The structure area was 0.272 mm², which yields a theoretical oxide capacitance, C_{ox} of 22.4 pF. One high and one low stress oxide were deposited. The deposition conditions were the following:

- 100W, 3 min 45 s, 729 sccm N₂O, 121 sccm SiH₄, 1 Torr, 300°C (low stress oxide made at high power),
- 100W, 10 min, 360 sccm N₂O, 40 sccm SiH₄, 1 Torr, 300°C (high stress oxide made at high power).

Fig. B.14 and B.15 shows the C-V measurement for respectively, low and high stress PECVD oxides.

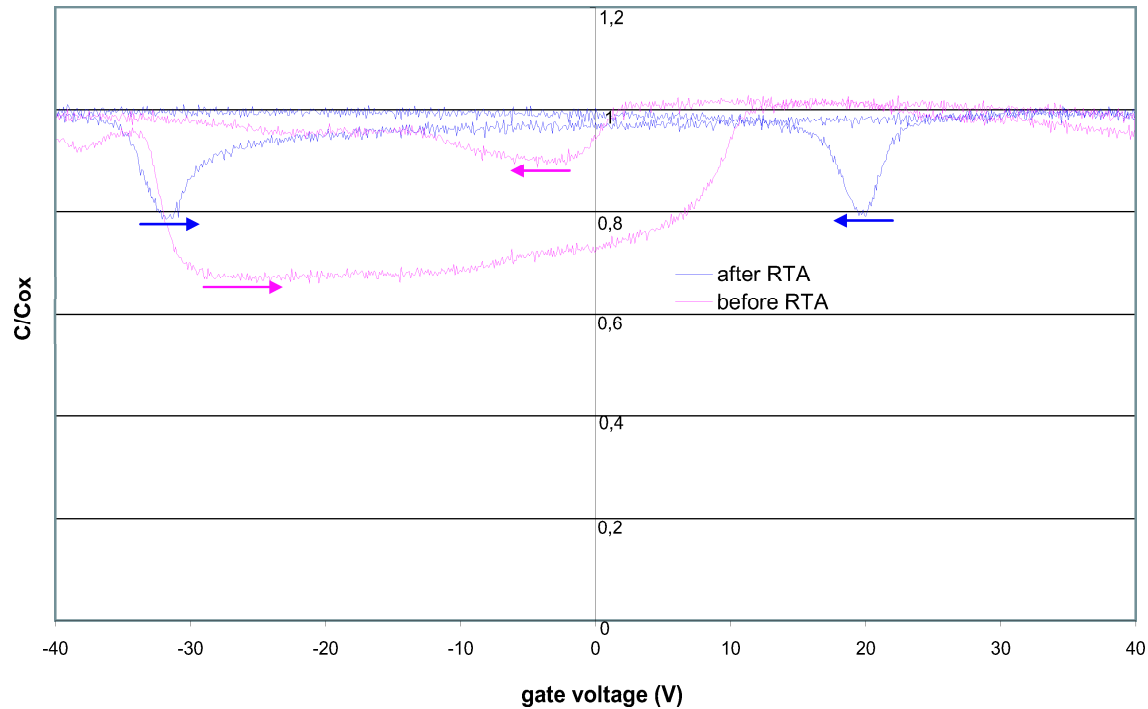


Figure B.14: C-V measurement of a low stress oxide made at high power before and after RTA.

The gate voltage was biased from -40 V to +40 V and immediately after this first scan from +40 V to -40 V. The hold time at -40 Volts was 120 s, the QSCV integration time 60 ms, the leak integration time 200 ms, and the delay time 0

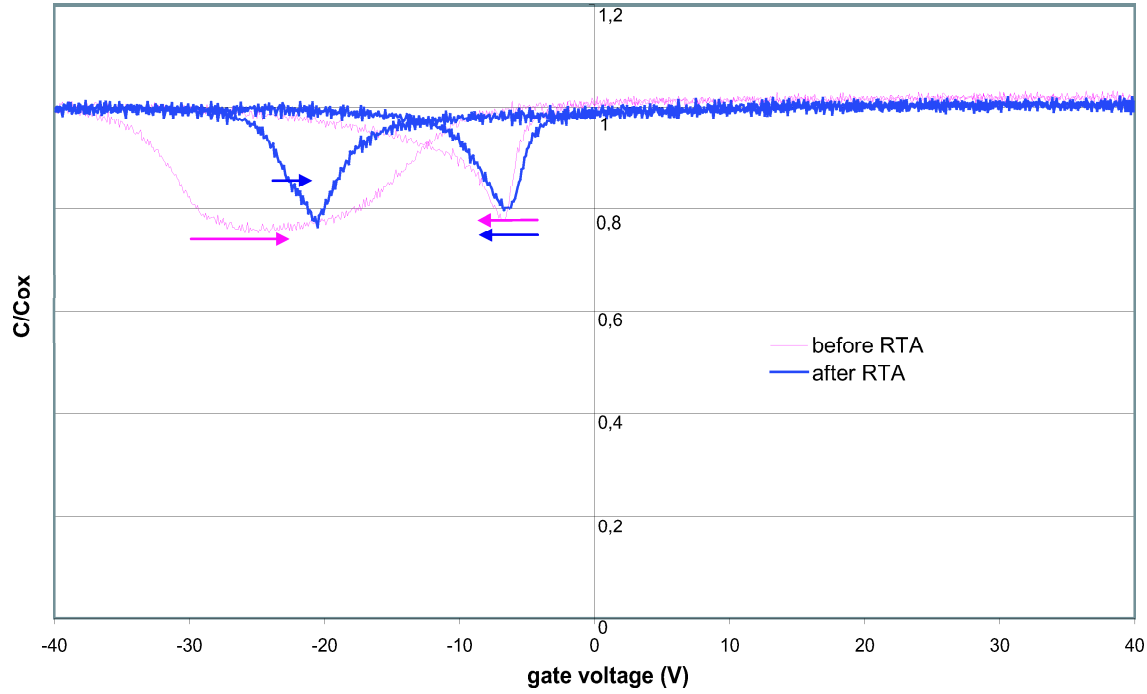


Figure B.15: C-V measurement of a high stress oxide made at high power before and after RTA.

s. For both of those oxides the forward curve before RTA presents a very large splay beginning around -30 V for which the MOS capacitance value, C decreases to 70% of the C_{ox} value in the case of the low stress oxide and to 80% of its value in the case of the high stress oxide. The value of the MOS capacitance reaches again the C_{ox} value around +10 V in the case of the low stress oxide and around -12 V in the case of the high stress oxide. The backward voltage scan shows also a drop in the value of the MOS capacitance but of a much smaller magnitude in the case of the low stress oxide (90% of the C_{ox} value), and for a higher gate voltage, between +3 V and -15 V for the low stress oxide and between -5 V and -15 V for the high stress oxide. The drop in the C-V curve being visible for both negative and positive voltages in the case of the low stress oxide, it means that the oxide traps can accept either electrons or holes. The very large splay of the two C-V curves before RTA indicates a very high concentration of interface traps. The dependence of the capacitance drop position on the previous gate voltage (the drop being not at the same position for the forward and backward measurement curve) shows the

presence of oxide traps [13],[14]. The effect of the RTA on the two PECVD oxides is directly visible in terms of interface traps density. Although our equipment does not allow performing high frequency measurements which are necessary to quantify the interface traps density, one can see that the splay of the C-V curves is considerably reduced after RTA, giving an indication of a lower interface trap density [15]. The oxide traps are not much affected by the RTA. For the high stress oxide, the positions of the drop of the capacitance value for the forward and reverse curves are centred on the same gate value. Those traps having a capture and emission time in the range of the tens of seconds, they acts as if they would modify the total oxide charge and then modify the flat band voltage and thus the position of the capacitance drop. The recombination and emission time has not been measured but I_g - V_g curves have been performed and gives a good indication of the emission time of the traps responsible for the charging of the oxide (Fig. B.16).

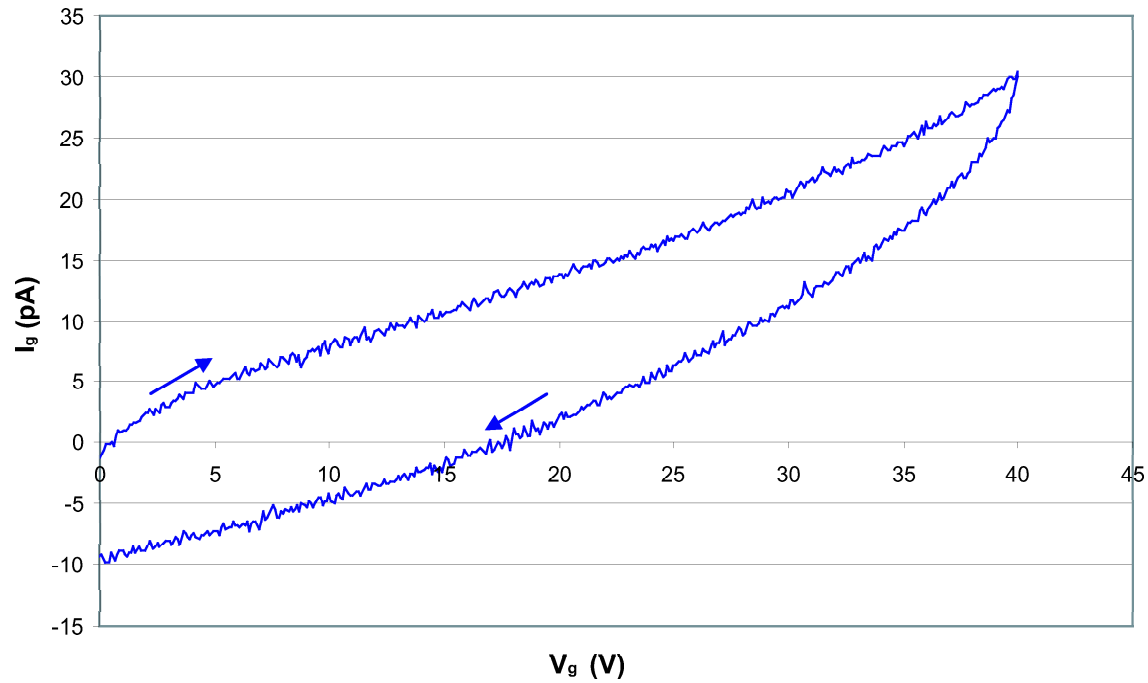


Figure B.16: I_g - V_g measurement of a low stress oxide after RTA.

V_g was scanned from 0 V to +40 V and then decreased to 0 V. The gate potential was held at 0 V during 30 s and then the plotted curve was recorded. It is interesting to notice that at after the first cycle, the remaining gate current was -10 pA, and that after 30 s in short circuit, the gate current was still -2 pA, meaning that some electrons were still emitted from the PECVD oxide into the bulk.

B.7 Conclusion

Stress reduction in PECVD oxide has been demonstrated, by tuning the plasma parameters and by performing a RTA after deposition. Although low stress PECVD oxides would not bow the wafer on which they would be deposited, and avoid thus wafer bonding, their physical properties are not very good.

Most of the low stress oxides present an evolution of the stress with the time after deposition, due to water absorption. More work should be invested in reducing this transient time. Treatment of the PECVD oxide in DI water could be a way of investigation [16].

The surface roughness is not low enough to perform the bonding of a handle wafer directly on PECVD oxide. However, in our process the PECVD oxide has to be planarized by CMP before bonding. The surface roughness could thus be decreased during the CMP.

The electrical properties of the PECVD oxides are a problematic issue. Though the RTA reduces the concentration of interface traps, it does not remove all the oxide traps, which decreases the isolating properties of oxide. More work has to be done to solve this problem.

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APPENDIX C

HIGHLY SELECTIVE ETCHING OF SiO_2 WITH RESPECT TO SI

In process presented in Sec.1.2.2, once the polysilicon buried mask has been revealed, an oxide layer must be etched by RIE. The mask used for this etching is the polysilicon buried mask and the etch stop layer is the active silicon film. The trench etched in the oxide has the dimension of the transistor gate. This small dimension of the etched structure requires to develop a specific RIE recipe as the etch rate of a given plasma developed on a blank surface varies when etching narrow trenches. The use of the active silicon film, which is very thin, as etch stop layer requires a highly selective etching recipe.

C.1 CF_4 / H_2 based plasma

Selective etching of silicon dioxide with respect to silicon is achieved in fluorocarbon based plasma [1],[2],[3]. RIE in CF_4 , CF_4/H_2 , CHF_3 , C_4F_8 has been widely studied these last decades. Publications describe the experimental behavior of the RIE and the physical description and modeling of the etching process [4],[5]. CF_4/H_2 based plasma offers the best selectivity with respect to silicon for oxide etching. Experiments reports a highest selectivity of 40, when simulation shows that CF_4 based plasma could yield an infinite selective etching of silicon dioxide with respect to silicon [6],[7]. However due to the large amount of different species in a plasma discharge and the complexity of its physics, most of the publications present simplified modeling of RIE in CF_4 based plasma. Etching rate simulation have been published assuming given conditions for the plasma composition, the ion energy, or the ion flux density, yielding interesting results for the understanding of the RIE mechanisms and shows that silicon etch rate strongly depends on the the H_2 concentration. Experimental studies have demonstrated that etching occurs through a steady state fluorocarbon film deposited on the substrate surface during etching [8],[9],[10]. The

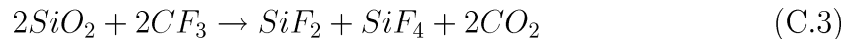
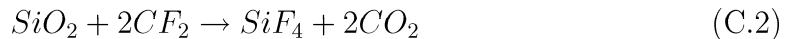
film thickness and composition depends on the substrate type and on the plasma composition.

The etching of silicon in fluorine ambient is described by the following equation:



Silicon is etched through reaction with atomic fluorine. Atomic fluorine is brought to the fluorocarbon film by the incoming ion flux. Fluorine diffuses through the fluorocarbon film and reacts with silicon to form volatile SiF_4 [11], [12]. The presence of this steady state fluorocarbon film result from a balance between deposition and removal of the film [13]. The fluorocarbon film is removed by sputtering of incoming ions and through reaction with atomic fluorine to form volatile CF_x compounds. The diffusion of fluorine through the fluorocarbon film can be enhanced by energetic ions. On the other hand, in the case of low energy ions, the removal rate of the fluorocarbon is lower, the film thickness increases and the etch rate decreases. Jagadesh-Kumar *et al.* studied the influence of H_2 addition in a CF_4 plasma on the silicon etch rate [4]. H atoms reacts with F atoms to form volatile HF. The Si etch rate decreases when adding H_2 to the plasma due to the reduction of F concentration.

Oxide reacts with CF_2 and CF_3 ions according to the following equations:



The thickness of the fluorocarbon film is in the standard condition much lower on oxide than on silicon surface. On the oxide surface the carbon of the fluorocarbon film reacts with the oxide of the film to form CO_2 and CO yielding thus to a film thickness lower than 1 nm in most of the etching conditions. As the fluorocarbon is removed through reaction with the substrate and through sputtering by energetic ions, the ion energy is a key parameter to control the fluorocarbon film thickness, as it can affect the balance between deposition and removal of the film. In particular conditions, the component of the ion momentum perpendicular to the etching

direction is very low, thus the removal of the fluorocarbon film on the etched wall does not balance the deposition any more. In this case the etch rate in the direction perpendicular to the etching direction can be drastically decreased and yields a highly anisotropic etching. This effect is widely used in fluorocarbon based plasma. Our goal was to develop highly selective etching of silicon dioxide with very high selectivity with respect to silicon and to study the etching rate of silicon and silicon dioxide in function of process parameter like feed gas composition, pressure and etching time. The anisotropy was also studied in the different etching condition. A highly selective and anisotropic etching of oxide with respect to silicon was finally found.

C.2 Experimental set up

Samples used to characterize the etching rates were 1 cm² pieces held on a 3 inch bulk silicon wafer during the etching. The Si etch rate has been characterized by measuring the thickness of the silicon layer from a SOI substrate before and after etching. The oxide etch rate has been characterized by measuring the thickness of an oxide film grown in wet ambient at 1000 °C on a silicon substrate before and after etching. The RIE was performed in a Plasmalab System 100 from OXFORD. The reactor chamber is feed by six different mass flows able to deliver a gas flow up to 200 sccm per minute. The gas inlets are connected to a shower on the top electrode. The substrate electrode is connected to a 13.6 MHz generator with automatic capacitance matching (AMU). The RF power can vary to 300 W. The chamber dimensions are 380 mm diameter for 200 mm height. The substrate electrode is kept at constant temperature by a helium flow. Temperature of the substrate can be varied from -40 °C to +40 °C. A turbomolecular pump with a dual stage rotary as backing pump can ensure a working pressure from 1 to 100 mTorr. In bibliography the etch rate was characterized in function of the ion flux and ion energy. We varied this parameter indirectly by tuning the process parameters such as pressure and plasma composition. In our set of experiments, the pressure varied from 5 to 50 mTorr, the H₂ concentration from 5 to 65% and the etching time from 1 to 8 minutes. The film thicknesses were measured before and after RIE by spectroscopic ellipsometry.

The deposited fluorocarbon film was also characterized by ellipsometry. Its optical index was determined by fitting the parameters of a Cauchy model based on the measurement of a 100 nm thick fluorocarbon film. The deduced optical index which was then used in the whole set of analysis was:

$$n(\lambda) = n_0 + \frac{n_1}{\lambda^2} + \frac{n_2}{\lambda^4} \quad (\text{C.4})$$

$$k(\lambda) = k_0 + \frac{k_1}{\lambda^2} + \frac{k_2}{\lambda^4} \quad (\text{C.5})$$

with

$$n_0=1,448 \quad n_1=9.2 \times 10^3 \quad n_2=-3.7 \times 10^8$$

and

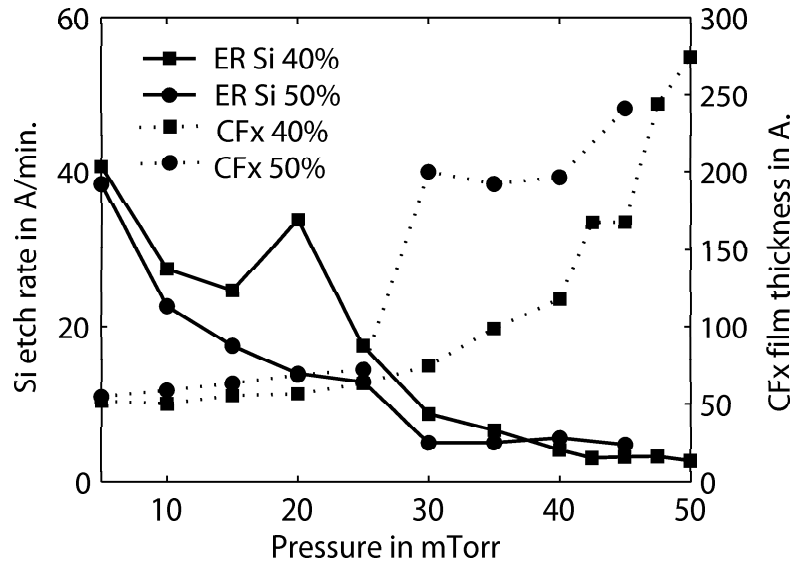
$$k_0=5,3 \times 10^{-2} \quad k_1=-1.52 \times 10^4 \quad k_2 = 2 \times 10^8.$$

C.3 Result and discussion

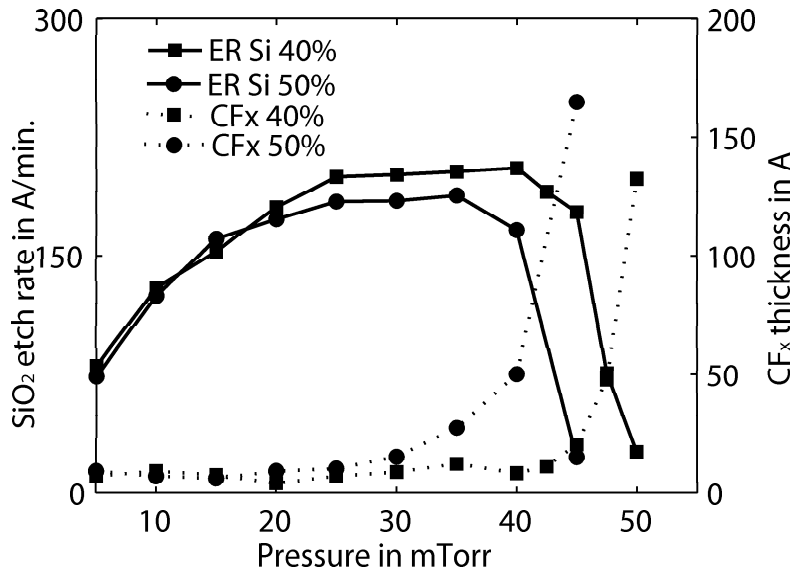
C.3.1 Influence of pressure

Fig. C.1 plots Si and SiO₂ etch rate and fluorocarbon film thickness in function of the pressure for two different H₂ concentrations. The etching was performed at 20°C, the total gas flow was 60 sccm/min and the RF power was fixed to 150 W.

Silicon etch rate is significant only at low pressure. The etch rate decreases from 40 Å/min to 5 Å/min when the pressure varies from 5 to 25 mTorr. For this range of pressure the etching is performed through a 50 Å thick fluorocarbon film that has been measured by ellipsometry on the surface. As described in the introduction, this steady state fluorocarbon film results of a balance between deposition and removal rate of the fluorocarbon film. At low pressure the ions suffers less collisions than at higher pressure and have thus a rather high energy. The fluorine diffusion through the film and the fluorocarbon film sputtering are thus enhanced yielding a high silicon etch rate [11]. The silicon etch rate is higher for a hydrogen concentration of 40% than for a hydrogen concentration of 50%. As explained in the introduction, hydrogen neutralize fluorine by forming HF, reducing thus the amount of fluorine available to react with silicon. At pressure above 25 mTorr, the fluorocarbon film



(a)



(b)

Figure C.1: Etch rate in function of pressure for (a) silicon and (b) oxide.

thickness increases exponentially. At higher pressure the mean free path of the ions is reduced and they lose energy through each collision. When reaching the fluorocarbon surface, the ion energy is not sufficient enough to enhance the fluorine diffusion and to sputter the fluorocarbon film. The deposition is not balanced any more and the film thickness increases. As fluorine is not assisted any more to diffuse through the film the silicon etch rate decreases. It can be distinguished two regimes for the etching of silicon: Etching through a thin steady state film and through

a thick steady state film. The transition between the thick film and the thin film regime is detailed below. Fig. C.2 plots the etched silicon thickness, the fluorocarbon film thickness and the oxide etch rate in function of the etching time for two different etching conditions.

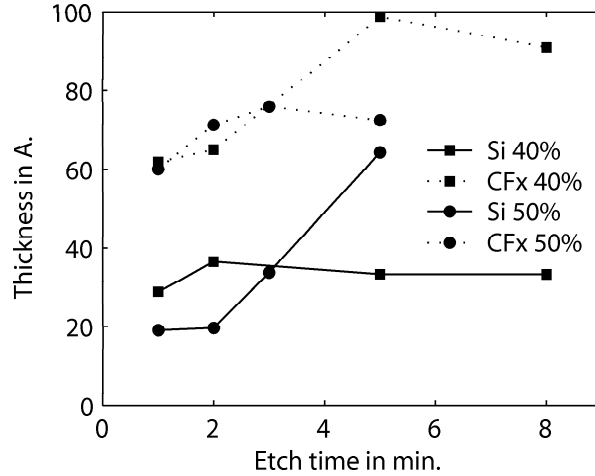


Figure C.2: Silicon etched and fluorocarbon deposited thicknesses. The etching were performed at a total gas flow of 60 sccm/min. and a RF power of 150 W. H_2 concentrations were 40 and 50% at respective pressure of 35 and 25 mTorr.

At 25 mTorr and 50% H_2 , as can be seen on Fig. C.1, the etching is still in the thin fluorocarbon film regime. The deposited fluorocarbon film on silicon reaches its steady state thickness of 70 Å after 2 min. The silicon etched thickness linearly increases with the etching time; we have in this case etching of silicon. At 40% H_2 and 35 mTorr, it can be seen on the Fig. C.1 that the etching is done in the thick fluorocarbon film regime. The Fig. C.2 shows that 30 Å of silicon are etched within the first minute but that silicon etching stops after this first 30 Å. After 5 minutes the film thickness is stabilized at a value of 100 Å. In this case the fluorocarbon film inhibits any further etching of silicon. The etch rate of oxide is stabilized after 1 min. It does make sense to define this etching condition as an almost infinite selective etching of oxide with respect to silicon.

From 5 to 40 mTorr, the deposited fluorocarbon film on oxide is thinner than 10 Å. The oxide etch rate is also very low. A possible explanation is that due to the low transit time of the species in the chamber, CF_4 and H_2 do not dissociate completely yielding small amount of CF_2 and CF_3 , and thus low etch rate of oxide [14]. The etch rate increases with pressure until the pressure reaches 20 mTorr. From 20 to 40

mTorr the oxide etch rate is stable around 200 Å/min. At higher H₂ concentration, H ions neutralize the CF_x compounds by forming CHF_x yielding thus a slightly lower oxide etch rate. For pressure above 40 mTorr, the oxide etch rate drops abruptly to reach a value of 50 Å/min. This drop in etch rate is linked to a deposition of a fluorocarbon film of 150 Å on the oxide which decreases the etch rate. Morishita *et al.* have shown that for longer residence time, i.e. at high pressure, a thick fluorocarbon film is deposited [14]. A possible explanation is that this fluorocarbon film could be formed because due to this long residence time CF₄ and H₂ dissociate completely and reacts with each other to form a film poor in CF₂ and CF₃ species. The reactivity of this film with the oxide would thus be quite low, explaining the low oxide etch rate and the low fluorocarbon removal rate. This drop in etch rate and its correlated increase in fluorocarbon thickness occurs at lower pressure for higher H concentration.

C.3.2 Influence of H₂ concentration

Fig. C.3 plots the respective etch rates of silicon and oxide and the fluorocarbon film thicknesses deposited on these substrates in function of the H₂ percentage at 20, 25 and 30 mTorr.

Knizikevicius simulated the composition of a CF₄/H₂ plasma in function of the H₂ concentration for a given ion energy [5]. At low H₂ concentration the plasma is mainly composed of CF₄, CF₃, and F atoms. Increasing the H₂ proportion neutralizes the F atom via the formation of HF, but also allows the formation of CF₂. Above a certain threshold in H₂ concentration all the F atoms have been neutralized by the hydrogen. At high H₂ concentration, CF₃ is not to be found any more in the plasma and the concentration of CF₂ decreases.

The silicon etching is strongly dependent on the thickness of the fluorocarbon film. It can be distinguished three regimes for the silicon etching in function of H₂ concentration. In the first regime, at low H₂ concentration, the silicon etch rate decreases linearly with the increase in H₂ percentage. In pure CF₄, silicon is etched at 200 Å/min. The thickness of the fluorocarbon film deposited on the silicon surface is in the 30 Å range. When increasing the H₂ percentage up to 15%, the etch rate decreases to 50 Å/min. For this range of H₂ concentration,

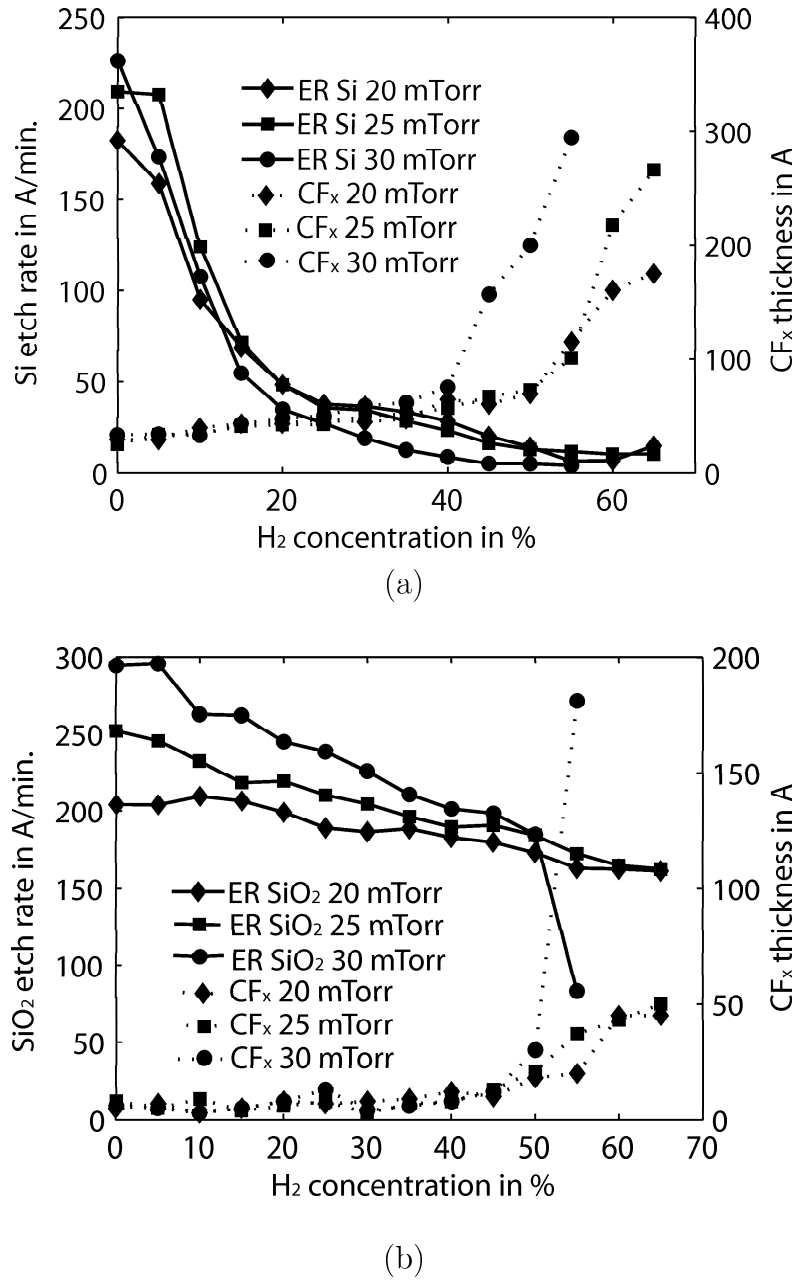


Figure C.3: Etch rate in function of H_2 concentration for (a) silicon and (b) oxide.

the fluorocarbon film thickness is constant. In poor H_2 plasma, the dissociation of CF_4 yields a large amount of fluorine atoms that are not neutralized by HF. They react with the fluorocarbon film yielding thus a high removal rate and a thin steady state fluorocarbon film. Fluorine atoms can thus reach the silicon surface easily. The silicon is then etched and forms SiF_4 after reaction with F. Increasing the H_2 concentration decreases the amount of fluorine atoms as they are neutralized by H to form HF. Between 15% and 45% H_2 , there is an other regime for silicon etching. The

silicon etch rate decreases exponentially as the fluorocarbon film thickness increases linearly. The amount of fluorine has decreased due to its neutralization by hydrogen and the removal rate of the fluorocarbon film decreases yielding a thicker film. Fluorine has to diffuse through the whole fluorocarbon layer to reach the silicon and reacts with it. Therefore is this exponential decay to observe. The third regime comes after a threshold in H_2 concentration which increases with the pressure, 45% H_2 at 30 mTorr and 55% H_2 at 20 mTorr. In this third regime the fluorocarbon thickness increases exponentially with the H_2 concentration. The calculated silicon etch rate remains stable at a value around 5 Å/min. In fact as shown in the Fig. C.2, 30 Å are etched during the time for the fluorocarbon film to be deposited and on the substrate and to act as an etch inhibiting layer. There is thus no etching of silicon under steady state conditions in this regime. In this regime the fluorine is totally neutralized by hydrogen, avoiding any removal of the fluorocarbon film and etching of silicon.

The oxide etch rate is decomposed in two regimes. In the first regime, the fluorocarbon film thickness on the oxide is less than 10 Å and the etch rate decreases linearly with the increase in H_2 concentration. The etch rate at low H_2 concentration is around 250 Å/min and increases linearly with the pressure as can be seen on the Fig. C.1. As demonstrated by Knizikkevicius, CF_3 content is high at low H_2 concentration and vanishes at high H_2 concentration [5]. The CF_2 concentration is null at low H_2 concentration and slowly increases until it reaches a maximum which corresponds to the vanishing of CF_3 species. After this maximum the CF_2 concentration decreases when further increasing the H_2 proportion due to the decrease of the CF_4 proportion. The second regime is only seen on the etching performed at 30 mTorr. The fluorocarbon layer increases exponentially as the etch decreases abruptly with an increase in the H_2 content. The combination of a low CF_2 content and a high hydrogen concentration makes the fluorocarbon film rich in inert species toward oxide. The fluorocarbon is not removed any more and sticks on the oxide surface. The CF_2 has to diffuse through the fluorocarbon film to reach the oxide, decreasing thus the etch rate. This second regime occurs at lower H_2 percentage for higher pressure. The deposition of a fluorocarbon film on the oxide surface results of a combination of high H_2 content in the plasma and long transit time of the species

in the chamber.

Etching at high H_2 percentage yields an almost infinite selective etching of oxide with respect to silicon. The silicon is not etched because of the low fluorine content and the thick fluorocarbon film deposited on silicon, while oxide is etched.

C.3.3 Conditions for anisotropic etching

A photolithography was made on the oxide samples. The samples were then etched in different conditions of pressure and plasma composition. SEM pictures were made after etching to check the anisotropy of the etching. Fig. C.4 shows the profile of the structure etched at two different hydrogen concentration for a pressure of 20 mTorr.

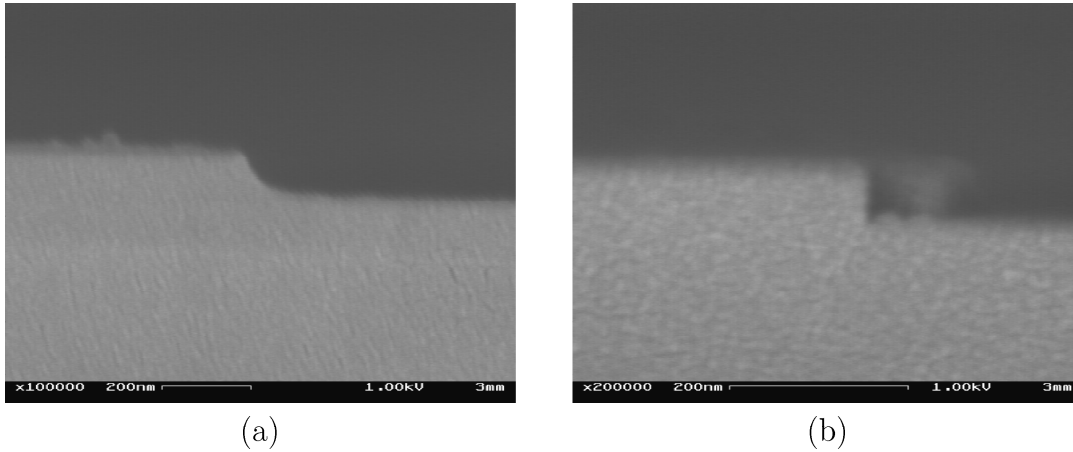


Figure C.4: RIE at 150 W RF, 60 sccm/min. total gas flow, 20 mTorr and (a) 5% H_2 (b) and 65% H_2 .

It appears clearly that the anisotropy is better at higher hydrogen concentration. The component of the ions momentum perpendicular to the vertical walls surface is very low, as the ions are accelerated toward the surface of the substrate. Due to this low energy of the ions the deposited film is removed only by reacting with the substrate. As shown previously, at low hydrogen concentration, the fluorocarbon film is very reactive with oxide and thus isotropic etching occurs. At higher hydrogen concentration, the film is less reactive to oxide. Etching occurs because energetic ions provides enough energy for CF_2 to diffuse through the fluorocarbon film and to react with the oxide. On the vertical wall, this energetic ion induced etching does not occur due to the direction of the ion flux. Oxide etching occurs only in the direction of the ions flux and not in the direction perpendicular to it. The etching

is thus highly anisotropic.

As shown in the previous section, at high hydrogen concentration, fluorocarbon starts to deposit on the oxide. As it has been shown before at low H_2 concentration the film reacts with oxide therefore is the anisotropy so bad. At high H_2 concentration, the reaction rate of the film with oxide is low, therefore without any contributions of energetic ions to enhance diffusion of CF_2 through the fluorocarbon film, which is the case on the vertical walls, the etch rate of oxide is decreased.

Fig. C.5 shows the profile of structure etched at two different pressure in a plasma performed at 50% H_2 .

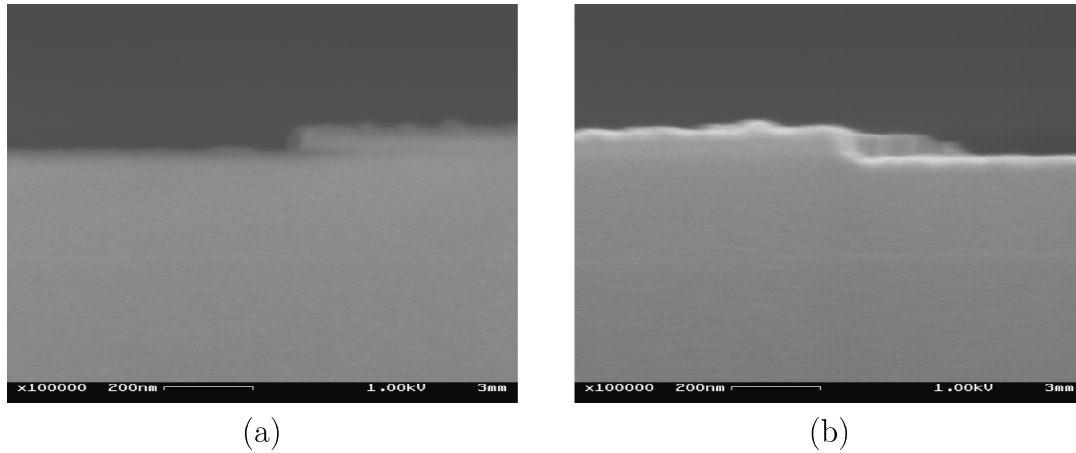


Figure C.5: RIE at 150 W RF, 60 sccm/min. total gas flow, 50 H_2 and (a) 10 mTorr (b) and 40 mTorr.

It can be seen that at lower pressure the anisotropy is better. At low pressure the mean free path of the ions in the plasma is rather long. The main component of the ion momentum will be directed by the ion flux direction. The component of the ion momentum perpendicular to the vertical walls of the etched structure will be very low. The etching will thus be enhanced in the direction of the ion flux yielding a highly selective etching of oxide. At higher pressure, the mean free path is lower, the ion suffers a large amount of collisions and the component of their momentum perpendicular to the ion flux becomes significant. Etching in the direction perpendicular to the ions flux can occurs. The etching becomes isotropic.

C.4 Conclusion

RIE of silicon and oxide have been studied in various conditions of pressure and plasma composition in CF_4 / H_2 . It has been found that high pressure or high H_2 content of the plasma yield an almost infinite selective etching of oxide over silicon. The silicon etching is inhibited by the presence of a fluorocarbon film on the surface. This fluorocarbon layer arises at lower pressure for highly H_2 concentrated plasma. The etching anisotropy of oxide has also been investigated. Lower pressure yields better results in term of anisotropy due to the longer mean free path of the ions in the plasma. The anisotropy benefits also of highly H_2 concentrated plasma, due to the composition of the fluorocarbon film deposited on oxide during etching. At high H_2 concentration the fluorocarbon film is poorer in active species and needs ion enhanced diffusion of the active species through the film to etch the oxide. On the vertical wall, the component of the ion momentum perpendicular to the surface wall being very weak, etching occurs only in the direction perpendicular to the ion flux, yielding anisotropic etching.

In order to combine high selectivity and good anisotropy, a RIE at low pressure but very high H_2 concentration is proposed. The best set of parameters is 150 W RF power, 60 sccm/min total gas flow, 65% H_2 and 20 mTorr. The oxide etch rate in these conditions is 180 Å/min, and the consumed silicon thickness during the fluorocarbon film deposition is 60 Å.

The removal of the fluorocarbon deposited on the silicon surface during etching has been characterized by spectroscopic ellipsometry. An oxygen plasma followed by a standard cleaning with HF dipping is sufficient to remove enough of the fluorocarbon film so that the remaining thickness is below the detection limit of the ellipsometer. SIMS or XPS measurement should be performed to analyze the cleanliness of the silicon after etching. Indeed, as the etch stop layer for the etching is the silicon on which the gate oxide will be grown, no contamination should remained.

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APPENDIX D

ETCHING OF SILICON ON AN OXIDE THIN FILM ETCH STOP

Sec. C presented the selective etching of oxide with respect to polysilicon, but in Sec. 1.2.3 selective RIE of polysilicon with respect to oxide is needed during the definition of the future Back Gate. The gate mask being a light field, the surface covered by the photoresist mask is negligible. The RIE needed in this case can be compared to the etching of a blank wafer as the RIE mask is the gate mask. The RIE of the polysilicon gate is a critical step as the etch stop layer is the gate oxide which is very thin which covers the active silicon which has the same composition as the film which is etched. A recipe with a high selectivity would not be sufficient for a so critical step due to the low thickness of the etch stop layer. A recipe with end point detection has thus been developed.

D.1 End point detection

The end point detection can be made by measuring in situ the etched sample, by laser ellipsometry or spectroscopic ellipsometry [1],[2]. Alternative methods are based on the detection of a change of one plasma parameter induced by a change of the etched material. The plasma is indeed composed of the feed gas and the reactions products. Depending on the type of material that is etched, the plasma does not have the same composition also when the feed gas is fixed. Changes in the plasma composition can be monitored in different ways. The most commonly used method is based on the measurement of the spectral photo-emission of the plasma [3]. The end point conditions can also be tested by monitoring changes in the fundamental and the first four harmonic components of the RF current, RF voltage, phase between RF voltage and current, RF discharge power and RF impedance [4]. Our end point detection method was based on the monitoring of the DC bias, which is the potential difference between the sample and the RF electrode induced by the plasma.

D.2 SF₆ based plasma

SF₆ is a widely used gas for silicon RIE, so it was chosen as etching gas [5]. The dissociation of the SF₆ molecules is due to the RF power injected in the chamber which creates a plasma where F atoms and SF_x compounds are present. The F atoms react with silicon and oxide according to the following equations [6], [7]:



As can be seen in the Eq. D.1 and D.2, the reaction byproducts are not the same for silicon etching as for oxide etching. The plasma being composed of the feed gas and the reaction byproducts, effective end-point detection would be possible if the reaction byproducts are not negligible in front of the feed gas. The following Sections investigate the plasma parameters for which the end point detection is optimal.

D.3 Experimental set-up

2000 Å oxide were grown on 3 inches (100) bulk silicon wafer. A 6300 Å polysilicon layer was then deposited by LPCVD at 625 °C on the half of the batch. In view of testing the anisotropy of the etching, a light field photolithography was performed on the wafer on which polysilicon had been deposited. The wafers were then etched in various process conditions. The polysilicon and oxide thicknesses were measured by spectroscopic ellipsometry before etching and after etching. The RIE reactor used was the Plasmalab OXFORD System 100 described in Sec. C. SEM imaging of the cross section were performed to check the anisotropy of the etching. The measure of the DC bias was given by the control software of the machine.

D.4 Result and discussion

D.4.1 DC bias drop

In RIE reactor the DC bias measured between the RF electrode and the wafer depends on the impedance of the plasma and thus on its composition. As seen in Eq. D.1 and D.2, the plasma composition is not the same depending on that silicon or oxide is etched. It has been observed during the RIE of an SOI wafer that the DC bias dropped of more than 20 V when the BOX was reached.

Fig. D.1 plots the DC bias in function of the etching time during the etching of an SOI wafer.

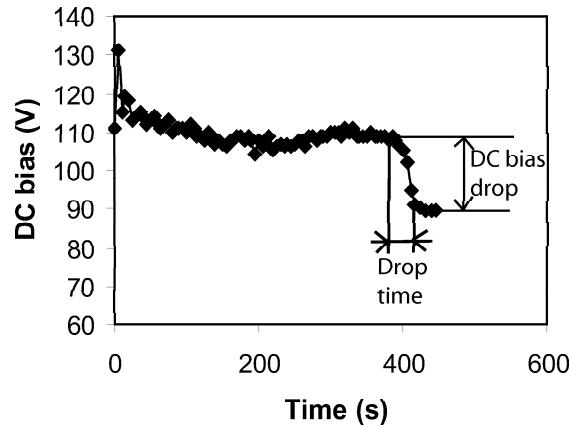


Figure D.1: DC bias in function of time

The etching was performed in the following conditions: a SF_6 gas flow of 3 sccm, a pressure of 5 mTorr, a RF power of 30W. The DC bias drop is important and sharp. Due to the very low SF_6 gas flow, one can assume that most of the SF_6 reacts. The reaction byproducts present in the plasma are thus not negligible compare to the dissociated SF_6 . The sharpness of the DC bias drop is due to the low pressure. Indeed, the lower the pressure is, the shorter the residence time of the species in the plasma chamber is. The plasma composition is then immediately modified if the etched layer has changed in composition.

In the etching conditions described above the etch rate of respectively, polysilicon and oxide were 840 Å/min, and 190 Å/min. This selectivity of 4.5 is not high enough to use the oxide as etch stop layer for polysilicon etching. We therefore tried to maximize the end point detection rather than the selectivity. For this purpose the

plasma parameters like pressure, gas flow and power have been varied in order to get better end point detection but also to conserve a good anisotropy of the etching.

D.4.2 Impact of the gas flow

To measure the impact of the gas flow, the pressure was kept constant at 5 mTorr, the power was fixed at 60 W and the gas flow was varied between 3 and 20 sccm. Fig. D.2 shows cross section of the samples etched at different gas flow.

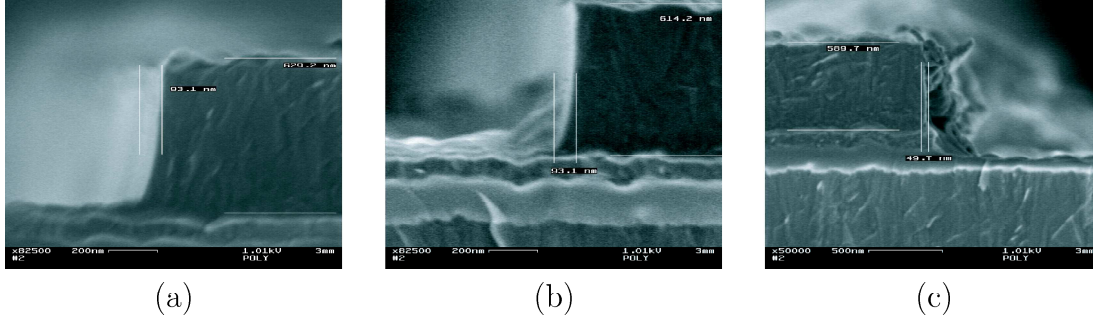


Figure D.2: SEM cross section of the sample after RIE. The photoresist mask has been removed. SF_6 gas flow of: (a) 3 sccm, (b) 10 sccm, (c) 20 sccm.

Table D.1 summarizes the anisotropy results and the end point detection sensitivity of the etching.

SF_6 sccm	in	DC bias drop in V	Drop time in s	Polysilicon etch rate in $\text{\AA}/\text{min}$	Vertical wall inclination in $^\circ$
3		15	7	120	8
10		10	9	174	7
20		3	8	180	5

Table D.1: SF_6 gas flow influence on the end point detection and anisotropy.

The anisotropy is slightly improved at higher gas flow. The etch rate seems to saturate above 10 sccm. The end point detection is lost at 20 sccm. One can conclude from the saturation of the etch rate at high gas flow that above 10 sccm the SF_6 is in excess. The F ion flux at the polysilicon surface exceeds the reaction capacity of the polysilicon in the condition of power at which the measure was performed. The plasma becomes thus mainly composed of feed gas which has not reacted. This explains why the DC bias drop becomes very small at high gas flow, the reaction by-products becoming negligible in front of the dissociated SF_6 . The

DC bias drop time does not vary significantly when increasing the gas flow. Indeed at low pressure, the residence time of the species in the chamber is very short so a change in the reaction by-products composition is immediately reflected in the plasma composition.

At 5 mTorr, and 60 W RF, a gas flow of 10 sccm ensures a very good compromise between end point detection, high etch rate, rapid DC bias drop and fairly good anisotropy of the etching.

D.4.3 Impact of the pressure

To measure the impact of the pressure, the gas flow was kept constant at 3 sccm, the power was fixed at 60 W and the pressure was varied between 5 and 25 mTorr. Fig. D.3 shows cross section of the samples etched at different pressure.

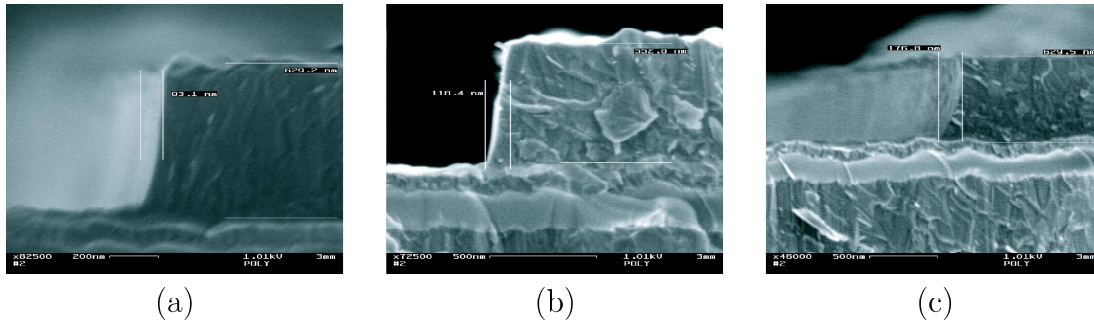


Figure D.3: SEM cross section of the sample after RIE. The photoresit mask has been removed. Chamber pressure of : (a) 5 mTorr, (b) 15 mTorr, (c) 25 mTorr.

Table D.2 summarizes the anisotropy results and the end point detection sensitivity of the etching.

Pressure in mTorr	DC bias drop in V	Drop time in s	polysilicon etch rate in Å/min	vertical wall inclination in °
5	15	7	120	8
15	13	30	150	12
25	13	40	156	12

Table D.2: Plasma pressure influence on the end point detection and anisotropy.

At high pressure the mean free path of the ions is shorter and they suffer more collisions with each other. They thus do not have a preferential direction. The etching anisotropy is then decreased. The DC bias drop does not vary significantly when increasing the pressure. As explained above, due to the low gas flow, all the

SF_6 is consumed and the plasma is composed for a significant amount of reaction by-products. We therefore observe a large drop in the DC bias. However at high pressure, the DC bias drop time increases up to 40 s. It is explained by the large residence time of the species in the plasma due to the high pressure. More time is required to wash-out the plasma chamber of the reaction by-products and to influence the DC bias value.

Increasing the pressure has a negative impact on the anisotropy, as already reported in literature [8]. Moreover, the DC bias drop time is increased which is not acceptable as the selectivity between silicon and oxide etch rate is poor. The etching must therefore be performed at low pressure.

D.4.4 Impact of the power

To measure the impact of the RF power, the gas flow was kept constant at 3 sccm, the pressure was fixed at 5 mTorr and the RF power was varied between 30 and 100 W. Fig. D.4 shows cross section of the samples etched at different pressure.

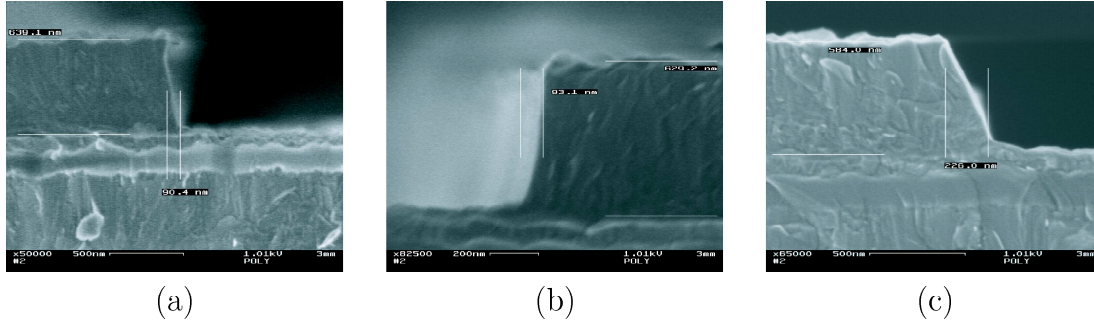


Figure D.4: SEM cross section of the sample after RIE. The photoresist mask has been removed. RF power of : (a) 30 W, (b) 60 W, (c) 100 W.

Table D.3 summarizes the anisotropy results and the end point detection sensitivity of the etching.

Power in W	DC bias drop in V	Drop time in s	polysilicon etch rate in Å/min	vertical wall inclination in °
30	6	7	84	8
60	13	7	120	8
100	17	7	132	21

Table D.3: Plasma power influence on the end point detection and anisotropy.

The etch rate increases with the RF power. It is easily understandable as more RF power means better ionization of the SF_6 molecules and thus more reactive species. It is more surprising to observe that the anisotropy is lost at high power. It can be interpreted as a very high reactivity of the feed gas which makes the chemical component preponderant compares to the physical component of the RIE. The DC bias time remains very low, due to the low pressure of the chamber. The DC bias drop increases with the etching power. However, as the DC bias also increases with the RF power (respectively 70 V, 190 V and 270 V for respective RF power of 30 W, 60 W and 100 W), the sensitivity of the end point detection is constant when varying the RF power.

At a low pressure of 5 mTorr and a gas flow of 3 sccm, a RF power ensures the best end point detection such as a fairly good anisotropy.

D.5 Conclusion

An anisotropic etching of polysilicon on oxide etch stop layer has been developed. The RIE is done in SF_6 based plasma. Our efforts were not concentrated in increasing the selectivity of the etching but in maximizing the end point detection. The end point detection was based on the measure of the DC bias between the RF electrode and the wafer. Increasing the pressure increases the DC bias drop time and decreases the anisotropy, increasing the gas flow decreases the DC bias drop amplitude but increases the anisotropy and the etch rate. Increasing the power decreases the anisotropy and increases the etch rate but has no influence on the etch DC bias drop selectivity. The Table D.4 summarizes the effects of the different parameters

Parameter	DC bias drop sensitivity	DC bias drop time	Etch rate	Anisotropy
Gas flow	$\searrow$	-	$\nearrow$	$\nearrow$
Pressure	-	$\nearrow$	$\nearrow$	$\searrow$
Power	-	-	$\nearrow$	$\searrow$

Table D.4: Plasma parameters influence on the end point detection, etch rate and anisotropy.

The best parameters, which ensure a good compromise between etch rate, anisotropy and end point detection are a pressure of 5 mTorr, a SF_6 gas flow of 10 sccm and a

RF power of 60 W.

D.6 Conclusion

The fabrication of the starting wafers for the *negative buried mask in recrystallized Si- α* and *positive buried mask in recrystallized Si- α* processes includes a step of wafer bonding between recrystallized Si- α and oxide. We demonstrated that recrystallized Si- α should be used instead of polysilicon for bonding as the surface roughness of polysilicon is too high to be bonded. We also showed that oxidation of recrystallized Si- α increases the rms surface roughness up to a value of 14 Å which is fatal for wafer bonding.

The wafer bonding pre-and post treatment were optimized to obtain the largest bonded surface. A standard cleaning / rinsing / O₂ plasma / rinsing ensures a good pre-bonding preparation. A load of 60 bars during 10 min at 60 °C followed by a 5 h anneal at 1000 °C increases significantly the bonded surface.

PECVD oxide used for the capping of the back gate before bonding to a handle wafer were characterized. The goal was to minimize their residual stress, which could avoid the bonding due to wafer bow.

Low RF power, high total gas flow or low [N₂O/SiH₄] ratio give low stress oxide, with a very high BHF etch rate and a large density of interface states and oxide traps. The stress of these oxides of poor quality increases with time immediately after deposition due to the water absorption.

High RF power, low gas flow or high [N₂O/SiH₄] give oxides of better quality in terms of BHF etch rate or interface states and traps densities but which present a higher residual stress.

The stress and interface states and traps densities of the oxide could be reduced by RTA. The BHF etch rate is also reduced after RTA.

The surface roughness of PECVD oxides is however too high to perform a wafer bonding. The roughness should be reduced by CMP and bonding tests should be performed.

Selective etching of oxide with respect to silicon which is needed for the RIE of the front gate using the revealed recrystallized Si- α buried mask has been achieved in CF_4/H_2 plasma. A pressure of 20 mTorr for a H_2 concentration of 65 % and a RF power ensure an almost infinite selective etching with a very good anisotropy. In these plasma conditions a fluorocarbon film deposits on the polysilicon surface and acts as a mask for the etching.

End point detection in RIE etching of silicon with etch stop on oxide is achieved in an SF_6 plasma. The end point detection is based on the measure of the DC bias drop. The RF power does not impact the sensitivity of the method but the best anisotropy is obtained at 60 W. A pressure of 5 mTorr ensures a short transient time for the DC bias drop. A 10 sccm gas flow is a good compromise between large DC bias drop and good anisotropy.

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