Statistical Modeling of Timing Variability due to Random Telegraph Noise in Logic Gates

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In MOS transistors of nanometer dimensions, stochastic performance variations arise not only from factors related to the fabrication process, which do not change over the lifetime of the device. These include variability of physical dimensions, doping profiles and material granularity (e.g. metal grain granularity). Besides these time-zero variability effects, other factors that lead to performance variation from one instant in time to the other start playing a significant role. Random Telegraph Noise is among these relevant time-dependent variability sources. Due to the intrinsic nature of Random Telegraph Noise, each device has a different stochastic behavior of the threshold voltage over time.. In this work we model the statistical parameters of the electrical performance variations induced by Random Telegraph Noise. The area scaling of this performance variability is detailed and discussed, supporting designers in transistors sizing towards a more reliable design. Additionally, it is demonstrated that it is possible to exploit sensitivity analysis with the analytical model presented, to implement automated, fast and accurate estimations of the time-dependent performance variability of devices, logic gates and circuits composed of MOSFETs. Monte Carlo simulations are run to corroborate the model and illustrate its applicability.

Keywords: device-to-device variation, within-device variation, random telegraph noise, time-dependent variations.

1. Introduction

MOSFETs are widely employed in integrated circuit (IC) design. Yield and reliability of these ICs depend on the variability of the transistor parameters and on noise power. Both parameter variability and low-frequency noise scale inversely with area [1]. Conversely, cost scales directly with area, and increasing area may also increase capacitive load, decreasing performance and increasing power consumption. To achieve a balance between cost, reliability, and performance, designers need comprehensive statistical models to assist with tasks like device sizing and reliability evaluation.

Sources of device variability may be time-independent (time-zero), i.e. present in fresh (new) devices, due to the discrete nature of matter and to imperfections in the fabrication process; or time-dependent, in which electrical parameters stochastically change over time. Examples of time-independent variability include line edge roughness, random dopant fluctuations, and metal (or poly) gate granularity [3]–[5]. Time-dependent variability sources include aging effects, such as bias temperature instability and hot carrier injection [6], [7], which lead to increased degradation over time, and noise sources, such as Random Telegraph Noise (RTN) [1], [8]–[11], which result in stochastic parameter variations from one instant in time to another [4, 5].

There are well-established models for the time-zero variability, which are, to a first order, inversely proportional to the square root of the area [1], [3-5]. This is well-known and widely used by circuit designers. These static sources of variability, however, are not expected to induce period jitter in ring oscillators nor time-dependent propagation delay fluctuations in logic gates, which are a result of time-varying parameters. In digital circuits, for instance, the RTN — which is due to the capture and emission of charge carriers by traps — may cause propagation delay fluctuations, impacting circuit performance and reliability. Due to the intrinsic nature of these traps, each device has a different RTN behavior. This is of particular importance for nanometer-size devices in which time-dependent within-device fluctuations are impacted by device-to-device variability [2]. Thus, to comprehensively assess reliability, the designer needs a fully stochastic model that encompasses both within-device fluctuations and device to device variations, to study their combined effects. Methodologies that combine analytical statistical analysis and deterministic circuit simulations may be computationally efficient and insightful for the circuit designer [26].

This work presents a simple analytical model to assess propagation delay jitter in digital circuits, considering both device-to-device and within-device variability due to RTN. Equations can be easily implemented in circuit simulators to estimate the impact of RTN on the time-dependent device-to-device variability from transistor level up to circuit level. We demonstrate not only that both device-to-device and within-device fluctuations due to RTN increase with area downscaling, but also that device-to-device variability increases at a stronger rate compared to within-device variability. The area dependence of the RTN-induced variability is discussed and its impact is demonstrated through circuit-level Monte Carlo simulations of logic gate delay and oscillator frequency jitter.

2. Analytical Model

A. Model Derivation

The capture and emission of a charge carrier (electron or hole) by a trap, which is the core mechanism underlying the RTN [11-15], causes discrete fluctuations of the drain current (δI_D) that may be translated into threshold voltage fluctuations, δV_T , according to $\delta I_D = g_m \, \delta V_T$, where g_m is the transconductance[1, 3, 11]. If the trap is empty, the device is assumed to be at a lower V_T and, hence, at a higher current state. If the trap is occupied, the device is assumed to be at a higher V_T and, hence, at a lower current state. Thus, when a single trap switches between its occupied and empty states, it causes a δV_T fluctuation in threshold voltage. The effect of multiple traps is cumulative, leading to a time varying threshold voltage. The variance of the threshold voltage may be seen as a threshold voltage jitter.

Figure 1 (a) shows a simulated RTN time trace on a small area nMOSFET, originating from a single trap. The threshold voltage fluctuates between two states (high-V_T and low-V_T), and the voltage difference between these two states is δV_T, which is the equivalent threshold voltage shift due to this single trap. Due to the random number of traps (as well as the random impact of each trap) and to the stochastic nature of the capture and emission processes themselves, devices that by design should be identical may exhibit very different RTN. This is exemplified in Fig. 1 (b). A statistical model must, therefore, address not only the V_T fluctuations in a device (within-device variation), but also its variability among devices that by design should be identical (device-to-device variation). The details of the numerical simulations that lead to the results shown in Fig. 1 are given in section 2.C.

Considering the *i-th* trap, δV_{Ti} is the V_T fluctuation due to the *i-th* trap. The value of the V_T fluctuation due to all traps at time t, here called $\Delta V_T(t)$, is then evaluated as the sum of the contribution of all n traps found in a device:

$$\Delta V_T(t) = \sum_{i=1}^{n} \delta V_{Ti} \, S_i(t) \, . \tag{1}$$

Under the assumption of stationary RTN, the time-averaged value of $\Delta V_T(t)$ is assumed zero, as is conventionally assumed in noise modelling. This is particularly convenient as it leads to an elegant resolution for the model equations. To obtain $\Delta V_T(t) = 0$, $S_i(t)$ is written as

$$S_i(t) = \begin{cases} -P_i(1) & if\ the\ trap\ is\ empty \\ +P_i(0) & if\ the\ trap\ is\ occupied \end{cases} \tag{2}$$

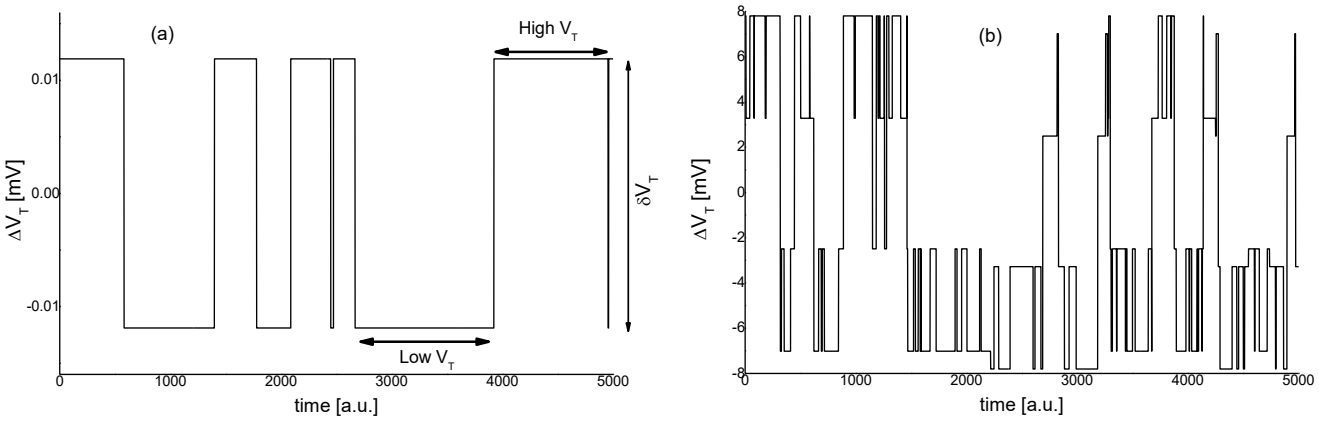

Fig. 1. Monte Carlo simulation of threshold voltage variation over time $\Delta V_T(t)$ due to Random Telegraph Noise (RTN). The first 5000 points of Monte Carlo runs for two 42.2nm x 23.1nm devices are show. Device (a) shows a single trap of small amplitude, where the threshold voltage is seen to randomly jump between a higher and a lower state. The amplitude of the V_T fluctuation is δV_T. Due to random number of traps and related parameters, devices that by design should be identical show different behavior. Device (b) shows much larger V_T fluctuation over time. Note that the formulation used here does lead to zero average value, without changing the waveform.

where $P_i(1)$ is the probability of the *i-th* trap being occupied and $P_i(0)$ is the probability of the *i-th* trap being empty. Under the assumption that the process is stationary, these probabilities are time independent, given by

$$P_i(0) = \frac{\tau_{c,i}}{\tau_{c,i}+\tau_{e,i}} \tag{3}$$

$$P_i(1) = \frac{\tau_{e,i}}{\tau_{c,i}+\tau_{e,i}} \tag{4}$$

where $\tau_{c,i}$ and $\tau_{e,i}$ are capture and emission time constants of the *i-th* trap, respectively.

Please note that this notation does not change the waveform of the RTN. It just removes the average value (DC component) of the waveform. The amplitude of the $\Delta V_T(t)$ induced by the the *i-th* trap keeps being δV_{Ti}, since $P_i(0)+ P_i(1)=1$. See Fig. 1, where this is exemplified. The average value (DC component) of the waveform does not contribute neither to jitter (V_T variation over time) nor to noise. Adding or subtracting a constant value to a random variable does not change its variance [6]. Hence, it is appropriate to remove it, besides facilitating the statistical analysis.

The $\Delta V_T(t)$ variance of a single device - i.e. the time- dependent within (intra) device-fluctuation, here called $V^2_{T\text{jitter}}$ - is evaluated from

$$V^2_{T\text{jitter}} = \overline{\Delta V_T(t)^2} - \overline{\Delta V_T(t)}^2 \,, \tag{5}$$

where $\overline{\Delta V_T(t)}$ is the first order time-average of $\Delta V_T(t)$, equal to zero by construction, and $\overline{\Delta V_T(t)^2}$ is the second order time-average of $\Delta V_T(t)$. Using (1), $\overline{\Delta V_T(t)^2}$ is evaluated as

$$\overline{\Delta V_T(t)^2} = \sum_{i=1}^{n} {\delta V_{Ti}}^2 \overline{S_i(t)^2} \,. \tag{6}$$

From [13], (6) can be rewritten as

$$\overline{\Delta V_T(t)^2} = \sum_{i=1}^{n} {\delta V_{Ti}}^2 \frac{\beta_i}{(1+\beta_i)^2} \,, \tag{7}$$

where $\beta_i = \tau_{c,i}/\tau_{e,i}$.

When an ensemble of devices is considered, however, devices that should be identical by design may exhibit very different

Table 1
Parameter Values Used in Monte Carlo Simulations

Area (nm^2)	E[n]	E[δV_T] (mV)
484	0.774	19.0
725	1.17	12.7
975	1.56	9.44
1937	3.10	4.75

RTN time traces, since the number of traps in each device as well as the characteristics of these traps (i.e. trap impact and time constants) are random. Consequently, $V_{T\text{jitter}}^2$ for any given device from the ensemble is random. The expected value of the ensemble of $V_{T\text{jitter}}^2$ of different devices is estimated as

$$\mathrm{E}[V_{T\text{jitter}}^2] = \mathrm{E}[n]\mathrm{E}[A^2] \,, \tag{8}$$

where A is the amplitude contribution of a trap to the threshold voltage variance, being $\mathrm{E}[A^2]$ evaluated as [11] [13]

$$\mathrm{E}[A^2] = \mathrm{E}\left[\delta V_T{}^2 \frac{\beta}{(1+\beta)^2}\right] , \tag{9}$$

and E[n] is the average number of active traps in device.

To fully grasp the randomness of the threshold voltage variation due to RTN, the ensemble variance of $V_{Tjitter}^2$ can be evaluated as [13]

$$\mathrm{Var}[V_{T\text{jitter}}^2] = \mathrm{E}[n]\mathrm{E}[A^4] \tag{10}$$

assuming that the number of traps is Poisson-distributed.

$V_{Tjitter}^2$ is the RTN noise power. Thus, $\mathrm{E}[V_{T\text{jitter}}^2]$ is the expected noise power from an ensemble of devices, whereas $Var[V_{Tjitter}^2]$ is the noise power variance of an ensemble of devices.

If *i)* E[n] is assumed proportional to device area (WL); *ii)* $\mathrm{E}\left[\delta V_T{}^2\right]$ is assumed inversely proportional to the device area squared, $1/(WL)^2$; and *iii)* β is assumed area independent [11, 19, 27], then, from (8), the expected value of $V_{T\text{jitter}}^2$ is inversely proportion to device area, $1/(WL)$, and the variance of $V_{T\text{jitter}}^2$ is inversely proportional do the cube of the device area, $1/(WL)^3$. Hence, the normalized standard deviation is inversely proportional to square root of the area:

$$\frac{\sqrt{\mathrm{Var}[V_{T\text{jitter}}^2]}}{\mathrm{E}[V_{T\text{jitter}}^2]} = \frac{\sqrt{\mathrm{E}[n]\mathrm{E}[A^4]}}{\mathrm{E}[n]\mathrm{E}[A^2]} \propto \frac{1}{\sqrt{WL}} \tag{11}$$

Area downscaling, therefore, not only increases the expected value of $V_{T\text{jitter}}^2$, i.e., the within-device time-dependent fluctuations, but also increases the variability of $V_{T\text{jitter}}^2$, i.e. the device-to-device time-dependent variations. This is a significant challenge for circuit designers. Consider two transistors supposedly identical by design: due to the random number of traps and related parameters, one may exhibit a small V_T fluctuation over time, whereas the other may exhibit a much larger V_T fluctuation over time, as exemplified in Fig. 1.

The works [13, 27] related the statistics of the RTN power with the statistics of the $1/f$ noise spectral density. The expected value of $V_{T\text{jitter}}^2$ is related to the expected value of the *1/f* noise spectral density. Equation (8) above has the same form and same area dependence as the equation for the expected *1/f* noise PSD, as given by (34) in [11]:

$$\mathrm{E}[S(f)] = \frac{\mathrm{E}[A^2]N_{dec}WL}{f} \quad (12)$$

where $ln(10)N_{dec}$ is trap density per unit area and frequency decade [3]. Hence, the average number of traps per device is proportional to $N_{dec}\times W\times L$.

Both equations (8) above and (34) in [11] are proportional to $\mathrm{E}[A^2]$ and proportional to the average number of traps for a given device size. This is expected, since average value of $V_{T\mathrm{Jitter}}^2$ due to RTN is related to the average $1/f$ noise due to RTN. Also, similarly to $1/f$ noise (frequency domain) traps that have maximum contribution to $V_{T\mathrm{Jitter}}^2$ (time domain) are the ones with capture time similar to the emission time, i.e., $\beta \approx 1$.

Similarly, the variability of $V_{T\mathrm{Jitter}}^2$ among devices is related to the variability of $1/f$ noise power spectral density. Equation (10) above has the same form and same area dependence as the equation for $1/f$ noise power variability among devices, as given by (38) in [11]:

$$\mathrm{Var}[S(f)] = \frac{2\mathrm{E}[A^4]N_{dec}WL}{\pi^2 f^2} \quad (13)$$

Both equations (10) above and (38) in [11] are proportional to $\mathrm{E}[A^4]$ and proportional to the average number of traps in a given device size. This is expected, since $V_{TJitter}^2$ variability among devices (and variability of jitter of signals) due to RTN is related to the variability of 1/f noise among devices.

Equation (34) in [11] is for the average value of the noise spectral density in an ensemble of devices designed to be identical, while (7) above is for the average $V_{T\mathrm{Jitter}}^2$. Equation (38) in [11] is for the variance of noise spectral density among devices, while (10) above is for the variance of $V_{T\mathrm{Jitter}}^2$ among devices designed to be identical.

As seen in *1/f* noise, not only is the expected (average) value of $V_{T\mathrm{Jitter}}^2$ increasing with device area downscaling, but also its variability among devices strongly increases with device downscaling. Each device has a random number of traps. And traps have random amplitudes and random time constants. The threshold voltage variation over time of a device is given by its particular number of traps and related parameters. Number of traps and related parameters vary among devices. The smaller the device size, the more the threshold voltage variation over time differs among devices that by design should be identical. In the same way, the smaller the device size, the more the $1/f$ noise power differs among devices that by design should be identical.

B. Monte Carlo Simulations

Monte Carlo simulations were performed at the device (transistor) level to confirm the behavior predicted by the analytical model and illustrate model applicability. For each transistor, the time evolution of the threshold voltage is simulated. Please note that number of traps per transistor is a random variable. The V_T fluctuation induced by a single trap and trap time constants are also random variables.

The MC simulations were performed under the following assumptions: *i)* charge trapping and de-trapping are stochastic events governed by characteristic time constants, which are uniformly distributed on a log scale (no relation between device area and time constants is assumed); *ii)* the number of active traps is assumed to be Poisson distributed, and the average number of active traps in a device is proportional to the device area; and iii) the V_T fluctuation induced by a single trap is a random variable, exponentially distributed, being the average amplitude inversely proportional to device area, which is in agreement to experimental data [1], [11], [14], [15], and also with TCAD analysis [16]. Please note that these assumptions are only required to perform the MC simulations, both at device level (this section) and circuit level (next section). The analytical model derived in the previous section is valid for any statistical distribution of the V_T fluctuations (i.e. no particular distribution is assumed in model derivation). The same applies to the methodology presented in the next section for jitter evaluation at the gate and circuit level. The MC simulations at device (transistor) level were performed with R [29], while the circuit level transient simulations, presented in the next section, were performed with our in-house modified version of NGSPICE [23].

Due to the random characteristics of traps and the devices' random characteristics, each trap has a distinct impact on the threshold voltage, δV_T . Excellent investigation of the expected impact among different traps, $\mathrm{E}[\delta V_T]$, has been done in the literature, with typical values being, approximately, 2 times higher than the classical value given by a single charge at the dielectric interface [15], i.e., q/C_{ox}, where C_{ox} is the gate oxide capacitance (in Farads) in inversion. Therefore, in this work we approximate $\mathrm{E}[\delta V_T] = 2q/C_{ox}$. For the 22 nm node case study technology [17], random values of δV_T were calculated assuming

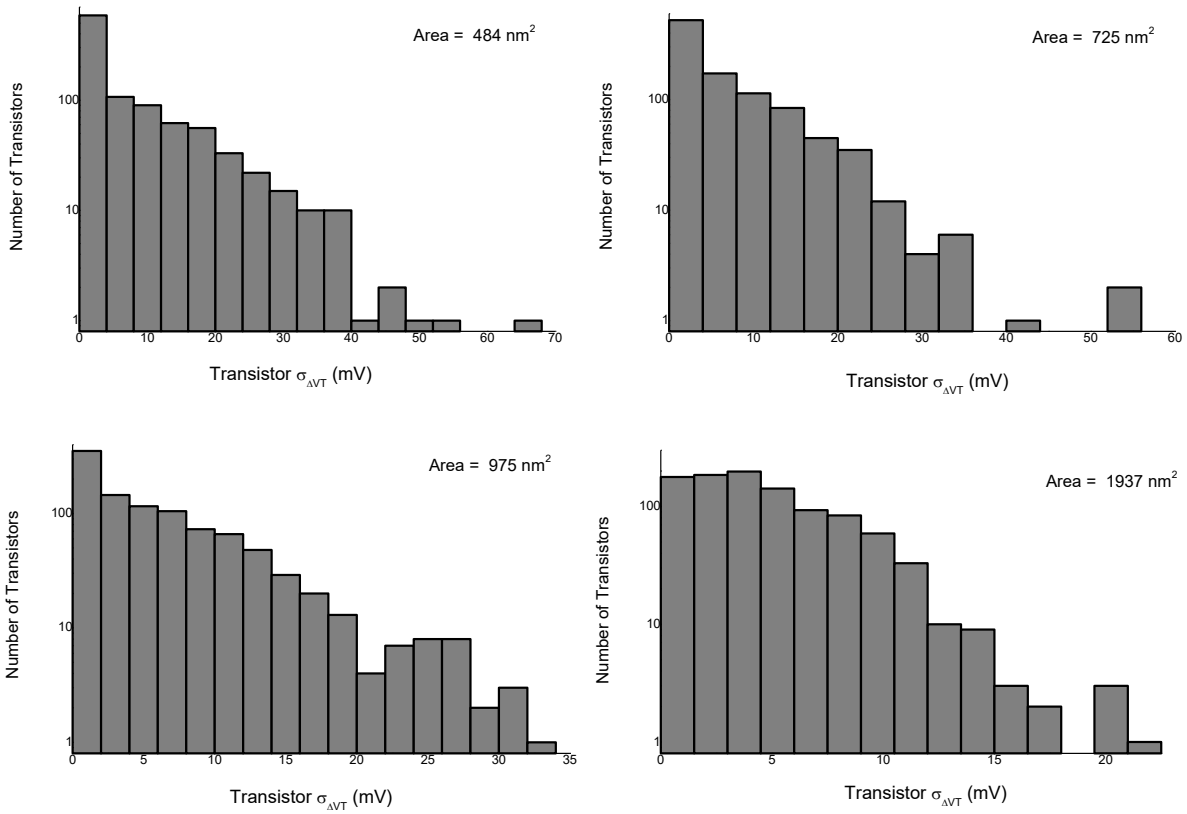

Fig. 2. Standard deviation of the threshold voltage ($\sigma_{\Delta V_T} = \sqrt{V^2_{T\text{jitter}}}$) estimated from time traces obtained from transistor-level Monte Carlo simulation of the four different devices sizes. 1,000 devices were simulated for each device area, resulting in 1,000 time traces and, thus, 1,000 randomly distributed standard deviations.

E[δV_T] = 9.2μVμm^{-2}/(WL). For the calculation of average number of active traps per device, E[n], an active defect density of 1.5×10^{11} cm^{-2} is assumed [1], [14]. Same trap density and trap amplitude are assumed for both p- and n-MOSFETs.

Table 1 shows the transistor sizes used in the Monte Carlo simulations, as well as the respective average number of active traps per device E[n] and the expected V_T fluctuation due to a trap E[δV_T].

For each device size, 1,000 Monte Carlo simulations were performed. For each simulation, the size of the time series is $3x10^5$ points. At each simulation time step, trap transition probability (capture or emission event) is evaluated according to the trap time capture or emission time constant. As an example, figure 1 shows the first 5000 points of Monte Carlo runs for two 42.2nm × 23.1nm devices. Notice that each device has its own $V^2_{T\text{jitter}}$; the device in Fig. 1(a) displayed $V^2_{T\text{jitter}} = 150\ \mu\text{V}^2$, whereas the device in Fig. 1(b) displayed a much larger $V^2_{T\text{jitter}} = 31.6\ \text{mV}^2$, illustrating that $V^2_{T\text{jitter}}$ (i.e. noise power) is, itself, a random variable.

Figure 2 shows the histograms of the Monte Carlo simulations for the four different device sizes. Each histogram displays $V_{T\text{jitter}} = \sqrt{V^2_{T\text{jitter}}}$ - the empirical standard deviation of the time-dependent fluctuations, $\Delta V_T(t)$ - of 1000 transistors of same size. As discussed in the previous section, due to the random number of traps in device, as well as random trap characteristics, $V^2_{Tjitter}$ is different for each device. Therefore, it is necessary to address the question of how the V_T fluctuation varies between devices that by design should be identical (i.e., have the same W×L). This is achieved by looking at the normalized standard deviation of $V^2_{T\text{jitter}}$, given by equation (11).

Table 2
Transistor Time Dependent V_T Variation
Results From Monte Carlo Simulations and Analytical Model

Area (nm^2)	$E[V_{Tjitter}^2]$ (mV^2)		Normalized Standard Dev.	
	Monte Carlo	Model	Monte Carlo	Model
484	133	139	2.69	2.80
725	94.0	94.4	2.28	2.27
975	70.2	69.5	1.92	1.96
1937	33.8	34.9	1.43	1.40

Table 2 shows the average $V_{T\text{jitter}}^2$ (i.e. average noise power) calculated from Monte Carlo runs and from (8), as well as the normalized standard deviation of $V_{T\text{jitter}}^2$ calculated from Monte Carlo runs and from (11).

Notice that the analytical calculations, (8) and (10), require the second and fourth moments of A. Under the assumption that the RTN power is primarily due to traps whose capture and emission time constants are approximately equal ($\tau_c \approx \tau_e$), β is approximately equal to 1, which results in $E[A^2] \approx E[\delta V_T^2]/4$ and $E[A^4] \approx E[\delta V_T^4]/16$. Additionally, by assuming δV_T exponentially distributed, the second and fourth moments can be further simplified to $E[\delta V_T^2] \approx 2E[\delta V_T]$ and $E[\delta V_T^4] \approx 24E[\delta V_T]$ [19]. We reinforce, however, that the analytical model is suited for any distribution of trap impacts, provided the second and fourth moments are known.

The results show good agreement between MC (Monte Carlo simulation) and analytical model.

It is also interesting to observe the shape of the distribution. As seen in Fig. 2, the distributions are clearly non-Gaussian, with variability increasing as the device area scales down. This behavior has been experimentally reported, but analytical modeling was lacking (see, for instance, [8]–[10]). Moreover, this behavior follows that observed in frequency domain. In [11] it has been observed that the distribution of noise power among devices is clearly non-Gaussian and asymmetrical for the smaller devices. Please see Fig. 7 in [11] and related discussion.

3. Circuit Level Analysis

A. CMOS Logic Gate Delay

Estimating delay through a CMOS logic gate is crucial in VLSI design. As dimensions scale down to nanometers, gate delay becomes random, with time-dependent variability playing a significant role [1, 4, 5, 22]. Hence, a pertinent question is how to estimate the uncertainty of a logic gate delay under time-dependent variability sources, such as RTN. The threshold voltage fluctuation model developed in the previous section and the classical error propagation formula provides means to compute such uncertainty estimate.

In order to evaluate the impact of RTN induced V_T fluctuation on gate delay, we study the delay through a CMOS inverter loaded by the capacitance of a similar inverter. Next, we study the jitter in ring oscillators composed by these inverters. The applicability of the methodology here presented is not limited to inverters and ring oscillators. Inverters and ring oscillators are used as case study to illustrate the applicability of the proposed methodology and simulation approach.

The switching of the states of traps in transistors change the drive (drain) current, changing the propagation delay. If a trap is empty, we consider that the device is at a lower V_T (hence higher drain current), leading to a shorter propagation delay. If a charge carrier is trapped, we consider the device is at a higher V_T (hence lower drain current), leading to a longer propagation delay. In summary, trap switching causes time-dependent variability (jitter) of propagation delay.

The average propagation delay (t_p) of a logic inverter can be estimated as $t_p = (t_{pHL} + t_{pLH})/2$, where t_{pHL} and t_{pLH} are the propagation delays of the high-to-low and low-to-high transitions, respectively.

Using propagation of uncertainty [20], the variance of the propagation delay of an inverter can be estimated using

$$\sigma_{t_p}^2 = \frac{1}{4}\left(\frac{\partial t_{pHL}}{\partial \Delta V_{T_N}}\right)^2 V_{T\text{jitter},N}^2 + \frac{1}{4}\left(\frac{\partial t_{pLH}}{\partial \Delta V_{T_P}}\right)^2 V_{T\text{jitter},P}^2 \quad (14)$$

where σ_{t_p} is the delay jitter; $V_{Tjitter,N}^2$ and $V_{Tjitter,P}^2$ are the threshold voltage variances for the n- and p-MOSFETs, respectively, as discussed in the previous section. The derivatives may be very cheaply evaluated numerically with the aid of circuit level (Spice) deterministic simulation, as in [21].

As discussed in the previous section, $V_{T\text{jitter}}^2$ (i.e. noise power) itself is a random variable. Therefore, $\sigma_{t_p}^2$ is different among

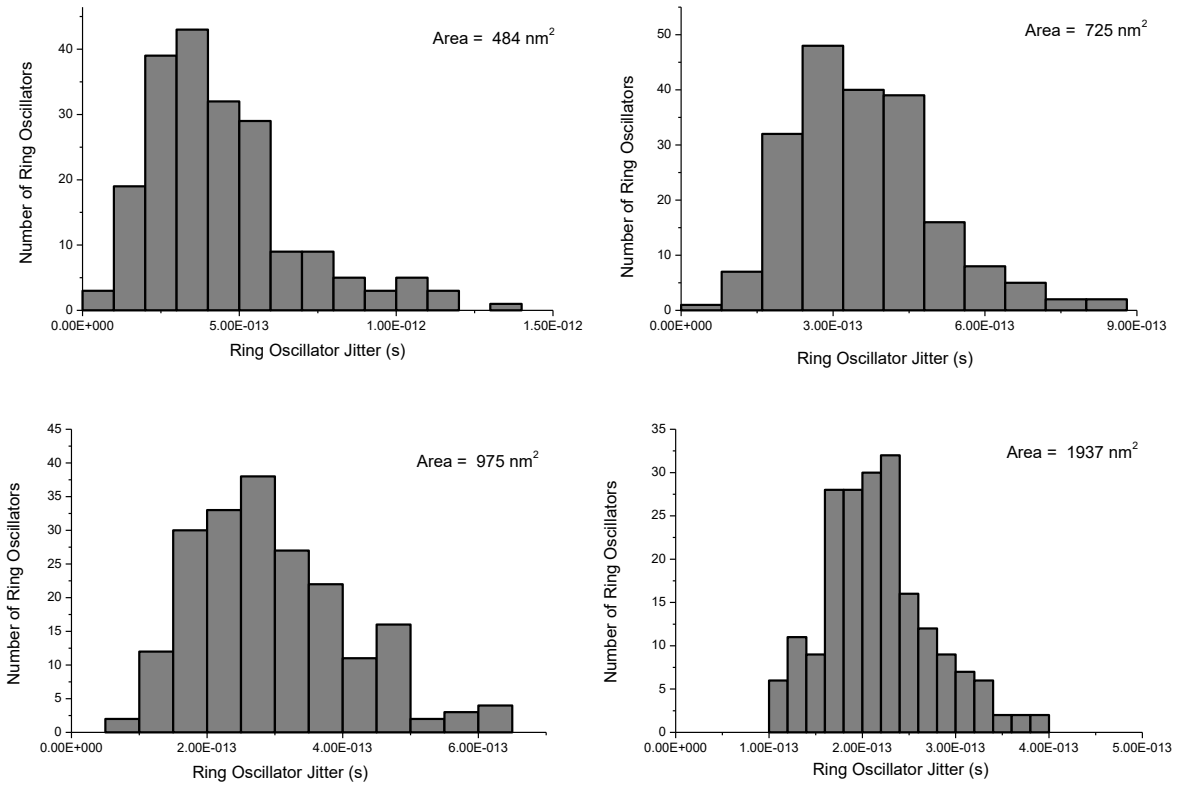

Fig. 3. Estimated ring oscillator jitter, σ_{Trosc}, from time traces obtained through Monte Carlo simulation of the four different device sizes.

inverters that are supposedly identical by design. The expected value of $\sigma_{t_p}^2$ for the ensemble of inverters is

$$\mathrm{E}\left[\sigma_{t_p}^2\right] = \frac{1}{4}\left(\frac{\partial t_{pHL}}{\partial \Delta V_{T_N}}\right)^2 \mathrm{E}\left[V_{T\mathrm{jitter},N}^2\right] + \frac{1}{4}\left(\frac{\partial t_{pLH}}{\partial \Delta V_{T_P}}\right)^2 \mathrm{E}\left[V_{T\mathrm{jitter},P}^2\right] \tag{15}$$

and the variance of $\sigma_{t_p}^2$ is

$$\mathrm{Var}\left[\sigma_{t_p}^2\right] = \frac{1}{16}\left(\frac{\partial t_{pHL}}{\partial \Delta V_{T_N}}\right)^4 \mathrm{Var}\left[V_{T\mathrm{jitter},N}^2\right] + \frac{1}{16}\left(\frac{\partial t_{pLH}}{\partial \Delta V_{T_P}}\right)^4 \mathrm{Var}\left[V_{T\mathrm{jitter},P}^2\right] \ , \tag{16}$$

B. Jitter in Ring Oscillators

Once the delay jitter of an inverter has been derived, one can derive the jitter in circuits composed of inverters. In this section, a case study of a ring oscillator is presented. The oscillation period of a ring oscillator is given by

$$T_{\mathrm{Rosc}} = 2\sum_{i=1}^{M} t_{p,i} \ , \tag{17}$$

where *M* is the number of stages.

From uncertainty propagation, the variance of the oscillation period can be calculated as

$$\sigma_{T\mathrm{rosc}}^2 = \sum_{i=1}^{M} 4\left(\frac{\partial T_{\mathrm{Rosc}}}{\partial t_{p,i}}\right)^2 \sigma_{t_{p,i}}^2 \ , \tag{18}$$

where $\sigma_{t_{p,i}}$ is the delay jitter of the *i-th* inverter. From the previous section, seemly identical inverters from an ensemble may

Table 3
Ring Oscillator Period Jitter
Results from Monte Carlo Simulations and Error Propagation Model

Area (nm^2)	$E[\sigma^2_{Trosc}]$ (s^2) Monte Carlo	Model	Normalized Standard Dev. Monte Carlo	Model
484	2.50E-25	2.03E-25	1.16	0.93
725	1.49E-25	1.36E-25	0.80	0.74
975	1.02E-25	1.01E-25	0.77	0.65
1937	5.03E-26	5.04E-26	0.53	0.43

exhibit different delay jitter due to the inherent nature of the RTN; thus, σ^2_{Trosc} is itself a random variable, and σ^2_{Trosc} is different among oscillators that are supposedly identical by design. Therefore, the expected value of $\sigma^2_{T\mathrm{rosc}}$ is estimated as

$$\mathrm{E}[\sigma^2_{T\mathrm{rosc}}] = 4M\mathrm{E}\left[\sigma^2_{t_p}\right]. \tag{19}$$

Substituting (15) in (19) leads to

$$\mathrm{E}[\sigma^2_{T\mathrm{rosc}}] = M\left(\frac{\partial t_{pHL}}{\partial \Delta V_{T_N}}\right)^2 \mathrm{E}\left[V^2_{T\mathrm{jitter},N}\right] + M\left(\frac{\partial t_{pLH}}{\partial \Delta V_{T_P}}\right)^2 \mathrm{E}\left[V^2_{T\mathrm{jitter},P}\right], \tag{20}$$

which has a similar form to (30) in [28], derived using noise power evaluation in frequency domain.

Similarly, the variance of $\sigma^2_{T\mathrm{rosc}}$ for an ensemble of oscillators is estimated as

$$\mathrm{Var}[\sigma^2_{T\mathrm{rosc}}] = M\left(\frac{\partial t_{pHL}}{\partial \Delta V_{T_N}}\right)^4 \mathrm{Var}\left[V^2_{T\mathrm{jitter},N}\right] + M\left(\frac{\partial t_{pLH}}{\partial \Delta V_{T_P}}\right)^2 \mathrm{Var}\left[V^2_{T\mathrm{jitter},P}\right]. \tag{21}$$

From (20) and (21), $\mathrm{E}[\sigma^2_{T\mathrm{rosc}}]$ scales proportionally to $1/(WL)$, in the same way as $\mathrm{E}[V^2_{T\mathrm{jitter}}]$, and $\mathrm{Var}[\sigma^2_{T\mathrm{rosc}}]$ scales proportionally to $1/(WL)^3$, in the same way as $\mathrm{Var}[V^2_{T\mathrm{jitter}}]$. Hence, the normalized standard deviation, $\sqrt{\mathrm{Var}[\sigma^2_{T\mathrm{rosc}}]}/\mathrm{E}[\sigma^2_{T\mathrm{rosc}}]$, scales as $1/\sqrt{WL}$.

C. Monte Carlo Simulations

To validate the proposed analytical model, circuit simulations were performed. Monte Carlo simulations were run using a modified set of BSIM4 equations [18]. The trap kinetics were implemented within the BSIM4 model, producing time-varying threshold voltage fluctuations for each transistor, simulating the RTN mechanisms. The transient simulation is performed using NGSPICE [23]. The stochastic capture and emission events of the traps are evaluated along the transient simulation, with the same assumptions used for the Monte Carlo simulations of single transistors, as described in section 2 above (i.e., the same algorithm is implemented in NGSPICE for the transient simulation, which is written in C programming language). The transistor model employed is the Predictive Technology Model for the 22-nm node [17].

To allow direct comparison between the jitter for the different sizing, transistors where sized so that all inverters show the same propagation delay, regardless of area. Both p- and n-MOSFETs were designed with same area. The four MOSFET sizes ($W\times L$) used were 22nm *x* 22nm (Area=484nm^2), 32.4nm *x* 22.4nm (Area=725nm^2), 42.2nm *x* 23.1nm (Area=975nm^2) and 79.4nm *x* 24.4nm (Area=1937nm^2). The case study ring oscillator is composed of 5 inverters. All ring oscillators show same period of 28ps, regardless of sizing (transistor area).

In the presence of time-dependent variability introduced by RTN, it is necessary to run the transient simulation for a large number of oscillation periods, since due to trap activity each oscillation period may be different. The period jitter of each oscillator is evaluated as the variance of its oscillation period over 1500 periods. Furthermore, since ring oscillators designed to be identical will be composed of transistor with random number of traps with random parameters, a significant number of

ring oscillators of each size needs to be simulated. For each size (area), 200 oscillators are simulated. Oscillators of a given area are identical, except for the random number of traps and random trap activity. This results in a computationally expensive simulation. Figure 3 shows the results of Monte Carlo simulation of ring oscillator period jitter (considered as the standard deviation of the period).

The values obtained in the Monte Carlo simulations are compared to the analytical model in Table 3. To evaluate (18), first σ_{t_p} is evaluated using (14). The derivatives of propagation delay with respect to V_{T} are numerically evaluated by perturbating V_{T} in circuit simulation. $\mathrm{E}[V^2_{T\mathrm{jitter}}]$ is as obtained from (7), whose values are listed in Table 2.

Numerically obtaining the derivatives of propagation delay with respect to V_{T} requires two cheap deterministic circuit simulations of a single inverter (with no trap activity) for each transition (t_{pHL} and t_{pLH}). This is by many orders of magnitude more computationally efficient than running numerous MC trials.

The results show reasonable agreement between MC (Monte Carlo simulation) and analytical model. In agreement to the model here presented, it is seen that the expected period jitter ($\mathrm{E}[\sigma^2_{T\mathrm{rosc}}]$) increases with $1/(WL)$, while the variability of period jitter ($\mathrm{Var}[\sigma^2_{T\mathrm{rosc}}]$) increases with $1/(WL)^3$. This increase in variability with decreasing device size has been also experimentally observed. In [24], authors observed that by slightly increasing the transistor size more than 50% reduction of ring oscillator frequency uncertainty can be achieved. Ring oscillator uncertainty was related to transistor delay uncertainty due to RTN.

The results presented in Table 3 for the normalized standard deviation show weaker agreement to MC results for the smallest areas. This may be due to intrinsic accuracy of MC and error propagation. Better frameworks could be used. However, the development of a compact methodology must account for the amount of effort required to parameterize the observed effects. This is an inherent limitation of compact modeling, in which accuracy is exchanged for time. Error propagation and Monte Carlo simulations are techniques widely employed in commercial tools. For a discussion on the limitations of error propagation for automated analysis of time-dependent circuit variability, see, for instance [25].

4. Conclusion

This work advances the state of the art on the modeling of the time-dependent random variability induced by RTN, providing analytical models for the time-dependent within-device and device-to-device threshold voltage fluctuations produced by RTN. Not only the average (expected) value is addressed, but also the variability. Besides analytical modeling, Monte Carlo simulations are run and corroborate the analytical model. The area scaling of RTN-induced time-dependent threshold voltage fluctuation and its variability among devices is detailed and discussed, aiming to support circuit designers in transistor sizing towards a more reliable design. Additionally, we leverage an analytical approach, alongside propagation of uncertainty and sensitivity analysis based on deterministic SPICE simulations, to estimate the impact of the time dependent threshold voltage fluctuations on logic gate delay variability, as well as ring oscillator period jitter variability, avoiding costly Monte Carlo Simulations. This methodology allows for the estimation of the RTN impact on the time-dependent device-to-device variability from transistor-level up to circuit-level.

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