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High quality silicon-based substrates for microwave and millimeter wave passive circuits

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ABSTRACT

Porous silicon substrate is very promising for next generation wireless communication requiring the avoidance of high-frequency losses originating from the bulk silicon. In this work, new variants of porous silicon (PSi) substrates have been introduced. Through an experimental RF performance, the proposed PSi substrates have been compared with different silicon-based substrates, namely, standard silicon (Std), trap-rich (TR) and high resistivity (HR). All of the mentioned substrates have been fabricated where identical samples of CPW lines have been integrated on. The new PSi substrates have shown successful reduction in the substrate's effective relative permittivity to values as low as 3.7 and great increase in the substrate's effective resistivity to values higher than 7 kΩ cm. As a concept proof, a mm-wave bandpass filter (MBPF) centred at 27 GHz has been integrated on the investigated substrates. Compared with the conventional MBPF implemented on standard silicon-based substrates, the measured S-parameters of the PSi-based MBPF have shown high filtering performance, such as a reduction in insertion loss and an enhancement of the filter selectivity, with the joy of having the same filter performance by varying the temperature. Therefore, the efficiency of the proposed PSi substrates has been well highlighted.

1. Introduction

At the dawn of 2020 the deployment of Internet of Thing (IoT) will become a reality. The concretization of IoT is unsurprisingly based on the concept of sensing network in which the sensing nodes (SN) will attract major interest towards the success of this challenge. A massive production of these SNs will emerge, and industrials will need to tradeoff between efficiency and cost to keep the competiveness of their products. In fact, to accomplish this tradeoff, a suitable choice of the components should be performed, the use of emergent active devices is highly recommended [1], and the quality factor of passive components should be accounted for [2]. One of the most important aspects impacting the performance of these components is the good choice of the substrate on which the SN is integrated. Indeed, bulk silicon is the most widely used substrate for the integrated circuits in the semiconductor industry. However, due to its high electrical conductivity and high-frequency losses, bulk silicon substrate suffers from significant losses at high frequencies which drastically reduce the performance of RF passive and active devices [2]. This degradation becomes more severe at millimeter-wave (mm-wave) frequencies.

Various Si-based substrates compatible with Silicon-on-Insulator (SOI) CMOS process have been proposed to overcome the problem of performance degradation such as High Resistivity SOI (HR-SOI), Trap-Rich Silicon (TR-Si) [3–7] as well as nanocrystalline porous silicon which is a very promising alternative to bulk silicon substrates for the fabrication of low cost RF circuits [8]. Porous Si exhibits low permittivity, whose value depends on the porosity between those of air ($\varepsilon_r = 1$) and that of silicon ($\varepsilon_r = 11.7$) [9]. It can be fabricated from a Si wafer by electrochemical dissolution of bulk crystalline silicon. The main advantages of PSi are its very low cost and its CMOS process compatibility enabling the integration of both passive and active devices on the same substrate and thus the development of a System-on-Chip (SoC). Furthermore, most investigated porous silicon substrates for RF applications are mesoporous made from n-type [9] and p+-type doped silicon owning a nominal resistivity lower than 20 mΩ cm [8–14]. In fact, many PSi-based materials were found suitable for a wide range of integrated circuits with high performance, as it has been demonstrated in previous studies [15–18].

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In the current study, p-type silicon substrates with resistivities of (1–10 Ω cm) and (5–20 mΩ cm) are used to realize two variants of PSi through an accurate fabrication methodology. The realized substrates own small relative permittivity and high effective resistivities, such parameters are required for RF and mm-wave applications as they offer decreased crosstalk levels and capacitive parasitic through the substrate between neighbouring circuit nodes. The introduced PSi substrates have been compared, through RF measurements, with three Si-based substrate technologies for RF passive device integration, namely, standard silicon, high resistivity (HR) silicon, trap-rich HR-Si. The performed comparison has emphasized the high insulating properties and quality factor of the proposed PSi substrates offering thus a low cost alternative to integrate RF passive circuits.

Aiming to validate the usefulness of the proposed PSi substrates for the integration of millimeter-wave passive circuits, a 27 GHz bandpass filter was integrated on. Indeed, the spectrum around 27 GHz is one of the bands retained for the 5th generation wireless communication that will constitute the core network to build up IoT [19,20]. Thus, it is pertinent to investigate the substrate impact on the electrical performance of mm-wave bandpass filters. The retained topology for this work is an interdigital filter under CPW configuration, which has already been implemented in standard silicon-based 0.18-μm CMOS [21]. The measurements of the fabricated filters have shown interesting electrical performance. Moreover, the mentioned features are kept unchanged even with submitting the filter under test to temperature variation. Consequently, the proposed PSi substrates are well suitable for millimeter-wave circuits integration.

2. Integration of CPW lines on Si-based substrates

A. *Si-based substrates preparation*

Five types of substrates are fabricated and investigated in this study: standard p-type silicon Std (ρ = 1–10 Ω cm), high-resistivity silicon HR (ρ > 4 kΩ cm), trap-rich HR-Si (TR), and two porous Si substrates. The characteristics of the five substrates are summarized in Table 1.Trap-rich HR-Si substrate consists of n-type HR-Si wafer with a nominal resistivity of 10 kΩ cm, and a layer of 500 nm-thick trap-rich poly-Si deposited through low pressure chemical vapor deposition (LPCVD). The two porous Si substrates were fabricated, respectively, from standard p-type (100) silicon wafer (ρ = 1–10 Ω cm, PSi-S) and highly doped p-type Si (ρ = 5–20 mΩ cm, PSi-M).

The sample PSi-M with 50 μm thickness of a mesoporous layer is obtained after anodization of p-type Si (ρ = 5–20 mΩ cm) in (50%) HF: ethanol (1:1), at current density of 75 mA/cm^2 during 40 min (Fig. 1). The pore size is 10 nm and the estimated porosity is about 50%, which was calculated by weighting the sample before anodization, after anodization and after etching of the PSi layer. The pores sizes of samples were measured by a field emission scanning electron microscope (FE-SEM, GEMINI Ultra 55 Zeis) under 3keV electron acceleration voltage.

Table 1
Characteristics for Si-based substrates.

Substrate	Thickness (μm)	Nominal resistivity (Ω-cm)	Porous thickness (μm)	Z_c	ε_{eff}	α (dB/mm)	Q@26/60 GHz
Std	381 ± 20	1–10	–	48	11.7	3.8	2.1/4.9
HR	725 ± 25	>4 k	–	50	9.6	1.6	4.5/10.5
TR	725 ± 25	>10 k	–	53	9.3	0.35	20.6/47.5
PSi-S	381 ± 20	1–10	50	80	3.7	0.18	25.2/58.3
PSi-M	381 ± 20	0.005–0.02	50	70	5.3	0.34	16.0/36.9

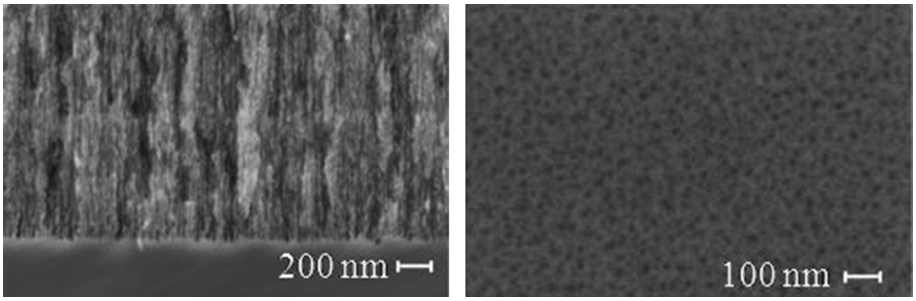

Fig. 1. Cross-sectional SEM image (left) and top view (right) of mesopores sample obtained after anodization of highly doped p-type Si (ρ = 5–20 mΩ cm, PSi-M).

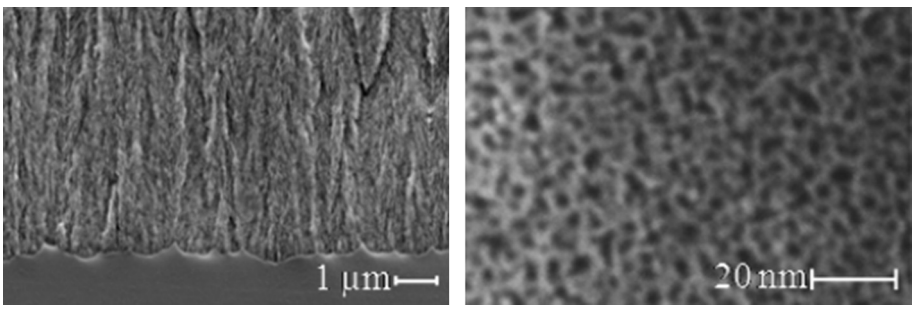

Fig. 2. Cross-sectional SEM image (left) and top view (right) of mesopores sample obtained after anodization of standard p-type Si (ρ = 1–10 Ω cm, PSi-S).

Also, standard p-type (ρ = 1–10 Ω cm) is exposed to an electrolyte based on (2:1) mixture of (50%) HF and ethanol, and the anodization is conducted at a current density of 10 mA/cm^2 during 100 min. Thus, the PSi-S with 50 μm thickness of mesoporous layer is obtained. The average porosity of 65% is evaluated by weight measurements with pore size less than 5 nm in diameter (Fig. 2).

Finally, the porous Si substrates are annealed first in oxygen at 300 °C for 2 h to strengthen the microstructure, then under nitrogen at 420 °C for 2 h in order to stabilize the structure.

On top of the substrates, a 500 nm-thick silicon oxide (SiO_2) is deposited at 300 °C by plasma-enhanced CVD, followed by 1 μm-thick layer of aluminium deposited by physical vapour deposition (PVD) for the definition of the RF CPW lines.

B. *RF characterization and parameters extraction*

Different lengths of CPW lines are fabricated on top of the oxidized substrates. The same CPW lines are integrated on the five above mentioned substrates, namely, Std, HR, TR, PSi-S and PSi-M. The dimensions of the CPW are: signal line width, W = 38 μm, signal line-to-ground plane distance, S = 18 μm, ground plane width, Wg = 208 μm, and line length, L = 8 mm, as sketched in Fig. 3.

RF measurements of these transmission lines on the five substrates were conducted in the frequency range from 10 MHz to 26.5 GHz. From the method explained in [22], the attenuation coefficient (α), the effective resistivity (ρ_{eff}), the characteristic impedance (Z_C) and the effective relative permittivity ($\varepsilon_{r,eff}$) are extracted from the CPW lines S-parameter measurements.

A comparison of the aforementioned extracted parameters is shown in Fig. 4. At 10 GHz, very low RF losses were achieved for TR around 0.35 dB/mm, see Fig. 4(a). These losses were reduced for PSi-M and PSi-S substrates down to 0.18 dB/mm. The Std substrate exhibits high losses around 3 dB/mm at 10 GHz, due to the highly conductive nature of its Si bulk. The significant improvement in performance between the Std substrate and the PSi-S substrate should be noted, since both substrates are initially created from the same type of standard resistivity silicon wafer. The HR substrate also shows poor performances, with losses of around 1.4 dB/mm at 10 GHz, and this is due to induced parasitic surface conduction (PSC) effects beneath the oxide layer that counterfeit the nominal high resistivity value of the Si bulk [23].

From Fig. 4(b) we can see that the PSi-M and PSi-S exhibit excellent effective resistivities, around 7 kΩ cm and 5 kΩ cm, respectively. TR presents a value of around 3 kΩ cm, while HR and Std substrate's effective resistivities are only a few tens of Ohms.

As for the extracted characteristic impedance Z_c, the Std depicts 45 Ω, the HR and TR shows value around 50 Ω, however it is much higher for PSi-M and PSi-S, since they own 70 Ω and 80 Ω, respectively. This larger value of Z_c is due to their lower effective relative permittivities [24]. PSi-S exhibits low effective relative permittivity (~3.7), as can be seen from Fig. 4(d), which is much

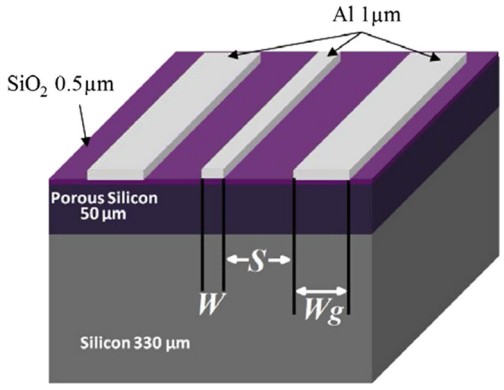

Fig. 3. Schematic of CPW transmission line fabricated on porous Si substrates.

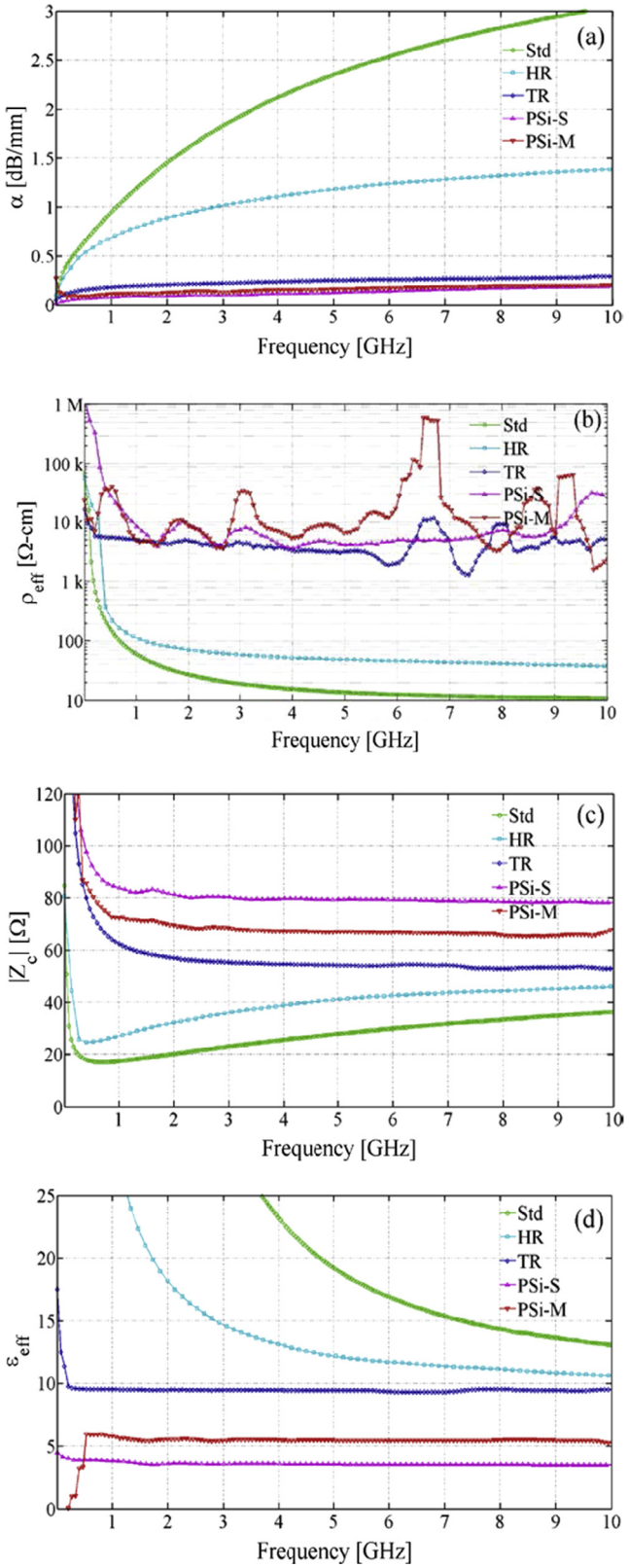

Fig. 4. (a) Attenuation, (b) effective resistivity, (c) characteristic impedance and (d) effective relative permittivity for CPW lines lying on five different Si-based Si substrates.

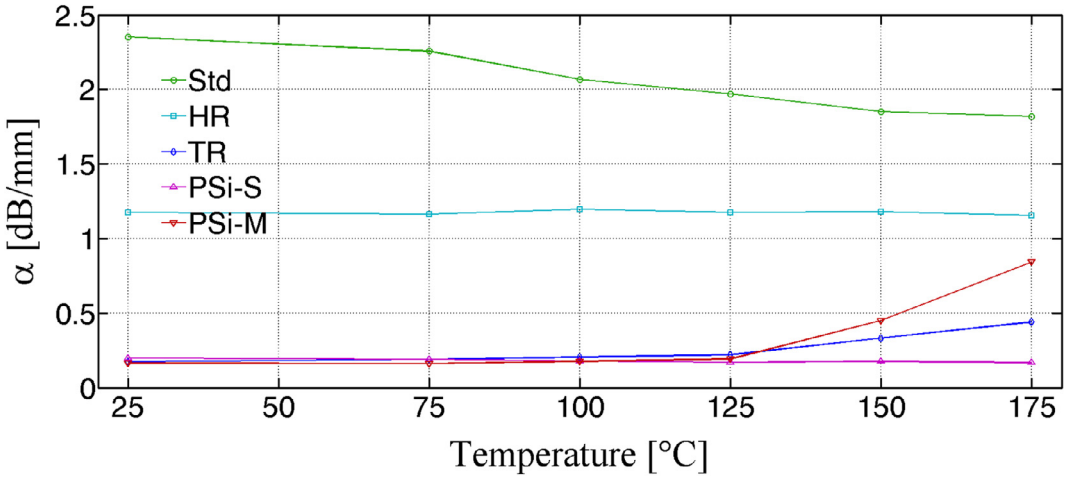

Fig. 5. Losses variation against temperature.

Table 2
Comparison of PSi-based transmission line performance to the state-of-the-art.

	Techno	Line type	Freq (GHz)	ε_{eff}	ρ_{eff} (kΩ cm)	α (dB/mm)	Q_{max}
This work	PSi-S	CPW	26	3.7	5	0.18	25
This work	PSi-S	CPW	60	3.7	5	0.18	58
[8]-1	PSi	CPW	100	2.2	NA	0.61	22
[8]-2	PSi	S-CPW	100	51	NA	4.4	15
[29]-1	BiCMOS-130-nm	μstrip	60	3.7	NA	0.5	20
[29]-2	BiCMOS 130-nm	S-CPW	60	13.3	NA	0.49	42
[32]	BiCMOS 130-nm ST	S-CPW	60	11	NA	NA	50
[33]	MNFM	SW-μstrip	60	36	NA	0.75	47

S-CPW: slow-wave coplanar waveguide.
PSi: Porous Silicon.
NA: Not Available.
MNFM: Metallic-nanowire-filled-membrane.

better for RF and mm-wave application than TR, Std and HR (∼11.7) to reduce crosstalk and noise coupling. Table 1 summarizes the parameters of the investigated substrates.

Furthermore, the designed CPW lines have been submitted to the temperature variation to observe their behaviour at high temperature. The achieved characteristics are shown in Fig. 5. We can note that the losses in PSi-S remain constant over the whole temperature range meanwhile the losses in other substrates depict small increase from 125°C.

Finally, to figure out the interest of the reached insulating properties of the proposed substrate, we have drawn Table 2. This latter summarizes the comparison of PSi-S substrate versus pertinent works reported in the state-of-the-art. As it is observed through this table, the proposed PSi-S shows the highest quality factor which demonstrating thus the significant fall in parasitic related to the substrate.

3. Bandpass filter on Si-based substrates

Aiming to validate its usefulness for millimeter-wave passive circuits, the proposed PSi substrates are used to integrate a mm-wave bandpass filter. The filter is designed around 27 GHz frequency which is one of the dedicated frequencies for 5G wireless broadband communication involved in IoT deployment.

In order to design the bandpass filter on the proposed PSi, the values of resistivity and permittivity experimentally extracted in Section 2. B have been considered. The retained topology is an interdigital filter given by the direct coupled method [25].

The layout and fabrication of the filter is depicted in Fig. 6, where a second order filter is synthesized in CPW configuration. It is important to note how the choice of CPW configuration is crucial. Unlike a microstrip structure, the CPW configuration keeps the filter near to the PSi layer (Fig. 3) enabling the full benefit from the

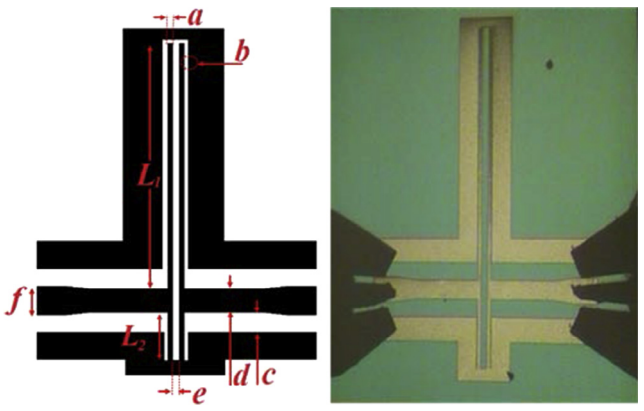

Fig. 6. Layout (left) and photography being measured on the probe station using 67 GHz GSG picoprobes (right) of mm-wave bandpass filter in CPW configuration.

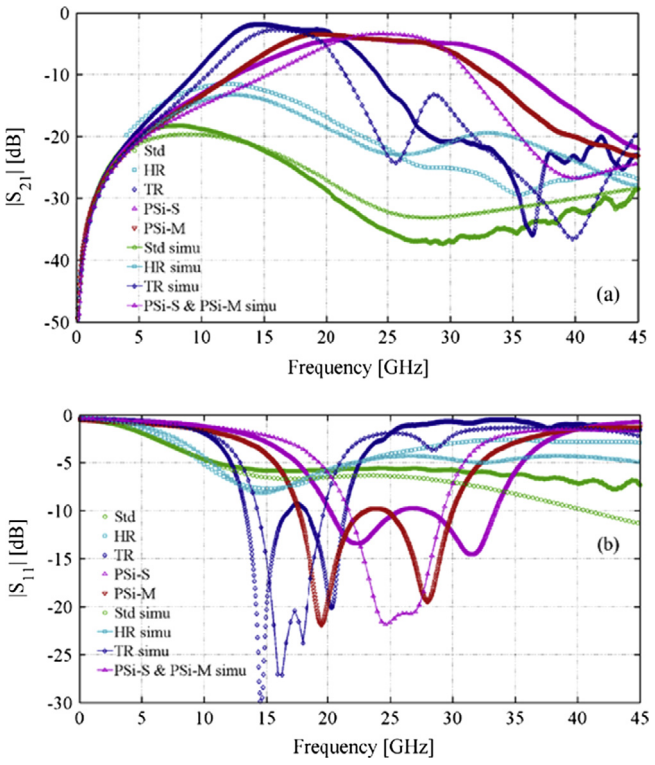

Fig. 7. (a) Insertion loss and (b) return loss for the mm-wave filter implemented on various Si-based substrates.

PSi insulating properties. In addition, having the ground on the same face as the filter prevents the use of vias which can increase the losses coming from shunt resistances.

The filter response is adjusted by optimizing the filter dimensions using the electromagnetic simulator Momentum of ADS 2015 (Keysight technologies). The structural parameters as defined in Fig. 6 (left) are (all in μm): $a = 15$, $b = 3$, $c = 67.5$, $d = 75$, $e = 30$, $f = 100$, $L_1 = 963.5$, $L_2 = 263.5$. The designed filter is integrated on all the investigated substrates depicted in Table 1.

A. *Characterization of the fabricated filters*

The characterization of the fabricated filters is carried out from 10 MHz to 67 GHz with an Agilent PNA-X vector network analyzer. Before measurements, calibration and de-embedding techniques were performed by the SOLT method [26].

The measured data are plotted against the simulated ones and shown in see Fig. 7. Pretty good agreement between simulations and measurements is obtained, except for a widening in the bandwidth.

The bandwidth widening is mainly due to a decrease in the capacitive Q factor of the bandpass filter. Such behaviour is expected as it might be related to the contamination of the silicon layer during the fabrication process. The utilized CAD tool conducts an electromagnetic (EM) simulation of the considered structure without accounting the effects of contamination tied to the manufacturing process. Therefore, the behaviour of the filter when integrated on the real physical substrate cannot be accurately predicted.

Nevertheless, it is evident from the measured performances that the insertion loss of the filter implemented in TR substrate returns with the best value with almost similar performance to PSi-S and PSi-M.

However, if we compare the measured responses of PSi-M and PSi-S, the latter depicts more interesting insertion loss with only 3.5 dB and remains constant over the operation band leading to a flat filter response, whereas, the former shows about 4 dB of losses which increase with frequency, thus, the filter flatness is lost. The filter flatness for the TR, PSi-S and PSi-M substrates is quantified, respectively, over the average insertion loss as follow: 2.82, 3.25 and 5 dB. These latter values are calculated by (maximum IL + minimum IL)/2.

Additionally, the frequency shift of the TR filter response is due to the value of its permittivity ($\varepsilon_r = 11.7$) which is higher than the PSi permittivities ($\varepsilon_r = 3.75$ and 5). Since, the filter was designed relying on the value of PSi permittivity, it was expected to obtain such a frequency shift in the trap-rich filter response (and the EM simulations also highlight this behaviour).

Finally, PSi-S and TR are the most suitable substrates for designing mm-wave bandpass filters, nonetheless, if we consider the fabrication process, the realization of PSi-S is less complicated, consequently it offers low-cost alternative to trap-rich high-resistivity silicon.

Besides the conclusion made above regarding the preference of PSi-S versus TR, it is primacy of place to highlight the advantages of integrating mm-wave filters in PSi-S against their conventional integration in 0.18-μm CMOS technology or even the other CMOS technologies. Aiming to figure out this aspect, we have compared the performance of the PSi-S-based mm-wave filter to relevant works tied to mm-wave filters fabricated in various CMOS technologies, this comparison is summarized in Table 3.

B. *Characterization at high temperature*

In this subsection, we are trying to evaluate the reliability of the proposed substrates against environmental parameters variation; in this case, the temperature variation is investigated. The filter integrated on PSi-M substrate is measured in air at 1 atm and left around 1 h at various temperature points before carrying out S-parameter measurements. As observed in Fig. 8, the filter response remains almost unchanged even at high temperature. The values of the insertion loss at the different temperatures are summarized in Table 4.

Table 3
Comparison of PSi-S-based mm-wave filter with filters implemented in CMOS process.

	Central Frequency (GHz)	Bandwidth (GHz)	Technology	Structure	Filter Order	Size (mm^2)	Minimum IL (dB)	Maximum IL (dB)	$\lvert S_{11}\rvert$ (dB)
This work	27	14	PSi-S	Interdigital	2	1.36	−3.5	−4	−13
[21]	35	16	0.18-μm CMOS	Foldded Interdigital	2	0.12	−5	−7	−9
[27]	60	6	0.18-μm CMOS	Parallel coupled line	3	0.95	−10	−12	−11
[28]	51	7.5	0.18-μm CMOS	Thin film microstrip	3	1.10	−10	−11	−6
[29]-1	61.8	11.2	0.13-μm CMOS S-CPW	T-Junction	1	0.10	−2.2	−3.2	−12
[29]-1	60.8	10.1	0.13-μm CMOS S-CPW	T-Junction	2	0.29	−4.2	−4.8	−12
[30]	53.4	5.2	65-nm CMOS SWS	Rectangular open Loop	2	0.087	−5.5	−6.5	−13
[31]	61.5	9	0.13-μm CMOS	Rectangular open Loop	2	0.21	−1.5	−2	−9.2

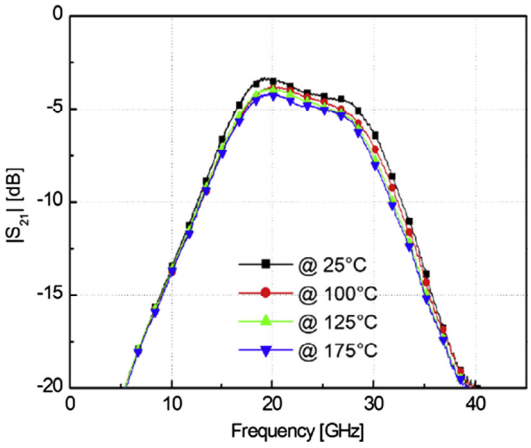

Fig. 8. Mm-wave filter insertion loss at various temperatures on PSi-M substrate.

Table 4
Variation of the insertion losses with temperature.

Temperature (°C)	PSi-M $\|S_{21}\|$ (dB)
25	−4
100	−4.5
125	−4.8
175	−5.4

4. Conclusion

With the foreseen deployment of 5G and IoT, the millimeter-wave spectrum becomes highly solicited. Nonetheless, at this specific frequency range the losses due to the silicon-based substrates increase significantly. Thus, to integrate high quality passive circuits, substrates with good insulating properties should be utilized. In this paper, new variants of porous silicon were introduced. Through accurately controlled fabrication process, very interesting nanocrystalline structure was achieved leading to substrates with good insulating properties, namely, low effective relative permittivity about 3.7 and high effective resistivity values of 7 kΩ cm. The obtained characteristics were emphasized, when compared with three Si-based substrates, i.e., standard silicon, high resistivity silicon, trap-rich HR-Si. Also the reached quality factor of the integrated CPW line was found higher compared to relevant works reported in the state of the art literature. Aiming to demonstrate its usefulness for the integration of mm-wave passive circuit, 27 GHz mm-wave bandpass filter was designed and fabricated on the proposed substrates. The carried out simulations showed that the filter offers better performance, in terms of insertion loss and selectivity, compared with the same filter implemented in standard resistivity silicon, high-resistivity silicon and other CMOS technologies introduce in the literature. These predicted high performances were validated through the fabrication of the designed filters, and good agreement has been achieved between simulated and measured data. Therefore, the proposed porous silicon substrate offers low cost alternative to 0.18-μm CMOS technology and trap rich technology, especially when mm-wave circuit design is accounted for. Furthermore, in order to evaluate the impact of temperature variation on the behaviour of the designed filter, another series of measurements were conducted, fortunately, the performance of the filters were maintained high demonstrating thus the reliability of the proposed PSi-based substrates.

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