Self alignment method by buried mask implantation for Double Gate MOS and nano devices fabrication

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The Silicon-on-Insulator (SOI) technology allows the fabrication of devices with reduced parasitic capacitances compared to bulk CMOS yielding higher switching speed[1]. Another advantage of this technology is the resistance to radiations and high temperatures[2]. The device isolation is also easier to achieve. Thus, fully depleted SOI double gate MOS transistors are promising devices. The active layer of double gate transistor being very thin, the inversion layer extends over the whole active silicon film giving rise to volume conduction, which increases drain current and transconductance and decreases the floating body effect[3]. The threshold voltage is better controlled and the short channel effects are reduced. The double gate architecture makes the subthreshold swing nearly ideal.

Two methods to fabricate self-aligned double gate transistors were previously described[4]. They are both based on implantation of a buried mask to define the second gate of the transistor. In the first case, the implanted buried mask is a negative mask. High dose of boron is implanted in a buried layer, with the top gate as implantation mask. After a few steps of Chemical Mechanical Polishing (CMP) and wafer bonding, the buried mask is revealed by Tetra Methyl Amonium Hydroxyde (TMAH) etching type creating a cavity below the gate. In the second case, a positive mask defines directly the bottom gate. Either p-type or n-type doping species can be used to define the buried mask. After the same CMP and wafer bonding steps as in the previous method the buried mask is revealed with a solution composed of Hydrofluoric acid, Nitric acid and Acetic acid (HNA). The bottom gate is then directly defined.

A demonstrator was made to prove the possibility to create self-aligned structures by buried mask implantation and HNA or TMAH revelation. The critical steps of this demonstrator fabrication were characterized. The TMAH etching rate of polysilicon and etching selectivity were measured for various doping concentrations. HNA etching showed encouraging qualitative results in terms of buried mask patterning but etching selectivity was difficult to measure due to reproducibility problems. An almost infinite selective Reactive Ion Etching (RIE) of silicon dioxide over polysilicon based on a CF_4/H_2 plasma was developed to etch the BOX layer.

Figures 1 and 2 show SEM cross section of the positive and negative revealed buried mask.

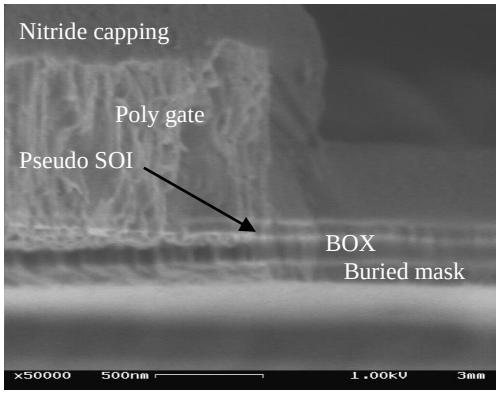

Figure 1: Buried mask revealed in TMAH solution.

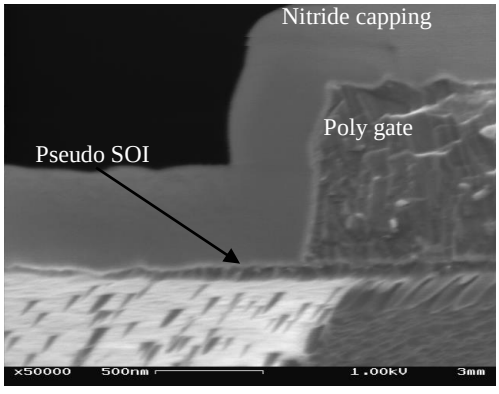

Figure 2: Buried mask revealed in HNA solution.

[1] M. Yoshimi, *Solid-State Electronics*, Vol. 46, (2002), pp. 951–958.
[2] Y. Li *et al*., *Solid-State Electronics*, Vol. 47, (2003), pp. 1111–1115.
[3] M. Cass *et al*., *Solid-State Electronics*, Vol. 48, (2004), pp. 1243–1247.
[4] R. Charavel *et al*., Fabrication of self aligned double gate MOS transistor, *URSI Forum 2003.*