Demonstration of Trap Recovery by In-Situ Annealing in 28nm FD-SOI MOSFETs at Cryogenic Temperatures

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***Abstract*—This work presents the first demonstration of the impact of active in-situ electro-thermal annealing at 4 K on the low frequency noise characteristics of N-type MOS transistor with thin high-k gate oxide from 28 nm Fully Depleted Silicon-on-Insulator (FD-SOI) process. Efficiency of local electro-thermal annealing inducing more than 475 K temperature rise is demonstrated on the device which features random telegraph noise behaviour at a given current level at 4 K, while presenting "typical" 1/f noise behaviour at room temperature. Experimental results reveal random telegraph noise mitigation both in temporal and spectral domains thanks to the traps healing by in-situ annealing at 4 K, with 58 % noise power reduction, without impacting performance at both 4 K and 295 K.**

Keywords- Cryogenic temperatures; FD-SOI; MOSFET, Low frequency noise; Random telegraph noise; In-situ annealing.

I. INTRODUCTION

Uncontrolled oxide and interface traps increasingly affect MOSFET performance as CMOS technologies continue to scale down [1][2]. This is particularly crucial for future in analog , RF and quantum applications. At both cryogenic and room temperatures, these defects can induce threshold voltage fluctuations, mobility reduction and subthreshold slope degradation, strongly impacting device stability and reliability [3][4]. This issue is especially critical for quantum computing applications, where cryogenic CMOS circuits are required for qubit control and readout [5], and where low-frequency noise remains a major limitation to the performance and reliability of Cryo-CMOS devices [4].

Thermal annealing techniques have been widely investigated to recover degraded MOSFET characteristics through defect neutralization at room temperature [6][7]. However, conventional furnace or wafer-level annealing remains constrained by post-processing thermal budgets and metallization reliability. Furthermore, devices cannot always be readily withdrawn from their operating environment to undergo external ex-situ annealing. As a proposed alternative, active in-situ electro-thermal annealing enables localized heating directly inside the transistor structure using Joule effect, allowing trap recovery without heating the entire chip [8][9][10]. Previous works demonstrated the efficiency of in-situ annealing in FD-SOI MOSFETs at room temperature, notably through improvements of DC characteristics and reductions of low-frequency noise and Random Telegraph Noise (RTN) in defective devices [11][12]. However, the impact of such recovery technique and its applicability at cryogenic temperatures has not yet been experimentally investigated. In this work, we demonstrate for the first time to the authors best knowledge the efficiency of active in-situ electro-thermal annealing on 28 nm Fully Depleted Silicon-On-Insulator (FD-SOI) MOSFETs at 4 K.

II. DEVICE DETAILS AND EXPERIMENTAL SETUP

The device under test is 30 nm long and 2 µm wide typical N-type MOSFET from 28 nm FD-SOI technology with standard high k metal gate thin oxide with 1.1 nm equivalent oxide thickness (EOT) from STMicroelectronics. The device features a dedicated structure to perform local annealing with two source contacts (S1 and S2), two drain contacts (D1 and D2), two gate contacts (G1 and G2) and a back-gate contact (BG) as depicted in Fig. 1. The silicide resistor formed between these source (and/or drain) contacts acts as a low-voltage local heater through Joule effect. Its electro-thermal behavior has been characterized and calibrated at room temperatures in previous studies [13]. A particular attention was paid to the design of the metallization layers in silicon demonstrators to withstand and current densities and thus the high temperatures required for thermal annealing while preserving gate oxide integrity.

LakeShore CPX cryogenic probe station is used to perform measurements from room temperature (295 K) down to liquid helium temperature (4 K). Drain current vs gate voltage, I_{ds}–V_{gs} DC characterization, low frequency Noise (LFN) measurements as well as transient RTN measurements were performed using Keysight A-LFNA noise Analyzer and B1500 semiconductor analyzer. LFN measurements were performed from 1 Hz up to 1 MHz and RTN current-time traces were recorded for 2.68 s with a time step of 5.11 µs. As the noise in a MOSFET is bias-dependent [14], it is evaluated at different levels of fixed drain current ~ 1 µA, 10 µA and 50 µA.

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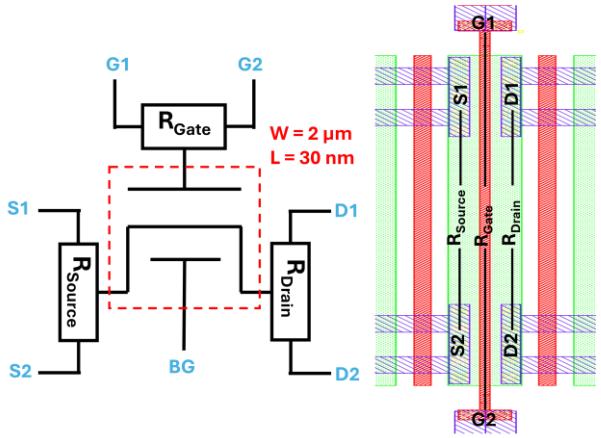

Fig. 1. Schematic representation and typical layout of the N MOSFET under test.

III. METHODOLOGY

As shown in Fig. 2, experimental procedure begins with DC and noise measurements of the device under test at room temperature and then at 4 K. These measurements are performed in the "standard" operating mode, using one contact on each terminal (D1, G1, S1, and BG) while leaving the other contacts in floating condition. Next, the device is annealed using both source contacts (S1 and S2) and both drain contacts (D1 and D2) simultaneously. The annealing step consists of three annealing cycles, each cycle involving the simultaneous application of a voltage ramp from 0 to 1.5 V in 10 mV increments between the respective source and drain contacts (S1,S2 and D1,D2). Joule effect is generated by the bias applied on source and drain resistances, and the heat is dissipated throughout the structure via thermal conduction.

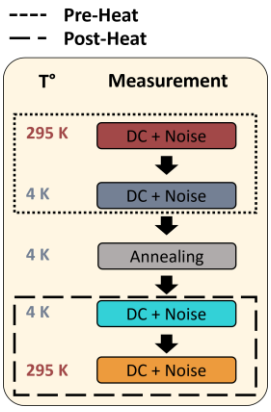

Fig. 2. Experimental measurement procedure.

In order to estimate the temperature rise caused by bias application between two source contacts S1, S2 and/or two drain contacts, the source (or drain) resistance as a function of the chuck temperature (calibration curve) as well as the source (or drain) resistance as a function of the V_{heat} bias applied between its two contacts S1 and S2 (or D1 and D2) at 4 K were measured (Fig. 3). Each bias point is maintained for 400 ms. One can see that the maximum temperature in the drain and source, estimated through linear extrapolation from the measured resistance, exceeds 470 K. The two contact gates are not used in this work, but they can also be used as temperature sensors [12]. After the annealing step, the same device is measured again (DC and noise) at 4 K and 295 K. This procedure was performed on three devices from different dies, with the results shown for a single device and current level for clarity.

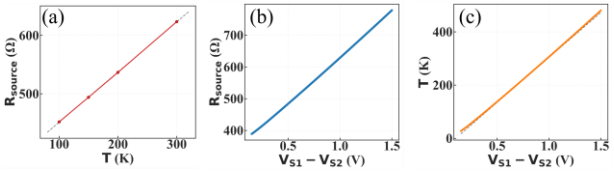

Fig. 3. Temperature monitoring: (a) Calibration measurement of source resistance vs chuck temperature; (b) Measurement of source resistance vs voltage applied on source contacts, (c) Source temperature vs voltage applied on source contacts during in-situ annealing.

IV. RESULTS AND DISCUSSION

The I_{ds}-V_{gs} characteristics of the NMOS transistor in linear regime (V_{ds}=50 mV) before and after annealing are presented in Fig. 4, for 295 K and 4 K. Device features a threshold voltage shift of about 20 mV after annealing both at 295 K and 4 K.

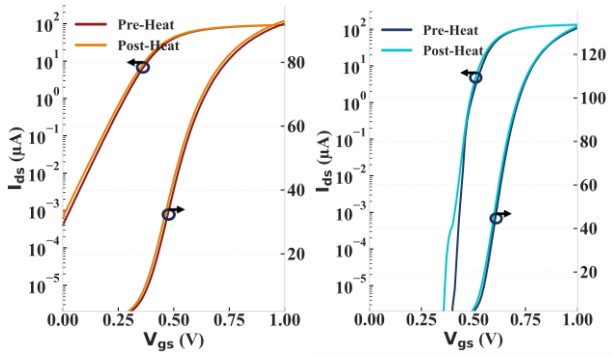

Fig. 4. Drain current I_{ds} vs gate voltage V_{gs} in linear regime (V_{ds}=50 mV) before (darker curve) and after (lighter curve) in-situ annealing. Ids-Vgs curves are measured at 295 K (left) and 4 K (right).

Fig. 5 shows an example of time domain measurements realized at at I_{ds} ~50 µA in linear regime at 295 K and 4 K. Before annealing, the time domain signature exhibits a typical behaviour with small random current fluctuations (followed gaussian distribution) around 50 µA at 295 K (Fig. 5a). However, a two level RTN signal, characteristic for a trapping/detrapping from a single trap phenomenon, is observed at 4 K before annealing (Fig. 5b). The current difference between two states $\Delta I_{ds} =$ 598 nA is extracted from the two gaussian current distributions (Fig 5b), while the mean emission and capture time constant $\bar{\tau_e} = 0.30$ ms and $\bar{\tau_c} = 1.19$ ms, respectively, are extracted from the exponential distribution ($f(\tau) = \frac{1}{\bar{\tau}}\exp(-\frac{\tau}{\bar{\tau}})$) of capture and emission time, as shown in Fig. 6. It is important to note that the noise measurements were performed at a constant current level (Ids ~50 µA) at both temperatures (4 K and 295 K), rather than at a constant overdrive voltage. The trap contribution may differ between the two temperatures,.

However, this work focuses on the traps in-situ healing and RTN mitigation at 4 K, which will be beneficial for real applications like quantum computing.

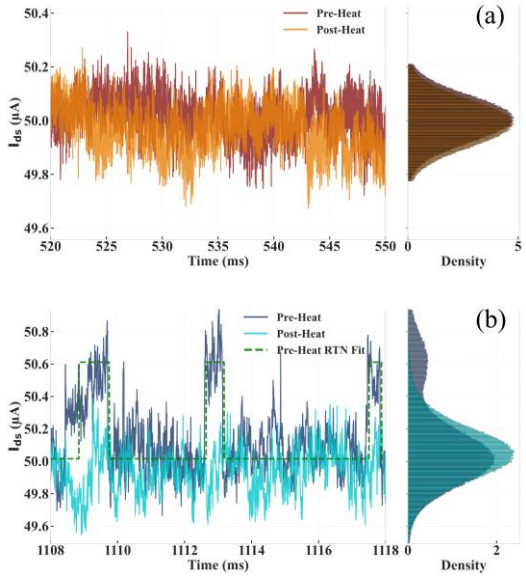

Fig. 5. Time trace measurements of the drain current measured at 295 K (a) and 4 K (b) before and after annealing in linear regime (V_{ds}=50 mV) for I_{ds}=50 µA (left), corresponding normalized current distribution (right). Reminder: annealing was performed at 4 K.

After annealing, the second current level at 4 K is no longer present in the time domain and in the histogram distribution (Fig. 5b) confirming the trap healing, while no significant effect is observed on the measurement at room temperature (Fig. 5a).

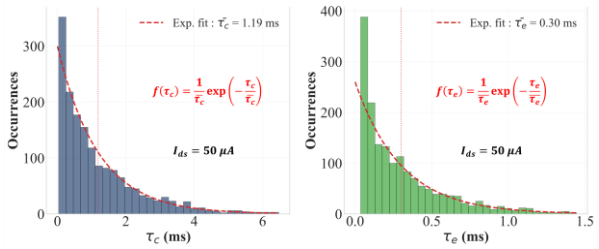

Fig. 6. Distribution of capture (left) and emission (right) times from time trace measurements of I_{ds} at 4 K in linear regime (V_{ds}=50 mV) for I_{ds}=50 µA before annealing.

Fig. 7 shows the power spectral density (PSD) noise, frequency domain, measurements at 295 K and 4 K before and after annealing, at I_{ds} ~50 µA. At room temperature, typical 1/f noise is obtained before and after annealing (Fig. 7a). However, at 4 K, clear Lorentzian-like (plateau followed by 1/f²) behaviour is observed before annealing (Fig. 7b), suggesting a dominant trap contribution at this bias condition. Introducing the parameters $\Delta I_{ds}, \overline{\tau_c}, \overline{\tau_e}$, extracted from the time domain current traces, in a Lorentzian model (Equation 1) [15] fairly reproduces the measured PSD in Fig. 7b.

$$S_{id,RTN}(f) = \frac{4\tau^2}{\overline{\tau_e} + \overline{\tau_c}} \frac{\Delta I_{ds}^2}{(1 + (2\pi f\tau)^2)} \quad \left[\frac{A^2}{Hz}\right] \qquad (1)$$

where $\tau = \frac{1}{\frac{1}{\tau_e}+\frac{1}{\tau_c}}$

The total noise power is then calculated as an integral over the frequency range (Eq. 2) from 1 Hz to 982 kHz (i.e. limited by the worst-case roll-off frequency of the equipment for respective bias conditions).

$$\sigma^2{}_{id} = \int_{1\,Hz}^{982\,kHz} S_{id,RTN}(f)\, df \;\; [A^2] \qquad (2)$$

After annealing, Lorenzian-like noise has been suppressed at 4 K and typical 1/f -like noise has been recovered with a decrease of 58 % of the noise power integrated over the bandwidth (Table 1). At room temperature, no significant effect of in-situ annealing done at 4 K is observed.

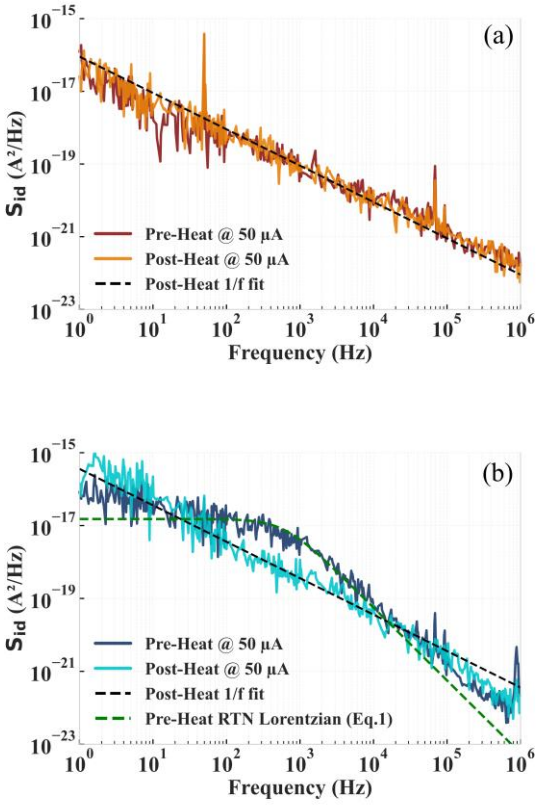

Fig. 7. Noise power spectral density of the N MOSFETs measured at 295 K (a) and 4 K (b) before and after annealing in linear regime (V_{ds}=50 mV) for I_{ds}=50 µA. (reminder: annealing was performed at 4 K).

	PRE-HEAT	POST-HEAT
σ^2_{id} @ 4 K [A²]	$1.56\ 10^{-14}$	$6.40\ 10^{-15}$
σ^2_{id} @ 295 K [A²]	$1.94\ 10^{-15}$	$1.92\ 10^{-15}$

V. Conclusion

The efficiency of in-situ annealing at cryogenic temperatures was demonstrated for the first time on high-k thin oxide MOSFET in 28 nm FD-SOI technology. Local in-situ electro-thermal annealing with 475 K maximum temperature rise results in a remarkable mitigation of Lorentzian noise component and 58% total noise power reduction in PSD at 4 K, without impacting noise behaviour at room temperature. Time domain measurements confirm the healing of trap related defects by in-situ annealing, leading to RTN mitigation as well as the improvement and stability of device performance, notably for analog applications. This recovery technique could be applied to other device flavors and opens new investigations on pulse(s) bias method to optimize the transistor in-situ healing.

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