



Bottom-Up Life-Cycle Assessment of MEMS Piezoresistive Pressure Sensors

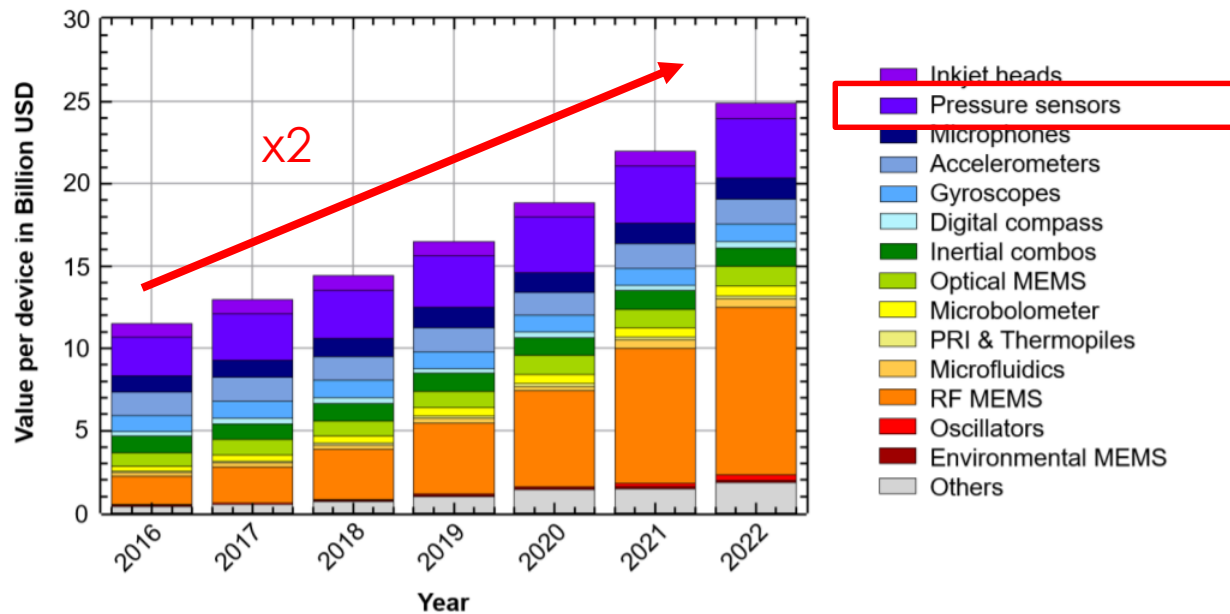
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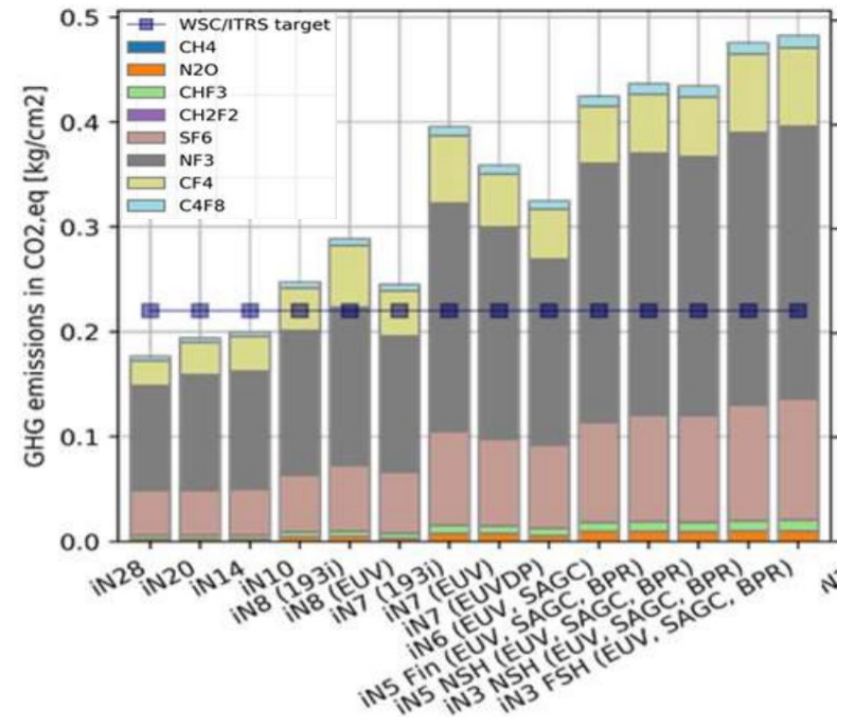
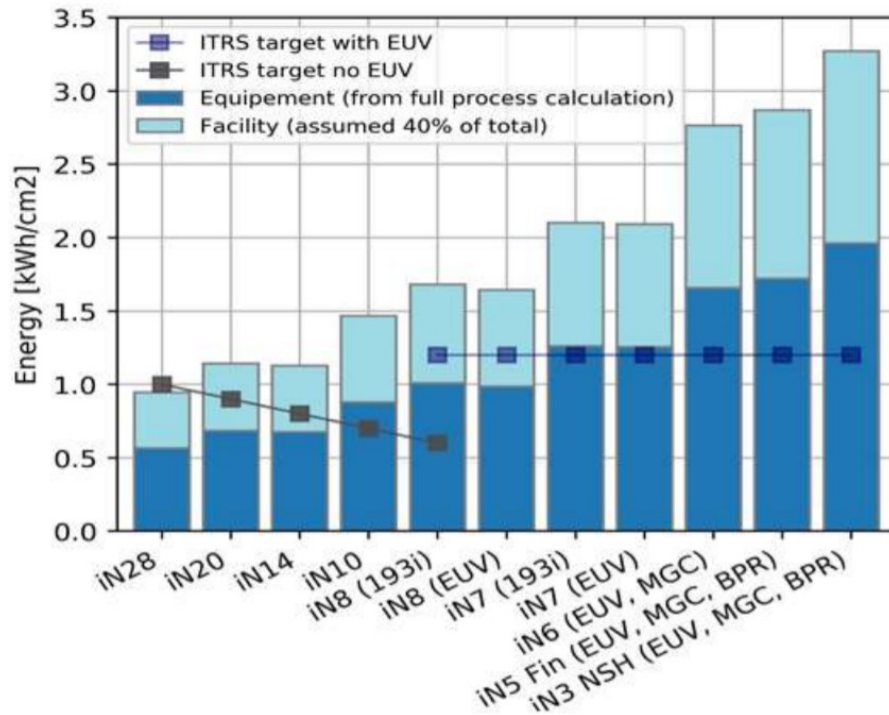
Introduction

- MEMS Market should rise tremendously [1]



Pressure sensors should have been the biggest part until 2018

Introduction



We need to be careful because advanced technologies often come with increased Energy Demand and GHG emissions: for example CMOS [2]

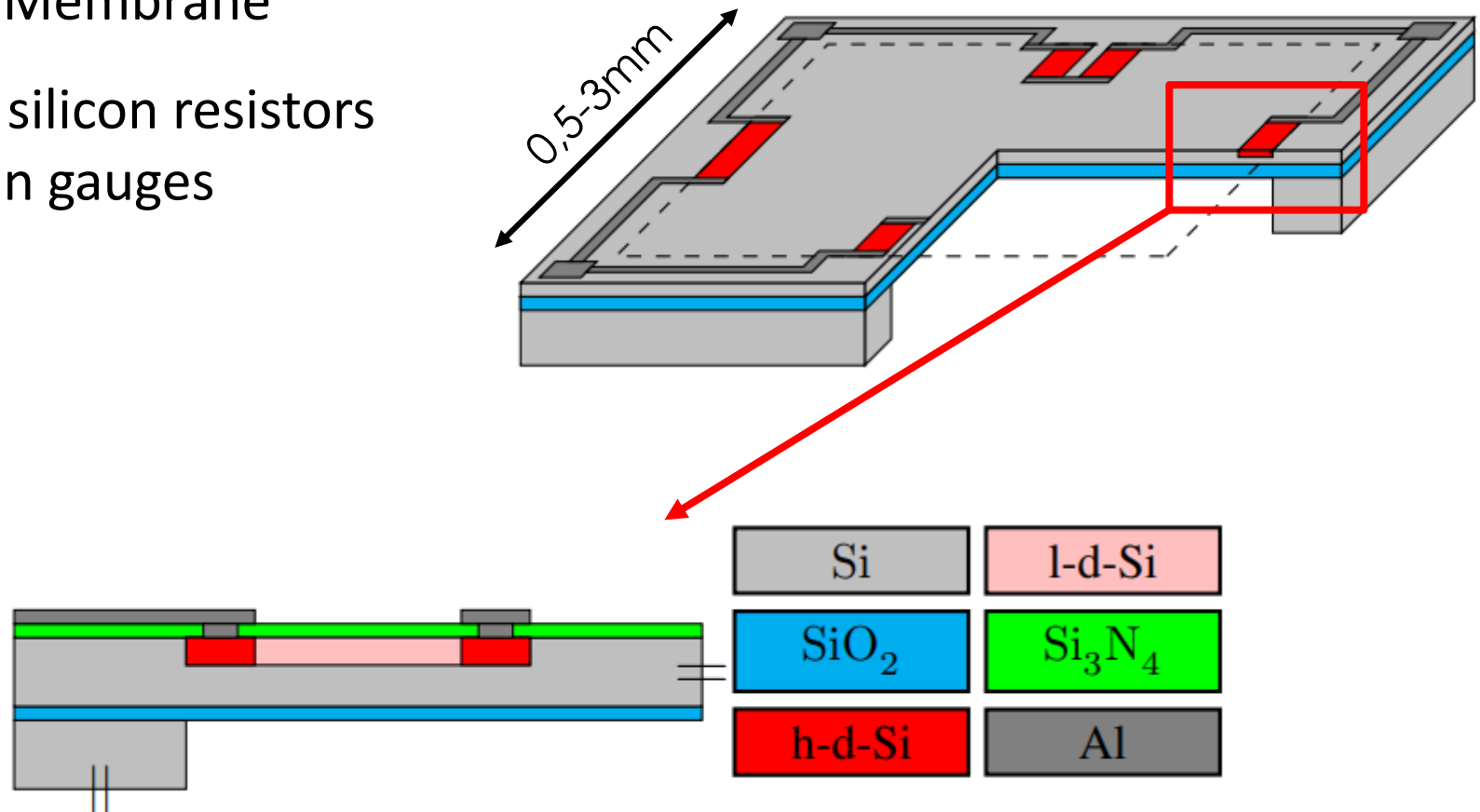
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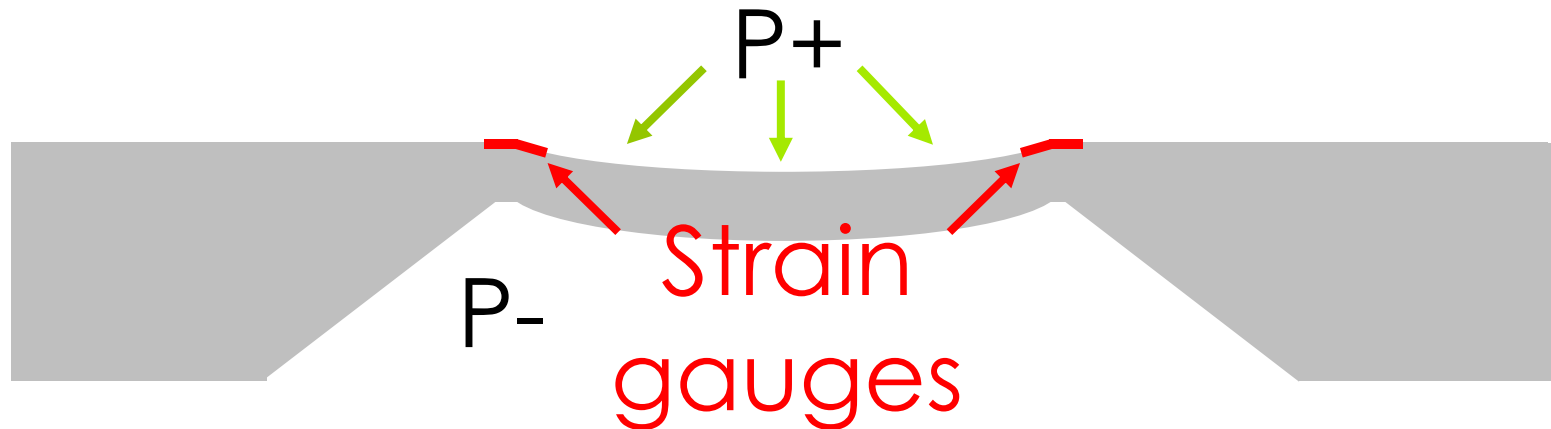
MEMS Piezoresistive pressure sensor: Principles and Process flows

Working principle

- Silicon Membrane
- Doped silicon resistors as strain gauges

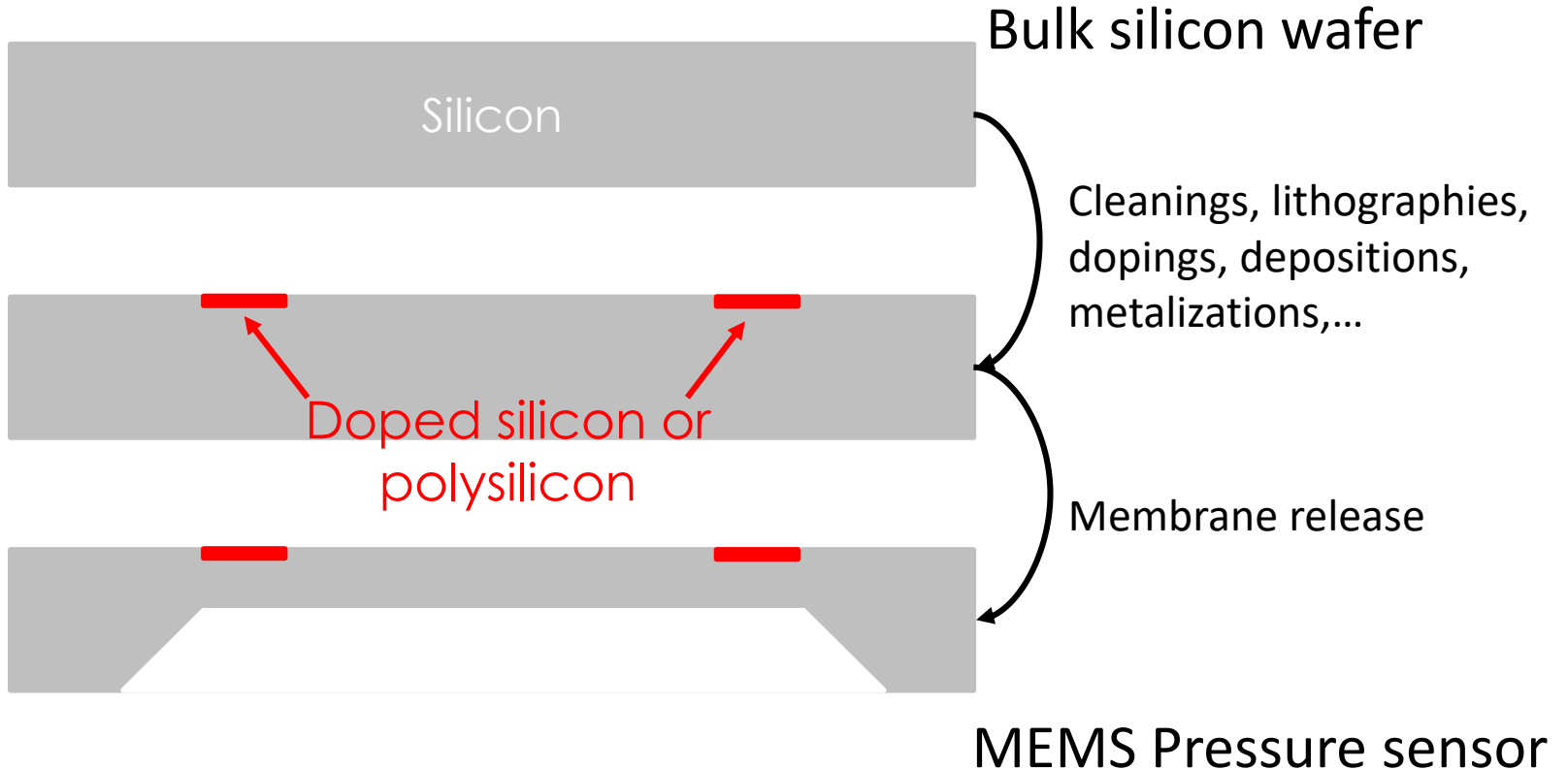


Working principle



- Differential pressure sensing
- Variable resistors as strain gauges

Basis of process flows



Basis of process flows



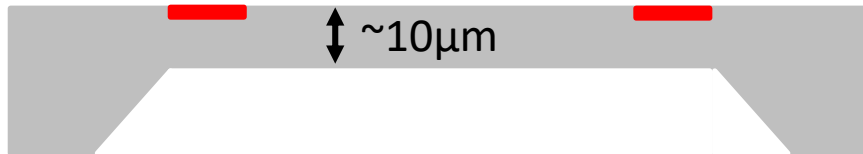
Membrane released by
anisotropic wet etching (KOH,
TMAH)

Membrane released by
anisotropic dry etching (SF_6 -
DRIE)

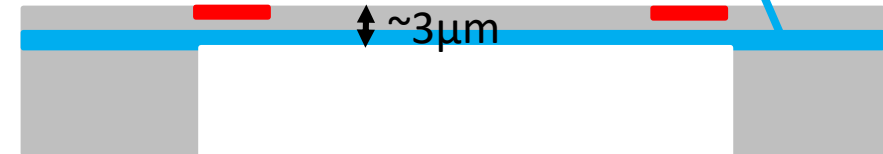
- Reduced Area thanks to no slope side walls

Basis of process flows

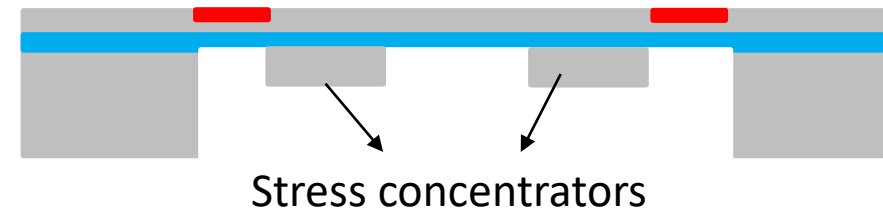
Bulk silicon



Silicon on Insulator



Silicon on Insulator with patterning

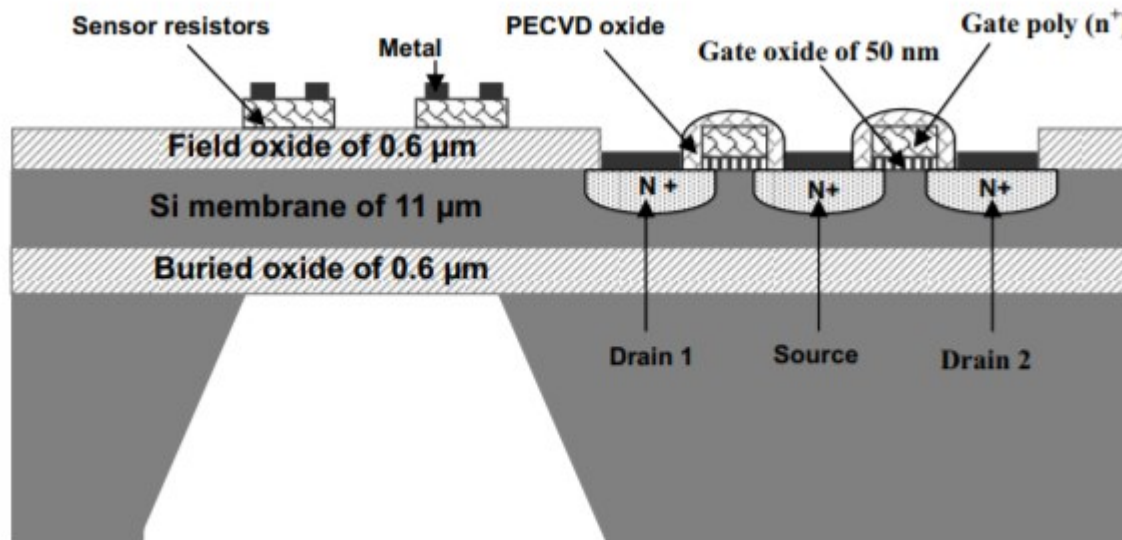


SOI :

- Reduced membrane thickness
- High precision membrane patterning

Case studies

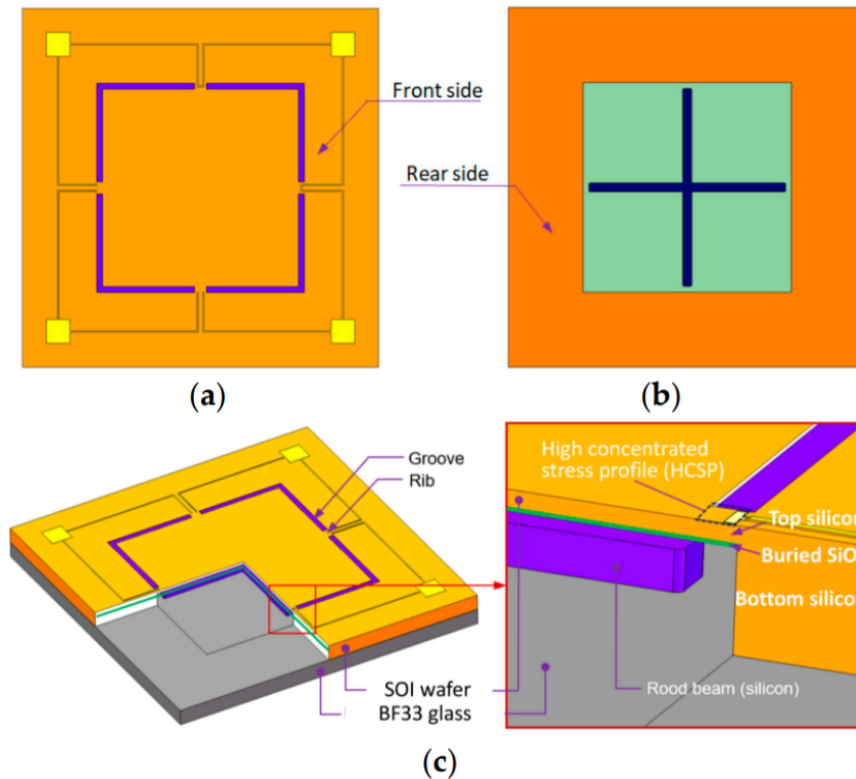
1) Kumar *et al.* (2006) [3]



- SOI substrate
- Membrane released by wet etching

Case studies

2) Li *et al.* (2018) [4]



- SOI substrate
- Membrane released by dry etching

Piezoresistive pressure sensor: Bottom-Up Life-Cycle Assessment

LCA : objectives

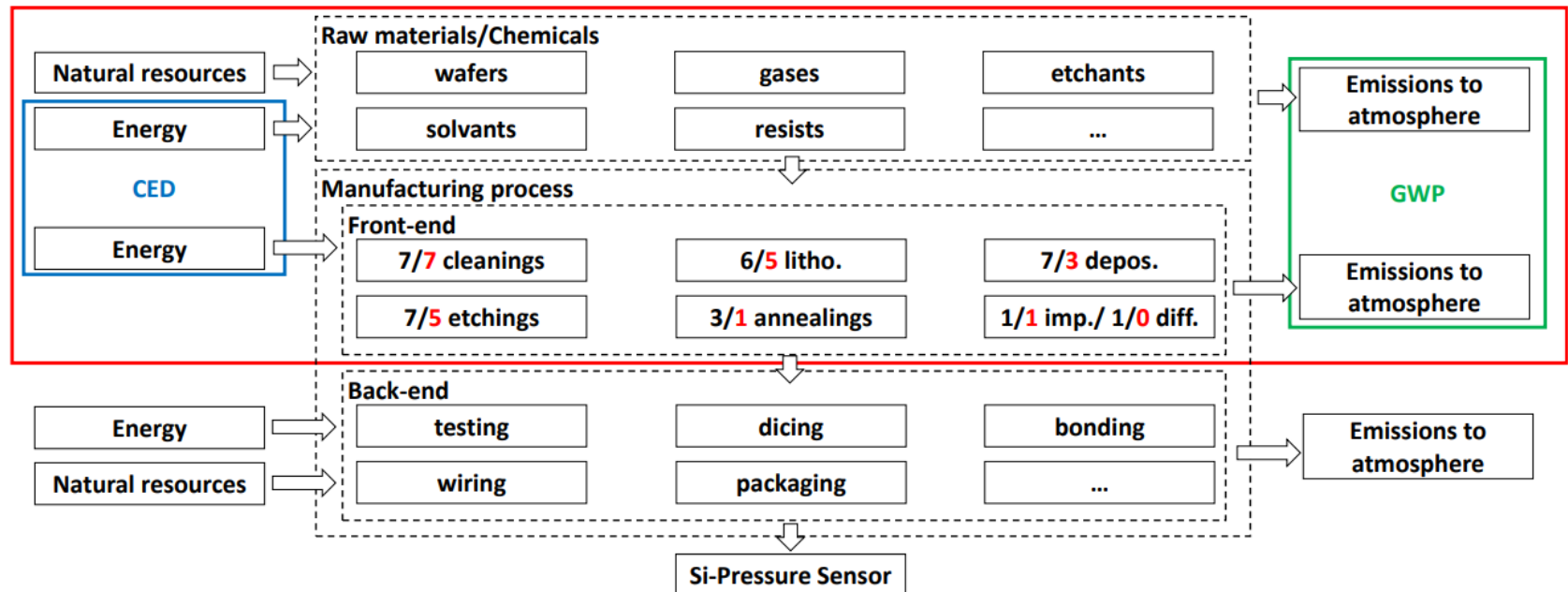
Quantifying :

- Cumulated primary Energy Demand (CED): Energy needed during the MEMS pressure sensors manufacturing.
- Global Warming Potential (GWP): Global Warming Potential of the greenhouse gases emitted during the MEMS pressure sensors manufacturing.

LCA : Method

Perimeter of the study

From cradle to front-end process



LCA : Method

Inventory model [5]

- For CED:

$$CED = CED_{mat} + CED_{proc} = \sum [m_{mat} \times e] + \sum [(m_{chem} \times e) + e_{proc}]$$

Raw material flows [kg] (points to m_{mat})

Chemical flows [kg] (points to m_{chem})

Energy associated with electricity use [kWh] (points to e_{proc})

Raw material energy intensities [kWh/kg] (points to e in the first sum)

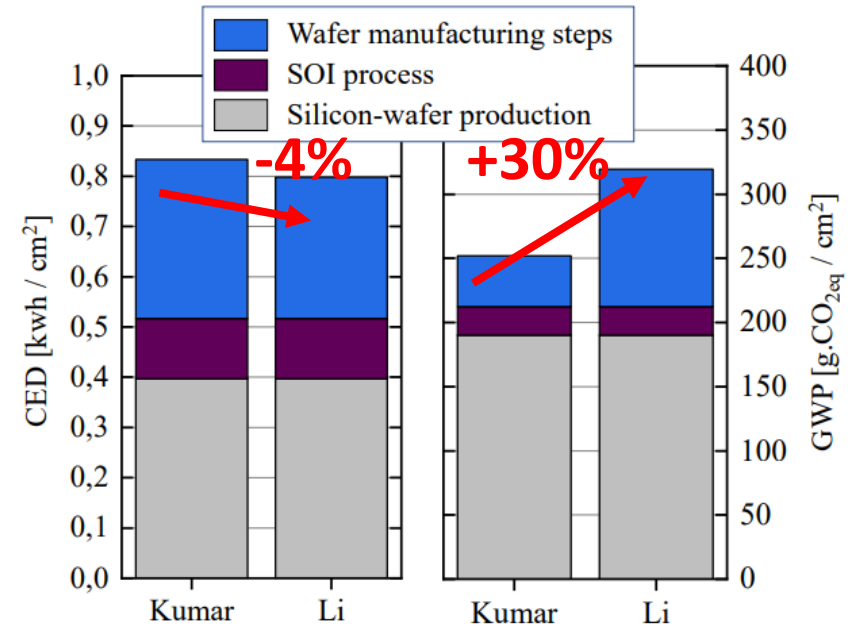
Chemicals energy intensities [kWh/kg] (points to e in the second sum)

- Idem for GWP

Data come from previously generated life-cycle inventories for CMOS processes [2,6-7]

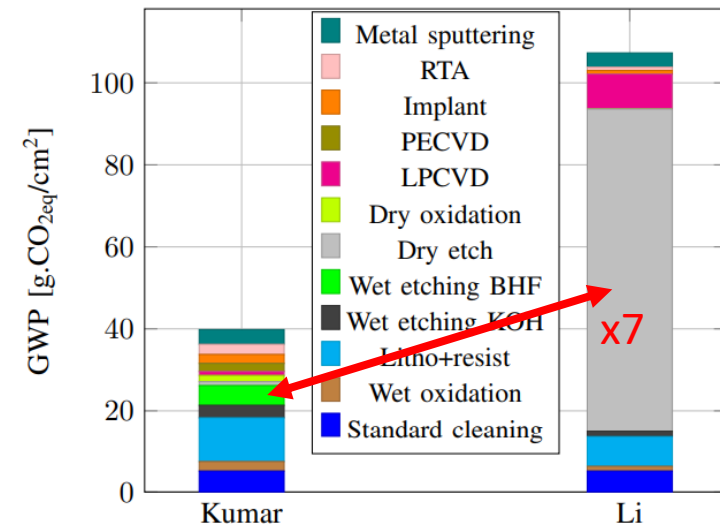
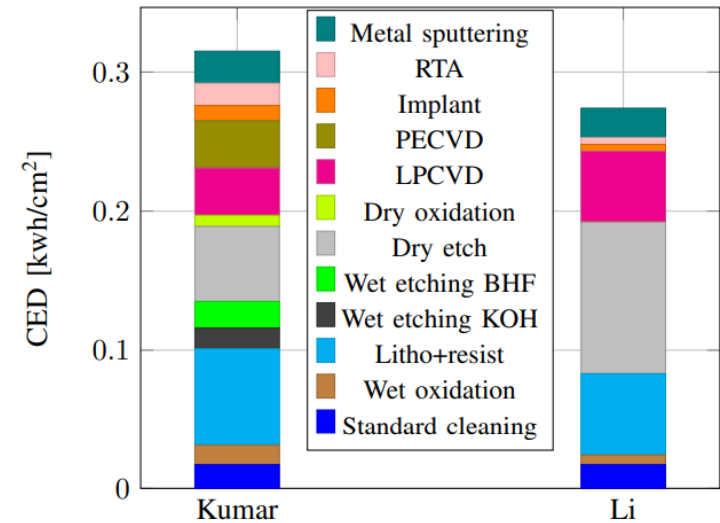
LCA : Main results

- Major contribution in CED and GWP is coming from the silicon wafer production
- Impact of SOI versus bulk silicon:
 - ~20% CED increase
 - ~10% GWP increase (only for the wafer)



LCA : Main results

- About process steps : dry etchings have a huge amount of GWP
- Impact of dry etching versus wet etching:
 ~ GWP multiplied by 7 for membrane release step, mainly due to SF_6 released in the atmosphere (90% abatement)

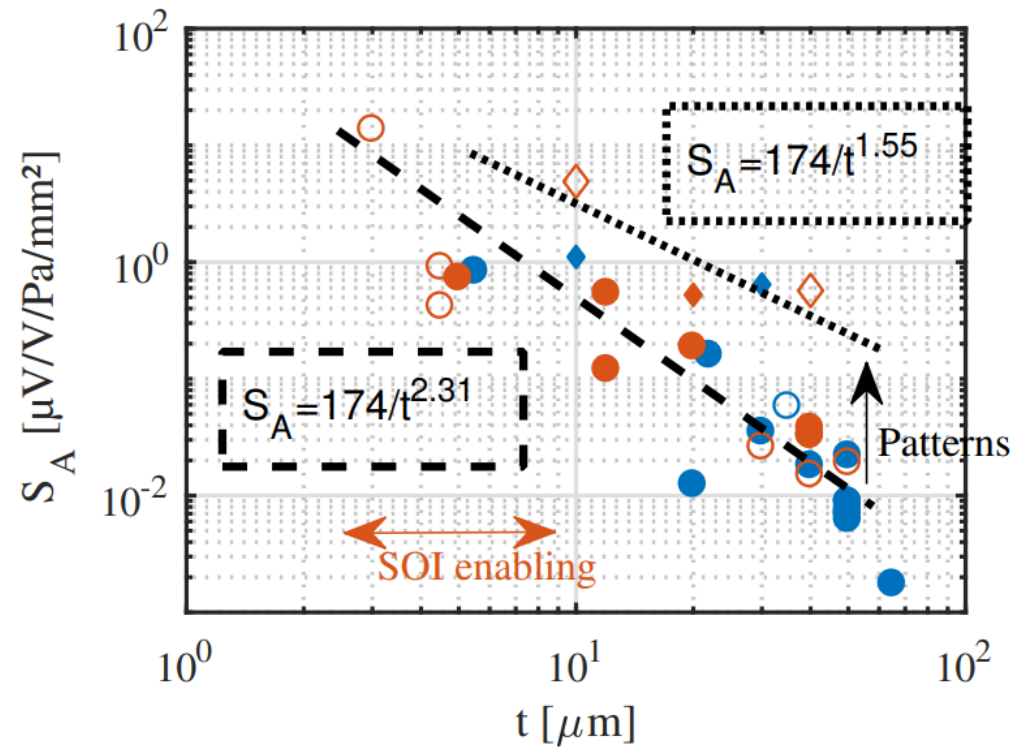


MEMS Piezoresistive pressure sensor: Impacts versus Performances

Mechanical figure of merit (FoM): S_A

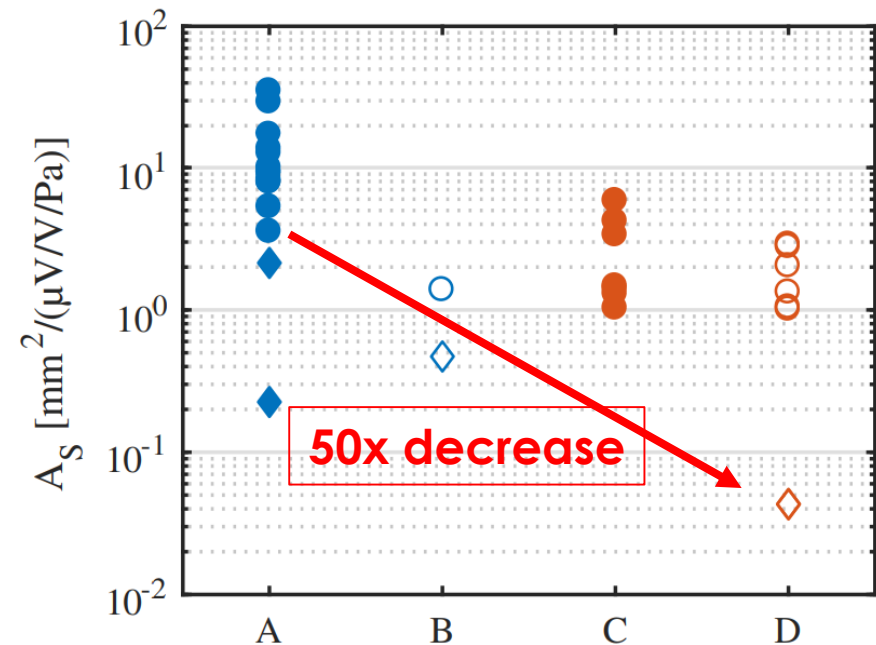
S_A = Sensitivity divided by membrane area [8]

- **SOI** + dry etching (empty symbols) allow for reaching thinner membranes (down to 3 μm)
- Membrane patterning allows a 6-fold increase of the Mechanical FoM at 10 μm



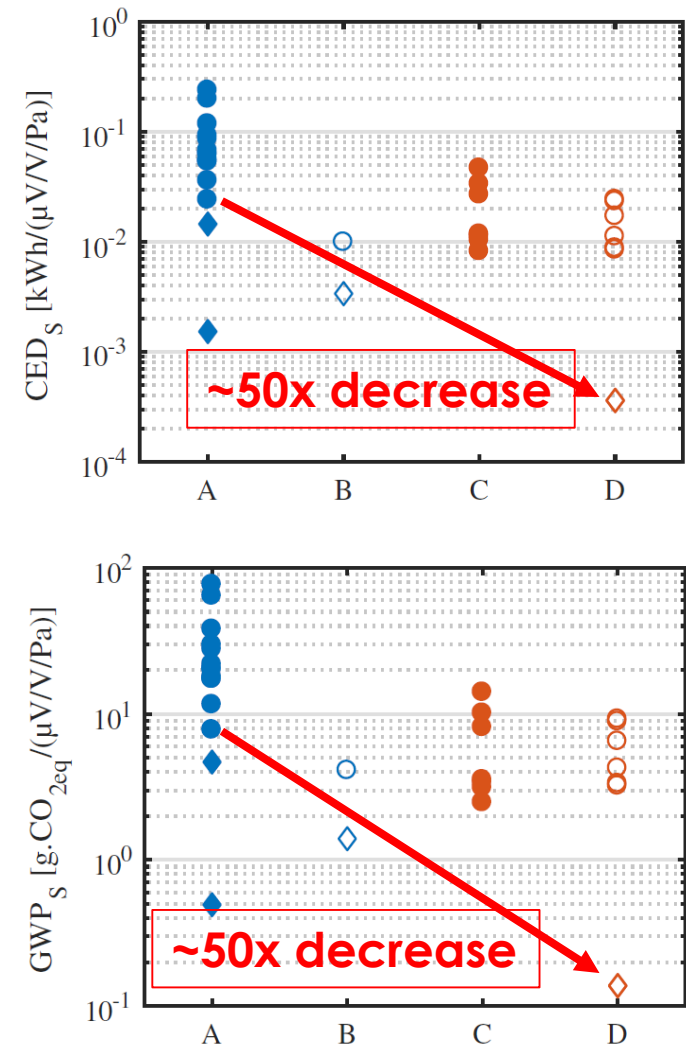
Area needed versus Sensitivity

- By normalization regarding to the membrane thickness, we found the best performances achievable depending on technology mix.
- Going from bulk-silicon, with membrane release by wet etching, to SOI with membrane released by dry etching with patterning allows for a 50-fold reduction of area needed per sensitivity units.



CED and GWP versus Sensitivity

- Improvement of S_A thanks to SOI, dry etching and membrane patterning is way bigger than the increase in CED and GWP, that become marginal.



Conclusions (1)

- IMPACTS:
 - Major impacts in CED and GWP are coming from the substrate
 - Increase of 20% and 10% of the substrate CED and GWP due to SOI substrate.
 - Multiplication by 7 of the release step GWP due to dry etching.
- IMPACTS vs PERFORMANCES:
 - A 50-fold reduction of area needed per sensitivity units, thanks to SOI substrate, dry etching and membrane patterning.
 - Performances improvement supplants by far impacts increases.

Conclusions (2)

- Improvement tracks:
 - Investigation about an low-GWP alternative to SF_6 for silicon dry etching to reduce release step GWP.
 - Analysis of Yield reduction versus wafer thickness reduction to reduce substrate impacts.

Acknowledgements

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