

# CHAPTER 1

## SOI TECHNOLOGIES FOR ANALOG APPLICATIONS

### ***1.1 Introduction***

The microelectronic industry is driven by the need of high performance circuits and devices for digital applications, which represent more than 90 % of the electronic production. For many years, bulk MOSFET was considered as the only viable solution to satisfy the well-known MOORE's Law, which states that the performances of processors are doubled every 18 months. Historically, device scaling remains the primary method by which the semiconductor industry has improved performances and productivity.

For sub-micron technologies, the reduction of the dimension of the devices increases the numbers of technological challenges to be solved. The short channel effect (SCE), and the increase of junctions leakage current make difficult for the industry to follow the MOORE's Law with bulk devices.

As presented in Figure 1.1, the performances of bulk devices and circuits will not be able to follow the Law since the complexity of problems to be solved. But, as it has been shown, the use of SOI can help to increase the performances [1].

Although it was still considered twenty years ago as an exotic technology, SOI has now reached maturity. SOI technology has been widely demonstrated and recognized to be a mature and alternative technology to mainstream bulk silicon for the realization of high-speed, low-power digital [2] and analog [3] CMOS circuits, as well as niche applications under extreme high temperature [4] or radiation conditions.

This chapter will present briefly some properties of the SOI technologies and SOI MOSFETs as an introduction for the next chapters. No recent scientific results will be presented.

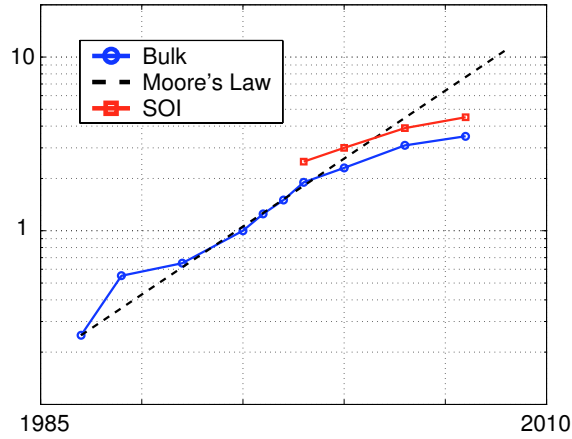


Figure 1.1: Evolution of the relative performances of SOI and bulk MOSFET compared to the Moore's Law

In the following sections, some general differences between SOI and bulk MOSFETs are presented. Then, some general properties of the SOI material are shown before introducing the different SOI technologies that have been used during this work. Finally the technological advances that have been observed along the last five years are presented.

## 1.2 Comparison of SOI and bulk MOSFET

The basic differences between bulk and SOI transistors are the following:

- Bulk MOSFETs are built atop the surface of a monocrystalline silicon wafer (Figure 1.2a).
- In SOI, the top active silicon region is separated from the under-laying mechanical substrate by a thick insulator layer (Figure 1.2b).

This difference leads to a number of advantageous device and circuit performances when compared to bulk silicon [5].

Some improvements of SOI CMOS compared to bulk CMOS are presented in the following paragraphs.

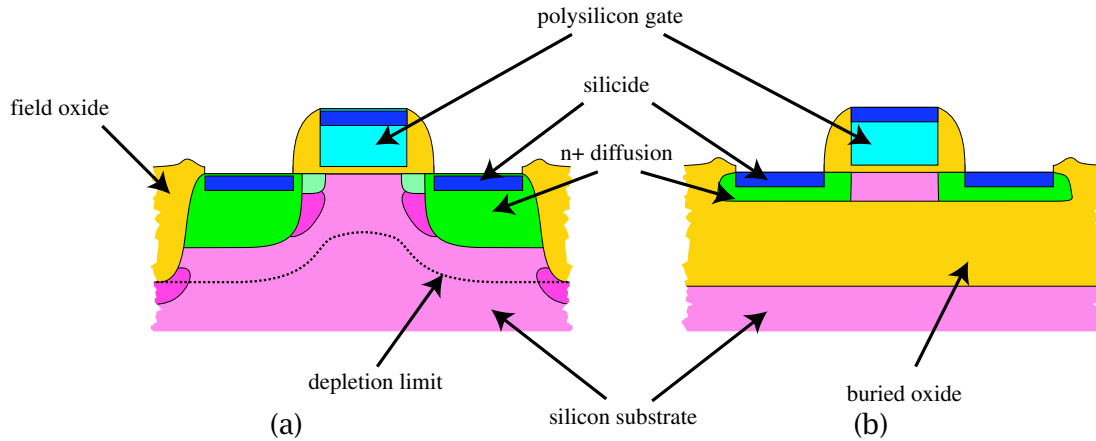


Figure 1.2: Cross section of a bulk (a) and a SOI (b) MOSFET

**Reduction of substrate parasitic capacitances** Capacitances are a key factor for the high frequency performances of devices. Any reduction of the total capacitance of a MOSFET will increase the cut-off frequency of the transistor, allowing using circuits at higher frequency. In bulk devices, the parasitic source and drain to substrate capacitances increase with the doping level, becoming larger for modern devices where the doping level is higher than in previous technologies. In SOI, the maximum capacitance between junctions and the substrate is the capacitance of the buried oxide. This capacitance is fixed by the thickness of the buried oxide. Thanks to the lower value of its permittivity, compared to silicon, these capacitances are smaller than what we can expect for bulk MOSFET [6].

**Small devices without latchup** A parasitic effect of CMOS technologies is called latchup. This effect consists in the triggering of an unwanted PNP thyristor which is present in the bulk structure. In SOI, there is no path for any current between devices, there cannot be any latchup, as presented in Figure 1.3 in the case of a CMOS inverter.

**Reduction of short channel effects (SCE)** The reduction of the SCE is necessary to increase the operating frequency of circuits. This effect is related to the loss of control of the channel by the gate. In the case of SOI MOSFET, and more precisely Fully Depleted (FD) SOI MOSFET, the space charge in the thin film of

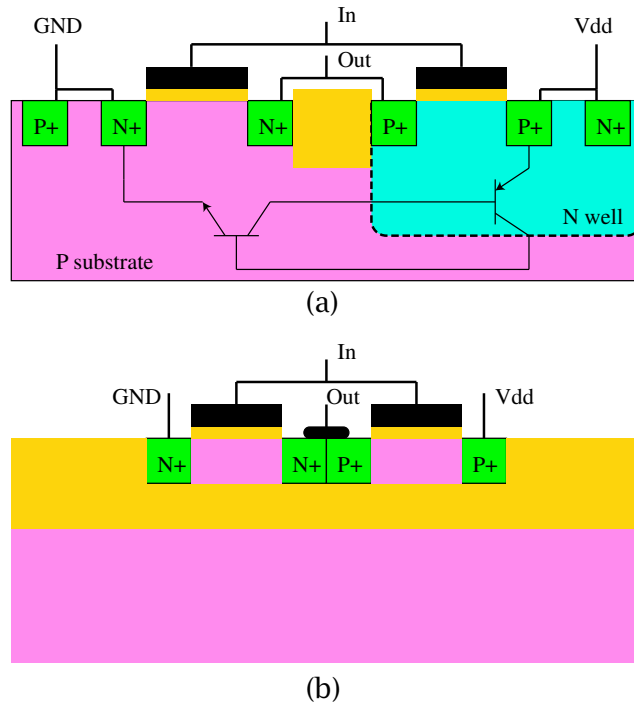


Figure 1.3: Cross section of a CMOS inverter in bulk (a) and in SOI (b) technology. The parasitic thyristor of the bulk inverter has been highlighted.

silicon is well controlled by the gate. As a consequence, the SCE are reduced when compared to classical bulk MOSFET.

**Better inverse subthreshold slope** The inverse subthreshold slope is defined as the inverse of the slope of the  $I_d$  vs  $V_d$  characteristic curve in the subthreshold regime. It has been proved and demonstrated [5] that the Fully Depleted SOI MOSFET has a lower inverse subthreshold slope than a bulk MOSFET, allowing better performances, in particular at low power supply.

### 1.3 The SOI materials

There are various kinds of SOI technologies depending on the thickness of the active film of silicon, the thickness of the insulator, the material used as insulator, the material used for the mechanical substrate, ...

In the next sections, the influence of the thickness of the silicon film will be shown, comparing the fully depleted (FD) and the partially depleted (PD)

MOSFET. Then we briefly describe the different substrates used in this work.

### ***1.3.1 Structure and properties of the various SOI MOSFET transistors, the influence of the silicon film***

#### ***1.3.1.1 Comparison between the structures of long channel FD and PD transistors***

The active film of silicon used to realize SOI MOSFET is at least partially depleted, as for a conventional bulk MOSFET. The maximum depth of the depletion zone can be approximated by the following equation, valid in the case of bulk MOSFET:

$$d_{max} = \sqrt{\frac{4\epsilon_{Si}\Phi_F}{qN_a}} \quad (1.1)$$

where  $\Phi_F$  and  $\epsilon_{Si}$  are the FERMI potential and the permittivity of the silicon,  $q$  is the charge of the electron, and  $N_a$  is the density of acceptors atoms.

This equation does not make any physical sense if  $d_{max}$  is larger than the thickness of the silicon film. But in that case, the silicon film will be completely depleted.

When the depletion zone extends over the entire thickness of the active film of silicon, the MOSFET is said to be fully depleted. If it is not the case, a small part of the silicon film is not depleted. It is called the floating body. The MOSFET is partially depleted. These two different structures are presented in Figure 1.4. Some properties of these devices are described in the next section.

#### ***1.3.1.2 Properties of FD and PD devices***

**Introduction** In order to express easily the difference between partially and fully depleted devices, a coefficient ( $\alpha$ ) has to be defined. This coefficient can be expressed as a function of the total gate capacitance, presented for both FD and PD in Figure 1.5. The gate capacitance of the FD is composed of three series capacitance, namely the front gate oxide capacitance, the capacitance of the silicon film and the buried oxide capacitance. The gate capacitance of the PD is composed of the front gate oxide capacitance connected to the depletion

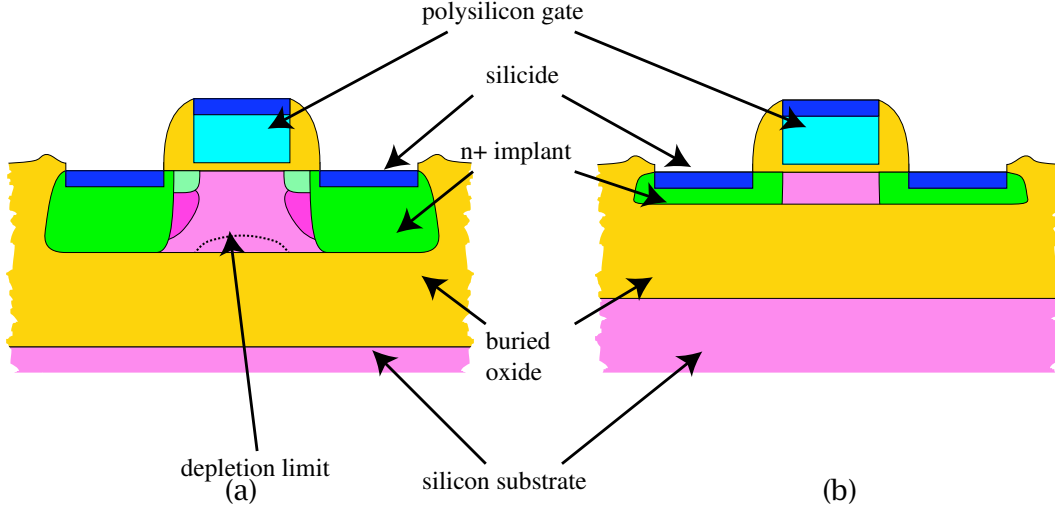


Figure 1.4: Cross section of a partially depleted (a) and a fully depleted (b) long channel SOI MOSFET.

capacitance of the silicon film.

The values of  $\alpha$  are given by the following equations for FD and PD MOSFET

$$\alpha_{FD} = \frac{C_{ox2}C_{si}}{C_{ox1}(C_{ox2} + C_{si})} \quad (1.2)$$

$$\alpha_{PD} \approx \frac{C_{depl}}{C_{ox1}} \quad (1.3)$$

where  $C_{ox1}$  and  $C_{ox2}$  are the gate and buried oxide capacitance,  $C_{depl}$  and  $C_{si}$  are the capacitances related to the depletion zone of the PD, and to the thin film of silicon.

The coefficient  $\alpha$  measures the efficiency of the coupling between the gate potential and the potential of the channel of the MOSFET ( $\Phi_s$ ) at the  $S_i - S_iO_2$  interface [5]. Better coupling is achieved when alpha is small.

Typically,  $\alpha$  is almost equal to zero for fully depleted SOI MOSFET, and to 0.3 ... 0.5 for partially depleted SOI MOSFET and bulk MOSFET. However, the value of  $\alpha$  increases for small devices, exhibiting the loss of control of the channel potential ( $\Phi_s$ ) by the gate.

**Saturation current** Using the classical charge sheet assumptions [7], it is possible to develop the expression for the saturation current of the long channel SOI MOSFET [8]:

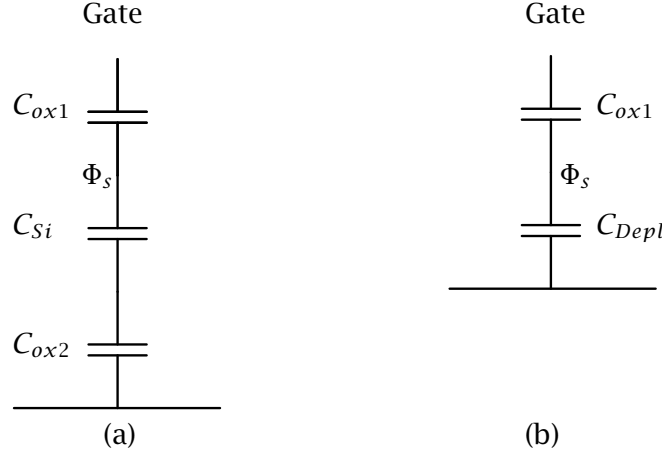


Figure 1.5: Simplified capacitive network seen from the gate of a fully depleted (a) and a partially depleted (b) SOI MOSFET

$$I_D = \frac{W}{L} \frac{\mu C_{ox1}}{2(1 + \alpha)} (V_{gs} - V_{th})^2 \quad (1.4)$$

where  $W$  and  $L$  are the width and the length of the transistor,  $\mu$  is the mobility,  $V_{gs}$  is the gate to source voltage, and  $V_{th}$  is the threshold voltage. From Equation (1.4), it is possible to deduce the following expression for the transconductance:

$$g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{W}{L} \frac{\mu C_{ox1}}{1 + \alpha} (V_{gs} - V_{th}) = \sqrt{2 \frac{W}{L} \frac{\mu C_{ox1}}{1 + \alpha} I_D} \quad (1.5)$$

From these ideal equations, it can be deduced that the fullydepleted device will have a higher current drive and transconductance than the partially depleted transistor with the same technological parameters, as the value of the coefficient  $\alpha$  is smaller for fully depleted than for partially depleted MOSFETs.

Moreover, partially depleted transistors have a special behavior in the saturation region called the kink effect. This effect is illustrated in Figure 1.6, and can be explained as follows. When the drain potential is raised, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs. The generated electrons move into the channel while the holes migrate to the lowest potential, which is the floating body. When a certain level of holes current is reached, the diode between the floating body and the source becomes forward biased. The body potential increases.

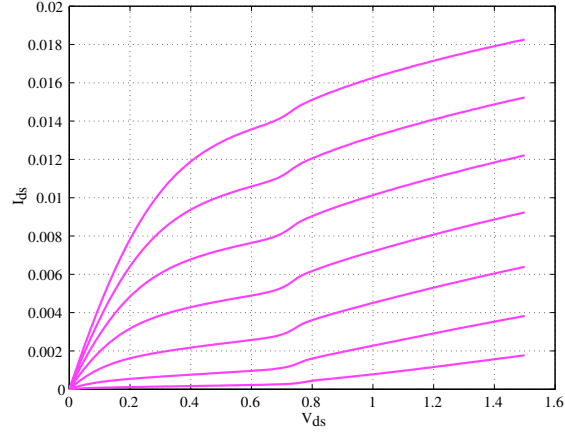


Figure 1.6: Output characteristic of a partially depleted SOI MOSFET with a gate length  $L = 0.25\mu m$  and a total width  $W = 80\mu m$

The “effective” threshold voltage of the MOSFET is reduced, as the potential of the body increases [5], inducing an increase of both the output current and the transconductance [9].

It is possible to avoid the kink effect by using a contact between the source or the ground and the floating body [10].

**Subthreshold slope** For SOI MOSFET transistors, the subthreshold slope can be expressed by

$$S = \frac{\partial V_{gs}}{\partial \log(I_d)} = (1 + \alpha) \frac{kT}{q} \ln(10) \quad (1.6)$$

where  $k$  is the BOLTZMANN constant,  $T$  is the temperature, and  $q$  is the charge of the electron.

Theoretically, the lowest possible value is 60 mV/decade, which is reached when  $\alpha = 0$ . Practically, values around 65 mV/decade can be obtained for long fully depleted devices at room temperature.

Partially depleted transistors cannot exhibit a subthreshold slope as good as fully depleted transistors do. But using some alternative structure of transistors, like the Dynamic Threshold MOSFET, which will be presented in Chapter 4, it is possible to obtain a nearly idealistic subthreshold slope in a partially depleted technology.



### 1.3.1.3 Threshold voltage

The threshold voltage of a PD MOSFET is defined in the same way as for a classical bulk MOSFET. Neglecting the interface charges, the threshold voltage can be expressed by

$$V_{th} = V_{fb} + 2\Phi_F + \frac{qN_a d_{max}}{C_{ox1}} \quad (1.7)$$

where  $V_{fb}$  is the flat band voltage,  $\Phi_F$  is the FERMI potential of the silicon,  $q$  is the charge of the electron,  $N_a$  is the density of acceptor atoms, and  $C_{ox1}$  is the gate oxide capacitance. The potential of the substrate is neglected for PD MOSFET in the expression of the threshold voltage, since it is left floating.

For FD transistors, the expression of the threshold voltage is much more complicated, since it is function of the state of the interface between the thin film of silicon and the buried oxide, which is called the back gate interface. Three different definitions of the threshold voltage can be obtained, if the back gate interface is either in depletion, in inversion or in accumulation. In this section, we will only cover the case of depletion, since it is the most common case.

When the back gate interface is in depletion, the threshold voltage can be expressed by

$$V_{th} = V_{fb} + 1 + \left( \frac{C_{Si}}{C_{ox1}} \right) 2\Phi_F - \frac{Q_{Si}}{2C_{ox1}} - \alpha_{FD} (V_B - V_{Bacc}) \quad (1.8)$$

where  $Q_{Si}$  is the depletion charge ( $Q_{Si} = -qN_a t_{Si}$ ;  $t_{Si}$  is the thickness of the silicon film) and  $V_B$  is the back gate voltage.

The back gate potential for accumulated back interface with inverted front interface ( $V_{Bacc}$ ) is given by

$$V_{Bacc} = V_{fb2} - \frac{C_{Si}}{C_{ox2}} 2\Phi_F - \frac{Q_{Si}}{2C_{ox2}} \quad (1.9)$$

where  $V_{fb2}$  is the flat band voltage for the back gate [5].

Usually, the buried oxide is thicker than the thin film of silicon. Then the

Equation (1.2) can be simplified to

$$\alpha_{FD} \approx \frac{C_{ox1}}{C_{ox2}} \quad (1.10)$$

If the back gate voltage is set to  $V_{Bacc}$ , the threshold voltage can be expressed by

$$V_{th} = V_{fb} + 2\Phi_F + \frac{qN_a t_{Si}}{C_{ox1}} \quad (1.11)$$

where  $t_{Si}$  is the thickness of the active film.

Comparing the expressions for threshold voltage of PD and FD transistors (Equations (1.7) and (1.11)), some properties can be deduced:

- If the same technological parameters are used ( $N_a$ ,  $C_{ox1}$ , ...), the threshold voltage of FD transistors will be lower than for PD transistors. This difference is given by

$$V_{thPD} - V_{thFD} = \frac{qN_a}{C_{ox1}} (d_{max} - t_{SiFD}) \quad (1.12)$$

- The threshold voltage of the FD MOSFET depends on the thickness of the silicon film. If the threshold voltage must be kept constant, when the thickness of the thin film is reduced, the doping level  $N_a$  must be increased, or  $C_{ox1}$  reduced. But an increase of the doping level  $N_a$  induces a reduction of the maximum depth of the depletion region  $d_{max}$ , as defined by Equation (1.1). As a consequence, there is a maximum in doping level that can be used for a given silicon thickness to ensure that MOSFETs are fully depleted.

Furthermore, if low doping level is used, like the natural doping level of the silicon film, the threshold voltage will be small, but nearly independent of the film thickness. Indeed, in that case, the threshold voltage will be equal to

$$V_{th} = V_{fb} + 2\Phi_F + \frac{qN_a t_{Si}}{C_{ox1}} \approx V_{fb} + 2\Phi_F \quad (1.13)$$

### 1.3.2 The position of industry

Since the 1980s, SOI CMOS has been identified as a possible method for increasing the performances of CMOS over that offered by simple scaling [5]. Prior to

the 1990s, SOI was not suitable as a substrate for mainstream applications. There were many barriers to its widespread use, the main ones being SOI material quality, device design, and steady progress in bulk CMOS performance through scaling. In the early 1990s, major companies such as IBM [11], started research projects on SOI. A few years later, some digital circuits demonstrated the benefit of using SOI at an industrial level [12] [13].

In the early 2000s, the microprocessors using SOI were shipped, and even Intel Corporation began to consider SOI as a future technology for VLSI circuits [14].

SOI is probably the future of CMOS for the next few years. But the last thing that is not clear yet, is what is the most suitable SOI technology for mainstream application? Partially or Fully Depleted SOI CMOS?

Answering that question is not easy, as two of the biggest microelectronic companies are still arguing to each other about that topic. After demonstrating that “*PD SOI has diminishing performance gain with scaling over standard bulk Si CMOS.*” [15] [16], researchers from Intel exhibit some results of a 50 nm FD SOI transistor demonstrating the benefit of using FD SOI transistors [14]. At the opposite, researchers from IBM are working on PD technologies, arguing that FD transistors do not allow the use of multiple threshold voltages. Indeed, higher threshold voltages are obtained by increasing the doping level of the channel ( $N_a$ ). The value of the maximum of depletion ( $d_{max}$ ) defined by Equation (1.1) is reduced. It is then more difficult to keep the transistor Fully Depleted. Also, PD transistors, unlike FD transistors, allow to use the technological solutions developed for bulk transistors [11] against SCE, drain induced barrier lowering (DIBL), ...

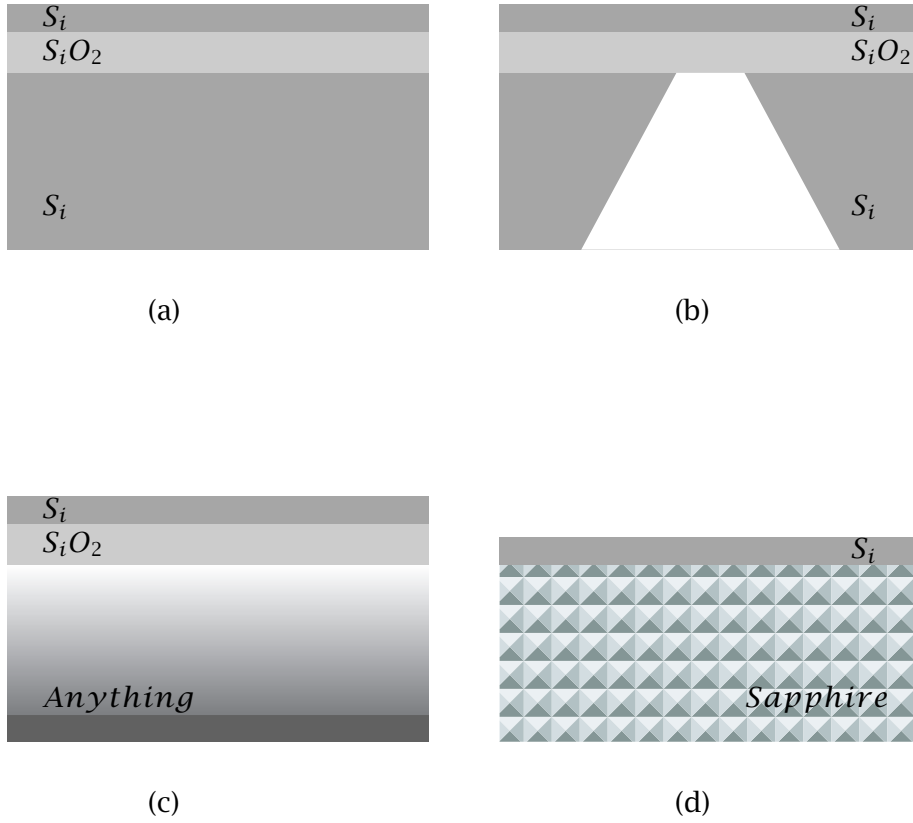


Figure 1.7: Cross section of the different SOI substrate used in this work. Classical or HRS SOI substrate (a), Silicon-on-Membrane substrate (b), Silicon-on-Anything (c), and Silicon-on-Sapphire (d)

## 1.4 Insulators and substrates used

In the following sections, the different kinds of SOI substrates that have been used for this work will be presented. Some advantages and drawbacks for RF applications of these substrates will be highlighted.

### 1.4.1 Classical SOI substrate

The classical SOI substrate used is presented in Figure 1.7a. Basically, it is composed of the thin film of silicon, a thick buried oxide laying on a medium resistivity substrate of silicon ( $\pm 20\Omega/cm$ ). Various processes are used to obtain SOI wafers:

- Separation by IMplantation of Oxygen or SIMOX: Oxygen ions are implanted beneath the surface of a bulk silicon wafer. Then, a thermal annealing al-

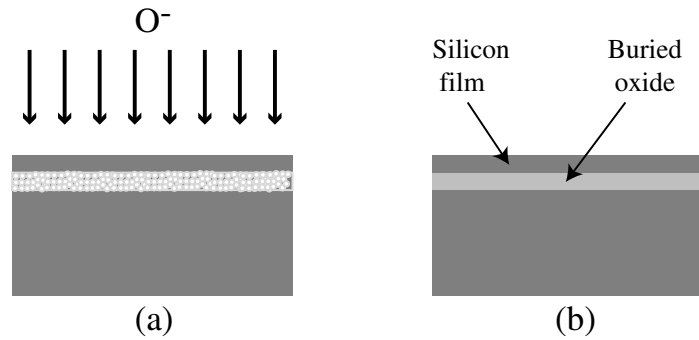


Figure 1.8: The SIMOX fabrication process: (a) Oxygen implantation, (b) results after annealing

lows creating a  $\text{SiO}_2$  layer buried inside of the silicon wafer (Figure 1.8). This layer is the buried oxide of the SOI wafer. Unlike usual implant used in microelectronics, which consists of the implant of a small number of impurities in the silicon, the implant used for SIMOX requires an enormous dose of oxygen ions. Indeed, to form the buried oxide the number of oxygen ions must be twice the number of silicon atoms. As a consequence, specific implanters have been developed specifically for mass production of the SIMOX process. If the SIMOX process is not optimized correctly, few silicon isles can be kept inside the buried oxide, inducing defects [17].

- **Wafer-bonding:** Wafer bonding materials are obtained by gluing two wafers together. This can be obtained by using some specific material layers or by creating hydrogen bonds between the two wafers. This method has been used intensively for the production of SOI wafers under the name of Uni-bond material, which is a trademark of the society SOITEC. The production steps of the SOI wafer are presented in Figure 1.9. First, a bulk silicon wafer is oxidized (wafer A). Then a high-energy implant of hydrogen ions is performed in order to create defects at a fixed depth in the silicon wafer. That wafer is then bonded to a silicon bulk wafer (wafer B), by using hydrophilic bonding. After a thermal annealing, the wafer A is divided into two parts; a small monocrystalline silicon which remains bonded to the wafer B, and the remainder of the wafer A. The remainder wafer A can still be used for the same process [18].

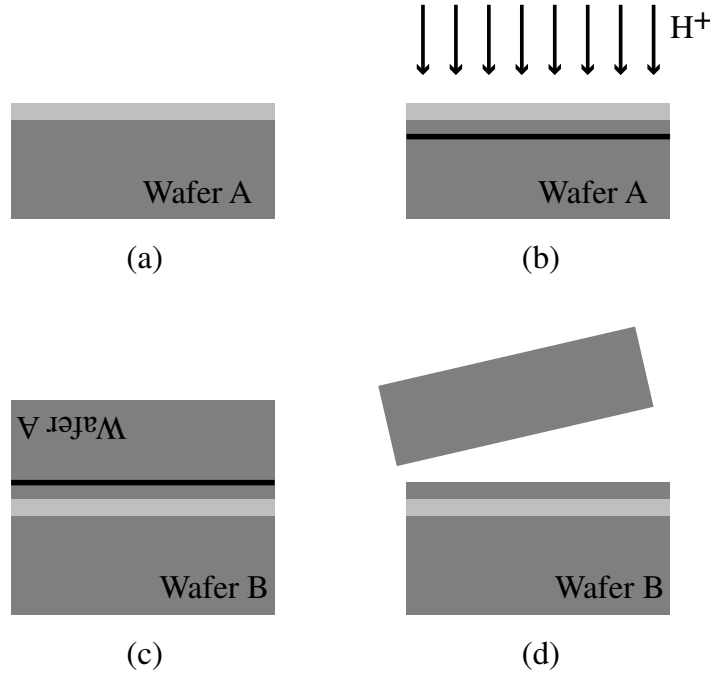


Figure 1.9: The Unibond fabrication process

Thanks to the buried oxide of the SOI structure, passive elements made on SOI, like transmission lines or inductors, can have better quality factor than in bulk technologies. Dielectric losses introduced by the substrate are usually lower in SOI than in RF bulk technologies [19]. Indeed, in order to reduce short channel effects, the silicon substrate used to fabricate RF BULK MOSFETs must be high to reduce the coupling between the drain and the source. As a consequence, the substrate is usually a low resistivity substrate ( $\ll 1\Omega/cm$ ) [20].

In fact, the resistivity of the SOI silicon substrate is independent of the devices that are made in the active film of silicon. It is then possible to have a medium resistivity substrate even when high doping level is required in the active film.

### 1.4.2 High Resistivity SOI substrate

As explained above, SOI can have lower dielectric losses for passive elements than bulk technologies. Using high resistivity silicon substrate (HRS) can reduce even more these dielectric losses. As we will show in the Chapter 5, the

resistivity of the substrate can have a strong influence on the losses of passive elements, like transmission lines or inductors.

Unfortunately, HRS SOI wafers are much more expensive than classical SOI wafers, as they require much more protections against contamination, in order to keep their resistivity to a high value, during the production of the wafer, but also during the CMOS process.

### **1.4.3 Silicon-on-Membrane**

*If the under-laying silicon substrate is a problem, we just have to remove it.*

This is the idea of the Silicon-on-Membrane, everywhere the substrate is a problem, it can be removed using bulk [20] or surface [21] micro-machining (Figure 1.7b). The substrate can be removed only on some part of the wafer in order to keep its mechanical properties. After that fabrication step, the devices are laying on top of a silicon dioxide membrane.

Obviously, removing the substrate under some components can affect their electrical behavior. In the case of a transmission line, removing the under-laying substrate will reduce the dielectric losses, but the effective permittivity of the medium will change. As a consequence, the lineic capacitance of the line will change, as well as its propagation constant and its characteristic impedance [22]. It is then necessary to re-optimize the design of components or circuits if the under-laying substrate is removed.

### **1.4.4 Silicon-on-Anything**

If the silicon substrate is a real problem, it can be replaced entirely (Figure 1.7c) by a more convenient mechanical substrate.

This is made, after the CMOS process, by using bonding techniques similar to those who were briefly described, when the Unibond process was presented.

It is possible to substitute, to the native silicon substrate a high quality substrate, like glass, for microwave operation [23] [24].

Changing substrate of a wafer is not enough to obtain optimal circuits on a technology. Indeed, substituting the substrate changes the electrical charac-

teristic of the wafer, as for Silicon-on-Membrane. The devices and the circuits must be optimized, taking into account the properties of the new mechanical substrate. Some results of integrated inductors made on a silicon and glass substrate are shown in Chapter 5. The use of glass instead of silicon induces higher peak quality factor, because of the low dielectric losses of the glass compared to silicon, but also a shift in the frequency of the maximum of the quality factor. The optimal frequency, for the use of the inductor, is then changed.

#### ***1.4.5 Silicon-on-Sapphire***

If the substrate is a problem for the applications, instead of using Silicon-On-Anything technique, the thin film of silicon can be grown on something else, like sapphire.

Silicon-on-Sapphire substrates are obtained by growing a silicon film on top of a monocrystalline sapphire substrate. This process is called *hetero-epitaxy*, since silicon and sapphire are different materials with different crystallographic structures. The difference between the lattice dimensions of silicon and sapphire introduces defects in the silicon film. These defects will induce a reduction of the mobility, which will then lower the performances of this technology compared to other kind of SOI [25].

Sapphire substrate has however interesting properties. Indeed, with an extremely high resistivity, a sapphire substrate allows using extremely high quality passive elements with nearly no dielectric losses.

Unfortunately, sapphire is also a non-reciprocal material. Its permittivity varies with the crystallographic plane used. The relative permittivity of the sapphire is equal to 9.4 or 11.6 depending on the orientation of the crystal [26]. Practically, the same capacitive structure may have different capacitance values depending on the crystallographic orientation of the substrate.



## 1.5 *Size Does Matter: Evolution of the Microelectronic*

Even if it is not based on any scientific aspect, the MOORE's Law is still driving the world of digital circuits, pushing the CMOS technologies to their limits. In order to fit the law, the size of the transistors are constantly reduced. Intensive work is done on the gate engineering. Also the number of available metal layers used for interconnect is increased. As a consequence, the overall density of integration on chip increases.

All these progresses made for digital applications have made silicon-based technologies, and especially SOI, a real contender for RF mixed analog-digital applications [27]. The gate length reduction of MOSFETs has increased significantly the cut-off frequency of transistors, allowing designing circuits working at several GHz [28]. Indeed, we will show with more detail in Chapter 4, that the cutoff frequency ( $f_t$ ) of a MOSFET approximately follows the relation

$$f_t \approx \frac{g_m}{2\pi C_{gg}} \quad (1.14)$$

where  $g_m$  is the transconductance and  $C_{gg}$  is the total input capacitance of the MOSFET transistor.

Reducing the gate length of a MOSFET induces an increase of its transconductance, which is proportional to  $1/L$ . The total capacitance being proportional to the area of the gate, the reduction of the gate length induces a reduction of the total input capacitance. As a consequence, the cutoff frequency of MOSFETs is increasing as the gate length is reduced. But as the dimension of the transistors are reduced, the source, drain and gate resistances are increasing. Thus technological advances are required in order to keep these resistances as low as possible (Silicidation [29], raised source-drain [14], metallic T-gate [30],É

As we will show in Chapter 4, other techniques allow to increase the performances of CMOS devices without any drastic scaling of the dimension, and especially in the fields of low power and low voltage application.

The increase of the numbers of metal layers in microelectronics has given the opportunity to design higher quality passive elements, such as inductors by stacking the different metal layers, reducing the conductor losses of these

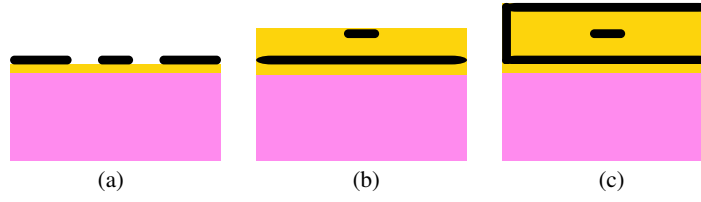


Figure 1.10: Different structures of transmission lines made on CMOS process: (a) CPW, (b) TFMS, and (c) a strip line

structures. It is also possible to draw these elements on the upper available metal layer to reduce the coupling between these elements and the substrate [31]. Furthermore, when only few metal layers were available, only coplanar wave guide (CPW) could be used as a transmission line. As the number of metal layers increases, it is possible to create other types of lines like thin film microstrip lines (TFMS) or even strip lines with characteristic impedances close to  $50\Omega$ . These different topologies, shown in Figure 1.10, are discussed in Chapter 5.

In the fields of RF characterization of MOSFETs, the evolution of the density of integration has an obvious influence on the design of the measurement structures. After each evolution, it is required to redesign the structure of the transistors and of the measurement pads in order to take the most benefit of the technological advances. Figure 1.11 shows the evolution of the dimension of the measured MOSFET that has been used during this work. The structure is evolving from a MOSFET with a gate length of  $0.75\mu m$ , which takes a significant surface inside the measurement pads, to a MOSFET with a gate length of  $0.08\mu m$ , which is nearly invisible within the pads.

With the reduction of the dimensions of the measurement pads and of the transistor, the 3D-structure of the transistors is also evolving, Figure 1.12 shows the difference between the MOSFET with  $L = 0.75\mu m$  and the MOSFET with  $L = 0.08\mu m$ . The use of more metal layers allows to have a more dense structure. But the transistor must be designed in order to minimize the effect of parasitic resistances and capacitances which are dependent on the tridimensional structure of the MOSFET. Indeed, depending on the 3D-structure of the MOSFET, some parasitic effects that were negligible for bigger devices needs to

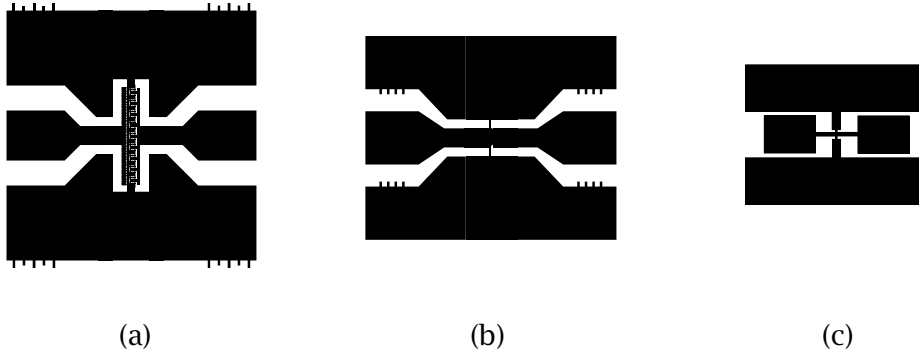


Figure 1.11: Top view of three MOSFETs embedded in RF measurement pads. These MOSFETs have the same W/L ratio and different gate length ((a): $L = 0.75\mu m$ , (b): $L = 0.25\mu m$ , and (c): $L = 0.08\mu m$ ).

be accurately modeled for smaller ones.

This problem will be considered in Chapter 3, where the small signal model of the MOSFET transistor is built.

## 1.6 Conclusion

In this chapter, we present the various SOI technologies that have been used in this work. Some of their properties were introduced. Also, the evolution of the technology was described, and its consequences were discussed.

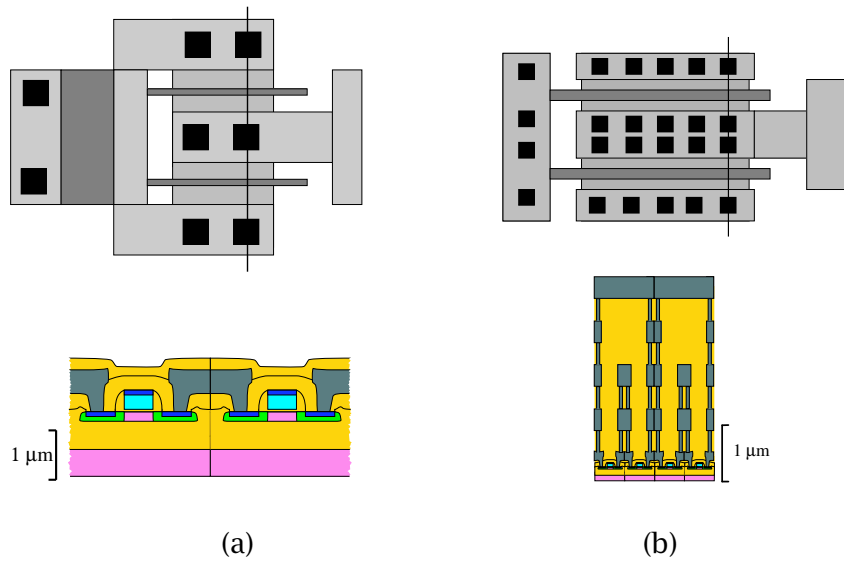


Figure 1.12: Top view and cross section of a MOSFET with  $L = 0.75\mu$  (a) and with  $L = 0.08\mu m$  (b). The respective scales have been adjusted in order to make both transistors visible

## References

- [1] R.R. Schmidt and B.D. Notohardjono, "High-end server low temperature cooling," *IBM Journal of Research and Development*, vol. 46, no. 6, pp. 739-751, November 2002.
- [2] A.G. Aipperspach et al., "A  $0.2\mu m$  1.8 v soi 550 mhz 64-b powerpc micro-processor with copper interconnects," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 11, pp. 1430-1435, 1999.
- [3] D.Flandre et al., "Fully-depleted soi cmos technology for low-voltage low-power mixed digital/analog/microwave circuits," *Analog Integrated Circuits and Signal Processing*, vol. 21, pp. 213-228, 1999.
- [4] D.Flandre, *High-temperature electronics*, chapter Silicon-on-insulator technology for high temperature metal oxide semiconductor devices and circuits, pp. 303-308, IEEE Press, r.kirschmann edition, 1998.
- [5] J-P.Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Kluwer Academic Publisher, 1991.
- [6] J.B.Kuo and S-C.Lin, *Low-voltage SOI CMOS VLSI devices and circuits*, Wiley interscience, 2001.

- [7] J.R.Brews, "A charge sheet model of mosfet," *Solid State Electronic*, vol. 21, pp. 345-355, 1978.
- [8] J-P.Colinge, "Fully depleted soi cmos for analog applications," *IEEE Electron Sevice Letters*, vol. 46, no. 5, pp. 1010-1016, Mai 1998.
- [9] O.Rozeau et al., "0.25 $\mu m$  soi technologies performance for low-power radio-frequency applications," *AICSP*, pp. 45-48, 2000.
- [10] J-P.Colinge, "Reduction of kink effect in thin-film soi mosfet's," *IEEE Electron Device Letter*, vol. 9, no. 2, pp. 97-99, 1988.
- [11] G.G.Shaidi, "Soi technology for the ghz era," *IBM Journal of Reserach and Developement*, vol. 46, no. 2/3, pp. 121-131, March 2002.
- [12] G.G.Shaidi et al., "A room temperature 0.1 $\mu m$  cmos on soi," *IEEE Transaction on Electron Device*, vol. 41, pp. 2405-2407, 1994.
- [13] D.J.Schepis et al., "A 0.25 $\mu m$  cmos on soi and its application to 4 mb sram," in *IEDM Tech. Digest*, 1997, p. 345.
- [14] R.Chau et al., "A 50nm depleted-substrate cmos transistor (dst)," in *IEDM Tech. Digest*, 2001, pp. 29.1.1-29.1.4.
- [15] R.Chau et al., "Scalability of partially depleted soi technology for sub-0.25  $\mu m$  logic applications," in *IEDM Tech. Digest*, December 1997, pp. 591-594.
- [16] K.Mistry et al., "Scalability revisited: 100 nm pd-soi transistors and implications for 50 nm devices," in *Symp. VLSI Tech Digest*, 2000, pp. 204-205.
- [17] H.Hovel, M.Almonte, J.Lee, D.Santana, A.Domeniccuci, and J.Bettinger, "Defects and electrical consequences in soi buried oxides," in *203 ECS meeting*. IBM Corporation, 2003.
- [18] C.Maleville, "Ulthrathin soi wafers fabrication and metrology," in *203 ECS meeting*. SOITEC, May 2003.
- [19] C.P. Yue and S.S.Wong, "On-chip spiral inductors with patterned ground shields for si-based rf ic's," *IEEE Journal on Solid State Circuits*, vol. 33, no. 5, pp. 743-752, May 1998.

- [20] J.M.Lopez-Villegas et al., "Improvement of the quality factor of rf integrated inductors by layout optimization," *IEEE Transaction on Microwave Theory and Techniques*, vol. 48, no. 1, pp. 76–83, January 2000.
- [21] M.Jurczak et al., "Silicon-on-nothing (son) - an innovative process for advanced cmos," *IEEE Transaction on Electron Devices*, vol. 47, no. 11, pp. 2179–2187, November 2000.
- [22] J-P.Raskin, G.Gauthier, L.P.Katehi, and G.M.Rebeiz, "Mode conversion at gcpw-to-microstrip-line transitions," *Trans. on Microwave theory and techniques*, vol. 48, pp. 158–161, Jan. 2000.
- [23] A.Wagemans et al., "A 3.5mw 2.5 ghz diversity receiver and a 1?2 mw 3.6 ghz vco in silicon-on-anything," in *IEEE International Solid-States Circuits Conference*, 1998.
- [24] J-B.Yoon et al., "Monolithic high-q overhang inductors fabricated on silicon and glass substrates," in *IEDM Tech. Digest*, 1999, pp. 753–756.
- [25] D.Levacq, M.Dehan, D.Flandre, and J-P.Raskin, "Figures-of-merit of intrinsic, standard doped and graded channel soi and sos mosfets for analog baseband and rf applications," in *203 ECS meeting*, 2003.
- [26] R.Shelby, J.Fontanella, and C.Andeen, "The low temperature electrical properties of some anisotropic crystals," *Journal of Phys. Chem. solids*, vol. 41, pp. 69–74, 1980.
- [27] C.Raynaud et al., "Fully-depleted 0.25 $\mu m$  soi devices for low power rf mixed analog-digital circuits," in *IEEE International SOI Conference*, October 1998, pp. 67–68.
- [28] M.Goffioul et al., "Microwave integrated cmos oscillators on silicon-on-insulator substrate," in *30<sup>th</sup> Microwave Week*, October 2000, pp. 407–410.
- [29] J.Chen, J-P.Colinge, D.Flandre, R.Gillon, J-P.Raskin, and D.Vanhoenacker, "Investigation of silicide process for thin-film soi microwave applications," in *48th Electrochemical society meeting*, September 1997, pp. 98–103.
- [30] T.Hirose, Y.Momiyama, M.Kosugi, H.Kano, Y.Watanabe, and T.Sugii, "A 185

ghz fmax soi dtmos with a new metallic overlay-gate for low-power rf applications," in *Proc. of the IEDM*, 2001, pp. 943-945.

- [31] J.N.Burghartz et al., "Microwave inductors and capacitors in standard multilevel interconnect silicon technology," *IEEE Microwave Transaction and Microwave Theory and Techniques*, vol. 44, no. 1, pp. 100-104, January 1996.

