# Impact of Power Loss in the Substrate on the Efficiency of RF GaN-on-Si HEMTs

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***Abstract*— In RF GaN-on-Si technology, the semiconducting Si substrate can couple to the overlying circuitry and cause substrate loss, which is known to degrade the performance of passive structures. An impact on active devices also exists. This paper presents the first experimental correlation between insertion loss measured on coplanar waveguide (CPW) lines and a degradation in the power added efficiency (PAE) of GaN-on-Si HEMTs. To quantify the PAE penalty suffered by using a lossy substrate, we propose a simple simulation procedure which accounts for the presence of a parasitic surface conductance (PSC) layer at the surface of the high resistivity Si. The simulated substrate, which can accurately reproduce the CPW line measurements of different wafers, is then used to generate an aggregated substrate resistance. A simple model of the power amplifier (PA) allows to estimate the PAE drop caused by power dissipation in the substrate. The simulated substrate impact, which can be as high as 15 PAE percentage points at 28 GHz, matches the experimentally observed difference between HEMTs fabricated on different substrates. Furthermore, the physics-based simulation enables analysis of operating frequency and dopant diffusion effects in Si. Finally, a specification on substrate effective resistivity for a negligible substrate impact on the PA is given.**

## I. Introduction

The combination of GaN HEMT performance and efficiency at high frequencies with the low-cost and maturity of a 200 mm Si substrate makes GaN-on-Si an important candidate for Frequency Range 3 (FR3, from ~7 GHz to ~25 GHz) to mm-wave bands [1]. One drawback of using a semiconducting substrate such as Si compared to, e.g. SiC, is the appearance of substrate loss, which can lead to increased harmonic distortion and a decrease of the performance of RF switches and passive structures [2], [3], [4], [5]. The precise origin of the increased substrate loss in GaN-on-Si is a widely studied topic [6], [7], [8], [9]. It is generally accepted that a parasitic surface conduction (PSC) layer forms at the surface of Si which degrades the substrate performance even when high-resistivity (HR) Si is used. The PSC layer is mostly formed by diffusion of Al and Ga atoms during metalorganic chemical vapour deposition (MOCVD) of the III-N layers, but other factors such as interface charge can contribute as well [5], [6], [10]. The substrate performance is typically assessed by measuring the insertion loss (α) along a coplanar waveguide (CPW) line. For high-performance engineered substrates, the effective resistivity ($\rho_{eff}$) is seen as a superior, metallization-agnostic figure of merit (FoM) [2], [11] (see Table I). When a PSC layer problem is present, $\rho_{eff}$ can decrease to well below the nominal resistivity of the HR Si ($\rho_{Si}$).

Going beyond the evaluation of substrate performance, this work aims to estimate the impact of a lossy substrate on the GaN-on-Si HEMTs utilized in power amplifiers (PAs), which constitute the main target application for GaN-on-Si. In turn, this will enable the derivation of substrate performance

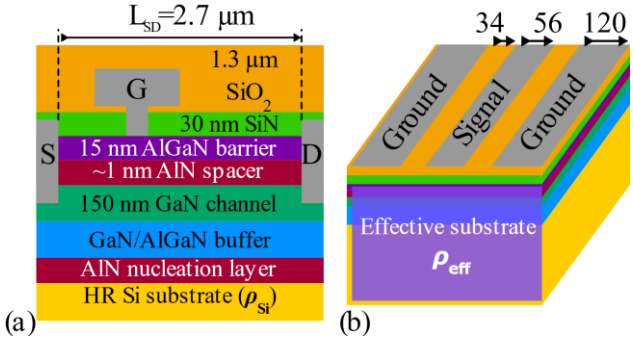


Fig. 1. (a) Epitaxial structure of the considered III-N stacks. (b) Coplanar waveguide line geometry (dimensions in micrometers) and effective substrate resistivity representation. The lines are fabricated using a ~1.4 µm-thick Al:Cu layer.

TABLE I
DEFINITION OF DIFFERENT RESISTIVITIES AND RESISTANCES USED IN THIS PAPER.

| Parameter | Definition |
|---|---|
| $\rho_{Si}$ [Ω·cm] | Nominal resistivity of the Si wafer. |
| $\rho_{eff}$ [Ω·cm] | Effective substrate resistivity, obtained from CPW measurements. It represents the resistivity of the equivalent homogeneous substrate that would cause the same loss ($\alpha$) as the non-homogeneous substrate under consideration. |
| $R_{sub}$ [Ω] | Lumped resistor used to represent the power dissipation in the substrate in the simplified PA model. |
| $R_v$,$R_h$ [Ω] | Individual vertical and horizontal lumped resistors used to mesh the substrate R-C network |

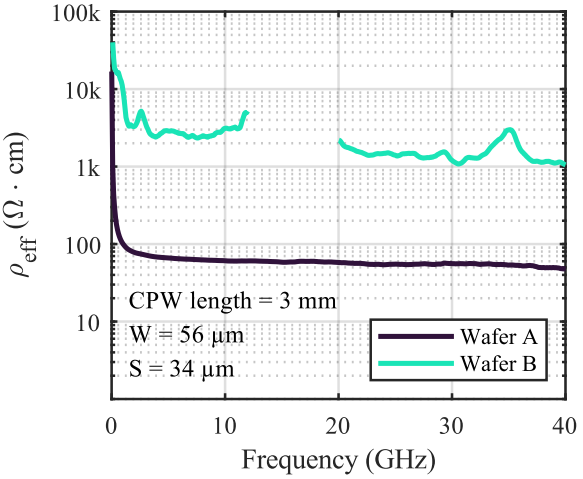


Fig. 2. Effective resistivity ($\rho_{eff}$) plotted against frequency for wafers A and B. Wafer A shows a relatively poor $\rho_{eff}$ of ~60 Ω·cm, while Wafer B has a high $\rho_{eff}$ of > 1 kΩ·cm. CPW dimensions are indicated in the inset and are chosen to provide a characteristic impedance $Z_c$ = 50 Ω (signal width W = 56 µm, spacing between the signal and planar grounds S = 34 µm).

specifications for high-efficiency HEMTs. The link between CPW FoMs such as $\rho_{eff}$ and the power dissipated under a HEMT is not straightforward. The complexity arises from the strongly non-homogeneous resistivity depth profile in the substrate and the difference between the CPW pitch and the HEMT source-drain spacing.

The paper is structured as follows. In Section II, we present, for the first time, load-pull measurements showing a degradation of the power added efficiency (PAE) correlated with decreased $\rho_{eff}$. The substrate signature is also observed in small-signal measurements of HEMTs fabricated on two different substrates. Section III introduces a simplified analytical model that can be used to extract an equivalent substrate resistance ($R_{sub}$), which is a common way of representing the substrate in electrical models of transistors [12], [13]. In such HEMT models, the substrate network must be either extracted at very low frequency or estimated, and the link to physical properties of the substrate or CPW FoM is not clear. The construction of the present model relies on relevant doping profiles and accounts for the pitch-dependent, non-homogeneous distribution of the electric field in the substrate. Section IV then connects, through the substrate model, the physical properties of the substrate with an associated power dissipation and consequently PAE penalty for the HEMT. The results are linked to the experimentally measured PAE difference between two substrates. The impact of operating frequency and $\rho_{eff}$ are discussed.

## II. EXPERIMENTAL EVIDENCE OF SUBSTRATE LOSS IN GAN-ON-SI HEMTS

### A. *RF substrates and HEMT devices*

Two different 200 mm GaN-on-Si wafers with different substrate effective resistivities are considered:

i. Wafer A: 1 mm-thick HR Si with ~1.85 µm-thick III-N layers.
ii. Wafer B: 725 µm-thick HR Si with ~1.8 µm-thick III-N layers.

All III-N growth were performed using MOCVD. The epitaxial stack is represented in Fig. 1a. Both wafers have a channel thickness of 150 nm and a 15 nm $Al_{0.28}Ga_{0.72}N$ barrier thickness with AlN spacer. The devices being characterized, similar on both wafers, consist of two 50 µm-wide fingers with a gate length $L_g$ = 150 nm.

1.4 µm-thick Al:Cu CPW lines were fabricated, together with the HEMT devices, on top of SiN passivation and a ~1.3 µm-thick $SiO_2$ layer. Ar-implantation was used to suppress the 2DEG underneath. The CPW line geometry is shown in Fig. 1b.

### B. *Effective resistivity extracted from CPW line measurements*

CPW lines were characterized and the substrate $\rho_{eff}$ was extracted from the RLCG parameters of the transmission line following the procedure described in more detail in [11]:

$$\rho_{eff} = \frac{F_{DIMS}}{G}, \quad (1)$$

in which $G$ is the measured shunt conductance and $F_{DIMS}$ a constant for a given CPW cross section. $G$ is extracted from $G = \Re(\gamma/Z_c)$, where $\gamma$, the propagation constant and $Z_C$, the characteristic impedance, are first extracted directly from measured S-parameters using the methodology developed in [14]. $F_{DIMS}$ accounts for the field distribution between the top (air) and the bottom (substrate) of the CPW line. It is based on closed-form analytical expressions derived in [15] and requires only geometric parameters (i.e., no information about the substrate composition is needed). The $\rho_{eff}$ represents the resistivity of the equivalent homogeneous substrate that would cause the same loss ($\alpha$) as the non-homogeneous substrate under consideration. It is considered a superior figure of merit compared to α as it is independent of the metallization material and thickness [2].

The results are shown in Fig. 2 for dies close to the centre of Wafers A and B. For Wafer A, $\rho_{eff}$ = ~60 Ω·cm, which is significantly lower than the nominal Si substrate resistivity ($\rho_{Si}$

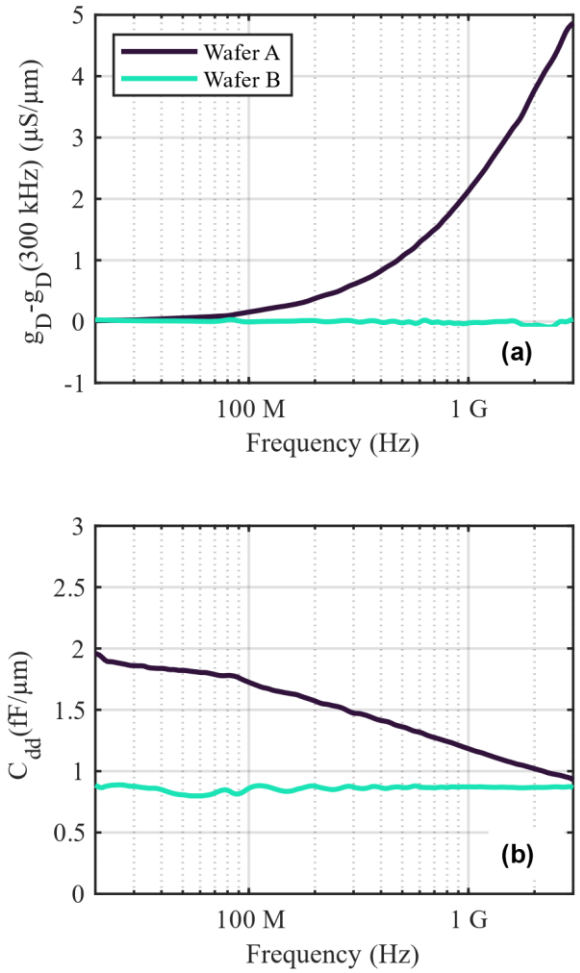


Fig. 3. Output conductance and capacitance extracted from small-signal measurements of HEMTs in off-state on Wafers A and B. The typical substrate effect is experimentally observed for Wafer A, while the more resistive Wafer B's transition frequency is too low to be measured.

> 3 kΩ·cm) owing to the formation of a PSC layer during the MOCVD growth of III-N layers. In most cases, the PSC layer is due to Al and Ga atoms diffusing into Si and doping the surface region (p-type). This PSC layer is significantly mitigated by improving the epitaxy in Wafer B. Consequently, its $\rho_{\text{eff}}$ stays high at values larger than 1 kΩ·cm (~3 kΩ·cm when averaged between 1 GHz and 5 GHz), which is competitive with state-of-the-art GaN-on-Si substrates [2]. The increased noise in the $\rho_{\text{eff}}$ extraction for Wafer B can be explained by the lower value of $G$ in eq. 1, which makes it relatively more sensitive to noise compared to Wafer A.

Because of higher substrate loss in Wafer A, a strong substrate signature is expected in HEMT output conductance ($g_D$).

### C. *Substrate signature in HEMT small-signal measurements*

The lossy substrate manifests itself as a transition in the output conductance of the transistor when plotted against frequency. As frequency increases, the free carriers in the PSC layer (in this case, holes which are majority carriers) cannot respond anymore to the small-signal AC voltage. The substrate capacitance then drastically decreases, accompanied by an increase in output conductance as demonstrated in [16], [17]. In first approximation and neglecting any dimensional effects that will be treated later, this transition frequency is proportional to the dielectric relaxation frequency of the substrate, which is given by:

$$f_{sub} \sim (2\pi\varepsilon_{Si}\rho_{Si})^{-1} \quad (2)$$

Output conductance ($Re(Y_{22})$) and capacitance ($Im(Y_{22}/\omega)$) are extracted from S-parameters measurements using an Agilent E5061B ENA. The devices are biased in off-state ($V_G < V_T$, $V_D$ = 0 V) to remove the impact of self-heating on $g_D$. For these devices, trapping effects have been shown to be small at $V_{DS,Q}$=10 V and are not impacting the measurements performed here. The access lines are de-embedded using the measurement of a Thru line [18]. Results are shown for both wafers in Fig. 3. A transition in $g_D$ and $C_{dd}$ is observed at a few hundreds of MHz for Wafer A. For Wafer B, showing almost 2 orders of magnitude higher $\rho_{\text{eff}}$ (and thus lower $f_{sub}$), the substrate-related transition takes place at frequencies lower than what is reachable with this measurement setup.

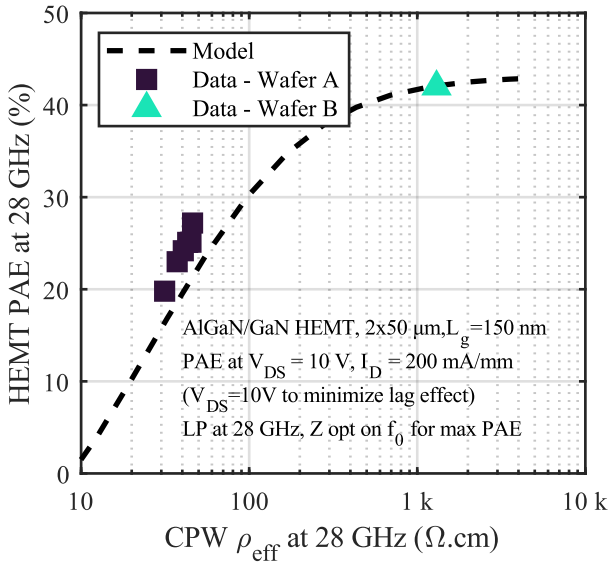


Fig. 4. Evidence of correlation between substrate loss and a device-level figure-of-merit: PAE. Load-pull measurements for devices fabricated on substrates characterized by different substrate losses show a clear correlation between a PAE degradation and the substrate losses. Note that under high intensity visible light the HEMT PAE is further degraded as well as the CPW losses (open squares).

### D. *Experimental correlation between PAE and substrate loss*

Further evidence of substrate loss can be found in a large-signal FoM such as PAE which is extracted from Load-Pull (LP) measurements.

The on-wafer fundamental LP setup is based on DELTA tuners (Focus Microwaves) which are directly connected to the RF probes for optimal impedance coverage. The large signal performance is measured in CW mode at a frequency of 28 GHz for a nominal bias point ($V_{DD}$ = 10 V, $I_D$ = 200 mA/mm) and the

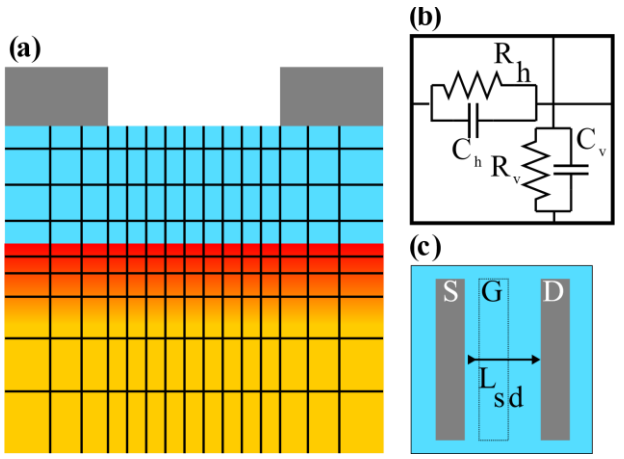


Fig. 5. (a) Representation of a typical RC mesh with a finer discretization in the PSC region. (b) Every cell of the RC mesh is made of one horizontal and one vertical RC element, and is connected to adjacent cells. (c) Top view of the simulated structure.

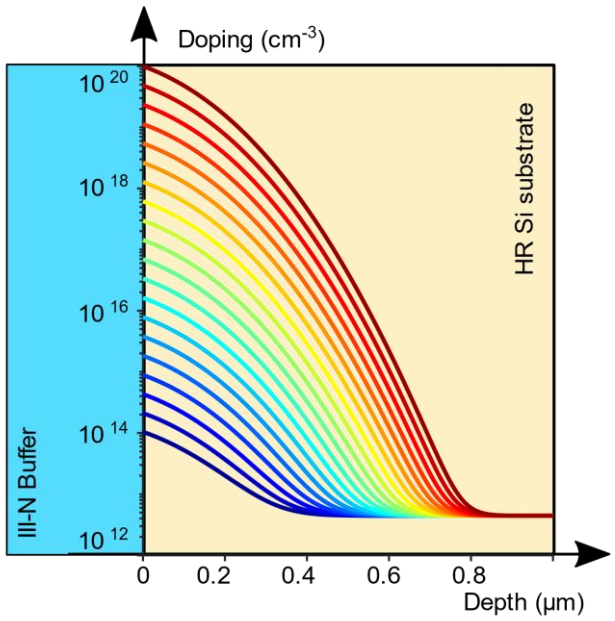


Fig. 6. Set of representative surface doping profiles used to represent substrates with varying effective resistivity (blue: limited PSC, red: significant PSC).

load impedance is set on each device for optimal PAE. For all wafers, this load impedance was close to $Z_L$ = (34 + 104$j$) Ω. During the large-signal measurement, the junction temperature rise is around ΔT=70°C at maximum PAE [1].

For each measured transistor, the small-signal parameters of a transmission line closely located on the same die at ~2 mm distance are also extracted using a PNA-X from Keysight. $\rho_{\text{eff}}$ can then be extracted as close as possible to the HEMT under test following the procedure described in Section II.B.

For Wafer A, the different data points represent different dies, illustrating a centre-to-edge variation in substrate loss across the wafer, which was not observed for Wafer B. The root cause for this variation is not known but could be linked to non-uniform conditions in the epitaxial reactor. It should be stressed that transistor-related parameters such as the 2DEG sheet resistance do not show such variation.

The influence of photogeneration (induced by turning the probe station light on) on the substrate loss was also studied for some dies of Wafer A, where a decrease in $\rho_{\text{eff}}$ together with a decrease in PAE were observed. The resulting variability in PAE does not originate from a $V_T$ shift as quiescent current is fixed for all measurements.

From Fig. 4, a clear correlation between PAE and $\rho_{\text{eff}}$ is observed with best results for $\rho_{\text{eff}}$ > 1 kΩ·cm at 28 GHz corresponding to Wafer B. A 17-percentage point difference in PAE is seen between the best die on the lossy Wafer A and the more resistive Wafer B.

The dashed line in Fig. 4 represents the physics-based model developed in this work, the conception of which constitutes the topic of the remainder of this paper. In the next sections, a combination of TCAD and electrical modelling will be used to better link the substrate properties with a representation of the substrate in a simple PA equivalent circuit.

## III. Substrate Electrical Modelling

### A. *Methodology*

To allow frequency-dependent modelling of non-uniform substrates, we introduce in this section a general approach.

i. An experimental spreading resistance profile (SRP) is used as doping profile in a 1D TCAD simulation of the substrate. The simulator includes SRH recombination equations as well as complete mobility modelling [19]. In GaN-on-Si technology, surface doping by Al and Ga is the main contribution to the PSC layer, and SRP allows extraction of the doping profile. The resulting DC simulation provides the free carrier distribution in the semiconducting substrate, from which a resistivity profile with depth is computed. Once this first step has been performed, a TCAD software is no longer required and different devices or frequencies can be simulated entirely in Matlab. The use of TCAD allows the simulation of various experimental conditions, such as temperature, which is known to affect substrate loss as described in [20], [21].

ii. In Matlab, an equivalent circuit of the substrate's cross section is built. It consists in an arbitrary number of cells (see Fig. 5a), where each cell comprises four elements (Fig. 5b). Each element contains the local electrical properties ($\rho$, ε) of the substrate:

$$R_h = \rho \frac{W_{cell}}{H_{cell}}; \quad (3)$$

$$R_v = \rho \frac{H_{cell}}{W_{cell}}; \quad (4)$$

$$C_h = \varepsilon \frac{H_{cell}}{W_{cell}}; \quad (5)$$

$$C_V = \varepsilon \frac{W_{cell}}{H_{cell}}, \quad (6)$$

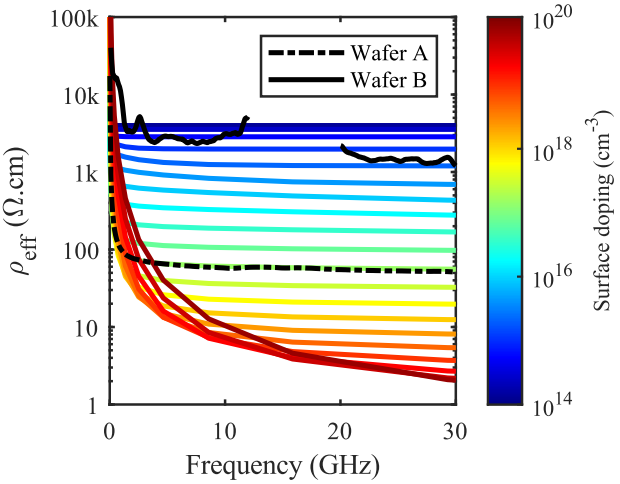


Fig. 7. Simulated effective resistivity as a function of frequency for the different PSC layer doping profiles shown in Fig. 6. The measured Wafers A and B are overlaid on the simulations, allowing to find the corresponding PSC profile.

where $W_{cell}$ and $H_{cell}$ are the width and height of the cell, respectively, and $\rho$ is provided by the TCAD-simulated resistivity profile mentioned above. The electrodes are modelled by a short circuit (i.e., zero-horizontal resistance elements are added in the relevant locations). Other boundaries are modelled as open circuits (i.e., dangling horizontal or vertical elements).

iii. The equivalent circuit is simulated at each frequency point to obtain the 2-port Y parameters between P1 and P2. P1 and P2 correspond to either source and drain (Fig. 5c) or signal and ground electrodes for the simulation of a transistor or a CPW line, respectively. From $Y_{12}$, equivalent $R_{sub}(f)$ and $C_{sub}(f)$ can be extracted (see Table I).

### B. *Model validation with CPW data*

The substrate network model is now used to reproduce CPW measurements. Because no SRP was available for the wafers in this study, a set of representative doping profiles were generated. These doping profiles are computed using the solution to Fick's second law:

$$N_A = N_{A,bulk} + n_0 \mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right), \quad (7)$$

in which $N_{A,bulk}$ is the doping concentration deep into the Si substrate (corresponding to 3 kΩ·cm as specified by the supplier), $n_0$ is the surface doping and $\sqrt{Dt}$ is the diffusion length. It is known that the doping profiles in Si respect eq. 7 for GaN-on-Si processes [22]. The diffusion length is set at 100 nm, which is typical for a GaN-on-Si thermal budget. $n_0$ is varied from $10^{14}$ cm$^{-3}$ (well-controlled Al diffusion) to $10^{20}$ cm$^{-3}$ (extremely severe Al diffusion). The resulting doping profiles are represented schematically in Fig. 6. The geometries for P1 and P2 were adapted to the CPW dimensions (see Fig. 2). After Y-parameter computation, the equivalent $R_{sub}(f)$ was used to extract $\rho_{eff}(f)$. Simulation results are shown in Fig. 7 overlaid with experimental data for Wafers A and B. The frequency dependence of $\rho_{eff}$ is well-captured by the model.

At low frequencies, the "slow-wave mode" translates into a substrate impedance dominated by the insulating buffer. For higher frequencies (quasi-TEM mode), the buffer impedance decreases and the substrate impedance is dominated by the conductive substrate. The transition frequency between these two regimes increases with decreasing substrate resistivity [23].

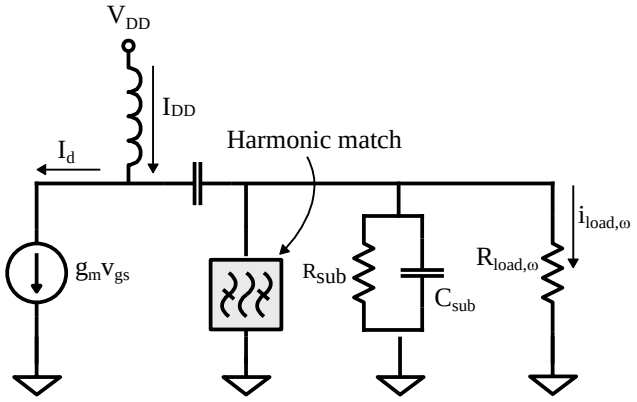


Fig. 8. Simplified circuit of the drain side of a power amplifier including substrate resistance and capacitance.

Each wafer can be related to a PSC surface doping by comparing its $\rho_{eff}(f)$ curve with a simulated curve. When experimental data is affected by noise, which is only the case for highly-resistive substrates, an average over a frequency range between 1 GHz and 10 GHz is used. Note that a single ($f$, $\rho_{eff}$) point can be associated to multiple surface doping values and it is thus important to consider the full frequency response. The match with experimental data is achieved for a surface doping of ~$10^{17}$ cm$^{-3}$ for Wafer A. For Wafer B, the match is less direct due to the measurement noise, however a surface doping upper bound of $10^{15}$ cm$^{-3}$ can be established.

Now that CPW measurements could be reproduced and the modelling methodology validated, dimensions can be modified to match a typical HEMT device.

## IV. Estimation of Power Loss in the Substrate for GaN-on-Si PAs

In this section, the substrate model introduced in Section III will be applied to typical transistor drain-source spacings (see Fig. 5c). The resulting $R_{sub}$-$C_{sub}$ will then be used in a PA simplified analytical model to estimate substrate power loss.

### A. *Analytical evaluation of $R_{sub}$ impact on HEMT performance*

Fig. 8 shows a simplified large-signal equivalent circuit of the drain side of a power amplifier [24]. In this circuit, the equivalent substrate network has been added between the source and drain nodes, in parallel with the load resistor. While the capacitance $C_{sub}$ can be compensated for by matching networks, $R_{sub}$ will lead to a shunt power loss and consequently efficiency degradation [25].

For this simplified circuit and considering B-class operation, a derivation analogous to what is done in [26] can be followed to obtain an analytical expression for the efficiency (B. Parvais and S. Yadav, private communication, 2024):

$$PAE = \frac{\pi}{4}\theta\left(1 - \frac{V_{knee}}{2V_{DD}}\right), \quad (8)$$

with

$$\theta = \frac{R_{sub}}{R_{load}+R_{sub}}, \quad (9)$$

in which $V_{knee}$ is the HEMT knee voltage, $V_{DD}$ is the supply voltage and $R_{load}$ the load resistance. Assuming that the small-signal $R_{sub}$ causes power dissipation during large-signal operation, the finite substrate resistivity will lead to a PAE penalty that increases as $R_{sub}$ decreases.

### B. *Modelling of $R_{sub}$ and discussion*

The impact of a conductive substrate on the PAE is now explored using the model described earlier. The same set of doping profiles is used as in Section III and the total dielectric thickness and permittivity are adapted for the simulation of a transistor (S/D contacts lie directly on the III-N, while CPW lines lie on an additional ~1.3 µm of $SiO_2$). The lateral dimensions of a typical HEMT ($L_{SD}$ = 2.7 µm) are then used to create the RC network.

Results for $R_{sub}$ and the resulting PAE penalty percentage points are shown in Fig. 9. The PAE penalty is calculated as the difference between the maximum value ($\theta$ = 1 in eq. 8) and the calculated value with finite $R_{sub}$. $R_{sub}$ is given for a 100 µm-wide device similar to what was measured above (Fig. 4). The results from Fig. 9 are discussed in detail in the following.

For very low frequency, the insulating buffer has a very large impedance. As a result, the conductive substrate is effectively disconnected from the HEMT and the aggregated $R_{sub}$ is very high, regardless of the doping in the PSC layer. The resulting PAE penalty is negligible.

At medium to high frequencies, the impedance of the insulating buffer decreases and the HEMT sees the conductive substrate, leading to a reduced $R_{sub}$ and a decrease in PAE. Counterintuitively, for a given frequency the evolution of $R_{sub}$ and PAE penalty with PSC doping is non-monotonous (i.e., there exists a minimal $R_{sub}$). Indeed, for a very conductive PSC layer, the transition frequency $f_{sub}$ from which the substrate starts to conduct can possibly be higher than the operating frequency, and equivalent $R_{sub}$ can be high with no PAE penalty. This regime correlates to the "slow-wave mode" in CPW line data. However, using low-resistivity Si for the realization of GaN-on-Si MMICs is not an acceptable solution, as such a circuit would suffer from increased crosstalk and the integration of low-quality factor passive elements. At the other end of the PSC layer doping spectrum (low doping), $f_{sub}$ is well below the operating frequency but $R_{sub}$ stays high owing to the highly resistive substrate.

Owing to more significant field penetration at high frequency, the worst-case PAE penalty increases with frequency: from less than one point at 100 MHz, a > 40-percentage point drop in PAE is predicted at 28 GHz for a surface doping of ~$10^{19}$ cm$^{-3}$. Consequently, a careful engineering of the RF substrate is critical to enable high-efficiency PAs at FR3 and mm-wave bands. To keep the impact of substrate loss under control with a PAE penalty of less than 1 percentage point regardless of the operating frequency, surface doping should be limited to ~$2 \times 10^{15}$ cm$^{-3}$.

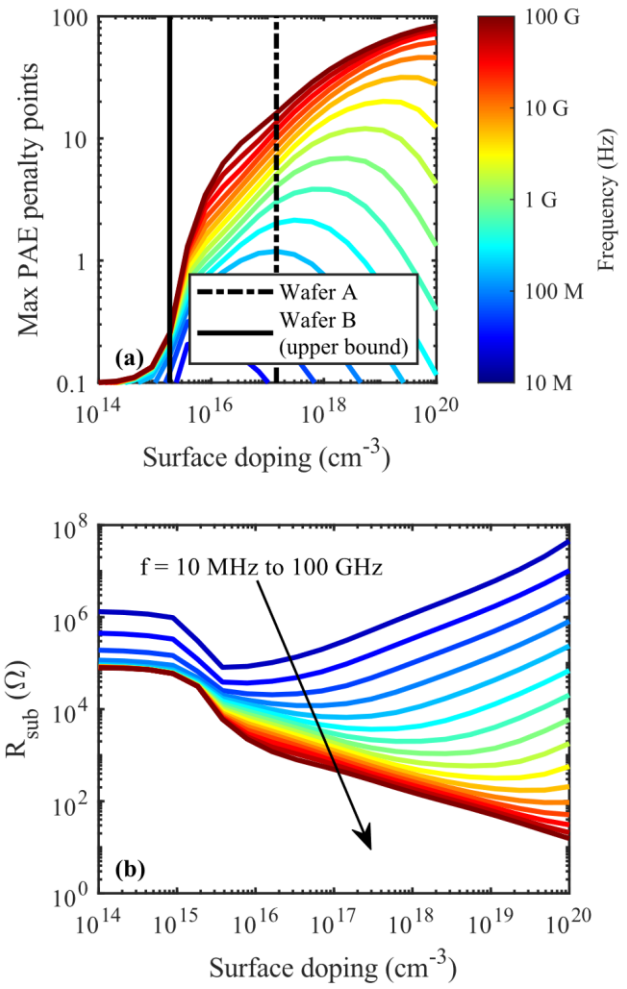


Fig. 9. (a) PAE penalty as a function of the simulated PSC layer surface doping for frequencies logarithmically spaced between 10 MHz to 100 GHz. The measured wafers are added in black after correlating effective resistivity with PSC surface doping. (b) Corresponding $R_{sub}$. The considered transistor has source-drain spacing of 2.7 µm.

### C. *Experimental validation and substrate specification*

Finally, it is possible to place Wafers A and B on the PAE penalty plot of Fig. 9a using the surface doping that fits the experimental $\rho_{eff}(f)$ (see Fig. 7). The predicted PAE penalty suffered when moving from Wafer B to Wafer A is ~15 percentage points at 28 GHz.

The information contained in Fig. 7 and Fig. 9 is now used to generate the dashed line $PAE(\rho_{eff}$ at 28 GHz) in Fig. 4. This curve is constructed as:

$$PAE\left(\rho_{eff}\ at\ 28\ GHz\right) = PAE_{MAX} - PAE\ penatly\ \left(\rho_{eff}\ at\ 28\ GHz\right), \quad (10)$$

where $PAE_{MAX}$ is estimated by adding the measured PAE for Wafer B to the predicted PAE penalty for Wafer B (~0.8 %). The resulting match between the model and the measured data points for Wafer A is excellent (Fig. 4), capturing both absolute values and trends, notably an expected saturation in PAE for quasi-dielectric substrates.

Based on Fig. 9, it is also possible to derive a specification

for $\rho_{\text{eff}}$. To keep the PAE penalty contained below 1 percentage point at all frequencies, a substrate at least as good as Wafer B must be used. For this particular HEMT source-drain spacing, this corresponds to a minimal $\rho_{\text{eff}}$ of 3 kΩ·cm provided that the main cause of substrate loss is Al and Ga doping diffusion.

## V. Conclusion

The substrate resistivity can have a significant impact for GaN-on-Si PAs, which becomes more severe as the operating frequency increases. In this paper, we presented a comprehensive simulation approach to link CPW figure-of-merit $\rho_{\text{eff}}$ to potential PAE drop caused by power dissipation in the lossy substrate. A physics-based distributed model of the non-uniform III-N stack was implemented to extract the equivalent substrate resistance. The model was validated against LP measurements. It was shown that for a $\rho_{\text{eff}} > 3$ kΩ·cm, there is no significant efficiency decrease (less than one percentage point). However, for a lower $\rho_{\text{eff}}$ of ~60 Ω·cm, the PAE penalty can be of up to 15 percentage points, depending on the operation frequency.

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