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LINEARITY ANALYSIS IN DOUBLE GATE GRADED-CHANNEL SOI DEVICES APPLIED TO 2-MOS MOSFET-C BALANCED STRUCTURES

R. T. Doria[1], A. Cerdeira[2], J. P. Raskin[3], D. Flandre[4] and M. A. Pavanello[1,5]

[1] LSI/PSI/USP, University of Sao Paulo
Av. Prof. Luciano Gualberto, trav.3 n.158, 05508-900 – São Paulo, Brazil
rdoria@lsi.usp.br

[2]Sección de Electrónica del Estado Sólido (SEES), CINVESTAV
Av. IPN No. 2508, Apto. Postal 14-740, 07300 DF, México

[3]Laboratoire d'Hyperfréquences
[4]Laboratoire de Microélectronique, Université Catholique de Louvain
Place du Levant 3, Maxwell Building, B-1348 Louvain-la-Neuve, Belgium

[5]Electrical Engineering Department, Centro Universitário da FEI
Av. Humberto de A. Castelo Branco, 3972, 09850-901 – São Bernardo do Campo, Brazil

This paper examines the linearity of 2-MOS MOSFET-C balanced structures using conventional and Graded-Channel (GC) Gate-All-Around (GAA) devices. The distortion analysis has been performed through the evaluation of third order harmonic distortion (HD3). The study has been carried out through experimental results, two-dimensional process and device simulations. Along this work, the best operation bias in terms of HD3 is determined for each analysed device and the couple device that exhibits lower HD3 is pointed out. The use of GC GAA devices in 2-MOS structures has showed to improve the linearity in relation to the conventional GAA. Finally, a discussion over the non-linearities causes is performed clarifying their origins and the improvement provided by the adoption of GC GAA devices in 2-MOS structures.

INTRODUCTION

When transistors are applied in analog circuits such as amplifiers (1,2) and continuous-time filters (3,4), some specific cares must be taken under consideration, since MOS transistors present non-idealities, which generate signal distortion. Therefore, the architecture of the device to be used is extremely important in order to improve its linearity properties. Besides that, depending on the application transistors showing different features are desirable. Thus, transistors of high gain are required for amplifier designs, while long transistors must be used for filters purposes since this application requires on-resistance higher than a few hundreds kΩ (5).

In this work we will carry out the evaluation of the linearity in Gate-All-Around (GAA) MOS transistors. These are double gate transistors (Figure 1(A)) which have their channel region surrounded by gate oxide and gate material. As the contribution of the current through the channel edges is negligible, the current preponderantly flows through

both the top and the bottom sides of the silicon film (6). The GAA technology has been reported in different studies showing several advantages in relation to planar single gate fully depleted SOI MOSFETs such as higher gain, improved transconductance, nearly ideal subthreshold slope and reduced short channel effects. In case of very thin silicon films the benefits of the volume inversion can also be observed (7).

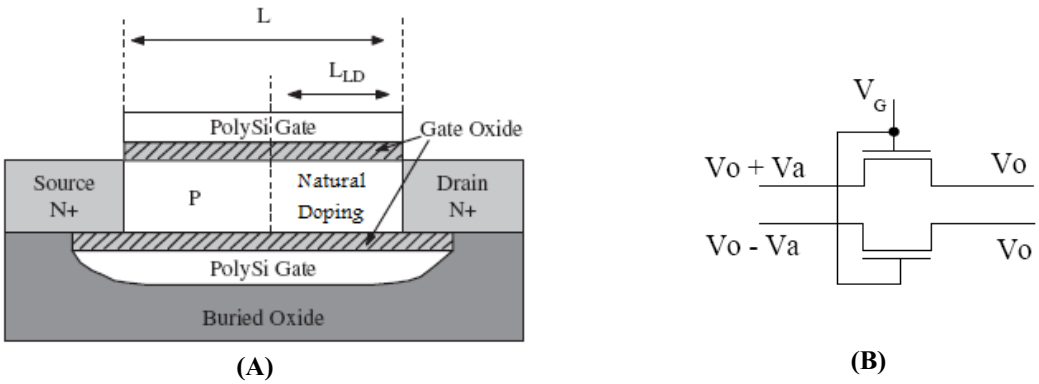

Figure 1. Cross-section of the Graded-Channel Gate-All-Around transistor (A) and 2-MOS balanced structure used in MOSFET-C filters (B).

Additionally to standard uniformly doped GAA transistors, the GAA devices evaluated along this work have been fabricated with the Graded-Channel (GC) architecture, whose cross section is presented in Figure 1(A). The GC transistor can be produced through a simple mask arrangement in the CMOS fabrication process, which is responsible for the preservation of the natural wafer doping in a region of length L_{LD} near the drain. Thus, this region can be considered as an extension of the drain and the overall threshold voltage is controlled by the rest of the channel, which becomes equal to the effective channel length ($L_{eff} = L - L_{LD}$) of the device, in saturation. The GC architecture has proven to provide excellent analog characteristics (i.e. GC presents low output conductance leading to an extremely large open-loop gain), since the majority of the potential applied to the drain drops in the interior of lightly doped region (8,9).

Recently, several works have highlighted the superior linearity properties presented by GC GAA. According to reference (10), 3μm long GC GAA devices operating in saturation as amplifiers have shown improvements in the order of 20 dB in the total harmonic distortion in relation to the single gate device. In reference (11), a comparison between the non-linearities exhibited by uniformly doped and GC GAA transistors is performed showing reduction of 30 dB in the total harmonic distortion when the GC GAA is applied. The improved performance of the GC GAA with respect to uniformly doped GAA is also presented for different channel lengths in reference (12), where a discussion on causes of the non-linearities is done. On the other hand, reference (13) exhibits the distortion behaviour of GC GAA devices operating in triode as continuous-time filters implemented through the use of 2-MOS (Figure 1(B)) or 4-MOS resistive structures. Here, the harmonic distortion is evaluated for a targeted on-resistance and, when applied to the 4-MOS structure the GC GAA outperforms the uniformly doped device by 7 dB.

The use of continuous-time antialias filters is primordial to any analog-to-digital conversion. However, the application of a single transistor as a resistive structure (i.e. source and drain are used as the resistor terminals and the gate voltage is tuned for a targeted on-resistance) results in a high harmonic distortion. Consequently, 2-MOS and 4-MOS balanced structures (14,15) have been frequently applied with the aim of reducing non-linearities, once these are differential structures that cancel out even order harmonics such as the second order distortion (HD2), commonly cited as the main non-linearity source in a single transistor circuit. Thus, the total harmonic distortion (THD) presents a significant reduction and is given mainly by the third order distortion (HD3).

This work presents an evaluation of the non-linearities presented by 2-MOS structures composed by uniformly doped and GC GAA devices as a function of the applied gate voltage. For the 2-MOS GC GAA circuits the determination of optimal bias condition and the L_{LD}/L ratio that exhibits the best linearity response is also performed. Along this study, third order harmonic distortion has been taken as the main figure of merit and has been obtained through the application of the Integral Function Method (IFM) (16,17) which allows the distortion determination based on DC measurements, without the need of AC characterisation as occurs with Fourier-based methods.

DEVICES CHARACTERISTICS AND MEASUREMENTS

The GC GAA transistors have been fabricated starting from a p-type wafer with concentration of $10^{15}cm^{-3}$ according to the process described in reference (18). The measured devices are composed by three fingers connected in parallel with both channel length and channel width (W) equal to 3 μm. The final thicknesses of the gate oxide, the silicon film and the buried oxide are 30 nm, 80 nm and 390 nm, respectively. Transistors with several L_{LD}/L were produced with the threshold voltage implanted region presenting p-type doping level around 10^{17} cm^{-3}.

Coupled process and bi-dimensional numerical simulations were performed using the Athena (19) and Atlas (20) tools, respectively. Analytical models accounting for the bandgap narrowing, doping-dependent carrier lifetime and mobility degradation due to both vertical and lateral electrical field were included in the simulation file. Except for the maximum values for low field electron and holes mobility of the Klaassen model, which have been set to 510 and 170 $cm^2/V.s$, respectively, default simulator coefficients were used. Uniformly doped GAA devices (named hereafter conventional GAA) have also been simulated in order to permit for a performance comparison.

Figure 2(A) shows the transfer characteristics of the drain current as a function of the gate voltage overdrive ($I_{DS} - V_{GT}$) at a fixed drain bias (V_{DS}) of 1.5 V for measured and simulated GC GAA devices with several L_{LD}/L ratios. As expected, the current rises with L_{LD} due to the reduction of the effective channel length. In Figure 2(B), the curves of the transconductance as a function of the gate voltage overdrive ($g_m - V_{GT}$) are exhibited for the same devices, and an increase in maximum g_m can be observed for the experimental and simulated curves when the GC GAA is applied. Additionally, there is a good agreement between measured and simulated curves presented in figures 2(A) and

2(B), independently of the GC GAA L_{LD}/L ratio, validating the process/device simulations at the device level.

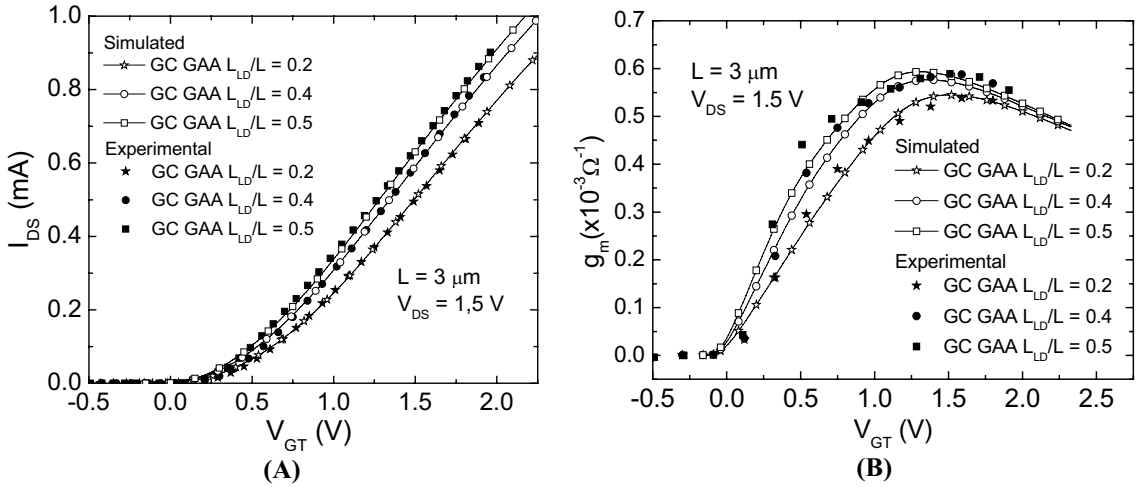

Figure 2. Simulated and measured (A) I_{DS} *vs.* V_{GT} ($V_{GT} = V_{GF} - V_{TH}$) and (B) g_m *vs.* V_{GT} with $V_{DS} = 1.5$ V for GC GAA devices with channel length of 3 μm.

The total harmonic distortion (THD) and the third order harmonic distortion (HD3) have also been extracted for measured and simulated devices as can be seen in figures 3 (A) and 3 (B), respectively. For the determination of both THD and HD3, the input signal was considered as DC voltage bias (V_0) associated to a sinusoidal-like signal of amplitude Va.sin(x) with $-\pi/2 < x < \pi/2$. Thus, the applied voltage to the drain of the devices is $V_D = V_0 \pm Va$. The harmonic distortion has been extracted for devices biased at $V_0 = 0$ V for Va ranging from 0 to 2.0 V at a fixed gate overdrive voltage V_{GT} of 2 V ($V_{GT} = V_{GS} - V_{TH}$ where V_{TH} is the threshold voltage).

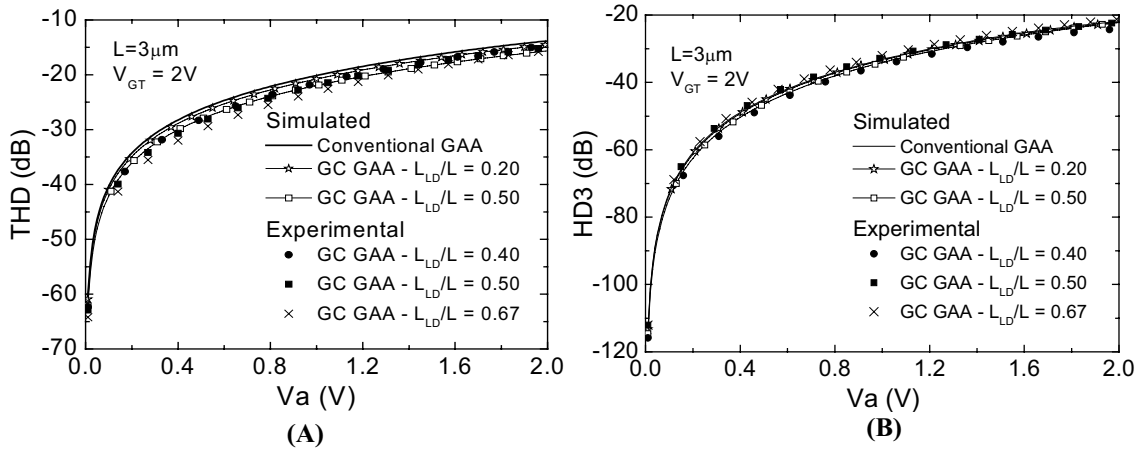

Figure 3. Measured and simulated curves of (A) THD (13) and (B) HD3 as a function of the input signal (Va) for the conventional and GC GAA devices (13).

The combination of the results from Figures 2 and 3 allows for using the 2D simulations as a tool for studying the 2-MOS circuit performance with conventional and GC GAA. Indeed, from Figure 3 not only THD, but also HD3, which is the dominant distortion in 2-MOS balanced structures, are validated. With this purpose the circuit analysis module of the Atlas tool has been employed with the same set of models adopted for the single device simulation presented in Figures 2 and 3.

HARMONIC DISTORTION EVALUATION

The 2-MOS structure harmonic distortion analysis has been performed through the determination of the third order harmonic distortion (HD3) which is closer to THD in balanced differential circuits, since the second harmonic distortion, which generally dominates the non-linearities in single transistor circuits, is partially suppressed and presents a significant reduction (14). As previously mentioned, in order to obtain HD3 directly form DC transfer characteristics, the Integral Function Method has been applied.

Considering that the 2-MOS structure input signal is given by a DC voltage bias (V_0) associated to a sinusoidal signal of amplitude Va, in order to evaluate HD3 as a function of V_{GT} aiming the determination of the operation bias voltage that presents the better linearity, the drain current (I_{DS}) *versus* drain voltage ($V_D = V_0 \pm Va$) characteristic has been simulated for V_D varying from –0.5 to 0.5 V for several V_{GT} between 0.6 V and 2.1 V. The minimum V_{GT} simulated has been chosen to keep the devices operating in the triode regime. The simulations have been performed for long devices of L = 10 μm with the purpose of keeping the on-resistance around 20 kΩ in the worst case in order to allow for a frequency bandwidth matching with the use of typical capacitors values. The curves of HD3 as a function of V_{GT} for devices with various L_{LD}/L ratios at a DC bias V_0 of 0 V are presented in Figure 4(A) for an input signal amplitude Va of 0.35 V and in Figure 4(B) for Va = 0.45 V. In a 2-MOS differential structure input amplitudes of 0.35 V and 0.45 V represent peak-to-peak signal amplitudes of 700 mV and 900 mV, respectively.

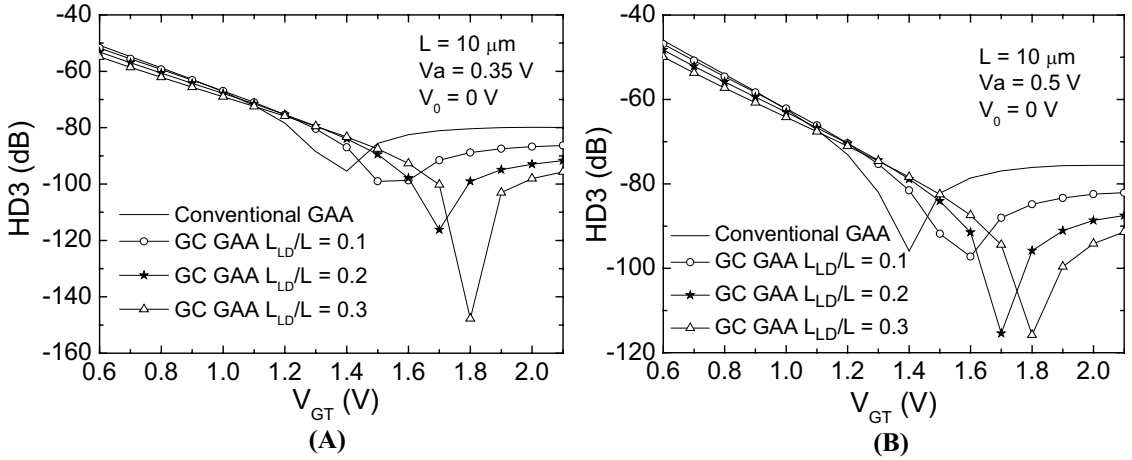

Figure 4. Simulated HD3 *vs.* V_{GT} curves for 2-MOS balanced structures with 10 μm-long conventional and GC GAA devices at an input amplitude Va of (A) 0.35 V and (B) 0.5 V.

Figure 4(A) shows the better linearity results among the studied range of input amplitudes (i.e. the larger linearity peaks). For values of V_{GT} inferior to 1.1 V, all the devices have presented a similar behavior and only a slight improvement on HD3 inferior to 4 dB can be observed for GC GAA transistor of $L_{LD}/L = 0.3$ in relation to the conventional one. When V_{GT} is increased over 1.1 V linearity peaks are seen at different gate voltages for each device. These peaks become more accentuated as L_{LD}/L rises, yielding higher linearity. For $V_{GT} = 1.8$ V, the GC GAA of $L_{LD}/L = 0.3$ presents HD3 inferior to -145 dB which represents 65 dB improvement in relation to the conventional device at the same gate bias. Thus, 2-MOS structures made with $L_{LD}/L = 0.3$ transistors at a gate voltage of 1.8 V give the impression to be the best choice for the current analysis.

However, biasing the devices at this linearity peak is unpractical due to process and temperature variations, which can move the HD3 peak through V_{GT} (4). Thus, a more realistic analysis can be done for the HD3 plateau on the right side of the linearity peak. In this region of the curves, for $V_{GT} = 2.1$ V, a lower HD3 is observed when the GC GAA is applied. In this case, the linearity rises as the L_{LD}/L ratio and HD3 of –95 dB is achieved for the GC GAA of $L_{LD}/L = 0.3$, which represents an improvement of 15 dB with respect to the uniformly doped device.

As the evaluation of HD3 in Figure 4(A) has shown the analysis in plateau region to be interesting, Figure 4(B) exhibits HD3 *vs.* V_{GT} curves for the worst case among the range of evaluated input amplitudes for this part of the curves. For the whole analyzed V_{GT} range, the distortion behavior is quite similar to the one presented in the curves of Figure 4(A). Except for the peaks region, a small degradation of HD3 is obtained for all the analyzed devices at Va = 0.5 V in comparison to the HD3 obtained at Va = 0.35 V. In the plateau region, the GC GAA device of $L_{LD}/L = 0.3$ exhibits HD3 = -91 dB which is 16 dB better than the HD3 presented by the conventional transistor. Structures composed of GC GAAs with L_{LD}/L higher than 0.3 have shown peaks, and consequently, plateaus for larger gate voltages being less interesting for low voltage applications due to higher V_{GT} required.

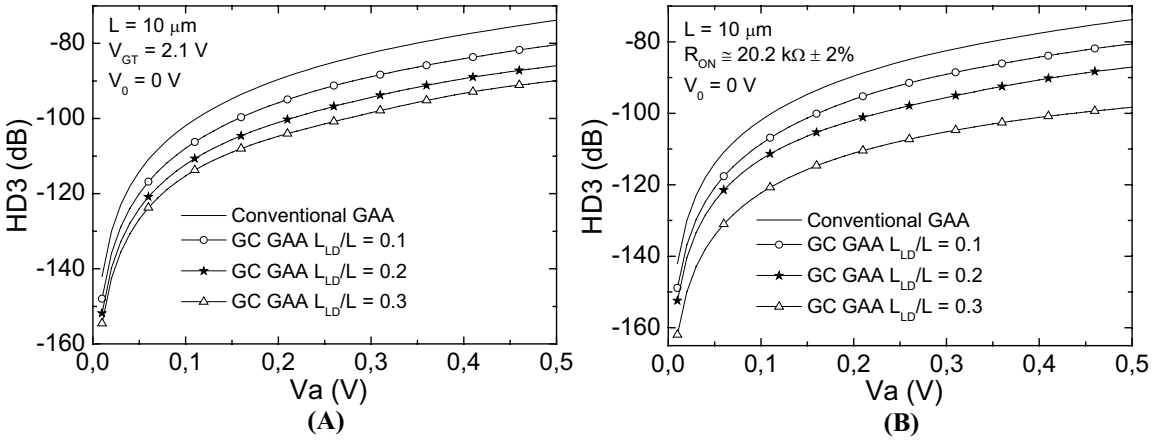

Figure 5. Simulated HD3 *vs.* Va curves for 2-MOS balanced structures with 10 μm-long conventional and GC GAA devices at (A) $V_{GT} = 2.1$ V and (B) $R_{ON} = 20.2$ kΩ ± 2%.

The curves of HD3 as a function of Va for gate overdrive voltage of 2.1 V are presented in Figure 5(A) for 2-MOS circuits composed by conventional and GC GAA transistors. As can be seen, for the whole input signal excursion the 2-MOS structures implemented with GC GAA devices have exhibited higher linearity. According to the curves, HD3 reduces as L_{LD}/L ratio is increased and a linearity improvement greater than 10 dB is obtained in the total Va range under study in relation to the conventional GAA device. Figure 5 (B) exhibits HD3 *vs.* Va at a fixed R_{ON} of 20.2 kΩ ± 2%. As mentioned before, a target R_{ON} is generally required for the circuit design. Thus, through the curves in Figure 5 (B), one can observe that the variation of HD3 at a fixed R_{ON} is quite similar to that one obtained in Figure 5 (A). In order to keep R_{ON} constant, V_{GT} has been varied from 1.9 V to 2.1 V amongst the simulated devices.

DISCUSSION

According to reference (21), the drain current for double gate devices operating in the linear region can be essentially described as a function of the mobility reduction coefficient (θ), the series resistance (R) and the dimensions of the devices as stated by equation [1].

$$I_{DS} = \frac{K\left(V_{GT}V_D - \frac{1+\delta}{2}V_D{}^2\right)}{1+(\theta + R.K)V_{GT} - R.K.\left(\frac{1}{2}+\delta\right)V_D} \qquad [1]$$

where δ and K are given for equations [2] and [3], respectively. In these equations Cox is the oxide capacitance per unit of area, Cs the silicon capacitance per unit of area, and μ_0 is the mobility of electrons.

$$\delta = \frac{Cs}{Cox + Cs} \qquad [2]$$

$$K = 2\frac{W}{L}Cox.\mu_0 \qquad [3]$$

Through reference (22), when devices operate in triode regime, the third order derivative of the drain current as a function of drain voltage can be related to HD3 for a 1 V-amplitude input signal as stated by equation [4] where the denominator term $\partial I_{DS}/\partial V_D$ corresponds to the transadmittance factor and shall be solved for $V_D = 0$.

$$HD3 = \frac{\frac{\partial^3 I_{DS}}{\partial V_D{}^3}}{24\frac{\partial I_{DS}}{\partial V_D}} \qquad [4]$$

Solving symbolically equation [4] for 2-MOS balanced structures, the third order harmonic distortion has been revealed to be proportional to the square of the mobility reduction coefficient, as presented in equation [5].

$$HD3\ \alpha\ -\frac{\left[\left[1+(\theta+RK)V_{GT}\right]-\left[RK\left(\frac{1}{2}+\delta\right)V_D\right]\right]^2}{1+(\theta+RK)V_{GT}} \qquad [5]$$

As shown in equation [5], the difference in the non-linearity for the studied devices is essentially given by the mobility degradation factor as well as the device dimensions (L and W), which are represented by the K term, since all the other parameters have been kept constant amongst the evaluated devices. Solving equation [5] with different θ indicates that for devices with higher mobility degradation an improvement in HD3 can be observed. However, the influence of θ only becomes important for larger V_{GT}. As demonstrated in reference (4) the body effect, which is practically the same among the analyzed devices, dominates the non-linearity at lower gate overdrive voltages. Thus, the HD3 *versus* V_{GT} curves of Figure 4 present a *v*-like shape where the body effect dominates in the left side of the linearity peaks and the mobility degradation in the right side (4) where the GC GAA devices present an improved HD3.

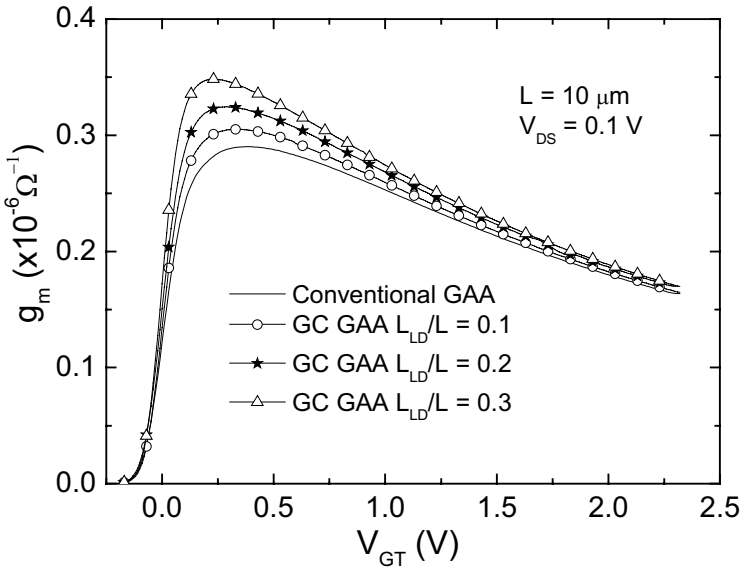

Figure 6. Simulated g_m as a function of V_{GT} for conventional and GC GAA devices of L = 10 μm with several L_{LD}/L ratios at V_{DS} = 0.1 V.

In order to determine the influence of mobility for the analyzed devices, the transconductance (g_m) has been determined for conventional and GC GAA transistors of several L_{LD}/L ratios at lower V_{DS} when the devices are operating in the triode region, since g_m is closely linked to the mobility and through its degradation θ can be estimated. Figure 6 presents simulated g_m curves as a function of V_{GT} for conventional and GC

GAA devices. Through the curves exhibited in Figure 6, the mobility reduction coefficient (θ) has been calculated for the different devices and is presented in Table 1.

Table 1 – Calculated mobility reduction coefficients (θ) for conventional and GC GAA devices of L = 10 μm and several L_{LD}/L ratios.

Device	θ (V^{-1})
Conventional GAA	0.307
GC GAA L_{LD}/L = 0.1	0.336
GC GAA L_{LD}/L = 0.2	0.369
GC GAA L_{LD}/L = 0.3	0.423

Due to the reduction of the effective channel length proportioned by the GC architecture as L_{LD}/L rises, the transconductance peak increases for larger L_{LD}/L ratios. However, a higher g_m reduction in the right side of the peaks is observed for GC GAA devices as L_{LD}/L is increased. This reduction is related to the mobility degradation in the lightly doped region of the channel (8) as well as similarity between the inversion charge densities in both sides of the channel as V_{GT} increases, leading the overall effective channel length to approach for that of a conventional transistor (5), and is responsible for improved linearity exhibited for higher V_{GT} in the Figure 4.

The observed linearity peaks tend to higher V_{GT} as L_{LD}/L is increased, what can be related to the higher saturation voltage presented by the GC device since the conventional transistor starts to operate in triode for smaller V_{GT} (8).

CONCLUSIONS

In the current work, an evaluation of the linearity obtained for 2-MOS resistive structures composed by conventional Gate-All-Around (GAA) and Graded-Channel (GC) GAA devices was performed. Third order harmonic distortion (HD3), which is the dominant distortion in 2-MOS balanced structures, was obtained for conventional and GC transistors of several L_{LD}/L ratios as a function of the gate overdrive voltage, aiming the determination of the device and bias voltage that presents the lowest harmonic distortion. Although, the 2-MOS circuits have shown some linearity peaks along the V_{GT} range, it is unpractical biasing the devices at these peaks since they can change due to temperature and process variations. Thus, we have opted to bias the devices at higher V_{GT} (≈2.1 V), in the plateau at the left side of the peaks, where an extremely good linearity is obtained. At this region, the GC GAA devices have shown to improve HD3 at least for 10 dB in the whole input signal range under study. Finally, a discussion was proposed in order to clarify the origin of the non-linearities in 2-MOS circuits, showing that the differences on HD3 among the studied devices is related to the larger mobility degradation presented by the Graded-Channel transistor.

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