A 0.9-nA Temperature-Independent 565-ppm/°C Self-Biased Current Reference in 22-nm FDSOI

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***Abstract*—Temperature-independent current references operating in the nA range are rarely area-efficient due to the use of large resistors occupying a significant silicon area at this current level. In this paper, we introduce a nA-range constant-with-temperature (CWT) current reference relying on a self-cascode MOSFET (SCM), biased by a proportional-to-absolute-temperature voltage with a CWT offset voltage. The proposed reference has been fabricated in a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology and, as a result of using an SCM, occupies a silicon area of 0.0132 mm^2 at least 4× smaller than state-of-the-art CWT references operating in the same current range. It consumes 5.8 nW at 0.9 V and achieves a 0.9-nA current with a line sensitivity of 0.39 %/V and a temperature coefficient of 565 ppm/°C.**

I. Introduction

Designing current references that are both area-efficient and robust to process, voltage and temperature (PVT) variations is a challenging task, which is not equally difficult depending on the target current. For example, Fig. 1(a) highlights the absence of area-efficient solutions for the generation of a constant-with-temperature (CWT) nA-range current. This gap originates from the fact that conventional CWT current references [Fig. 1(b)] consist in applying a reference voltage to a voltage-to-current converter, which is usually implemented by a gate-leakage transistor [1] or a resistor [2], [3]. These converters are respectively well suited to the generation of a pA- or μA-range current, in the sense that they occupy a reasonable silicon area at this current level. Unfortunately, the generation of a nA-range current would lead to a much larger area, as the resistance of the gate-leakage transistor (resp. resistor) needs to be decreased (resp. increased) by placing devices in parallel (resp. series). Besides, proportional-to-absolute-temperature (PTAT) current references operating in the nA range, such as [4], are area-efficient because they rely on a self-cascode MOSFET (SCM) biased with a PTAT voltage [Fig. 2(a)], hence generating a current proportional to a so-called specific sheet current and thus, to temperature.

In this work, we propose a nA-range CWT current reference based on an SCM, which differs from [4] by the addition of a CWT offset to the PTAT voltage biasing the SCM [Fig. 2(b)]. This offset voltage is obtained as the threshold voltage difference ΔV_T between two transistors of the same type, one of them being reverse body-biased to reduce its threshold voltage. The current reference is fabricated in GlobalFoundries (GF) 22-nm fully-depleted silicon-on-insulator (FDSOI) CMOS

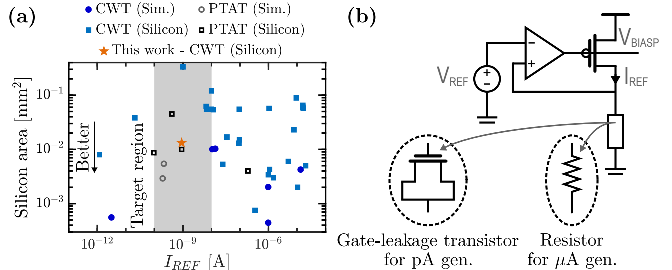

Fig. 1. (a) Trade-off between area and current, based on prior art, highlighting the absence of area-efficient solutions for the generation of a CWT nA-range current. (b) Conventional CWT current references are based on a reference voltage applied to a gate-leakage transistor or a resistor, which are respectively well suited to the generation of a pA- or μA-range current.

technology. Measurements over 20 dies demonstrate a 0.9-nA current with a 0.39-%/V line sensitivity (LS) from 0.9 to 1.8 V, a 565-ppm/°C temperature coefficient (TC) from -40 to 85°C, and a 9.20-% variability (σ/μ) due to combined mismatch and process variations at ambient temperature. The reference consumes 5.8 nW at $V_{DD,\min} = 0.9$ V and 25°C, while occupying a silicon area of 0.0132 mm^2. The paper is structured as follows. Section II explains the operation principle of the proposed current reference based on its governing equations. Sections III and IV respectively detail the methodology used to size the reference, and discuss the measurement results. Section V finally offers some concluding remarks.

II. Operation Principle and Governing Equations

To generate a nA-range current, the proposed reference [Fig. 2(b)] relies on a moderate-inversion SCM formed by M_{1-2}, requiring the advanced compact MOSFET (ACM) model [5] to describe the transistor I-V relationship. In this model, the drain current is given by

$$I_D = I_{SQ} S \left(i_f - i_r\right), \tag{1}$$

where $I_{SQ} = \frac{1}{2}\mu C_{ox}^{'} n U_T^2$ is the specific sheet current, μ the carrier mobility, $C_{ox}^{'}$ the normalized gate oxide capacitance, n the subthreshold slope factor, U_T the thermal voltage, $S = W/L$ the transistor aspect ratio, and i_f, i_r the forward and reverse inversion levels. In addition, the relationship between inversion level, gate and source/drain voltages is captured by

$$V_P - V_{S/D} = U_T \left[\sqrt{1+i_{f/r}} - 2 + \log\left(\sqrt{1+i_{f/r}} - 1\right)\right], \tag{2}$$

where $V_P = \frac{V_G - V_{T0}}{n}$ is the pinch-off voltage, V_{T0} is the threshold voltage at zero V_{BS}, and voltages are referred to the body of the transistor, which is actually the transistor's

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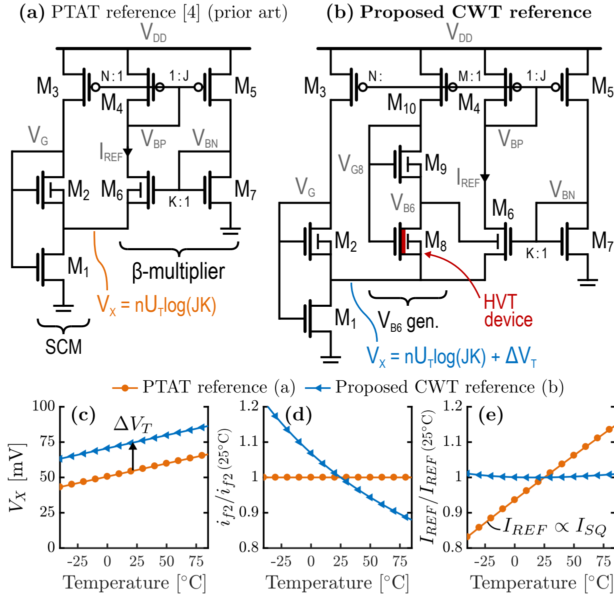

Fig. 2. The proposed circuit generates a CWT current by biasing an SCM using a PTAT voltage with a CWT offset. (a) PTAT reference generating a current proportional to I_{SQ} [4]. (b) Proposed CWT reference, with M_6 biased with $V_{BS6} > 0$, leading to $\Delta V_T = V_{T7} - V_{T6} = \gamma_b V_{BS6} > 0$. Analytical equations for (c) the voltage applied to the SCM, (d) the inversion level of M_2, and (e) the reference current as a function of temperature, with (d) and (e) normalized by their value at 25°C.

back gate in FDSOI. Applying these equations to the SCM and defining $\alpha \triangleq i_{f1}/i_{f2}$, voltage V_X is given by

$$V_X = nU_T \left[\left(\sqrt{1+\alpha i_{f2}} - \sqrt{1+i_{f2}} \right) + \log \left(\frac{\sqrt{1+\alpha i_{f2}}-1}{\sqrt{1+i_{f2}}-1} \right) \right]. \quad (3)$$

Note that the current flowing from M_6 (and M_8) only impacts the required ratio S_1/S_2. Next, applying the ACM equations to the β-multiplier formed by M_{6-7} and assuming these transistors operate in weak inversion, i.e., $i_f \ll 1$, leads to

$$V_X = \Delta V_T + nU_T \log\left(K_{PTAT}\right), \quad (4)$$

where $K_{PTAT} = JK$, J and K being current mirror ratios. With the effect of reverse body bias on the threshold voltage modeled as $V_T = V_{T0} - \gamma_b V_{BS}$, where γ_b is the body factor, we obtain $\Delta V_T = \gamma_b V_{BS6}$.

In Fig. 2(b), our work differs from [4] by adding a threshold voltage difference $\Delta V_T = V_{T7} - V_{T6}$ to V_X, obtained by biasing the body of M_6 with a non-zero V_{BS6}. Voltage V_{BS6} is generated by a voltage reference formed by M_{8-10} relying on the V_T difference between high- and regular-V_T (RVT) devices, and can be made temperature-independent by tuning the ratio S_9/S_8. Given that γ_b does not depend on temperature at first order in FDSOI, ΔV_T is a CWT offset voltage. Then, the reference current is found by applying (1) to M_2, giving

$$I_{REF}(T) = I_{SQ2}(T)\, i_{f2}(T)\, (S_2/N), \quad (5)$$

in which $I_{SQ2}(T) \propto T^{2-m}$, assuming $\mu = \mu(T_0)(T/T_0)^{-m}$ with m the temperature exponent of carrier mobility. The temperature dependence of i_{f2} is determined by solving the non-linear relation found by equating (3) and (4). Using a purely PTAT voltage as in [4], i_{f2} is temperature-independent and leads to $I_{REF} \propto I_{SQ}$ [Figs. 2(c) to 2(e)]. In the

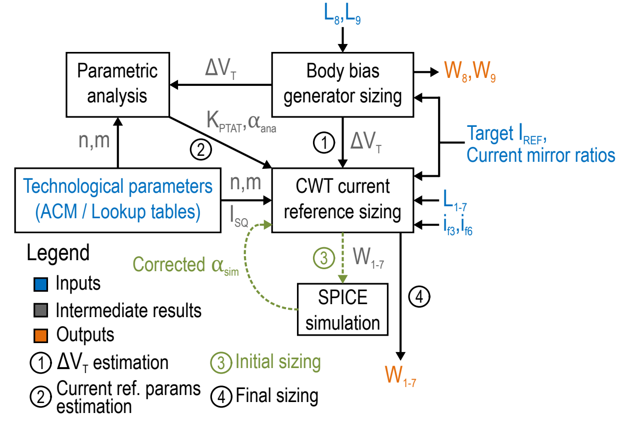

Fig. 3. Four-step flowchart of the design and sizing methodology.

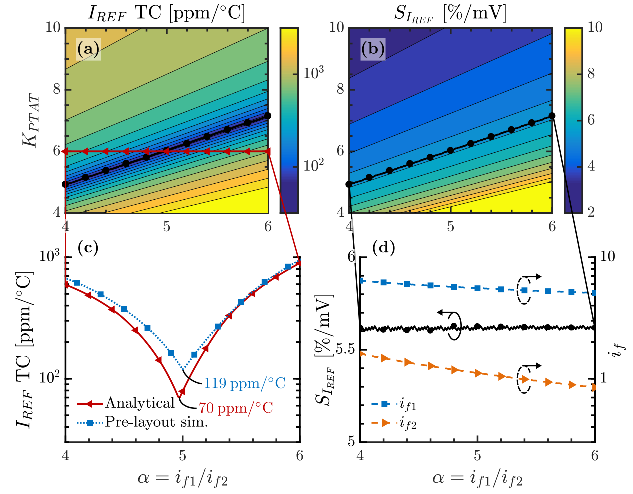

Fig. 4. Analytical sizing of the current reference for $\Delta V_T = 17.6$ mV, $m = 1$ and $n = 1.25$, computed by steps 1 and 2 of the sizing methodology. (a) I_{REF} TC and (b) $S_{I_{REF}}$ as a function of K_{PTAT} and α. (c) I_{REF} TC vs. α for $K_{PTAT} = 6$, based on analytical and pre-layout simulation results. (d) $S_{I_{REF}}$ and inversion level of M_{1-2} along the I_{REF} TC valley.

proposed reference, we add a CWT offset to the PTAT voltage [Fig. 2(c)], causing i_{f2} to vary with temperature. With a proper choice of K_{PTAT} and α, the temperature dependence of i_{f2} [Fig. 2(d)] can compensate that of I_{SQ2}, making I_{REF} temperature-independent [Fig. 2(e)]. Next, we define two important characteristics of the SCM, namely the sensitivity of I_{REF} to V_X computed as $S_{I_{REF}} = (1/I_{REF})(dI_{REF}/dV_X)$, which depends on i_{f2} through

$$S_{I_{REF}} = \frac{2}{i_{f2} n U_T} \left[\frac{\alpha}{\sqrt{1+\alpha i_{f2}}-1} - \frac{1}{\sqrt{1+i_{f2}}-1} \right]^{-1}, \quad (6)$$

and the required ratio of M_{1-2} aspect ratios, i.e.,

$$\frac{S_1}{S_2} = \frac{I_{SQ2}}{I_{SQ1}} \frac{1+M+N}{N} \frac{1}{\alpha - \beta}, \quad (7)$$

where $\beta \triangleq i_{r1}/i_{f2}$. Finally, in what follows, the LS and TC are computed using the box method, i.e.,

$$\text{LS} = \frac{(I_{REF,\max} - I_{REF,\min})}{I_{REF,\text{avg}}\,(V_{DD,\max} - V_{DD,\min})} \times 100\ \%/\text{V}, \quad (8)$$

$$\text{TC} = \frac{(I_{REF,\max} - I_{REF,\min})}{I_{REF,\text{avg}}\,(T_{\max} - T_{\min})} \times 10^6\ \text{ppm/°C}. \quad (9)$$

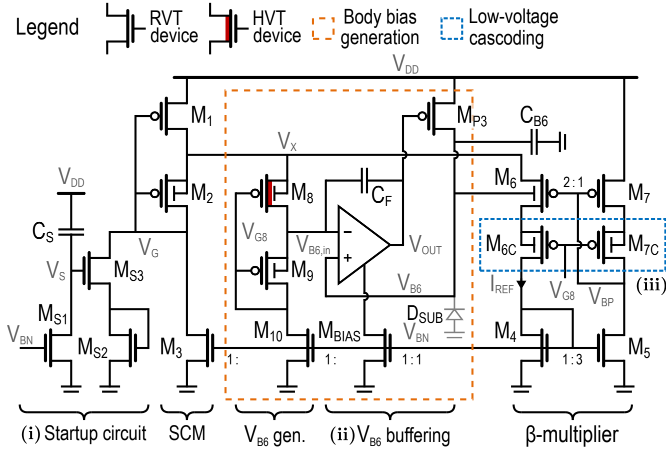

Fig. 5. Schematic of the proposed circuit with a pMOS SCM implemented in GF 22-nm FDSOI, which includes a startup circuit, a low-voltage cascode, and the generation and buffering of the reverse body-bias voltage of M_6.

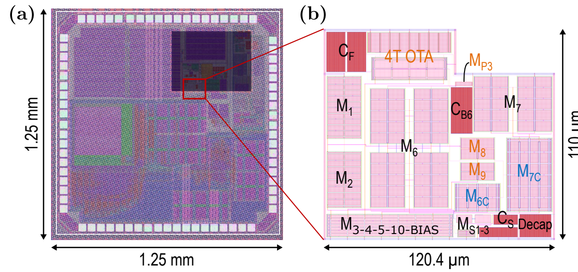

Fig. 6. (a) Chip microphotograph with overlaid layout and (b) layout of the proposed current reference in GF 22-nm FDSOI.

III. Design and Sizing Methodology

The design and sizing methodology is summarized by the flowchart in Fig. 3 and can be divided into four main steps: (i) the V_{B6} generator sizing, determining the CWT offset ΔV_T, (ii) the parametric analysis providing the values of $(K_{PTAT},\ \alpha)$ that minimize the TC of I_{REF}, (iii) an initial sizing of the current reference for different values of α, based on the equations in Section II, and (iv) a final sizing based on the value of α minimizing the TC of I_{REF} in pre-layout simulations. Fig. 4(a) demonstrates the existence of an I_{REF} TC valley, corresponding to a linear relationship between K_{PTAT} and α, but also to an iso-sensitivity curve in Fig. 4(b), in which $S_{I_{REF}}$ is computed from (6). Note that only a change in ΔV_T can change the location of this valley. For the choice of $K_{PTAT} = 6$ made for our design [Fig. 4(c)], a purely analytical approach yields a 70-ppm/°C TC for $\alpha = 4.98$, which is in line with the pre-layout simulation results based on the initial sizing, giving a 121-ppm/°C TC for $\alpha = 5$. Nevertheless, the initial sizing and subsequent SPICE simulations are performed for a range of α values, to ensure that the minimum TC location has been correctly identified. Moreover, Fig. 4(d) proves that along the I_{REF} TC valley, $S_{I_{REF}}$ remains constant around 5.6 %/mV while i_{f1} and i_{f2} at 25°C tend to decrease for larger values of $(K_{PTAT},\ \alpha)$ but remain in moderate inversion, i.e., $i_f \in [1;\ 100]$.

Fig. 5 depicts the complete schematic of the proposed reference, implemented with RVT pMOS transistors to limit

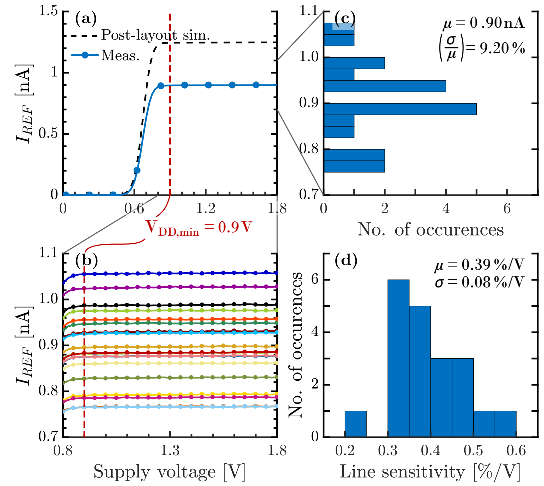

Fig. 7. (a) Post-layout-simulated and measured average I_{REF} at 25°C, with (b) details of the 20 dies. Measured histograms of (c) I_{REF} and (d) LS.

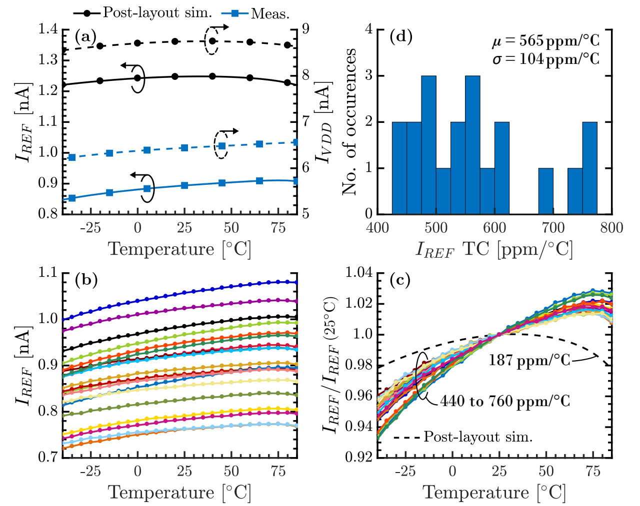

Fig. 8. (a) Post-layout-simulated and measured temperature dependence of the average I_{REF} and I_{VDD}. Measured temperature dependence of I_{REF} (b) without and (c) with normalization by the value at 25°C, for the 20 dies. (d) Measured histogram of I_{REF} TC.

the area overhead entailed by the different body voltages. Several elements have been added to this schematic: (i) a dynamic startup circuit, (ii) a simple 6T buffering stage for V_{B6}, to cope with the leakage of the parasitic nwell/psub diode D_{SUB} at high temperature, and (iii) a low-voltage cascode to improve the LS by reducing the impact of M_6 V_{DS} variations.

IV. Measurement Results

The proposed reference was manufactured in GF 22-nm FDSOI as part of the ICare biomedical microcontroller unit. The chip microphotograph is shown in Fig. 6(a), with the reference layout in Fig. 6(b). Currents were measured with a Keithley K2636A SMU, and an Espec SH-261 climatic chamber was used to sweep temperature from -40 to 85°C.

Figs. 7 and 8 respectively depict the measured dependence of I_{REF} to supply voltage and temperature variations, while Table I compares our simulation and silicon results to the state of the art. First, Fig. 7(a) represents I_{REF} as a function

TABLE I
COMPARISON TABLE OF TEMPERATURE-INDEPENDENT NA-RANGE CURRENT REFERENCES.

	Huang [6]	Far [7]	Kim [8]	Cordova [9]	Aminzadeh [10]	Kayahan [11]	Dong [12]	Ji [13]	Wang [14]	Wang [2]	Huang [3]	Lee [15]	**Lefebvre This work**	
Publication	ISCAS	ROPEC	ISCAS	ISCAS	AEU	TCAS-I	ESSCIRC	ISSCC	VLSI-DAT	TCAS-I	TCAS-II	JSSC	ESSCIRC	
Year	2010	2015	2016	2017	2022	2013	2017	2017	2019	2019	2020	2020	2022	
Type of work	Sim.	Sim.	Sim.	Sim.	Sim.	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Sim.	Silicon
Number of samples	N/A	N/A	N/A	N/A	N/A	90	32*	10	10	16	10	10	N/A	20
Technology	0.18μm	0.18μm	0.13μm	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	0.18μm	22nm FDSOI	
I_{REF} [nA]	2.05	14	27	10.86	6.7	25	35.02	6.64	6.46	9.77	11.6	1	1.25	0.9
Power at $V_{DD,\min}$ [nW]	5.1	150	N/A	30.5	51	28500	1.02	9.3	15.8	28	48.64	4.5/14$^{\triangleright}$	7.84	5.81
Area [mm^2]	N/A	**0.0102**	N/A	**0.01**	**0.46**	**0.0053**	0.0169	**0.055**	**0.062**	**0.055**	**0.054**	**0.332**	**0.0132**	
Supply range [V]	0.85 – 2.2	1 – 3.3	1.2	0.9 – 1.8	1.1 – 1.8	5	1.5 – 2.5	1.3 – 1.8	0.85 – 2	0.7 – 1.2	0.8 – 2	1.5 – 2	0.9 – 1.8	
LS [%/V]	1.35	**0.1**	N/A	**0.54**	**0.03**	**150**	3	1.16	4.15	**0.6**	1.08	1.4	**0.26**	**0.39**$^{\triangleleft}$
Temperature range [°C]	0 – 150	0 – 70	-30 – 150	-20 – 120	-40 – 120	0 – 80	-40 – 120	0 – 110	-10 – 100	-40 – 125	-40 – 120	-20 – 80	-40 – 85	
TC [ppm/°C]	**91**	**20**	327	**108**	**40.33**	**128**/250*	282	680/283†	**138**‡	**149.8**	**169**	289/265$^{\triangleright}$	**187**	565$^{\triangleleft}$
I_{REF} var. (process) [%]	7.5	N/A	3.7	15.8/11.6†	N/A	8/1.22*	4.7	N/A	N/A	+11.7/-8.7$^{\diamond}$	+17.6/-10.3$^{\triangleleft}$	N/A	+9.9/-9.5	**9.20**
I_{REF} var. (mismatch) [%]	N/A	**5.8**	N/A	N/A	**0.70**	**1.4** (sim.)	**1.6**	4.07/**1.19***	3.33	**1.6**	4.3	**1.26**/**0.25**†	**6.39**	
Trimming	No	No	No	Yes	No	No	No	Yes	No	Yes	Yes	Yes	No	No

* 16 dies in TT corner, 4 dies for each FF, SS, SF and FS corner. * Simulated and measured values. † Before and after trimming. ‡ Best TC, the average/median one is not reported. $^{\diamond}$ Estimated from figures. $^{\triangleleft}$ Mean measured value across the 20 dies. $^{\triangleright}$ For 25 and 2.5 minutes between two calibrations.

of the supply voltage, and exhibits a 0.9-V $V_{DD,\min}$ and 0.9-nA I_{REF}, compared to 1.25 nA in simulation, likely due to global process variations. Details of the 20 dies are shown in Fig. 7(b), with I_{REF} variability characterized in Fig. 7(c). The measured variability of 9.20 % is larger than the 6.39-% simulated one due to global die-to-die (D2D) process variations, whereas only local mismatch is accounted for in simulation. Lastly, Fig. 7(d) illustrates the histogram of LS and presents an average of 0.39 %/V, comparable with the 0.26 %/V obtained in simulation. Second, Fig. 8(a) illustrates the evolution of I_{REF} and the supply current I_{VDD} with temperature. I_{REF} presents a 2$^{\text{nd}}$ order behavior, with a slightly PTAT trend in measurement, and the current reference consumes 8.8 nA (resp. 6.4 nA) at 1.8 V in simulation (resp. in measurement). The temperature dependence of I_{REF} across the 20 dies is depicted in absolute value in Fig. 8(b) and normalized by the value of I_{REF} at 25°C in Fig. 8(c). In addition, Fig. 8(c) highlights the TC increase from 187 ppm/°C in simulation to 565 ppm/°C in measurement due to global D2D process variations, an issue which could be solved by adding a calibration scheme to the proposed reference. Finally, Fig. 8(d) shows that the TC has a standard deviation of 104 ppm/°C and reaches a minimum value of 440 ppm/°C.

V. CONCLUSION

We demonstrated a 0.9-nA current reference in 22-nm FDSOI, which relies on an SCM biased by a PTAT voltage with a CWT offset, realized as the threshold voltage difference between two transistors of the same type. This structure consumes 5.8 nW at 0.9 V and leads to a 0.0132-mm^2 area, a 0.39-%/V LS thanks to cascoding, and a 565-ppm/°C TC. Its main drawback is the relatively large 9.20-% variability due to its sensitivity to mismatch and process variations, which calls for a TC calibration scheme to be added in further work.

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