2021 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS) | 978-1-6654-3745-5/21/$31.00 ©2021 IEEE | DOI: 10.1109/EuroSOI-ULIS53016.2021.9560673

In-situ recovery of on-membrane PD-SOI MOSFET from TID defects after gamma irradiation

Amor Sedki
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium
Electronics and Micro-Electronics Laboratory, Physics Department Faculty of Sciences of Monastir
Monastir, Tunisia
sedki.amor@uclouvain.be

Valeriya Kilchytska
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium.
valeriya.kilchytska@uclouvain.be

Farès Tounsi
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium.
fares.tounsi@uclouvain.be

Nicolas André
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium.
nicolas.andre@uclouvain.be

Laurent A. Francis
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium
laurent.francis@uclouvain.be

Denis Flandre
Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM)
Louvain-la-Neuve, Belgium)
denis.flandre@uclouvain.be

***Abstract*— This paper demonstrates a procedure for total in-situ recovery of on-membrane n-type MOSFET from Total Ionizing Dose (TID) defects, due to the exposure to gamma radiation. After a total dose of 348 krad (Si), several annealing steps were applied using an integrated micro-heater with a maximum temperature of 364 °C. The electrical characteristics of the transistor are recorded initially in normal conditions, after irradiation and then after each step of the thermal annealing. The electro-thermal annealing of the transistor allowed a total recovery of the original characteristics after a major shift due to radiation-induced defects. Power Spectral Density (PSD) of noise measurements showed a clear domination of the Random Telegraph Noise (RTN) behavior due to the creation of oxide defects after irradiation. After annealing, the RTN behavior vanishes with a further important decrease of flicker noise. Low-frequency noise measurements of the transistor confirmed the neutralization of oxide defects after annealing.**

Keywords*— *Silicon On Insulator (SOI); MOSFET; Gamma irradiation; Total Ionizing Dose (TID); In-Situ Thermal Annealing; Flicker noise.

I. Introduction

Silicon-on-insulator (SOI) process has long been suitable for radiation environment applications. SOI made devices benefit from an intrinsic immunity to transient ionizing radiation effects thanks to the buried oxide (BOX) layer. The BOX reduces Single Event Effects (SEE) by blocking the induced ionizing particles in the substrate [1]. However, SOI devices remain more sensitive to Total Ionizing Dose (TID) effects, as the thick BOX forms an additional container for radiation-induced positive charges that directly impact the electrical characteristics of the MOSFETs [2]. Various techniques are used for the mitigation of SEEs such as radiation-hardened design, redundancy, shielding, etc. [3]. However, TID effects remain more challenging to mitigate due to the cumulative creation of fixed positive charges in the SiO_2 insulating layers as well as interlayers interface [4]. This issue produces problematic robustness and reliability considerations for CMOS circuits. Recently, an increasing interest is put on in-situ electro-thermal annealing techniques for the recovery of oxide defects begotten by TID [5-6]. This technique is based on the thermal hydrogen passivation of oxide traps [7]. The current paper demonstrates an in-situ recovery of On-Membrane Partially Depleted (PD)-SOI MOSFET by electro-thermal annealing after being exposed to ^{60}Co gamma radiation. The electrical characteristics of the MOSFET are remarkably shifted after a total dose of 348 krad (Si). A severe shift of the threshold voltage (V_{th}) is observed in addition to a decrease of the transconductance (gm). Low Frequency Noise (LFN) measurements are performed before and after irradiation, as well as after annealing in order to demonstrate the creation and neutralization of oxide defects. The noise PSD shows a clear dominance of a strong Random Telegraph Noise (RTN) behavior after irradiation. A remarkable decrease of the noise PSD is observed after annealing which confirms the neutralization of oxide defects.

II. Measurements setup

The Device Under Test (DUT) is a Body-tied 6µm-wide 1µm-long n-MOSFET implemented in a circular membrane with 600µm diameter. The device is located in the close vicinity of a Tungsten-based micro-heater, used for the in-situ thermal annealing by Joule heating. This design is fabricated using a

978-1-6654-3745-5/21/$31.00 ©2021 IEEE

1µm PD CMOS SOI technology (Fig. 1). Two PIN diodes are implemented underneath the micro-heater and next to the transistor side for temperature monitoring. An isolation process is used to reduce the flow of leakage current through the silicon substrate and thus the crosstalk among different transistors, which can eventually affect the logic state (On-Off) of each device. All the devices are embedded on-membrane after etching the back-silicon substrate with a deep reactive ion etching (DRIE) process. This design is widely used in gas sensors to minimize thermal dissipation through the substrate. The device showed initially a reliable characteristic in room temperature as well in high temperatures up to 280°C. The calibration of thermo-diodes and the temperature monitoring technique are described in a previous work [8]. The device was packaged in a Dual In-Line (DIL) ceramic package and connected to a pre-designed printed circuit board for direct characteristics recording. Next, the DUT was installed in a ^{60}Co gamma panoramic irradiator (in the Cyclotron Research Center at the Université catholique de Louvain, Belgium). Two sources of ^{60}Co are used providing a maximum dose rate of 1.2krad/h each. A HP4145 Semiconductor analyzer and a laptop with a pre-defined IC-CAP script to control measurements were installed in a shielded room and connected to the device through coaxial cables. A positive bias V_{gs} of 3V is applied to the transistor's gate during irradiation. The other contacts are connected to the ground. This configuration is usually used to separate the electron-hole pairs and increase the radiation sensitivity. A total dose of 348krad (Si) is obtained. LFN measurements were performed using a low-frequency noise analyzer (LFNA–*Keysight E4727A).* The RTN and flicker noise measurements were performed in saturation regime with V_{ds}=3V and by applying a constant drain current I_{ds}=10µA. The time trace measurements were recorded for 5s with a time step Δt of 1µs. This time resolution was sufficient to extract the emission and capture time constants. The PSD measurements were performed from 1Hz to 1MHz.

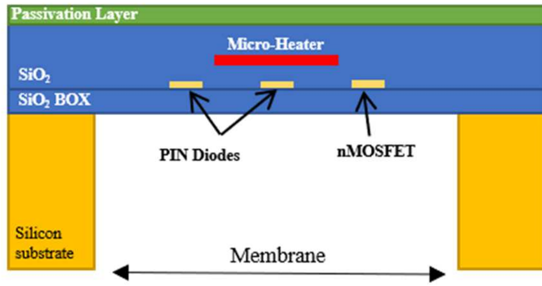

Fig. 1. Cross section schematic of the DUT.

III. Results Analysis

A. I-V measurements:

Fig. 2. presents the subthreshold characteristics of the MOSFET in linear regime with V_{ds} = 50mV, measured in fresh condition and at different doses of gamma radiation up to a total dose of 348krad (Si) during 286 hours. In fresh condition, a non-exponential behavior is observed in the subthreshold slope. This is could be explained by the post-process defects, created by the back DRIE etching [9]. The limited leakage current of this process-induced defects is modeled by a parasitic transistor in the subthreshold region [10]. At lower radiation doses, a remarkable degradation of the subthreshold slope is manifested due to the cumulative creation of positive traps at the side walls of the MOSFET. After a total dose of 348 krad (Si), the leakage current is drastically increased by more than one decade. The I-V measurements reveals an important shift of the threshold voltage (ΔV_{Th} = 850mV) after irradiation. The maximum g_m value at V_{ds} = 50mV decreased by 13% after the same total dose. These degradations are mainly due to the creation of positive charge traps in the BOX and at the Si/SiO_2 interface. The threshold voltage is directly dependent on radiation-induced charges Q_{total} as expressed in following model, by [11]:

$$V_{Th} = \Phi_{MS} + 2\,\Phi_t + \frac{\sqrt{2\,q\,\varepsilon_{si}\,N_a\,2\,\Phi_f}}{C_{ox}} - \frac{Q_{total}}{C_{ox}} \qquad (1)$$

where q is the electron charge, ε_{si} is the dielectric permittivity of silicon, N_a is the substrate doping, C_{ox} is the gate oxide capacitance per unit area, Φ_{MS} the metal–semiconductor work function difference, Φ_f is the Fermi level potential, and Q_{total} is the total gate oxide charge density per unit area at threshold. The negative shift of the threshold voltage could be expressed by:

$$\Delta V_{Th} = -\frac{Q_{total}}{C_{ox}} \qquad (2)$$

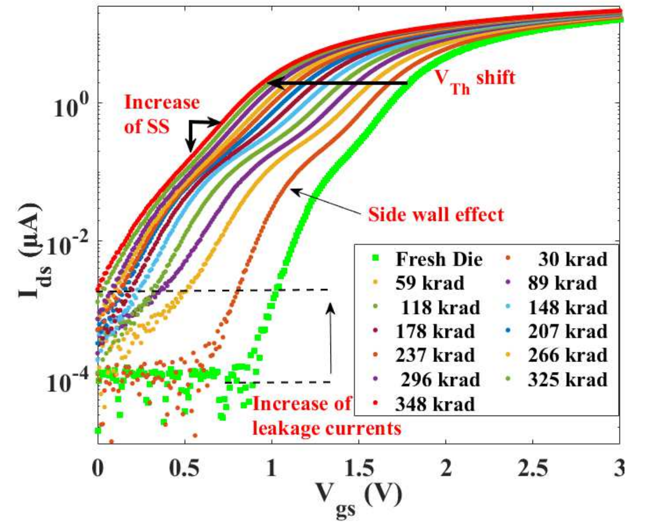

Fig. 2. I_{ds} versus V_{gs} measurements in the linear regime (V_{ds} = 50mV) extracted at different doses of gamma irradiation.

The thermal annealing is applied after the exposure to gamma radiation with a total dose of 348krad (Si). Fig. 3(a) presents the V_{Th} variations after exposure to gamma radiation and after each annealing step of 30 s at different annealing temperatures. For the same annealing temperature at 265°C, the threshold voltage slightly increased after each annealing step reaching a limit of V_{th}=1.33V after 16 annealing steps. The typical/pre-radiation threshold voltage is recovered after a maximum thermal annealing at 364°C. The evolution of the maximum

tranconductance with thermal annealing is presented in Fig. 3(b) where it shows a total recovery of g_m at 265°C annealing temperature.

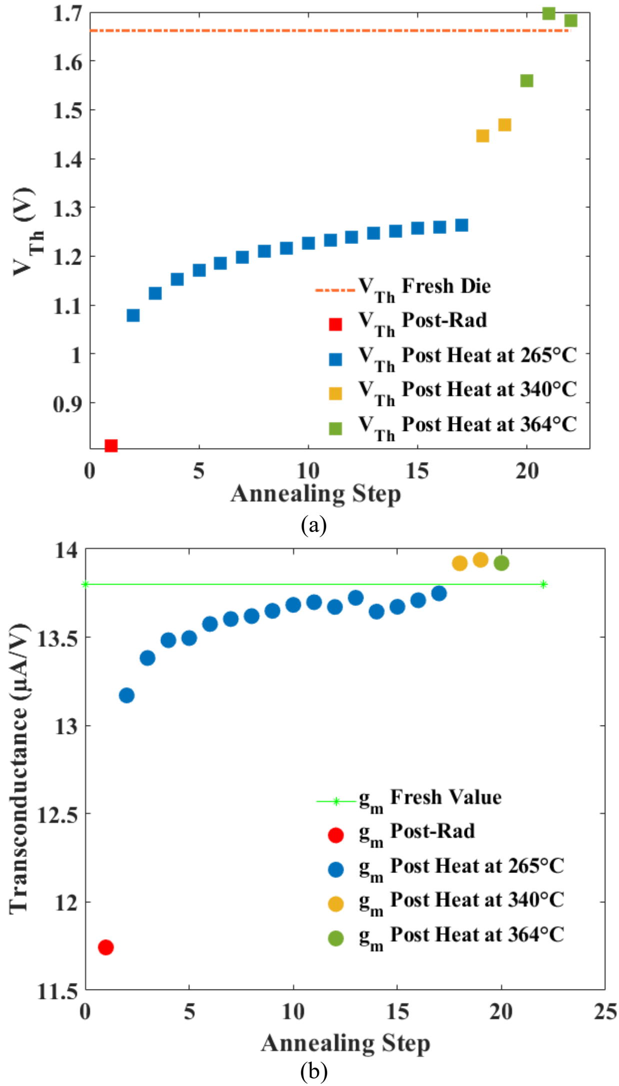

Fig. 3. (a) Threshold voltage of the MOSFET, extracted in linear regime after irradiation and after each annealing step, (b) Maximum transconductance of the MOSFET, extracted in linear regime after irradiation and after each annealing step.

B. Noise measurements

Fig. 4 presents the noise PSD, measured at a fixed drain current I_{ds}=10μA that corresponds to a voltage overdrive ($V_O = V_{gs} - V_{th} = 220$mV) with $V_{ds} = 3$V. Only low frequencies between 1Hz and 1kHz are considered due to the influence of output capacitances at high frequencies. The fresh die results are compared to the measurements after gamma irradiation and after the full-recovery annealing. The noise PSD measurement of the fresh die shows a 1/f flicker-noise behavior. After irradiation, a clear Lorentzian-like plateau and $1/f^2$ decrease are observed. This indicates the domination of RTN behavior, explained by the creation of oxide traps due to the ionizing radiation. After annealing, the RTN behavior vanished with an important decrease of the flicker noise related to the neutralization of defects caused by the irradiation, as well as caused by the DRIE process [9]. This can be quantified using the Lorentzian model (Eq. 3) and by extracting the capture and emission time constants (τ_c and τ_e) from the time trace $I_d(t)$ measurements, with τ is the equivalent time constant.

$$S_{id,RTN}(f) = \Delta {I_d}^2 \frac{4\,\tau^2}{\tau_e + \tau_c} \frac{1}{1 + (2\pi f \tau)^2} \tag{3}$$

The Lorentzian model is presented by the purple curve in Fig. 4. We clearly see the fair match between the model and the flicker noise measurements. This confirms the contribution of the RTN behavior to the PSD of noise and thus the ontribution of radiation-induced defects to the PSD of noise.

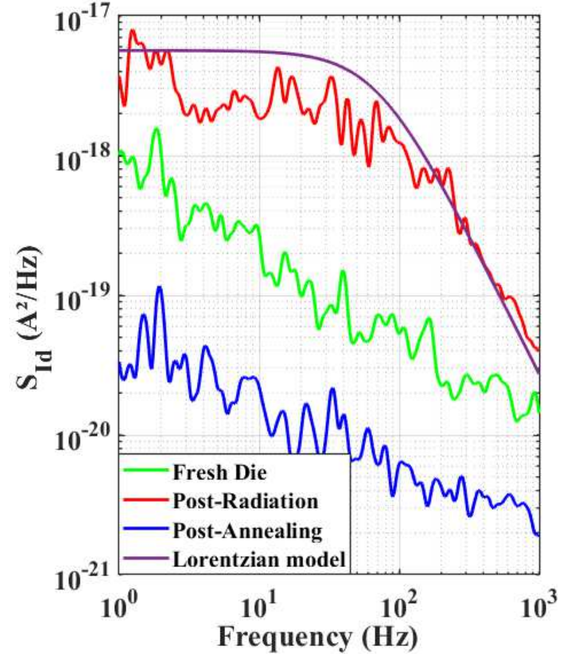

Fig. 4. Power spectral density of noise measurements before radiation, after radiation and after thermal annealing (Measured in saturation regime at fixed Ids=10μA and Vds=3V).

IV. Conclusion

This work studied the benefits of in-situ thermal annealing to recover an nMOSFET I-V characteristic after a strong gamma irradiation. After a TID of 348krad (Si), an important degradation of the transistor electrical characteristics such as the threshold voltage and the transconductance is observed due to the creation of positive charges in the BOX and gate-oxide layers. After an in-situ thermal annealing with a maximum temperature of 364°C, a total recovery of the initial electrical characteristics is achieved. Low-frequency noise measurements demonstrated the contribution of radiation-induced defects to the noise PSD. The strong RTN behavior observed after irradiation confirms the creation of oxide defects. After in-situ thermal annealing, the pre-radiation MOSFET characteristics are recovered with a further remarkable decrease of the flicker noise.

REFERENCES

[1] J. Alvarado, V. Kilchytska, E. Boufouss, B. S. Soto-Cruz and D. Flandre, “A Compact Model for Single Event Effects in PD SOI Sub-Micron MOSFETs,” in IEEE Transactions on Nuclear Science, vol. 59, no. 4, pp. 943-949, Aug. 2012, doi: 10.1109/RADECS.2011.6131345.

[2] B. Ning, D. Bi, H. Huang, Z. Zhang, Z. Hu, M.Chen and S. Zou, “Bias dependence of TID radiation responses of 0.13µm partially depleted SOI NMOSFETs”, Microelectronics Reliability, Vol. 53, pp. 259-264, 2013, doi: 10.1016/j.microrel.2012.08.005.

[3] Calligaro. C, “Rad-Hard Mixed-Signal IC Design, Theory and Implementation”, Springer International Publishing, pp. 273-297, 2020, doi: 10.1007/978-3-030-25267-0_17.

[4] M. L. Alles, R. D. Schrimpf, R. A. Reed, L. W. Massengill, R. A. Weller, M. H. Mendenhall, D. R. Ball, K. M. Warren, T. D. Loveless, J. S. Kauppila and B. D. Sierawski, “Radiation hardness of FDSOI and FinFET technologies,” IEEE 2011 International SOI Conference, 2011, doi: 10.1109/SOI.2011.6081714.

[5] S. Amor, N. André, V. Kilchytska, F. Tounsi, B. Mezghani, P. Gérard, Z. Ali, F. Udrea, D. Flandre and L. A. Francis, “In-situthermal annealing of on-membrane silicon-on-insulator semiconductor-based devices after high gamma dose irradiation”, Nanotechnology, vol. 28, pp 184001, 2017, doi: 10.1088/1361-6528/aa66a4.

[6] S. Amor, V. Kilchytska, D. Flandre and P. Galy, "Trap recovery by in-situ annealing in fully-depleted MOSFET with active silicide resistor," in IEEE Electron Device Letters. IEEE Electron Device Letters, vol. 42, no. 7, pp. 1085-1088, July 2021, doi: 10.1109/LED.2021.3079244.

[7] W. Markus, M. Masuaki, F. Katsuyuki, L. Ziyuan, A. Koichi, K. Yoshiya and F. Shinji,” Influence of H2-annealing on the hydrogen distribution near SiO2/Si(100) interfaces revealed by in situ nuclear reaction analysis”, Journal of Applied Physics, vol. 92, pp. 4320-4329, 2002.

[8] S. Amor, N. André, P. Gérard, S. Z. Ali, F. Udrea, F. Tounsi, B. Mezghani, L.A. Francis and D. Flandre, “Reliable characteristics and stabilization of on-membrane SOI MOSFET-based components heated up to 335 °C”, Semiconductor Science and Technology, vol. 32, pp. 014001, 2016, doi: 10.1088/1361-6641/32/1/014001.

[9] S. Amor, L. V. Brandt, V. Kilchytska, M. Machhout, L. A. Francis and D. Flandre, "Low-Frequency Noise Analysis Of On-Membrane Mosfet And In-Situ Thermal Annealing," DTIP, 2020, doi: 10.1109/DTIP51112.2020.913.

[10] K. O. Petrosyants, I. A. Kharitonov and L. M. Sambursky, “SOI/SOS MOSFET universal compact SPICE model with account for radiation effects,” EUROSOI-ULIS 2015: 2015 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, 2015, pp. 305-308, doi: 10.1109/ULIS.2015.7063834.

[11] M. M. Pejovic and A. B. Jaksic, “Contribution of fixed oxide traps to sensitivity of pMOS dosimeters during gamma ray irradiation and annealing at room and elevated temperature”, Sensors and Actuators, vol. 174, pp. 85-90, 2012, doi: 10.1016/j.sna.2011.12.011