Analysis of Mismatch on the Analog Characteristics of GC SOI MOSFETs

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***Abstract*— This paper presents an evaluation of mismatch impact on the analog characteristics of fully-depleted graded-channel (GC) SOI MOSFET. This study is carried out by means of electrical measurements and two-dimensional numerical simulations, comparing GC to uniformly doped transistors. Important basic parameters such as threshold voltage and sub-threshold slope were analyzed as well as analog parameters, namely transconductance, output conductance, Early voltage and intrinsic voltage gain.**

***Index Terms*— graded-channel transistor; SOI MOSFET; mismatch; electrical measurements.**

I. Introduction

Graded-Channel SOI MOSFET (GC) presents asymmetric doping concentration along the channel, which is divided in two regions [1]. The first is highly doped (HD), responsible for fixing the threshold voltage (V_{TH}) of the device and located near the source region. The second region is lightly doped (LD) and usually is kept with the natural wafer doping concentration. Due to the reduced threshold voltage of the LD region, it acts as an extension of the drain region and GC SOI MOSFET effective channel length is calculated as $L_{eff}=L-L_{LD}$, where L is the channel mask length and L_{LD} is the lightly doped channel region length, when the device is operating in saturation. A schematic figure of a GC SOI nMOSFET is presented in Fig. 1.

Several papers report advantages of GC SOI devices in comparison to uniformly doped ones, such as at device level, an increase of drain current (I_{DS}), transconductance (g_m), Early voltage (V_{EA}) and decrease of drain output conductance (g_D) [2, 3]. The potential of the graded-channel structures for application in microwaves [4] and high frequencies [5, 6] have also been verified.

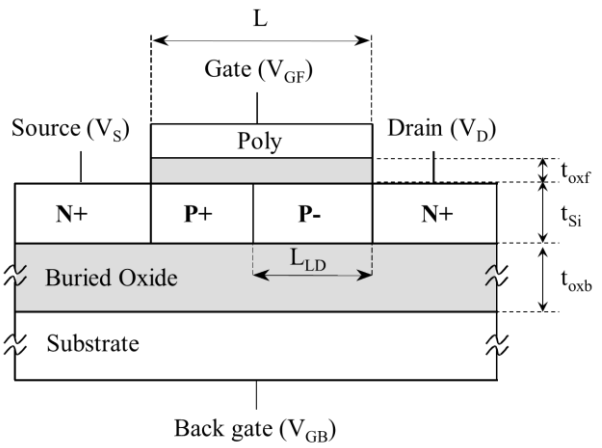

Fig. 1 Schematic cross-section of a Graded-Channel SOI nMOSFET.

The mismatch is an imperfection of MOS transistors directly related to high-performance analog circuits and characterizes the small differences of electrical characteristics of devices placed on the same chip and designed to be identical. Despite the quantity of papers presenting the advantages of GC transistors for analog applications, results on their matching properties have not been widely explored so far [7, 8]. Aiming to improve the knowledge about this important parameter and help analog designers, in this work, experimental and simulated evaluation of the mismatch of GC SOI MOSFETs are presented, focusing on analog parameters, namely transconductance in saturation, output conductance, intrinsic voltage gain and Early voltage.

II. Test Structure and Devices Characteristics

The measured devices were fabricated in an academic 2µm FD SOI technology at Université catholique de Louvain, Belgium [9]. This technology features buried oxide thickness (t_{oxb}) of 390 nm, gate oxide thickness (t_{oxf}) of 30 nm and silicon layer thickness (t_{Si}) of 80 nm. The doping concentration at the highly doped region is (N_{AH}) of 6×10^{16} cm^{-3}, whereas the lightly doped region is kept with natural wafer doping concentration ($N_{AL}=10^{15}$ cm^{-3}).

Dedicated structures have been designed for mismatch measurements. For each transistor size, the designed structure is composed by 20 identically-designed devices, with same distance between devices and pads. Drain, source and gate pads were placed in the same sequence for all devices, and each transistor was placed at the same relative position to the pads. Dummy pads were used in order to maintain structure symmetry, as can be seen in Fig. 2, which shows a photograph of part of one of the fabricated structures. Three arrays were fabricated with 20 µm wide and 2 µm long devices with independent drain, source and gate pads. Each array features a different L_{LD}/L mask ratio: $L_{LD}/L = 0$ (which corresponds to the uniformly doped devices), 0.25 and 0.375.

The devices were measured on-chip, using a Cascade-Microtech probe station REL 3600 and the I-V curves were obtained with a Keithley 4200 SCS. All measurements were performed at room temperature.

III. Experimental Results and Discussion

Experimental drain current (I_{DS}) curves were obtained as a function of gate (V_{GF}) and drain (V_{DS}) voltages for each transistor of the designed arrays. All measurements were performed with back-gate bias of 0V.

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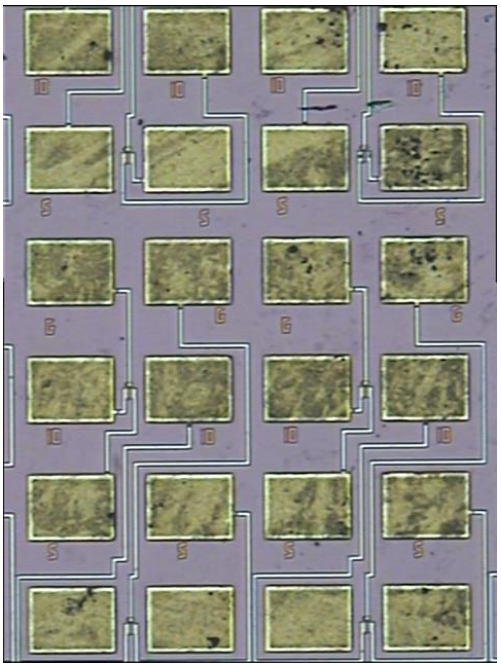

Fig. 2 Photograph of part of measured structure, showing six transistors.

Due to the fabrication process, there might be some imprecision in the definition of the boundary between highly and lightly doped regions, causing some variation on L_{LD}/L ratio. In order to evaluate this variation, the effective L_{LD}/L ratio has been experimentally obtained for the 20 devices of each L_{LD}/L ratio, according to the method described in [1]:

$$\left(\frac{L_{LD}}{L}\right)_{eff} = 1 - \left(\frac{I_{DS}}{I_{DS,GC}}\right) \quad (1)$$

The resulting mean effective L_{LD}/L and standard deviation are presented in Table I. As observed in this table, the standard deviation in the extracted L_{LD}/L slightly increases as this ratio is raised.

Table I. Effective channel length and subthreshold slope extracted from the mean current curves.

L_{LD}/L		S_{mean} (mV/dec)
mask	effective	
0.000	–	63
0.250	0.264 ± 0.0200	64
0.375	0.393 ± 0.0347	66

In order to increase accuracy in threshold voltage and subthreshold slope extraction, I_{DS} *versus* V_{GF} curves measured at V_{DS}=25 mV were obtained with 1 mV-step. The mean drain current curves as a function of gate voltage are presented in Fig. 3 both in linear and logarithmic scales. A well-known characteristic of GC devices is the increase of current level as L_{LD}/L ratio increases (L_{eff} reduction) and it can be seen in the presented curves. Also, no important degradation of subthreshold slope is observed, as confirmed by the extracted values presented in Table I, which are close to the physical limit (63 mV/dec for this technology at room temperature). For GC devices with shorter effective channel length (L_{LD}/L = 0.393, resulting in L_{eff} = 1.214 μm), no significant short-channel effect occurs, and subthreshold slope degradation remains limited.

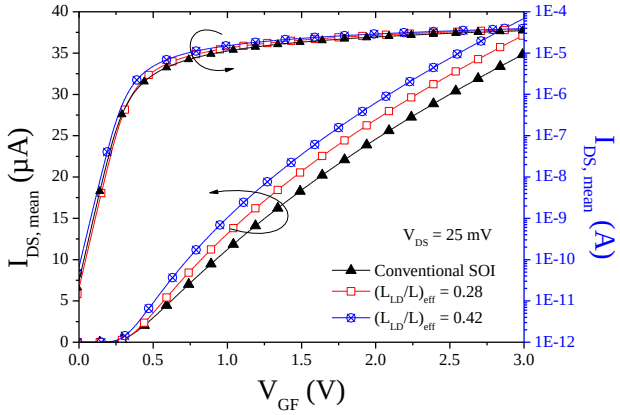

Fig. 3 Mean I_{DS} versus V_{GF} with V_{DS}=25mV, measured with 1 mV-step.

From each measured I_{DS} *vs* V_{GF} curves at low drain bias, and using the double derivative method [10], the threshold voltage (V_{TH}) has been extracted. The resulting mean threshold voltage ($V_{TH, mean}$) and standard deviation (σV_{TH}) are presented for the three different arrays of devices in Table II.

Table II. Measured mean threshold voltage and threshold standard deviation.

L_{LD}/L		$V_{TH,mean}$	σV_{TH}	$\sigma V_{TH}/V_{TH,mean}$
mask	effective	(mV)	(mV)	(%)
0.000	–	104.89	6.45	6.15
0.250	0.264	127.53	7.93	6.21
0.375	0.393	105.26	7.22	6.86

From the presented results, one can note that the use of GC architecture does not significantly affect the threshold voltage in comparison to the uniformly highly doped transistors. However, the relative standard deviation of the threshold voltage ($\sigma V_{TH}/V_{TH, mean}$) is slightly worsened in GC transistors. This can be related to the channel length reduction as the L_{LD}/L is increased and the larger standard deviation of experimental L_{LD}/L ratio.

The relative drain current mismatch can be expressed as a function of the mismatch in the threshold voltage and current factor [11, 12], as shown in equation 2 for the linear strong-inversion regime, where μ_{eff} is the effective carrier mobility and C_{ox} is the front gate oxide capacitance per unit area that influences β as can be seen in equation 3. The threshold voltage variation is highly affected by the variation of the doping concentration, t_{ox}, t_{Si} and the temperature (due to V_{thf} and μ_0 dependence on temperature) [13].

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{-\Delta V_{thf}}{V_{GF}-V_{thf}} + \frac{\Delta\beta}{\beta} \quad (2)$$

$$\beta = \mu_0 . C_{ox} . \frac{W}{L} \quad (3)$$

Fig. 4 presents the drain current relative deviation ($\sigma I_{DS}/I_{DS,mean}$) as a function of the gate voltage overdrive ($V_{GT}=V_{GF}-V_{TH}$), in order to dismiss the different threshold voltage values between measured arrays. As expected, the deviation is higher when the device is in weak inversion, since the threshold voltage impact on the drain current is more significant at low current levels (lower values of V_{GT}) [14]. For higher values of gate voltage, due to larger current

level, the threshold mismatch becomes less important, causing the deviation to be smaller. At large values of V_{GT} the predominant component of mismatch is the current factor (β). The presented curves show that GC devices have worst current matching, even in strong inversion, showing that there is another source besides usual β that contributes to the mismatch in the asymmetric channel device. According to [7] it must be related to the lack of precision in defining the boundary between the two regions with different doping concentrations, as confirmed by the larger deviation as L_{LD}/L ratio increases.

For all devices, the relative deviation reduces as devices bias move to strong inversion. For example, at V_{DS}=25mV and V_{GT}=2.5V, the GC SOI transistors with $(L_{LD}/L)_{eff}$=0.393 present $\sigma I_{DS}/I_{DS,mean}$= 1.3% and it slightly decreases when biased in saturation (V_{DS}=1.5V).

Fig. 5 presents the transconductance relative deviation ($\sigma g_m/g_{m,mean}$) as a function of the gate voltage overdrive for devices biased in saturation. In weak inversion the V_{TH} variation also causes the worsening of matching, when devices are in strong inversion, the relative deviation reduces and reaches values smaller than the values presented for drain current relative deviation. Once again, one can see a slightly higher deviation for GC transistors, although all devices have shown $\sigma g_m/g_{m,mean} \leq 1\%$ for $V_{GT} > 1.2V$.

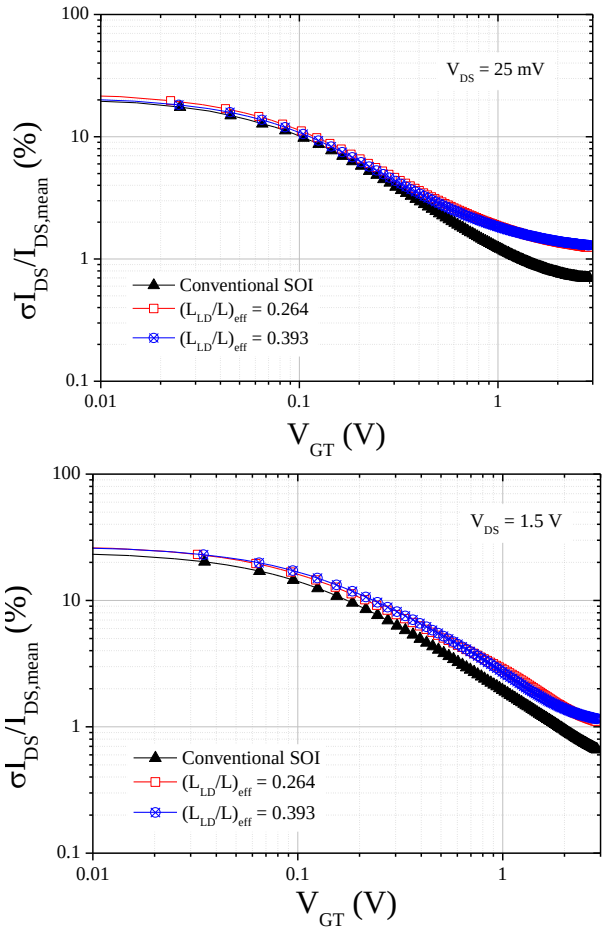

Fig. 4 Relative standard deviation of drain current as a function of the gate voltage overdrive measured at V_{DS}=25 mV (top) and 1.5V (bottom).

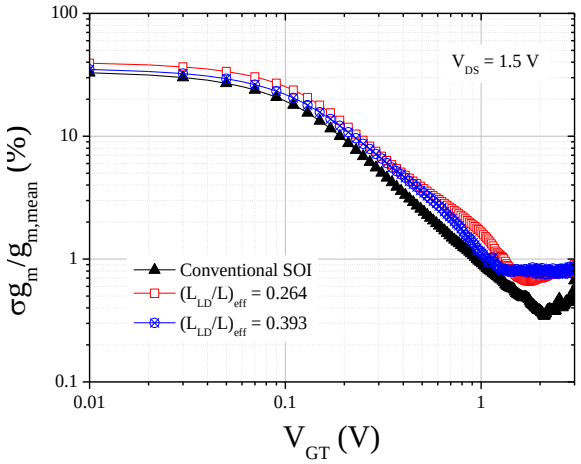

Fig. 5 Transconductance relative deviation as a function of the gate voltage overdrive with V_{DS}=1.5V.

Table III presents the transconductance mean values ($g_{m,mean}$) and respective standard deviation (σg_m) and relative deviation ($\sigma g_m/ g_{m,mean}$) for all devices biased at V_{GT} = 200 mV and V_{DS} = 1.5 V. These results show that the relative deviation is only slightly higher in GC device, even though standard deviation is worsened in GC devices with same gate length, due to variations in the current factor β. This occurs because the mean values are increased by the reduction of effective channel length.

Table III. Measured mean transconductance and transconductance standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L		$g_{m,mean}$	σg_m	$\sigma g_m/g_{m,mean}$
mask	effective	(μS)	(μS)	(%)
0.000	–	141.00	5.98	4.23
0.250	0.264	203.00	9.03	4.44
0.375	0.393	257.00	12.66	4.91

Fig. 6 shows the mean drain current curves as a function of the drain voltage measured at V_{GT}=200 mV. These curves show that as the L_{LD}/L ratio increases so does the current level, as reported in the literature. Also, a reduction of impact ionization effect is seen in GC devices in comparison to uniformly doped devices.

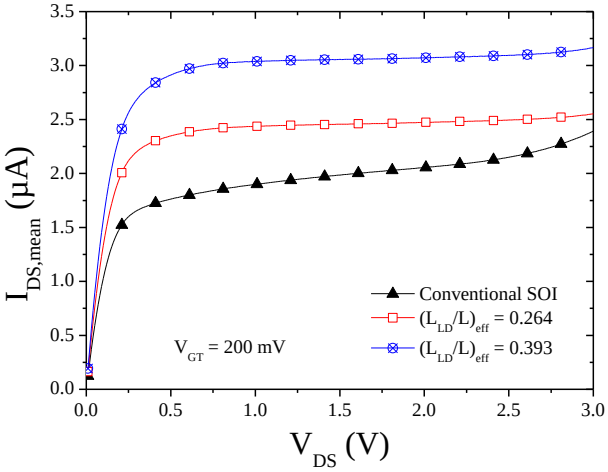

Fig. 6 Mean I_{DS} versus V_{DS} curves measured with V_{GT}=200mV.

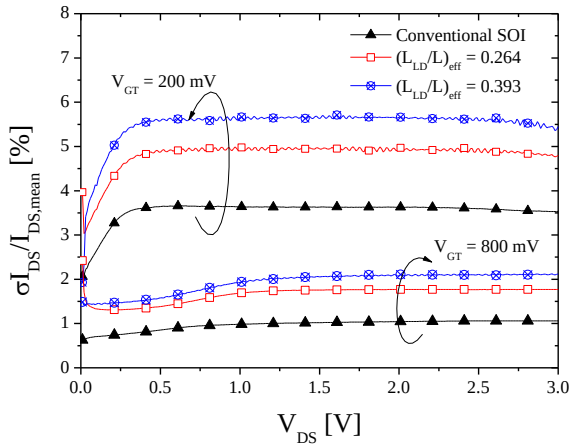

Fig. 7 Relative standard deviation of drain current as a function of the drain voltage with V_{GT}= 200 mV and 800mV.

The drain current relative deviation as a function of V_{DS} is presented in Fig. 7 for V_{GT}=200mV and 800mV. One can observe that the mismatch in saturation is practically constant for all L_{LD}/L ratio. As seen in Fig. 3 the L_{LD}/L ratio increase worsens the matching. Also, the increase of V_{GT} reduces the current mismatch as discussed previously. The mean output conductance and its standard deviation extracted at V_{GT}=200 mV and V_{DS} = 1.5 V are presented in Table IV. The relative standard deviation of g_D is slightly worst when using GC devices, contrarily to the results obtained for g_m. Despite the standard deviation being smaller in GC devices, g_D mean value is much smaller in GC transistors, worsening the relative deviation.

The Early voltage mean curves ($V_{EA}=I_{DS}/g_D$) is presented in Fig. 8. As shown by these results, V_{EA} is significantly higher in graded-channel transistors when compared to the conventional uniformly doped one. At V_{DS}=1.5V, the conventional transistor presents $V_{EA,mean}$ of 13V, whereas it can reach more than 150V in the GC transistor with L_{LD}/L=0.393. The larger value of V_{EA} provided by GC devices make the relative deviation become smaller, even though the current and output conductance deviations being worse in GC devices. The calculated values of relative deviation have not reached 3% in the whole range of applied V_{DS}, as presented in Fig. 9.

Finally, the intrinsic voltage gain ($A_V=g_m/g_D$) has been obtained at V_{GT}=200 mV and V_{DS}=1.5 V for each device in order to evaluate the mismatch. The mean value and the standard deviation are presented in Table V. One can notice that as the L_{LD}/L ratio increases so does the mean gain value, but there is a worsening of matching. Although the relative standard deviation increases, its maximum value does not surpass the values obtained in the relative standard deviation of the output conductance. This indicates the larger source of mismatch in GC SOI with longer L_{LD} is associated with the mismatch in g_D.

Table IV. Measured mean output conductance and its standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L		$g_{D,mean}$	σg_D	$\sigma g_D/g_{D,mean}$
mask	effective	(S)	(S)	(%)
0.000	–	1.47×10^{-6}	97.6×10^{-9}	6.63
0.250	0.264	0.27×10^{-6}	31.9×10^{-9}	11.60
0.375	0.393	0.22×10^{-6}	27.5×10^{-9}	12.40

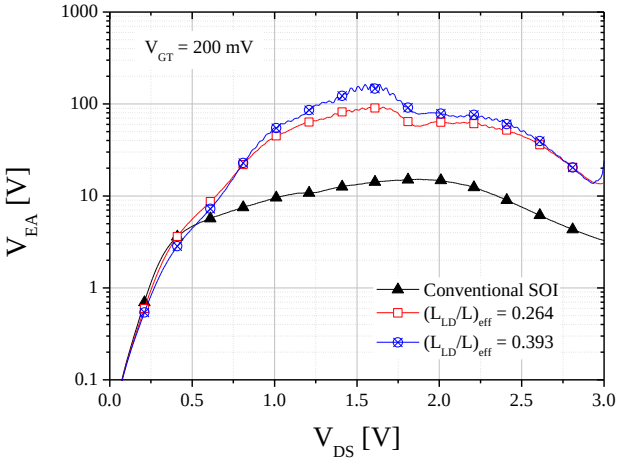

Fig. 8 Mean Early voltage as a function of the drain voltage extracted at V_{GT}= 200 mV.

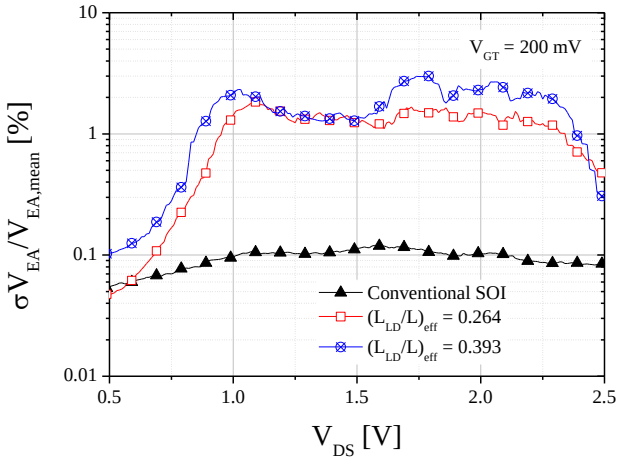

Fig. 9 Early voltage relative deviation as a function of the drain voltage with V_{GT}= 200 mV.

Table V. Measured mean gain and gain standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L		$A_{V,mean}$	σA_V	$\sigma A_V/A_{V,mean}$
mask	effective	(V/V)	(V/V)	(%)
0.000	–	95.99	3.94	4.11
0.250	0.264	744.75	73.99	9.93
0.375	0.393	1174.63	130.36	11.09

IV. Numerical Simulation Results and Discussion

As reported in [7], the highly doped channel length and its doping concentration are the most common variations during the production of a GC transistor. With the aim of analyzing the impact of these variation over the analog performance of graded-channel transistors, two-dimensional numerical simulations were performed through Sentaurus Devices software from Synopsys [15], imposing variations of the highly doped channel length and concentration.

Transistors with L=2µm, W=1µm, $N_{AH}=5\times10^{16}cm^{-3}$, $N_{AL}=1\times10^{15}cm^{-3}$, and L_{LD}/L ratios of 0.2, 0.3, 0.4 and 0.5 were taken as reference. Starting from these characteristics, two groups of simulations were performed:

1) The first group of simulated devices kept N_{AH} constant and a variation of ±30nm [7] in L_{HD} was imposed for

each L_{LD}/L ratio. These variations are not larger than 3%, as can be seen on Table VI.

Table VI. Percentage of imposed variation to the highly doped region length in simulated devices.

L_{LD}/L	$L_{HD,mean}$	L_{HD} (µm)	$\sigma L_{HD}/L_{HD,mean}$ (%)
0.2	1.60	1.57 – 1.63	1.88
0.3	1.40	1.37 – 1.43	2.14
0.4	1.20	1.17 – 1.23	2.50
0.5	1.00	0.97 – 1.03	3.00

2) The second group kept the L_{LD}/L ratio fixed and a variation in the N_{AH} of ±10% was simulated for each considered device.

From simulated I_{DS} *versus* V_{GF} curves biased at V_{DS}=50 mV, the subthreshold slope values were extracted and are presented in Table VII. The relative standard deviation is also presented. As in the experimental results, the increase of L_{LD}/L only slightly degrades the subthreshold slope. For each device the mean value of S has not been affected either by length or doping concentration variations. On the contrary, the relative deviation observed for ΔN_{AH} are higher compared to ΔL_{HD}. This indicates that subthreshold voltage variation among identically designed devices mainly originates from variations of doping concentration.

Table VII. Subthreshold slope mean values and standard deviation extracted from the mean current curves.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	S_{mean} (mV/dec)	$\sigma S/S_{mean}$ (%)	S_{mean} (mV/dec)	$\sigma S/S_{mean}$ (%)
0.2	65.7	0	65.7	0.30
0.3	66.2	0	66.1	0.31
0.4	67.2	0	66.9	0.48
0.5	68.3	0	68.3	0.44

The same trends were obtained for the threshold voltage, extracted from I_{DS} *versus* V_{GF} with V_{DS}=50 mV and presented in Table VIII. The presented mean values are the same for each variation type, whereas the relative deviation from ΔN_{AH} is again higher compared to ΔL_{HD}. Also, resulting V_{TH} variation is higher than the imposed variation, which is 10% in N_{AH}. On the other hand, effective channel length variation has led to negligible relative standard deviation.

Table VIII. Threshold voltage mean values and standard deviation extracted from the mean current curves.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	$V_{th,mean}$ (mV)	$\sigma V_{th}/V_{th,mean}$ (%)	$V_{th,mean}$ (mV)	$\sigma V_{th}/V_{th,mean}$ (%)
0.2	319	0.18	319	18.35
0.3	316	0.18	316	18.53
0.4	311	0.32	311	18.97
0.5	304	0.33	304	19.26

Fig. 10 presents the drain current relative deviation as a function of the gate voltage overdrive when L_{HD} (top) and N_{AH} (bottom) were varied, with V_{DS}=50mV. As can be noticed as the gate voltage increases the deviation becomes less important for all devices, as expected for MOSFETs

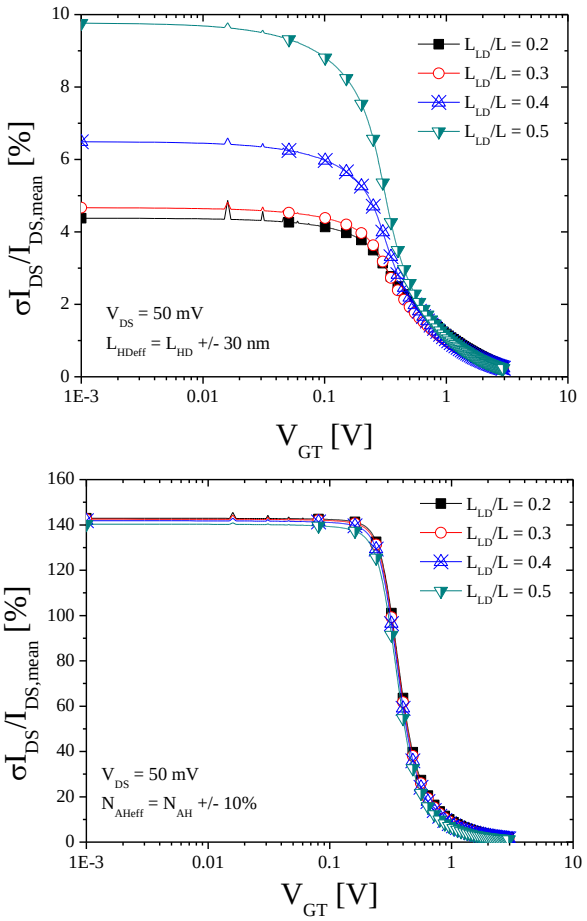

Fig. 10 Relative standard deviation of drain current as a function of the gate voltage overdrive measured at V_{DS}=50mV for imposed L_{HDeff} variation (top) and N_{AHDeff} variation (bottom).

operating in strong inversion. At V_{GT}=3V the standard deviation is smaller than 0.4% when varying L_{HD} and 2% when varying N_{AH}, both variations are lower than the imposed variation and one can notice that the variation of N_{AH} is more important to the mismatch effects. As devices move to weak inversion, deviation increases. When L_{HD} variation is imposed, the standard deviation of drain current becomes dependent on L_{LD}/L, reaching up to 10% at V_{GT}=0 with L_{LD}/L=0.5. It is worth noticing that the imposed variation in the effective length of this device is 3%, which is much smaller than the resulting current variation. Contrarily, when the doping concentration is varied, no dependence with L_{LD}/L is observed, although the relative deviation has an important degradation, reaching about 140% at V_{GT}=0 for all L_{LD}/L imposing a variation of 10%. It is in accordance with the results shown in Table VII and VIII, that shows that the deviation increases as we increase L_{LD}/L and the deviation is higher when applied ΔN_{AH} compared to ΔL_{HD}. Similar results were obtained when the drain bias is increased.

Fig. 11 presents the transconductance relative deviation as a function of the gate voltage overdrive for devices biased at V_{DS}=1.5V when L_{HD} (top) or N_{AH} (bottom) were varied, one can notice as the V_{GT} increases the standard deviation decreases and tends to be constant and lower than 1% for both variations imposed. Once again, it can be noticed that at lower values of V_{GT} the mismatch is higher when imposing the

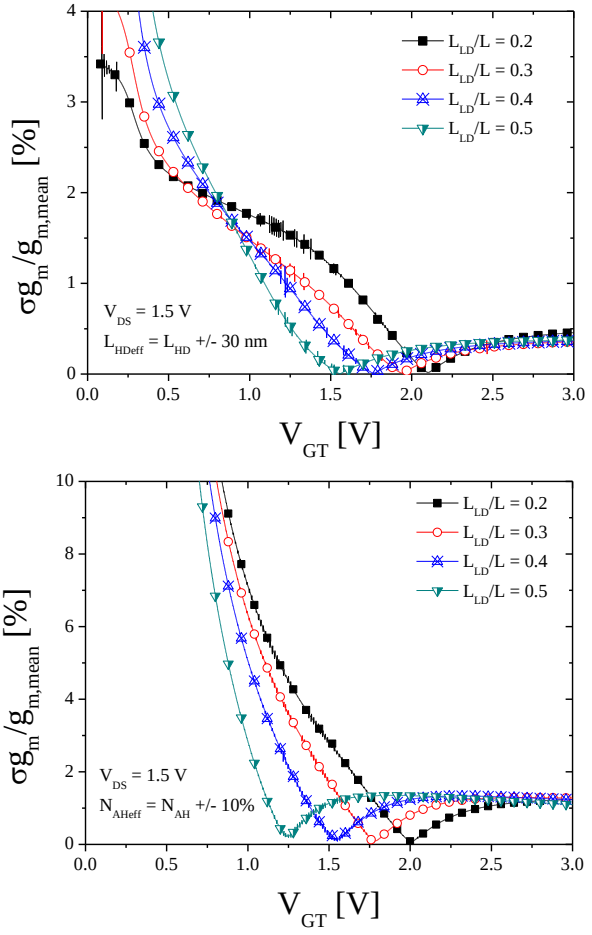

Fig. 11 Relative standard deviation of transconductance as a function of the gate voltage overdrive measured at V_{DS}=50mV for imposed ΔL_{HDeff} (top) and ΔN_{AHDeff} (bottom).

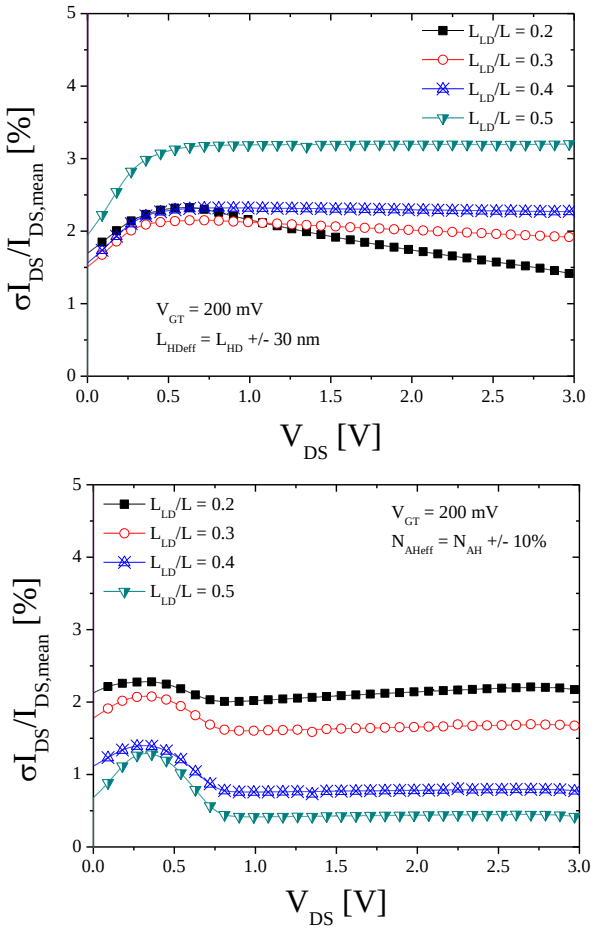

Fig. 12 Relative standard deviation of drain current as a function of the drain voltage measured at V_{GT}=200mV for imposed ΔL_{HDeff} (top) and ΔN_{AHDeff} (bottom).

variation on N_{AH}. Table IX presents the transconductance mean values and relative deviation for V_{GT}=200mV and V_{DS}=1.5V. Once can see that g_m deviation when applied ΔL_{HD} tends to increase as the L_{LD}/L ratio increases but its values are basically the same as the imposed variation (for example the imposed variation for L_{LD}/L=0.3 is 2.143% and the deviation obtained is 2.26%). The deviation when applied ΔN_{AH} tends to decrease as the L_{LD}/L increases, and its values are lower than the imposed variation of 10%.

Table IX. Measured mean transconductance and standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	$g_{m,mean}$ (μS)	$\sigma g_m/g_{m,mean}$ (%)	$g_{m,mean}$ (μS)	$\sigma g_m/g_{m,mean}$ (%)
0.2	7.5	1.96	7.59	1.82
0.3	8.71	2.02	8.68	1.44
0.4	10.28	2.26	10.23	0.86
0.5	12.60	3.21	12.68	0.48

Fig. 12 presents the relative deviation of the drain current as a function of V_{DS}, for devices biased at V_{GT}=200mV. The presented results show that the deviation still stays practically constant when in saturation both for doping concentration and channel length variation. However, the variation of L_{HD} has shown to cause larger deviation compared to ΔN_{AH}, even though the deviation obtained is about the imposed variation. The drain current deviation obtained is way lower than the imposed variation on N_{AH}, this indicates that the second term of equation 2 (related to β) is dominant in this bias condition.

From each drain current curve as a function of drain bias, the output conductance (g_D) has been extracted. Table X presents the mean output conductance and its standard deviation at V_{GT}=200mV and V_{DS}=1.5V. From these results, one notice that the mean values are about equal for both imposed variations. The g_D deviation when applying ΔL_{HD} tend to decrease as the L_{LD}/L ratio increases and the deviation is higher than the imposed variation. While the deviation when applying ΔN_{AH} tends to increase as the L_{LD}/L ratio increases and the deviations are lower than the imposed variation. One can notice that for lower values of L_{LD}/L the mismatch suffers larger influence of ΔL_{HD}.

Table X. Measured mean output conductance and standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	$g_{D,mean}$ (S)	$\sigma g_D/g_{D,mean}$ (%)	$g_{D,mean}$ (S)	$\sigma g_D/g_{D,mean}$ (%)
0.2	21.04	15.65	21.02	7.40
0.3	8.17	11.58	8.37	8.14
0.4	4.09	5.62	4.13	8.30
0.5	4.17	5.11	4.29	9.62

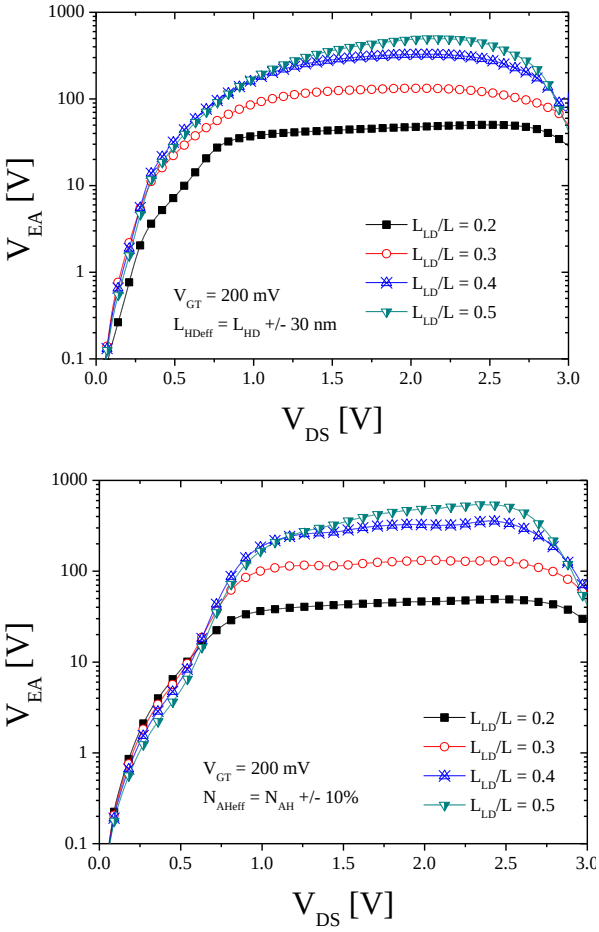

Fig. 13 Early voltage as a function of the drain voltage measured at V_{GT}=200mV for imposed ΔL_{HDeff} (top) and ΔN_{AHDeff} (bottom).

Fig. 13 presents the mean Early voltage. In this figure one can notice that for both L_{HD} and N_{AH} variations, the mean values are basically the same and the mean values increases as the L_{LD}/L increases. Table XI presents the Early voltage mean values and relative deviations for V_{GT}=200mV and V_{DS}=1.5V. While the relative deviation caused by ΔL_{HD} tends to decrease as the L_{LD}/L ratio increases, the opposite is seen when the doping concentration is varied, where the deviation rises with L_{LD}/L ratio increase. However, it does not surpass the imposed 10% variation. One can notice that for lower values of L_{LD}/L, just as the g_D deviations, the mismatch is more dependent on ΔL_{HD}, and as the L_{LD}/L increases the mismatch in the case of ΔN_{AH}.

Table XI. Measured mean Early voltage and standard deviation for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	$V_{EA,mean}$ (V)	$\sigma V_{EA}/V_{EA,mean}$ (%)	$V_{EA,mean}$ (V)	$\sigma V_{EA}/V_{EA,mean}$ (%)
0.2	43.37	17.61	42.8	5.34
0.3	127.69	14.09	121.3	6.92
0.4	301.15	7.96	289.5	7.76
0.5	367.14	2.05	355.7	9.05

Table XII presents the gain mean values and relative deviation for V_{GT}=200mV and V_{DS}=1.5V. The mean values are about equal for both variations imposed and it increases as the L_{LD}/L ratio increases. The relative deviation follows the same tendency of the Early voltage. While the variation of L_{HD} have more impact on the relative deviation for lower L_{LD}/L, the variation of N_{AH} tends to have more impact for devices with larger L_{LD}/L.

Table XII. Measured mean intrinsic voltage gain and standard deviation values for devices biased at V_{GT}=200mV and V_{DS}=1.5V.

L_{LD}/L	ΔL_{HD}		ΔN_{AH}	
	$A_{V,mean}$ (V/V)	$\sigma A_V/A_{V,mean}$ (%)	$A_{V,mean}$ (V/V)	$\sigma A_V/A_{V,mean}$ (%)
0.2	367.23	17.68	362.3	5.58
0.3	1078.46	14.05	1041.9	6.68
0.4	2525.40	7.92	2487.4	7.38
0.5	3022.65	2.42	2973.6	9.09

V. Conclusions

This paper has shown an experimental evaluation of the mismatch on the analog parameters of GC SOI transistors. Results show that the relative mismatch are higher for GC than for conventional transistors. The standard deviation of drain current on GC devices is also slightly higher. The measured mismatch on the output conductance is larger compared to the transconductance mismatch while the device is operating in saturation region, which is of interest for analog applications. This larger deviation of the output conductance is directly transferred to the voltage gain leading to similar mismatch in the latter. From the numerical simulations it was possible to isolate two sources of mismatch: definition of highly doped region length and its doping concentration. The obtained results allow to notice that the mean values are almost the same independent of the parameter in which the variation is imposed. These two variations affect analog parameters in different ways. For instance, ΔL_{HD} has higher influence over the transconductance while ΔN_{AH} has higher influence over subthreshold slope and threshold voltage. The deviation for g_m in saturation increases as the L_{LD}/L increases with ΔL_{HD} and decreases with ΔN_A. However, if a device suffers both variations (ΔL_{HD} and ΔN_{AH}) the contrary tendencies will make the deviation decreases. These opposite tendencies can be seen also in g_D, V_{EA} and A_V.

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References

[1] M. A. Pavanello, J. A. Martino, D. Flandre, “The graded-channel SOI MOSFET to alleviate the parasitic bipolar effects and improve the output characteristics” In*: Silicon-on-Insulator Technology and Devices 1999*, Pennington: The Electrochemical Society, 1999, pages 293-298.

[2] M. A. Pavanello, J. A. Martino, D. Flandre, “Analog performance and application of graded-channel fully depleted SOI MOSFETs”. *Solid-State Electronics*, v.44, n.7, 2000, pages 1219-1222.

[3] M. A. Pavanello, J. A. Martino, D. Flandre, “An asymmetric channel SOI nMOSFET for reducing parasitic effects and improving output characteristics”, *Electrochemical and Solid-State Letters*, v.1, 2000, pages 50-52.

[4] M. Dehan and J.P. Raskin. "An Asymmetric Channel SOI nMOSFET for Improving DC and Microwave Characteristics", *Solid-State Electronics*, vol. 46 n. 7, 2002, pages 1005-1011.

[5] M. Emam, et al. "Experimental Investigation of RF Noise Performance Improvement in Graded Channel MOSFETs". *IEEE Transactions on Electron Devices*, vol. 56, n. 7, 2009, pages 1516-1522.

[6] V. Kilchytska et al, "Influence of device engineering on the analog and RF performances of SOI MOSFETs". *IEEE Transactions on Electron Devices*, vol. 50, n. 3, March, 2003, pages 577-588.

[7] M. de Souza, D. Flandre, M. A. Pavanello, "Study of Matching Properties of Graded-Channel SOI MOSFETs". *Journal of Integrated Circuits and Systems*, vol. 3, n. 2, 2008, pages 69-75.

[8] M. de Souza, D. Flandre, M. A. Pavanello, "Impact of Mismatching on the Analog Properties of Standard and Graded-Channel SOI nMOSFETs". *Proceedings of EuroSOI 2011*.

[9] D. Flandre, et al., "Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/microwave circuits". *Analog Integrated Circuits and Signal Processing*, vol. 21, Dec, 1999, pages 213-228.

[10] A. Ortiz-Conde *et al.*, "Revisiting MOSFET threshold voltage extraction methods", *Microelectronics Reliability*, vol. 53, January, 2013, pages 90-104.

[11] J. A. Croon et al.; "Physical modeling and prediction of the matching properties of MOSFETs". *Proceedings of the 34th European Solid-State Device Research Conference*, 2004, pages 193-196.

[12] R. Difrenza et al.; "A new model for the current factor mismatch in the MOS transistor", *Solid-State Electronics*, v. 47, n.7, 2003, pages 1161-1171.

[13] J. A. Croon et al.; "An easy-to-use mismatch model for the MOS transistor". *IEEE Journal of Solid-State Circuits*, v.37, 2002, pages 1056-1064.

[14] L. Vancaillie et al; "MOSFET mismatch in weak/moderante inversion: model needs and implications for analog design", *Proceedings of the European Solid-State Circuits Conference*, 2003, pages 671-674.

[15] Synopsys. Sentaurus device user guide, 2016. Manual version M2016.12.