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we innovatively characterize

Mostafa Emam
mostafa.emam@incize.com

Jean-Pierre Raskin
jean-pierre.raskin@uclouvain.be

Tuesday 12 April 2016

http://www.linkedin.com/company/incize

Engineered Si-based Substrates for the State-of-the-art RF Devices and IoT Applications

Mostafa Emam
mostafa.emam@incize.com

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jean-pierre.raskin@uclouvain.be

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SEA
NETHER-
LANDS
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LONDON
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Brighton
Antwerpen
Hasselt
BRUXELLES
BELGIUM
Liège
Namur
Charleroi
Lille
Ardennes
LUXEMBOURG
LUXEMBOURG
Dieppe
Saint-Quentin
Amiens
Laon
Le Havre
Reims
Maas
Metz

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March 14, 2014

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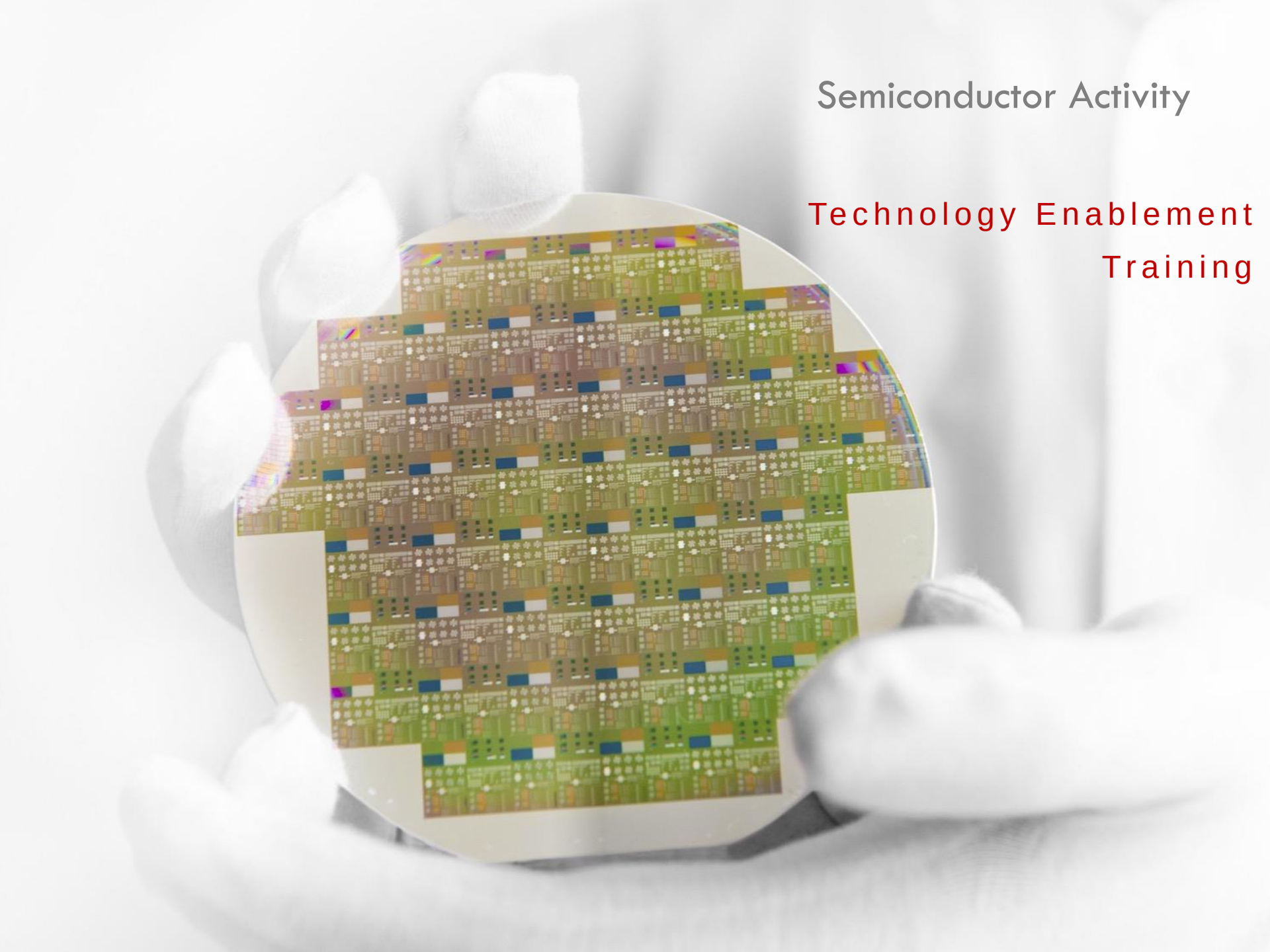
Customers

Wafer suppliers
Foundries
Fabless



Semiconductor Activity

Technology Enablement Training


Radiation Hardness
Characterization
Simulation

Louvain-la-Neuve, Belgium

UCL

Université catholique de Louvain

Exclusive License

10 years

Background


June 1, 2015

WELCOME – Characterization Facility

Frequency DC - 220 GHz

RF power -25 to 40 dBm

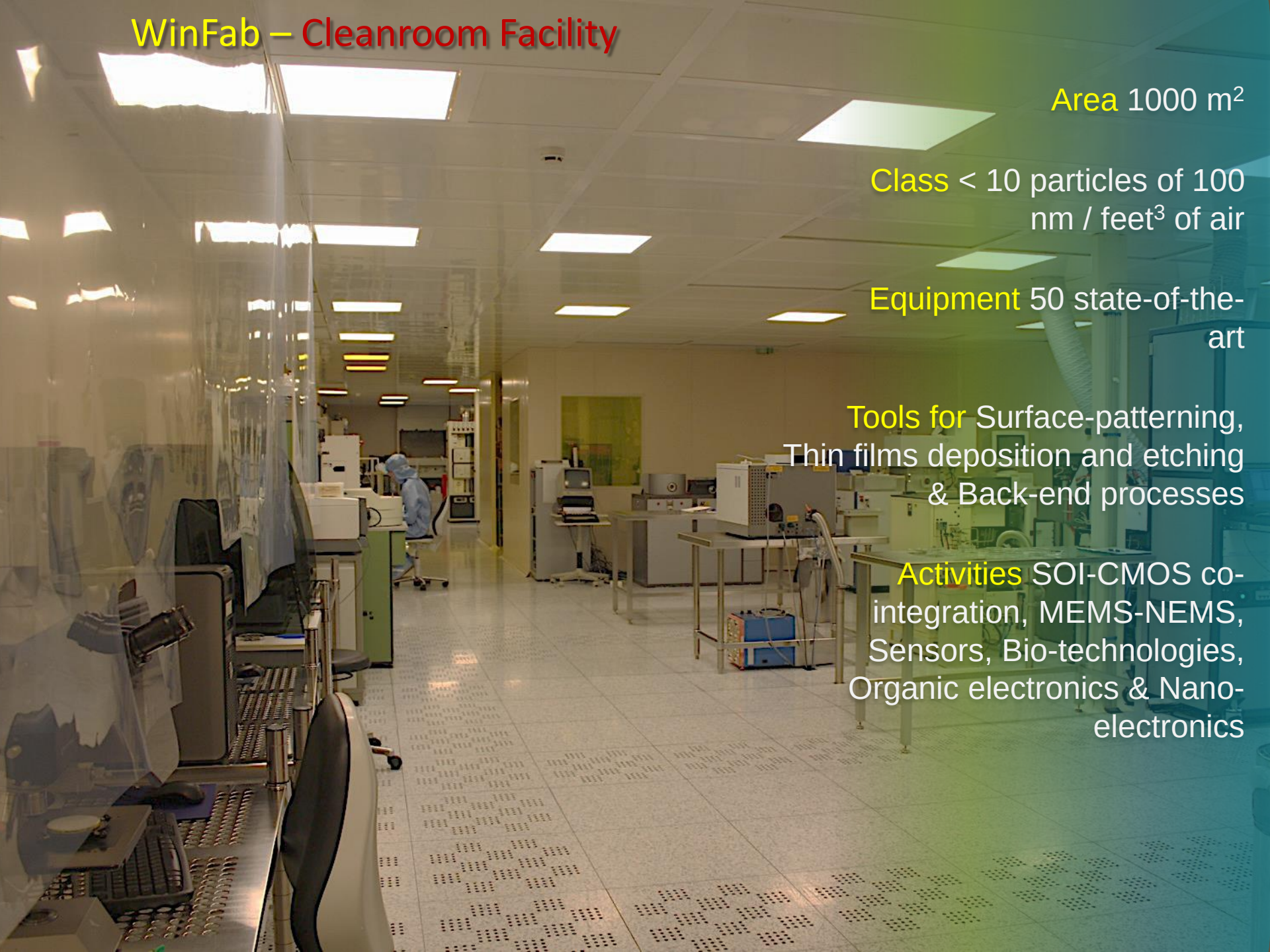
Load-pull 0.8 – 50 GHz

Temperature 4K – 600K

Noise RF and 1/*f*

Packaged, co-axial and on-wafer

WinFab – Cleanroom Facility



Area 1000 m^2

Class < 10 particles of 100 nm / $feet^3$ of air

Equipment 50 state-of-the-art

Tools for Surface-patterning, Thin films deposition and etching & Back-end processes

Activities SOI-CMOS co-integration, MEMS-NEMS, Sensors, Bio-technologies, Organic electronics & Nano-electronics


CRC – Cyclotron Resource Centre
Facilities Heavy Ion Irradiation, Proton Beam Line, Neutron and Gamma Irradiation
One of the most powerful cyclotrons in Europe
Co-located with WELCOME in Louvain-La-Neuve

Mostafa Emam
Founder and CEO

Jean-Pierre Raskin
Chief Scientific Advisor

César Roda Neve
Consultant

Sergej Makovejev
Senior Engineer

Anthony Mazzeo
Technician

Catherine Marcin
Business Developer

Technology Enablement

- TCAD Simulations
- Design and Fabrication of Test Structures
- Characterization and measurements
- Compact and Macro Modelling
- PDK Support
- Design of Demonstrator Circuits

Technology Enablement

Keywords

DC, analog & RF

Bulk & SOI

CMOS

Characterization & Modelling

Design

Cryogenic & High Temperature

Radiation Hardness

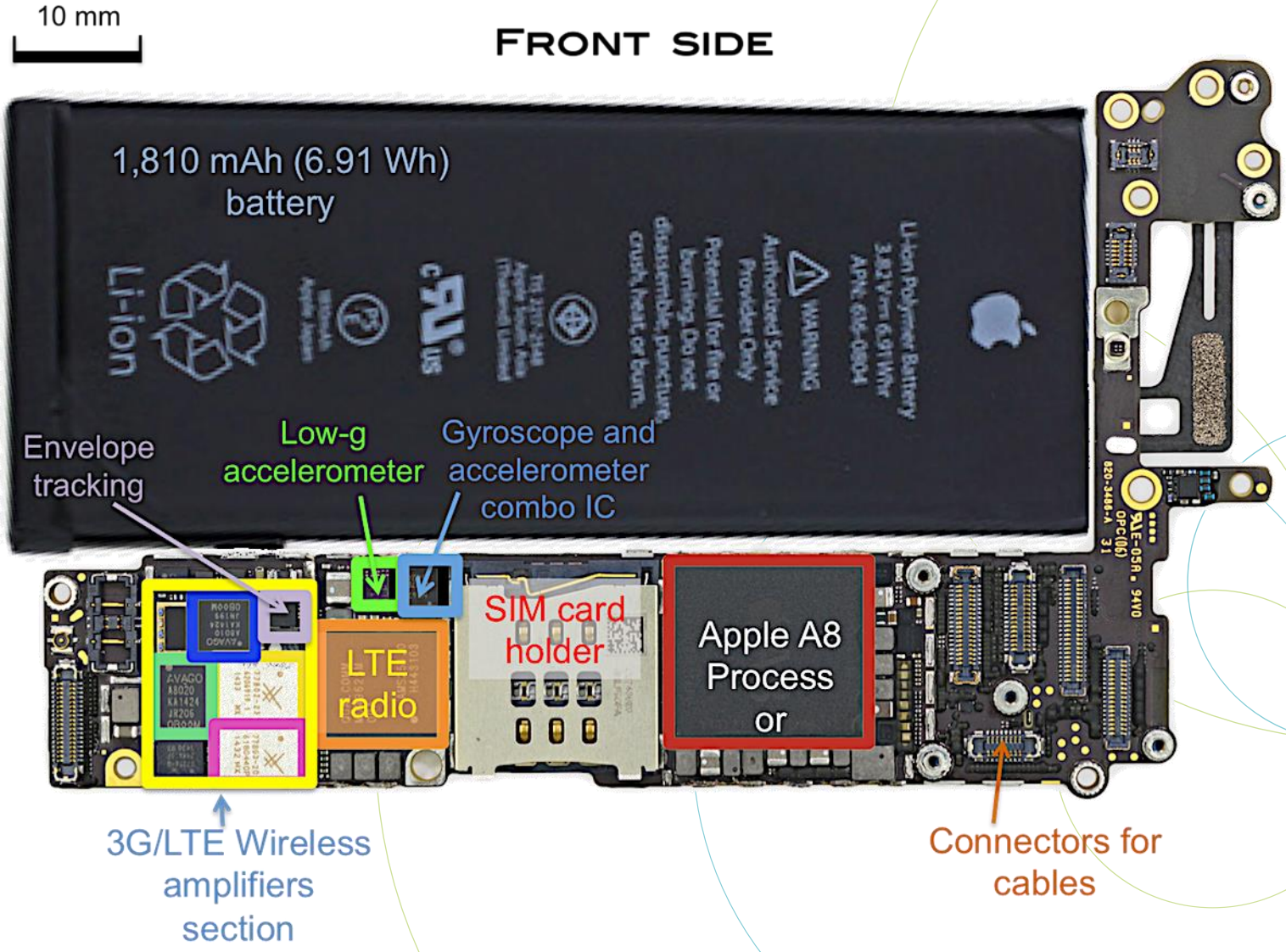
Macro & Compact Models

1/f and RF Noise

Small and Large Signal

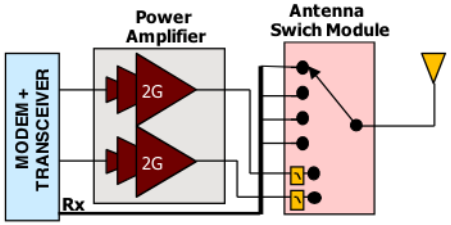
Technology Enablement – Mobile Applications

Front End Module

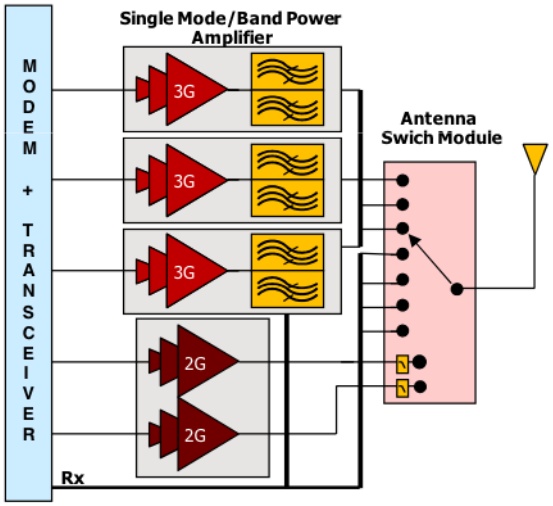


Courtesy: iFixit

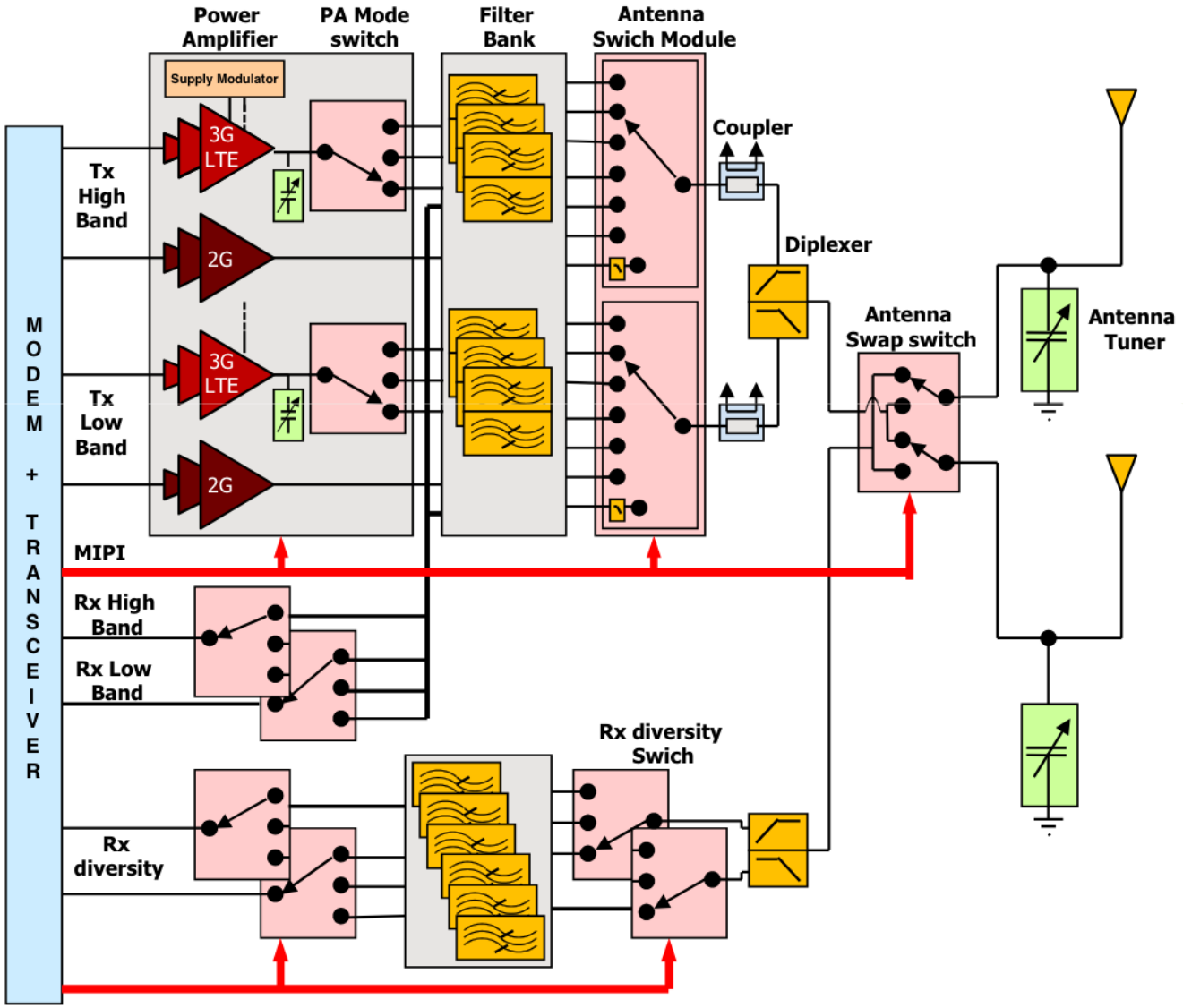
Front End Module – 2G



Front End Module – 3G



Front End Module – 4G/LTE



Standards and FEM Architecture Driving Tougher RF Performance

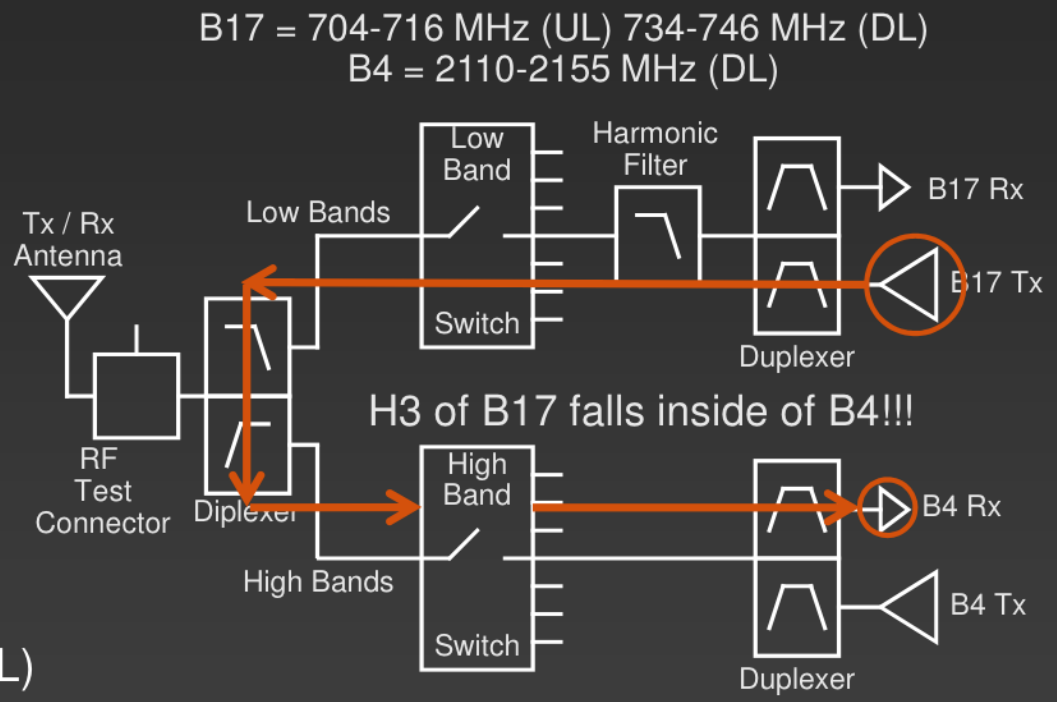
Lower insertion loss:
- Increased RF path loss

Higher linearity:
- Interference distortion

Improved isolation:
- Internal and external interferers
- Radiated coupling / layout

Increased efficiency:
- Higher PAPR (D / L and U / L)

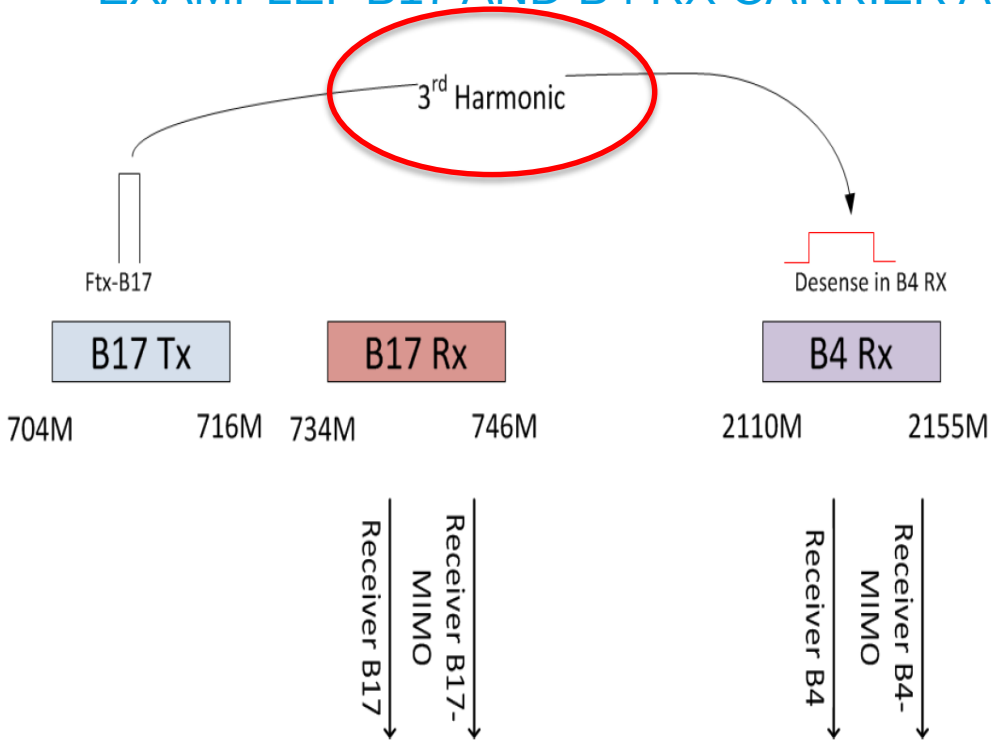
Carrier aggregation places additional burden on these requirements

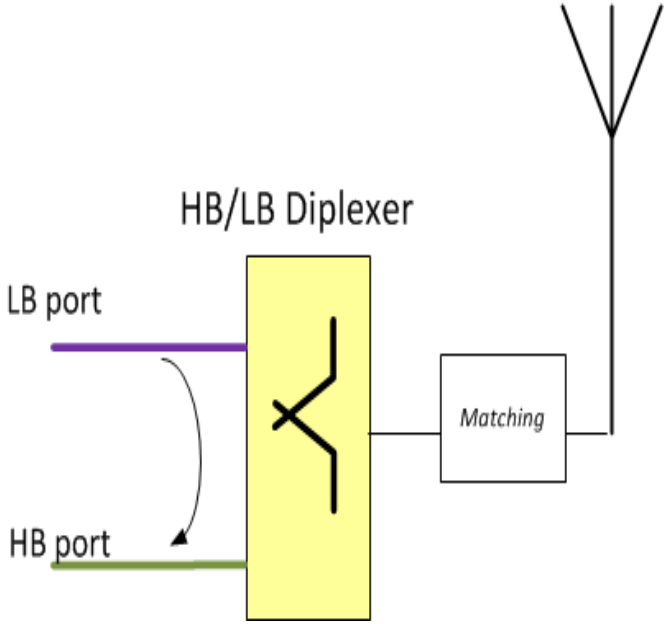


Source: Peter A. Rabbeni, Director RF Product Marketing and Business Development, GLOBALFOUNDRIES
SOI Consortium RF SOI Workshop – Shanghai, September 2015

Key Issue for Rel 9 Carrier Aggregation 4G Standards

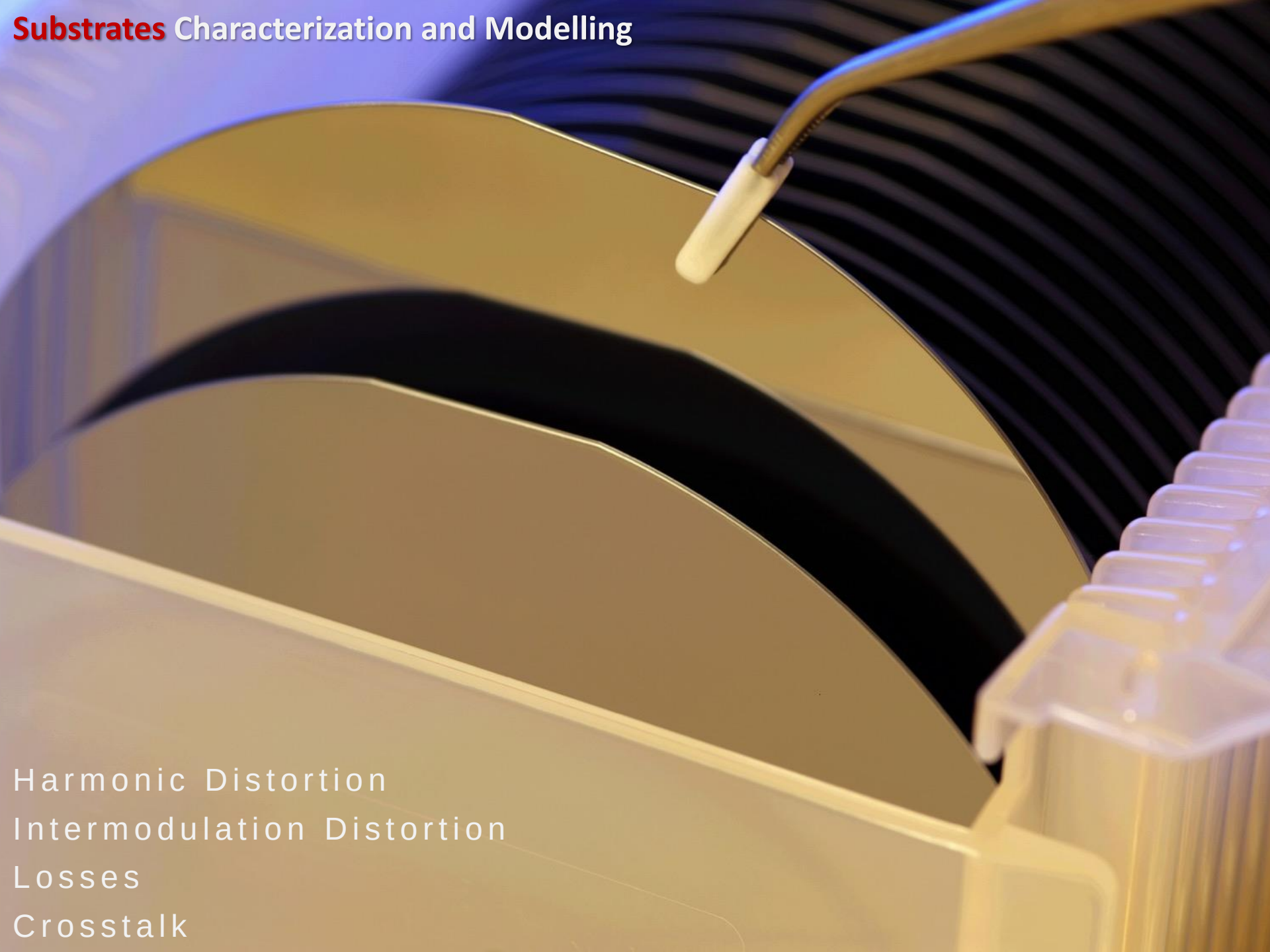
EXAMPLE: B17 AND B4 RX CARRIER AGGREGATION





- We need 4 receivers at the same time
- We need a linear transmitter chain during RX CA

Substrates Characterization and Modelling



Harmonic Distortion

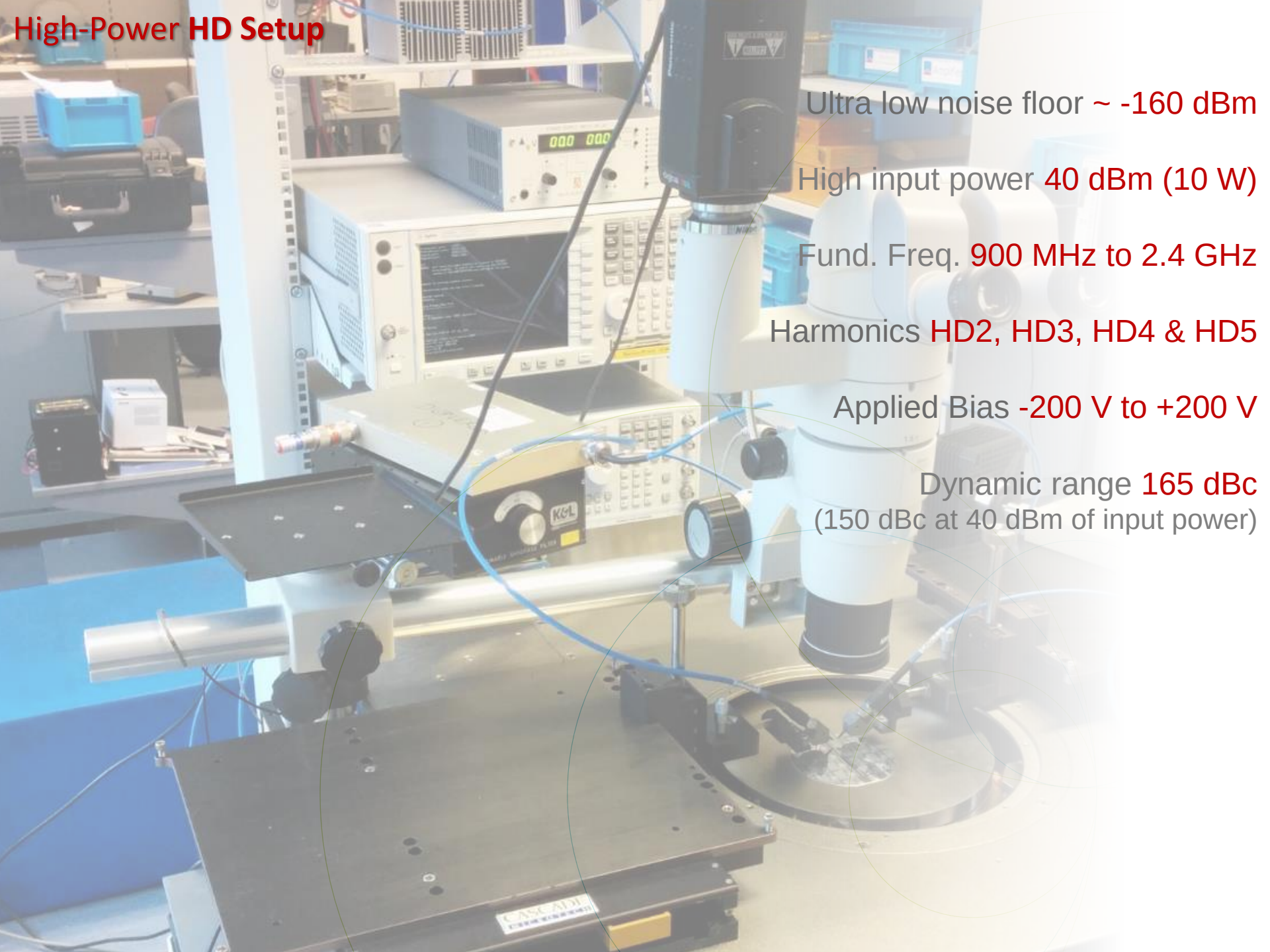
Intermodulation Distortion

Losses

Crosstalk


igh-Power HD Setu

High-Power HD Setup



Ultra low noise floor ~ -160 dBm

High input power 40 dBm (10 W)

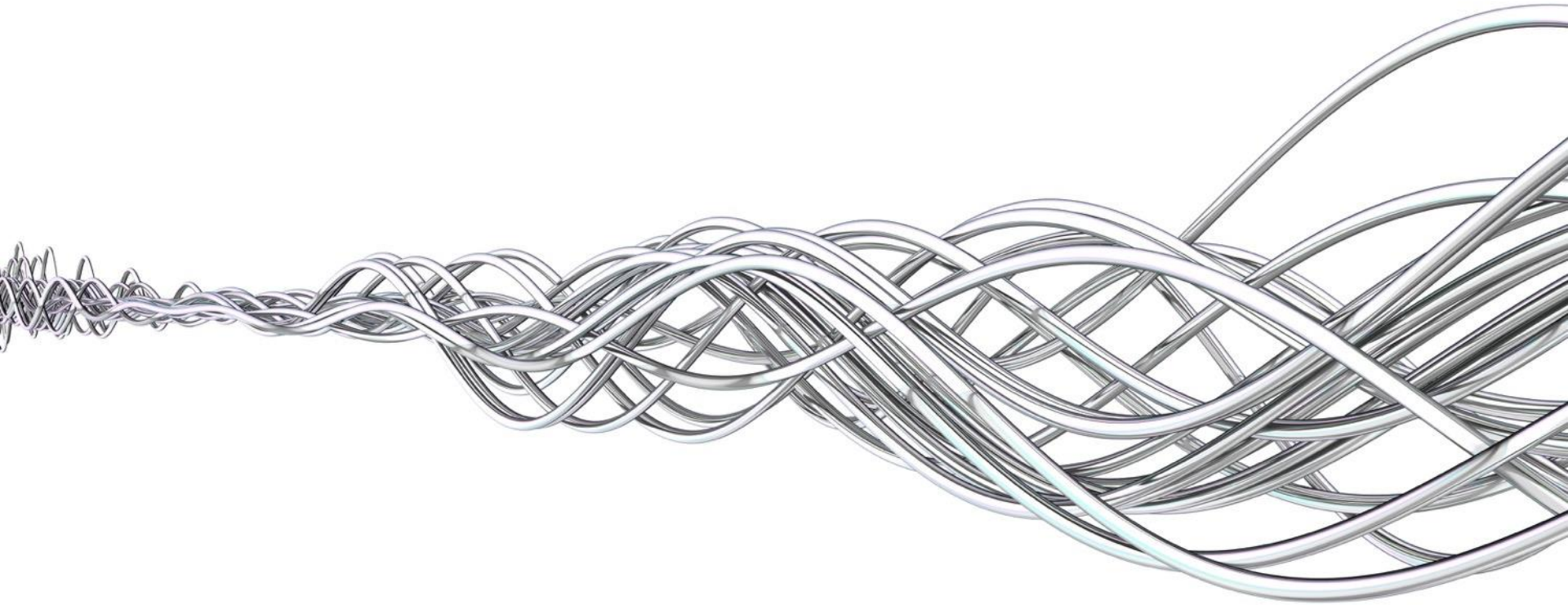
Fund. Freq. 900 MHz to 2.4 GHz

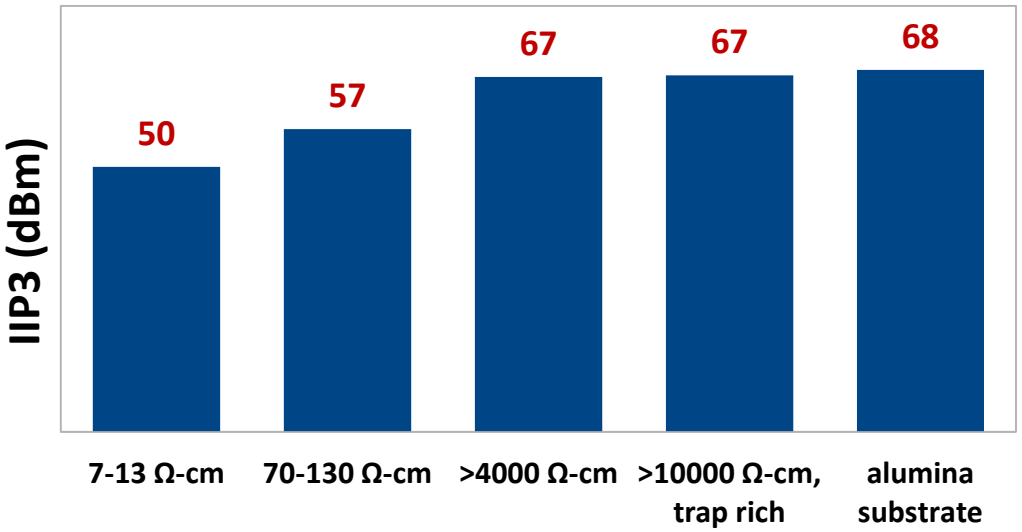
Harmonics HD2, HD3, HD4 & HD5

Applied Bias -200 V to +200 V

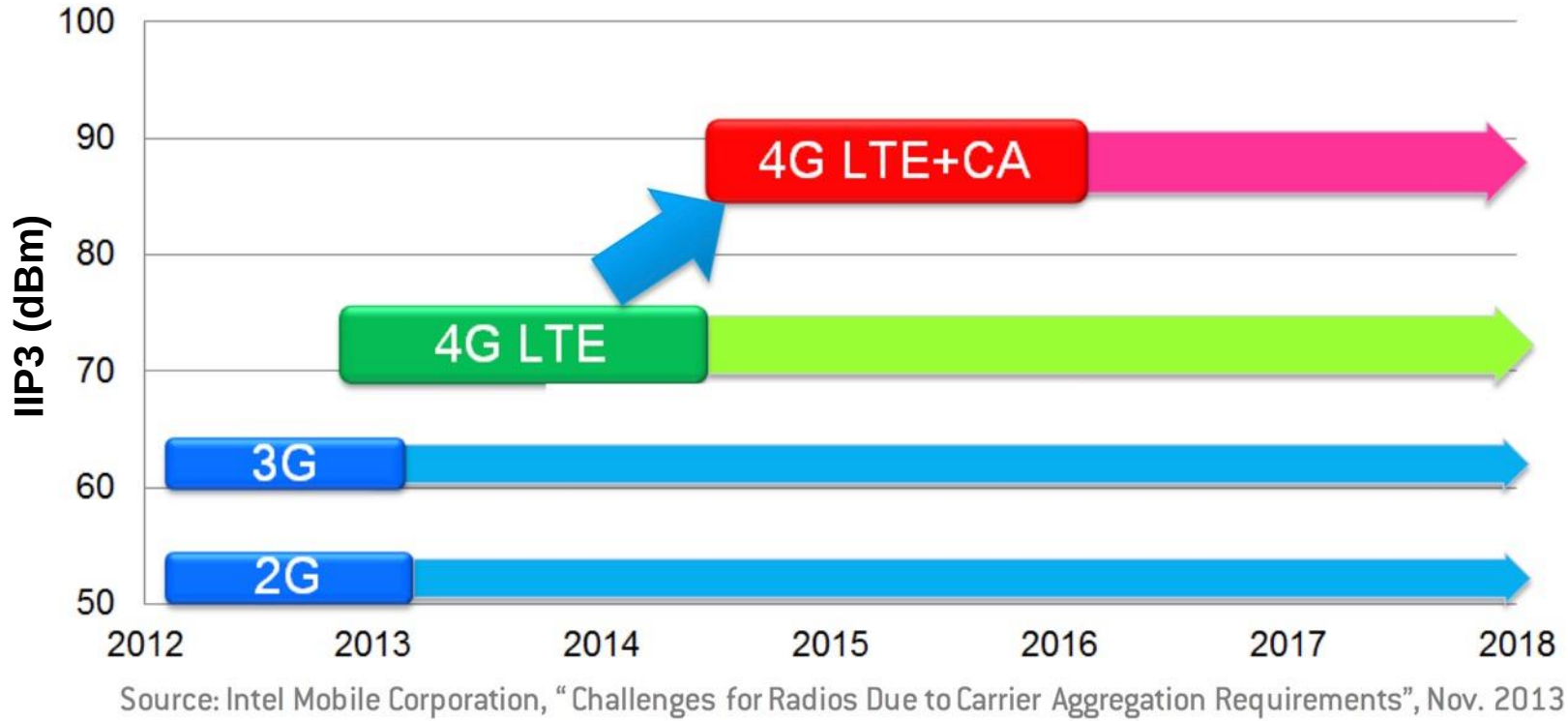
Dynamic range 165 dBc
(150 dBc at 40 dBm of input power)

Intermodulation Distortion Measurements





$P_1 = P_2 = 25$ dBm
$f_1 = 825$ MHz, $f_2 = 875$ MHz



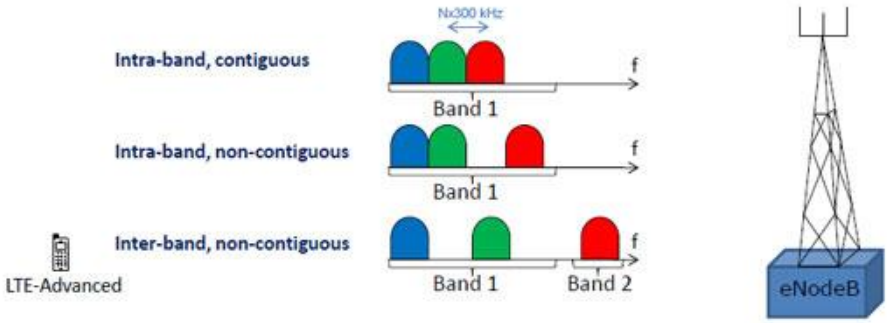
Source: Intel Mobile Corporation, "Challenges for Radios Due to Carrier Aggregation Requirements", Nov. 2013

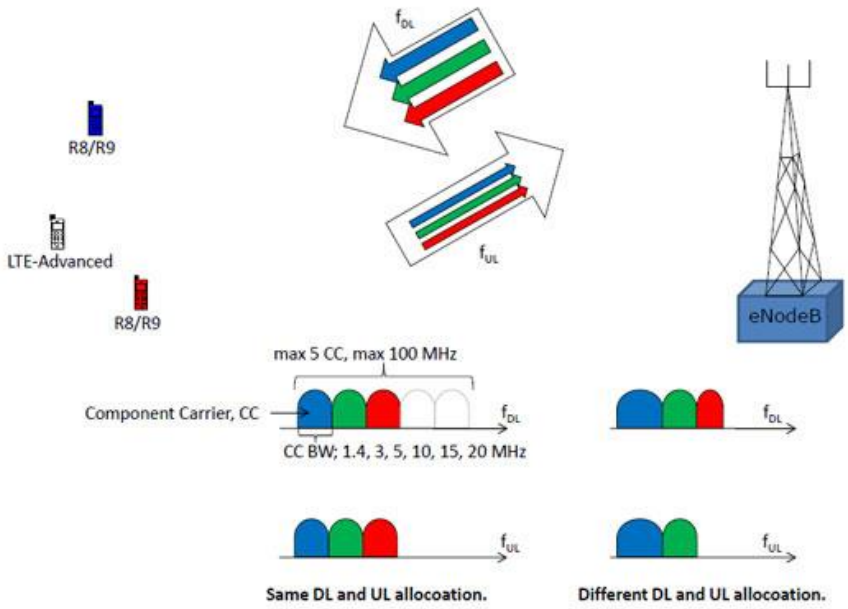
Why Intermodulation Distortion measurements?

Carrier Aggregation

Carrier Aggregation

- LTE-A = Long Term Evolution – Advanced
- Large number of bands, tightly packed
- Bandwidths 1.4, 3, 5, 10, 15 or 20 MHz
- Bandwidth ↑, data rate ↑
- 20 MHz = 150 Mbps
- CA = combining smaller bands into one
- Max 5 component carriers
- Total bandwidth 100 MHz max

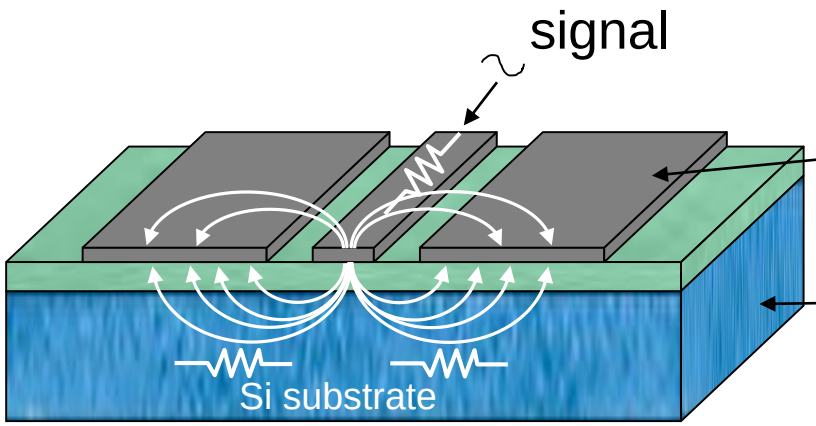




Source: Jeanette Wannstrom, for 3GPP, (Submission, June 2013)

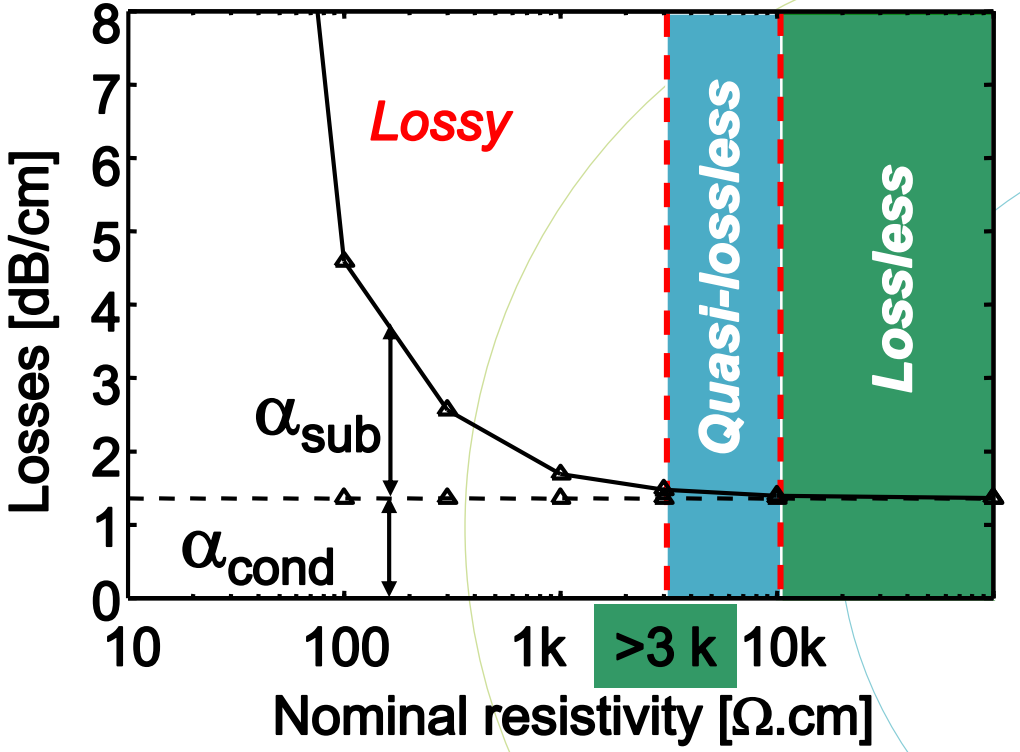
SOI Substrates – Characterization Techniques

High Resistivity SOI substrates: how high should we go?



Conductor losses (α_{cond})

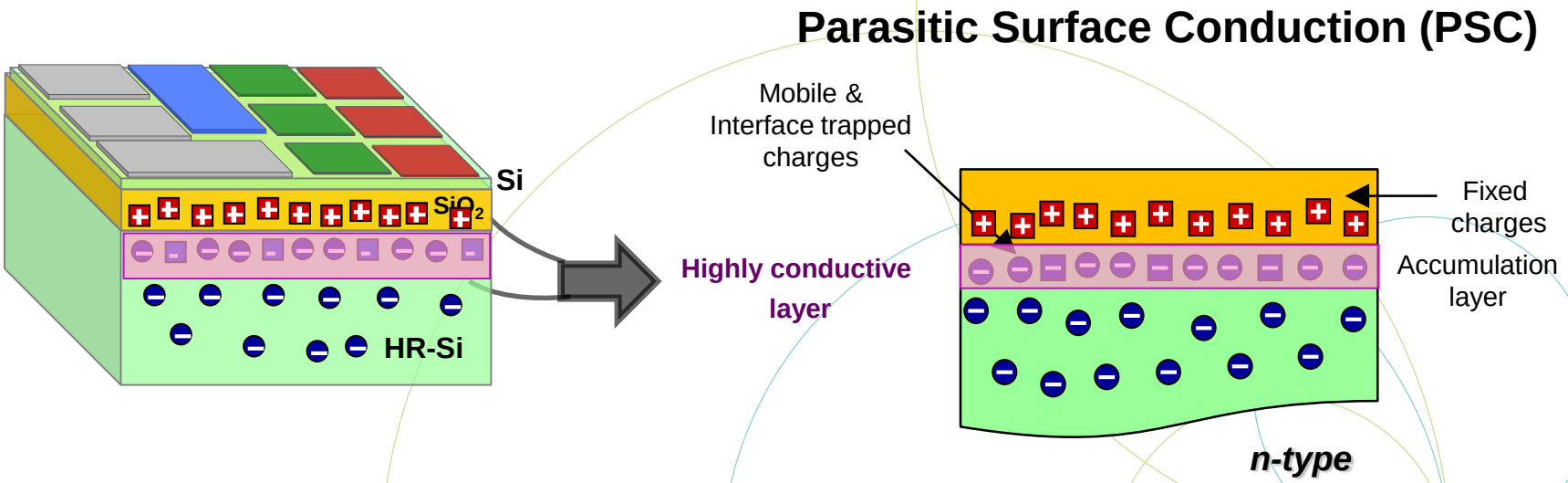
Substrate losses (α_{sub})



STD SOI: 20 Ω.cm → high losses

HR SOI of 10 kΩ.cm would correspond to a lossless Si substrate

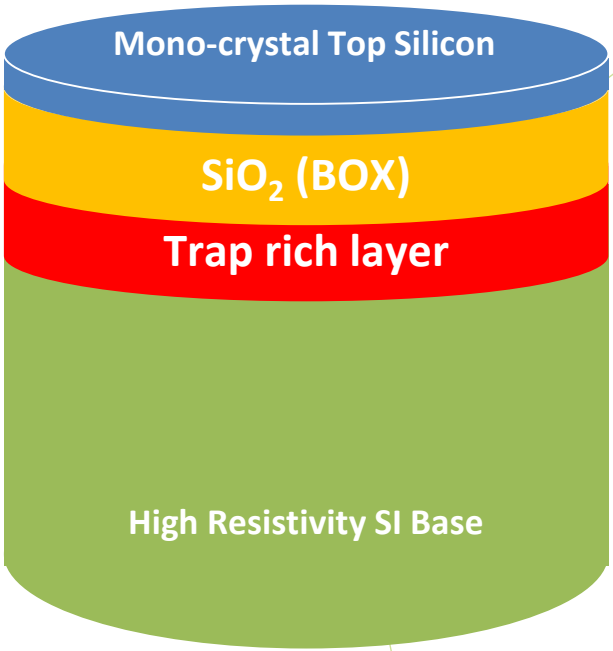
HR-SOI suffers from Parasitic Surface Conduction (PSC) effect at the SiO_2/Si interface.

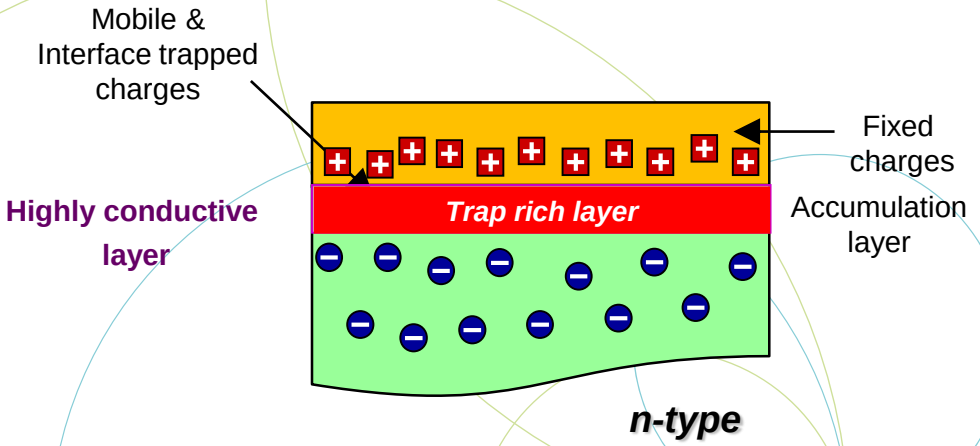


10 kΩ.cm + PSC ≈ 200 Ω.cm

[C. Roda Neve *et al.*, TED'12]

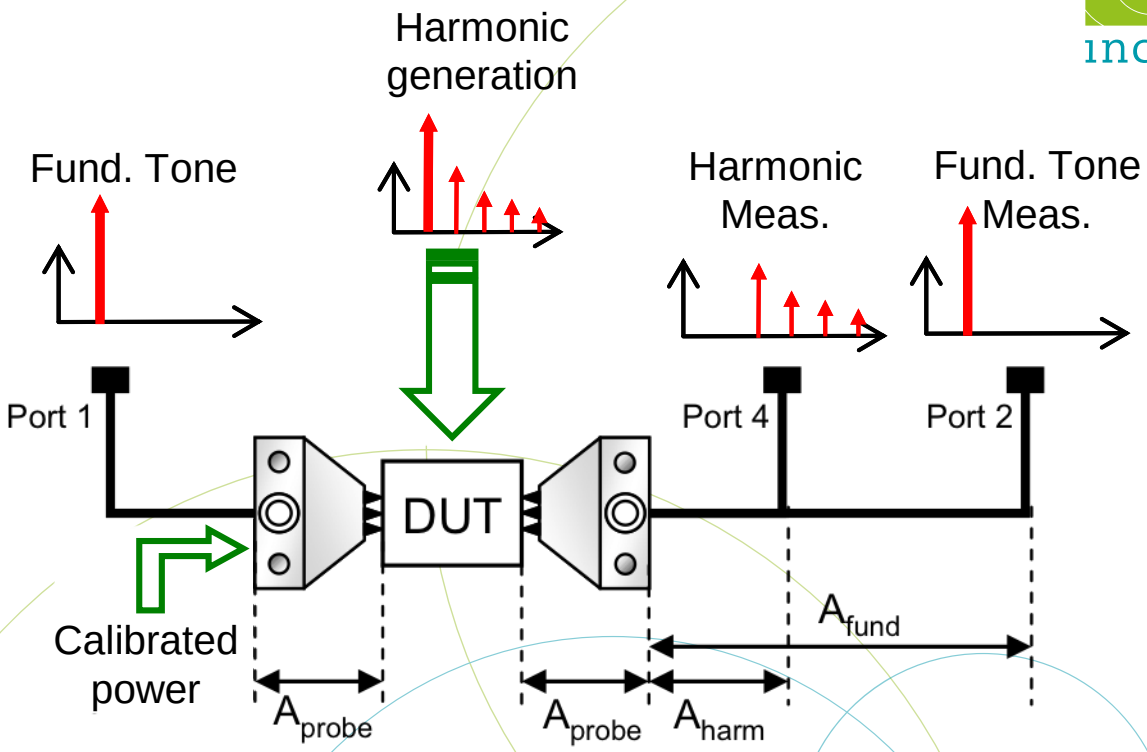
Trap Rich layer freezes the highly conductive layer at BOX – Handle interface



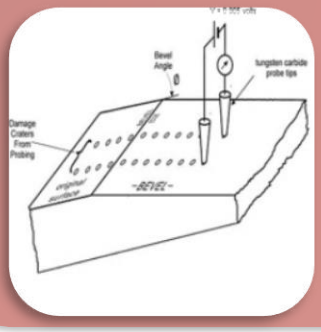


Substrates – RF Non-Destructive Characterization

- Harmonic Distortion
- Intermodulation Distortion
- S-Parameters
- Cross Talk
- Digital Noise

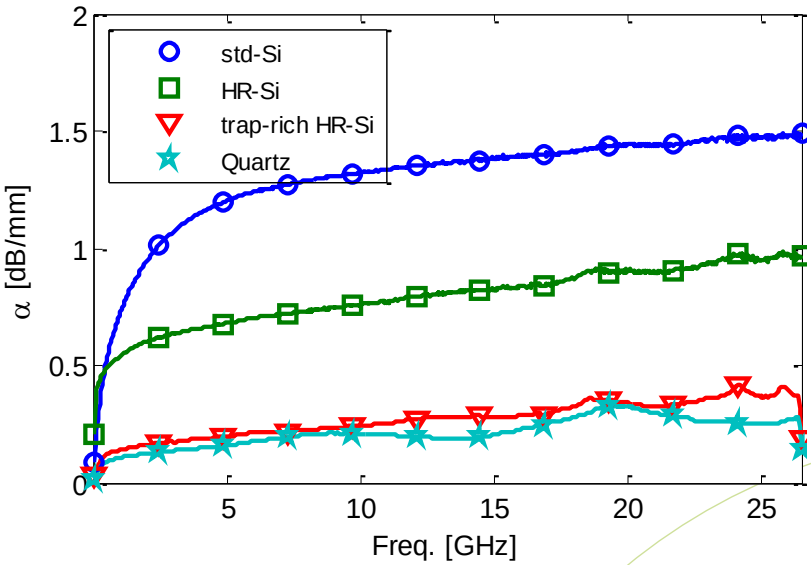


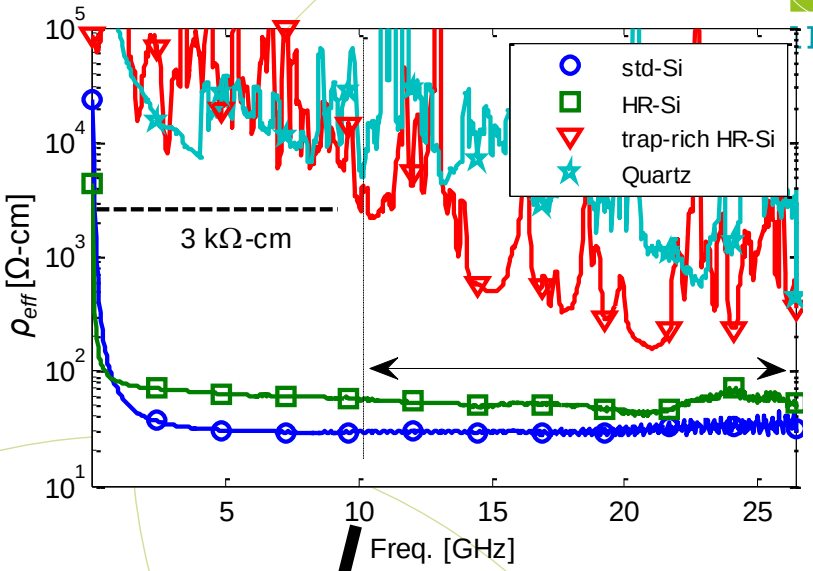
Spreading Resistance Profiling (SRP)



- Destructive. Difficult to get detailed wafer mapping.
- Does not capture interface conduction.
- Difficult to relate to final processed RF and Non-linear wafer behavior.
- **Expensive**

Substrates – Small Signal Characterization



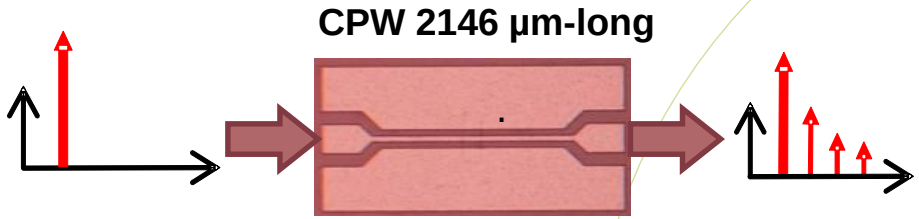


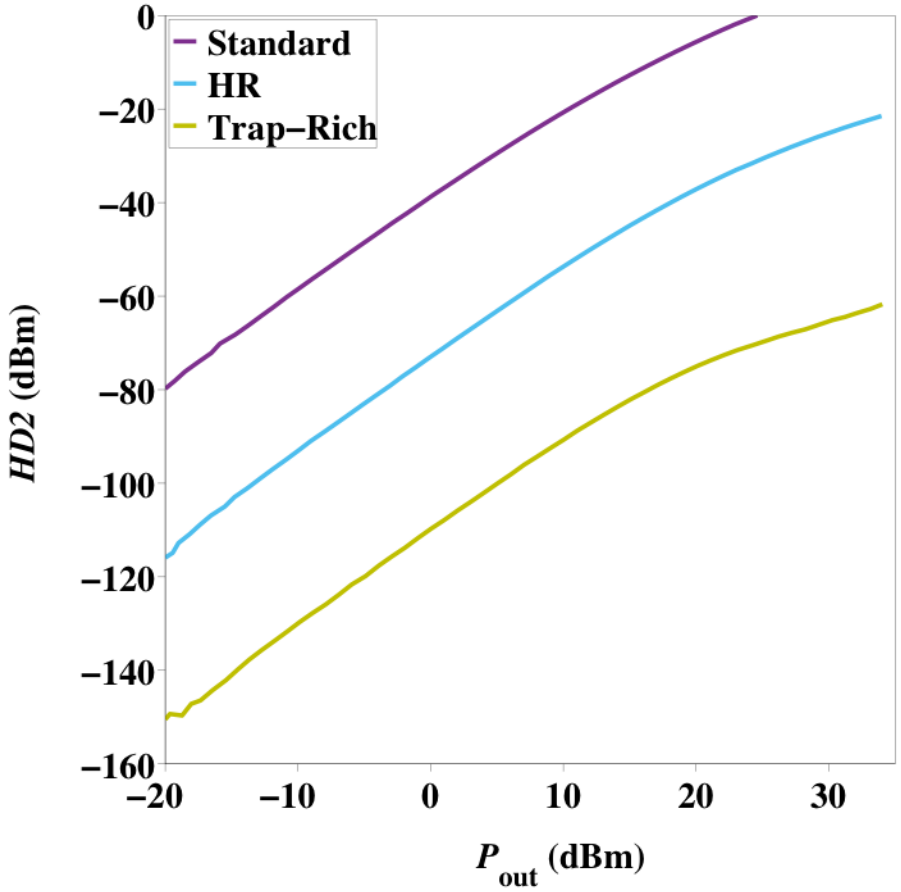
	ρ_{nom} [Ω-cm]	ρ_{eff} [Ω-cm]
std-Si	10	33
HR-Si	> 5 k	64
Quartz	-	> 5 k
trap-rich HR-Si	> 5 k	> 5 k

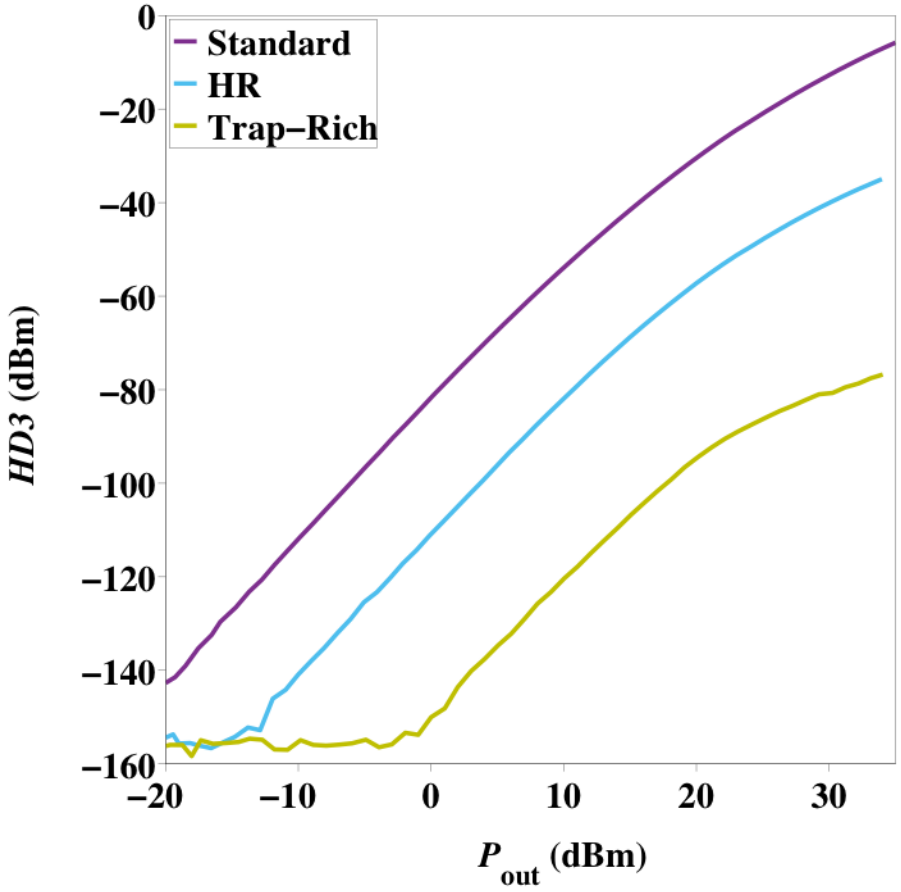
Q_f ~ 3x10^{11}

[Roda Neve *et al*., EUMIC'08]

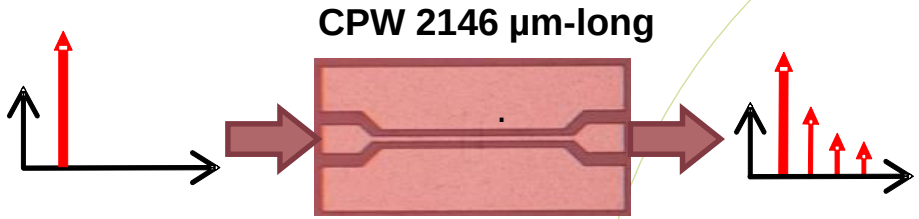
Substrates – HD Characterization

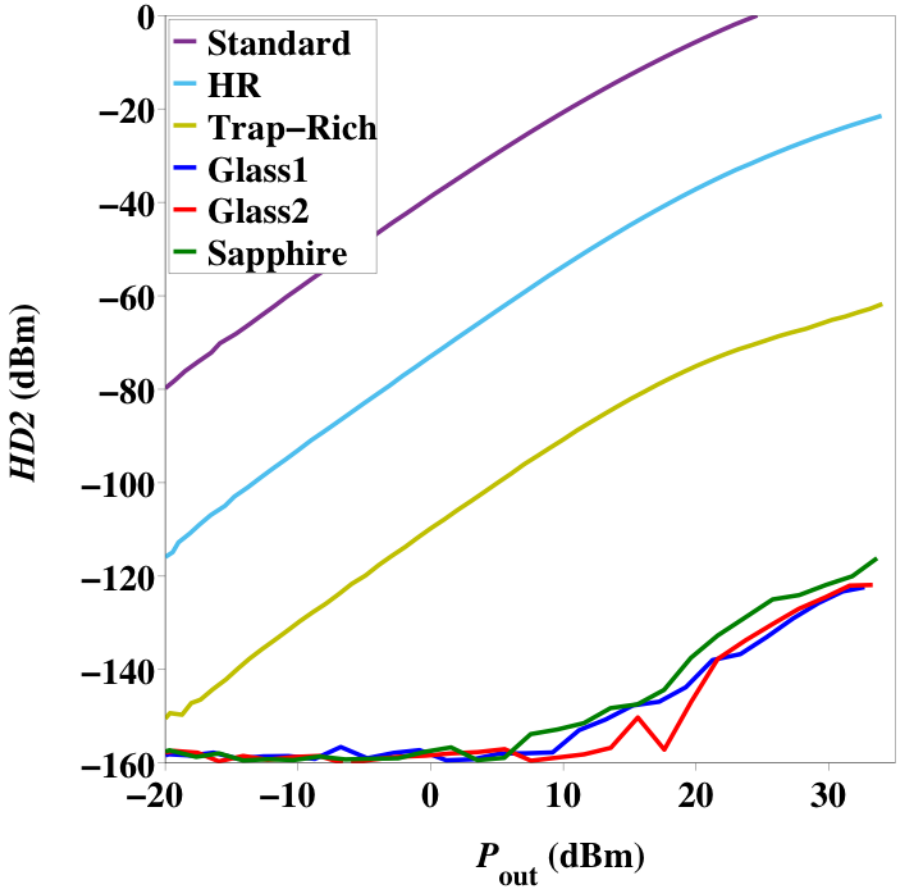


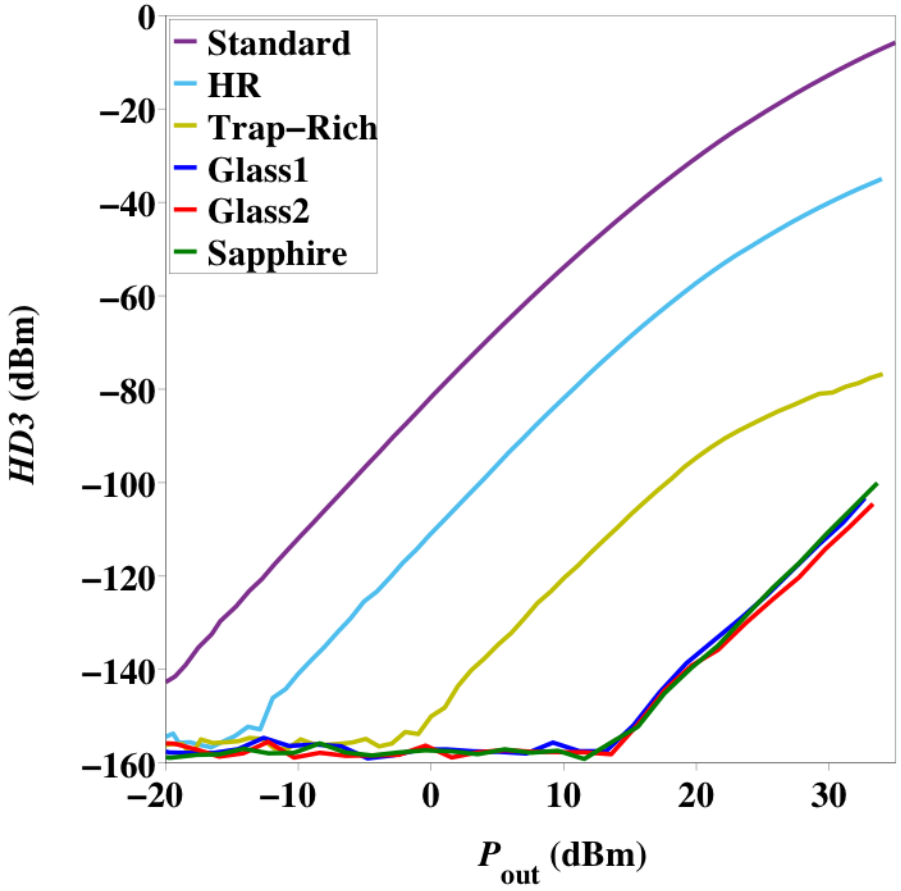




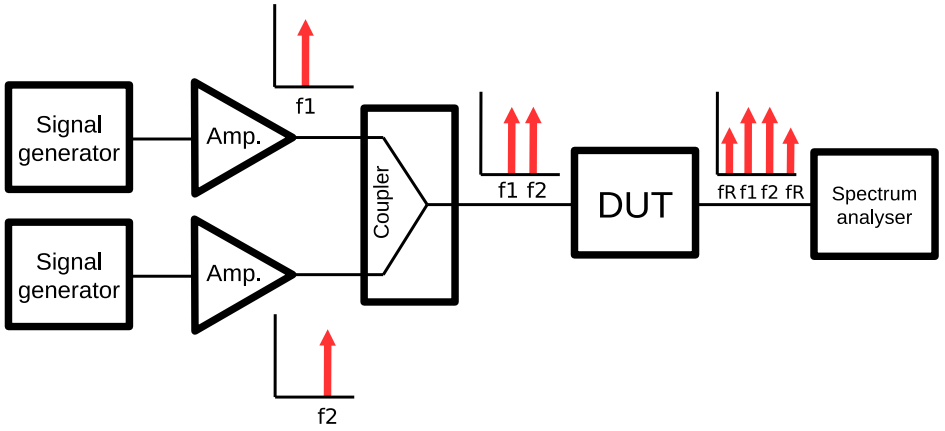
Substrates – HD Characterization

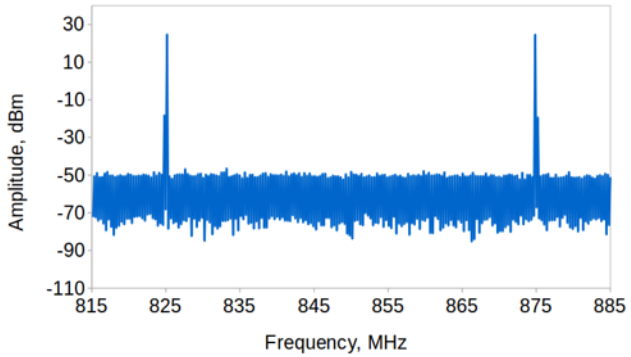


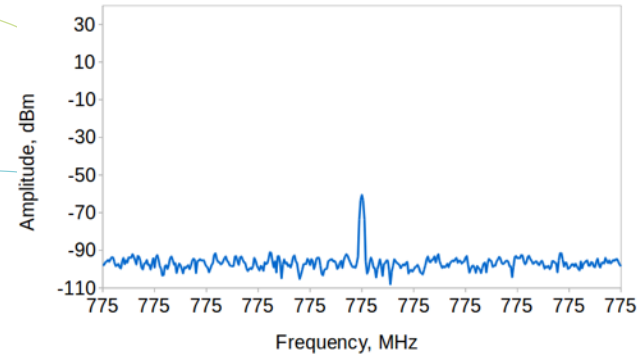


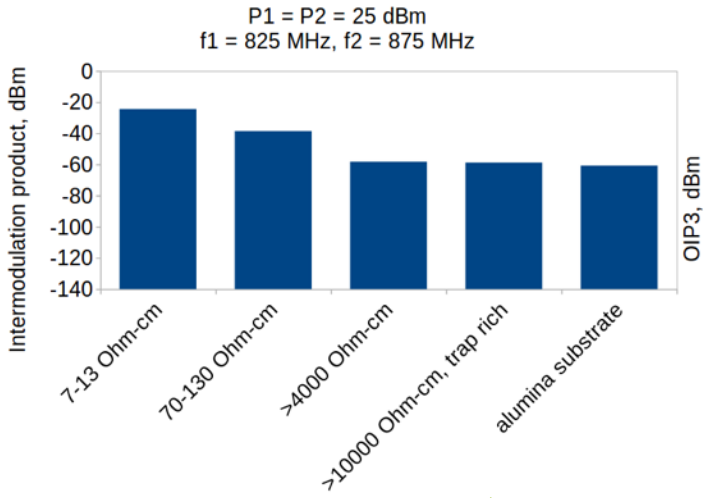


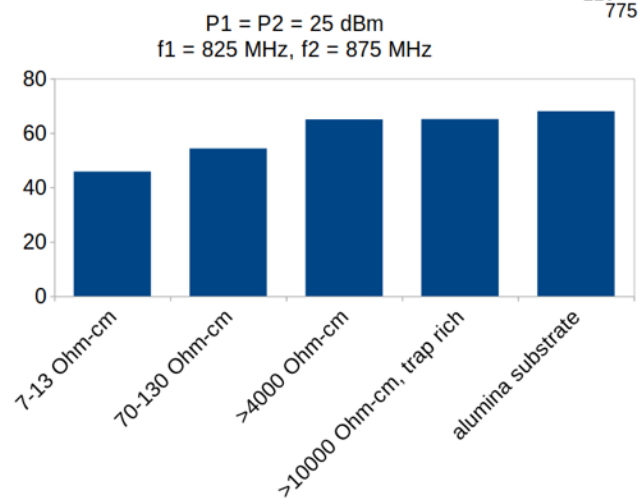
Substrates – HD Characterization (Two-tone)



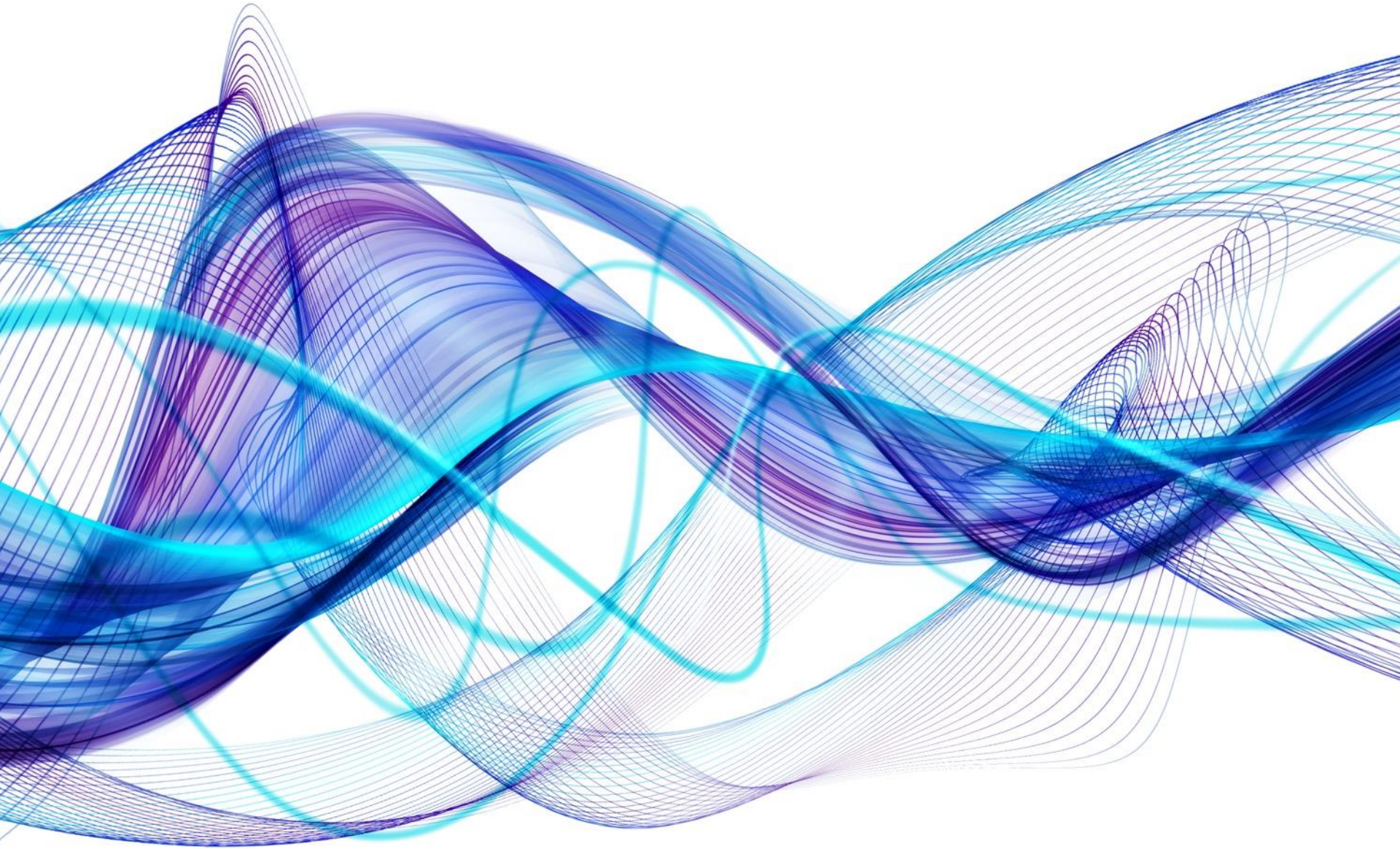








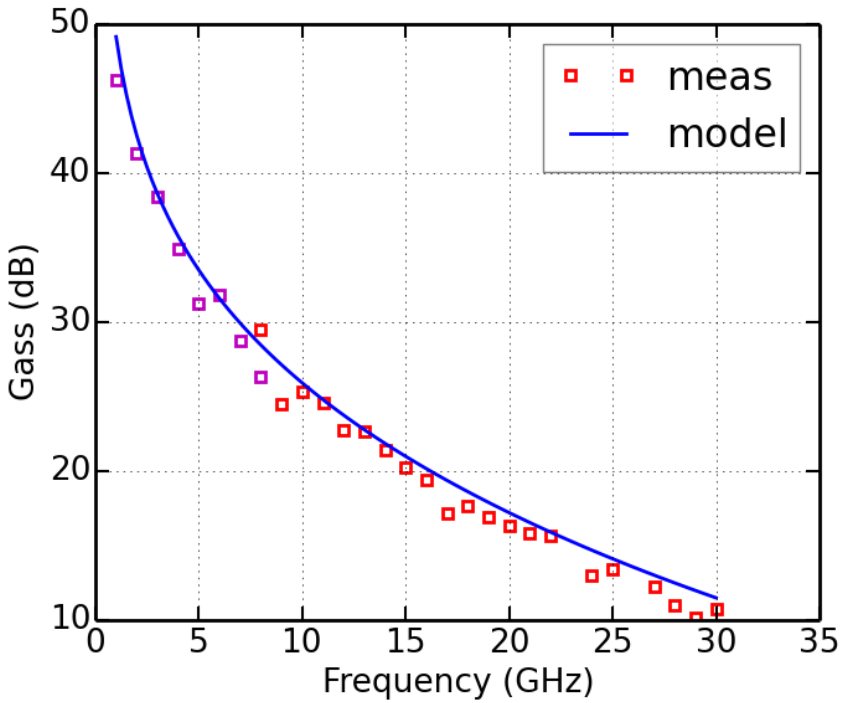
Technology Enablement – Transistor Noise

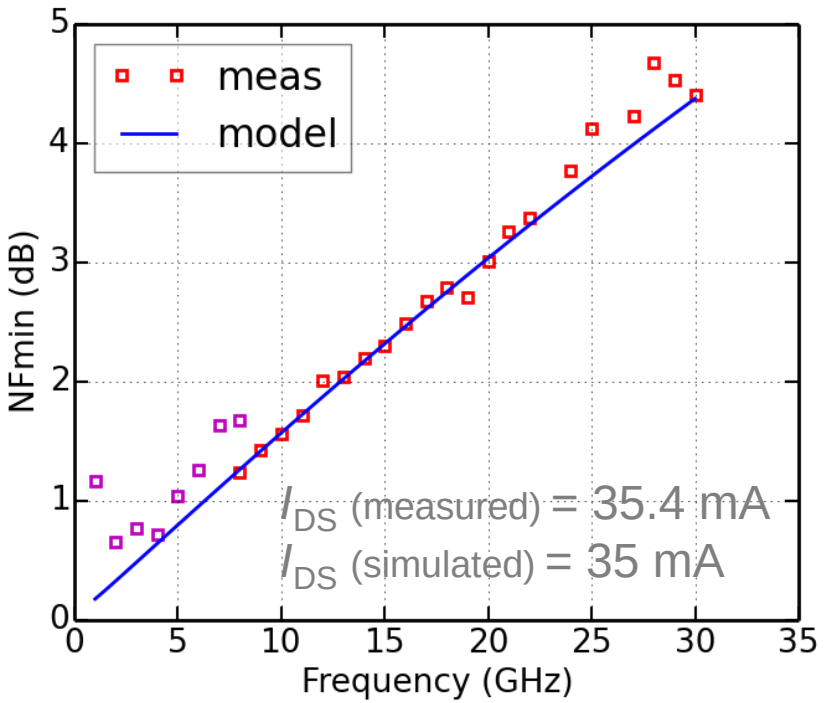


RF Transistor Noise

$L = 0.13\ \mu m$
$W_{finger} = 5\ \mu m$
$N_{finger} = 16$

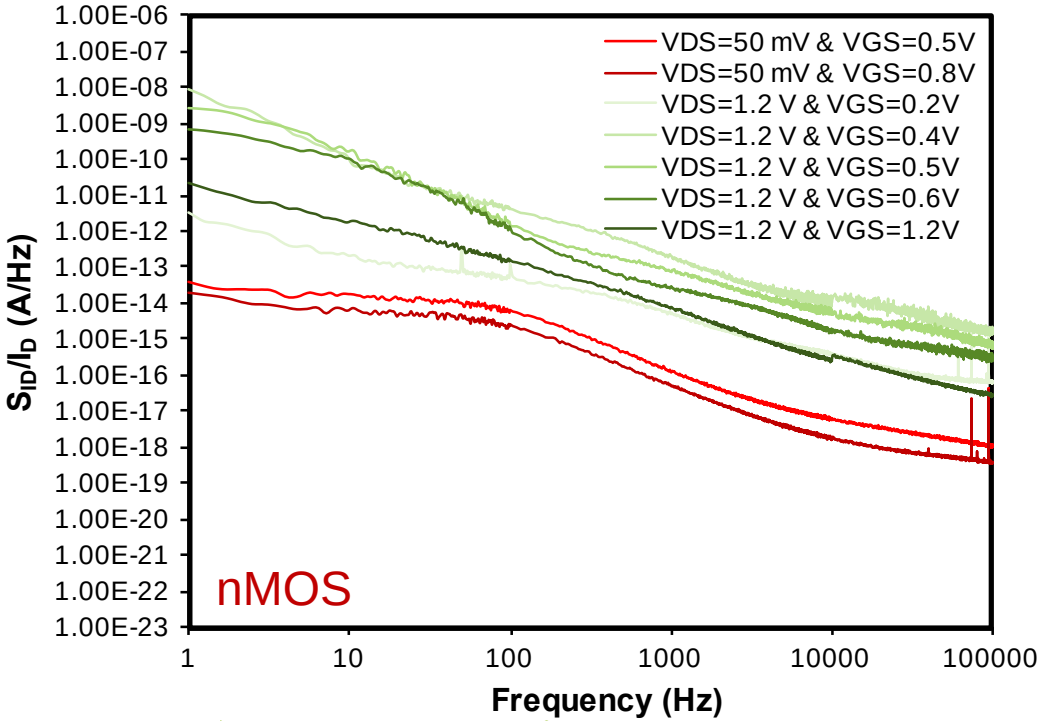
$V_{DS} = 1.0\ V$ & $V_{GS} = 1.25\ V$

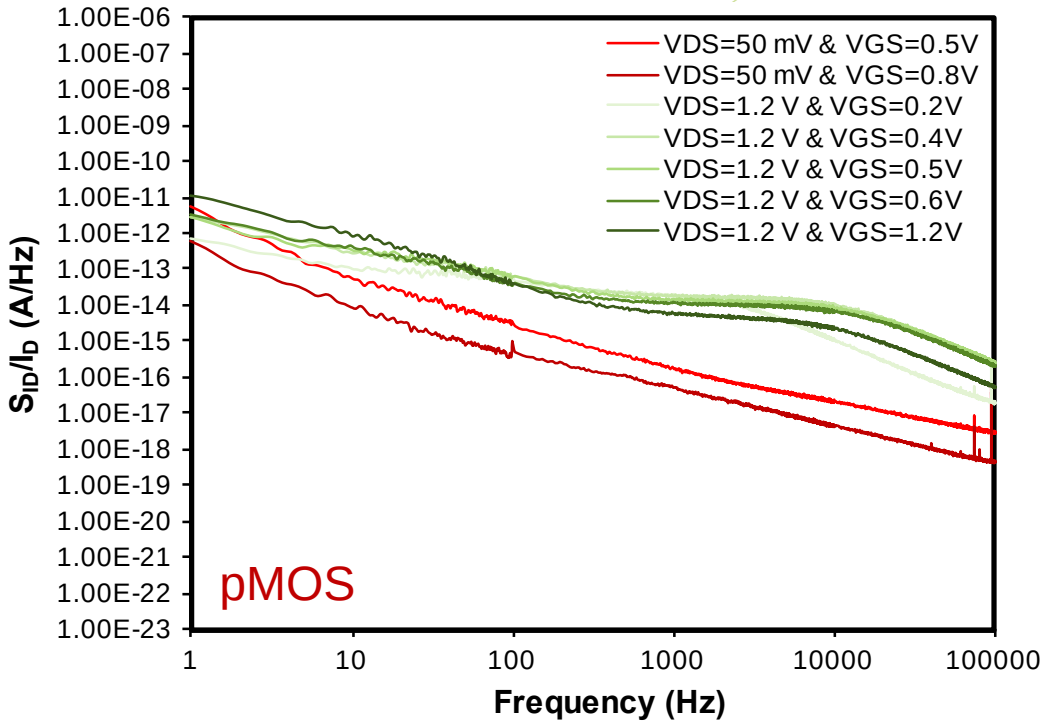




Measurements	**0.8 GHz to 75 GHz**
Parameters	**NF, NF_{min}, G_{ass}, Y_{opt} and R_n**
Modeling	**Interpretation and modeling services**
Simulation	**TCAD simulations and extractions**

1/*f* Transistor Noise






training

SOI

Substrates

FD SOI – Basics, fabrication, physics, applications, vs FinFET

RF SOI – Basics, Applications, Advantages, FoM

Nonlinearities – Origin, FoM, Solutions, Modeling

Transistors

SOI CMOS – Basics, physics, characterization, Modeling

On-wafer Characization – Setup, test-structures, hands-on

Self-heating – Origin, characterization, modeling

Noise – 1/f, RF, RTN, origin, physics, charac., modeling

Applications

Variability – Origin, impact, solutions, design

Reliability – Basics, FoM, mechanisms, design solutions

RadHard – Introduction, sources, characterization

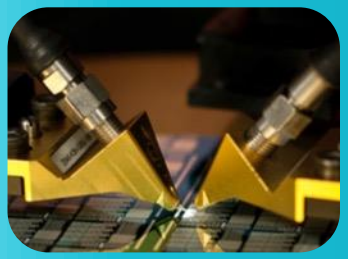
Analogue – Design tools, advantages, hands-on

MEMS – Introduction, RF applications, challenges


TAKE AWAY

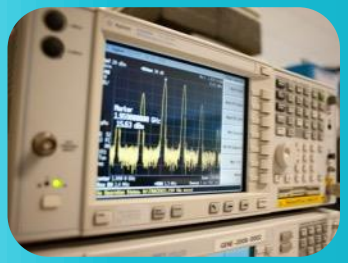
Take Away

incize



Technology Enablement services include: Characterization, modeling and PDK support for Si-based technologies with a focus on RF SOI

Training services include: customized training modules for topics related to SOI, RF SOI and advanced SOI technologies



Turn-Key Solutions provide our customers with specialized test-benches along with their control software, extraction routines and calibration kits


Thank
you!