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An Ultra-Thin Ultraviolet Enhanced Backside-Illuminated Single-Photon Avalanche Diode with 650nm-Thin Silicon Body Based on SOI Technology

Iman Sabri Alirezaei, Nicolas Andre, Amor Sedki, Pierre Gerard, and Denis Flandre

***Abstract*— We present the world's thinnest backside illuminated (BSI) single-photon avalanche diode (SPAD) with a silicon (Si) thickness of 650nm fabricated in complementary metal-oxide-semiconductor (CMOS) compatible silicon-on-insulator (SOI) technology. The well-optimized doping profile is exploited in this square-shaped BSI SPAD with ultrathin Si body consisting of n^{++}/p-well and n-well guard ring (GR) to outstandingly improve detection efficiency in ultraviolet (UV) spectral range. This BSI SPAD exhibits a low leakage current (≈0.1pA) and a low breakdown voltage (8.5V) at room temperature (RT). A low dark count rate (DCR) of 156.8cps/μm^2 at 3V excess bias is estimated at RT. A peak quantum efficiency (QE) of 96.41% is also measured under a wavelength of 423nm at 4V. This BSI SPAD indicates a peak photon detection probability (PDP) of 69.51% upon a wavelength of 423nm at 3V excess bias. A significant expansion of the UV sensitivity down to a wavelength of 291nm is represented with a PDP of 15.56% at 3V excess bias. To the best of our knowledge, the detection efficiency of this ultrathin BSI SPAD in the UV wavelength regime down to 291nm is the best result ever reported for Si-based BSI SPAD in spite of the absence of an integrated CMOS circuitry.**

***Index Terms*—Geiger-mode avalanche photodiode (G-APD), single photon avalanche diode (SPAD), backside-illuminated SPAD, ultraviolet (UV)-SPAD, low-level light detection, CMOS technology, silicon-on insulator (SOI), flexible SPAD.**

I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) operating in low light detection with a high sensitivity in UV spectral range are of great interest in quantum communications (~390nm) [1], quantum ghost imaging (QGI) and spectroscopy (QGS) in UV spectral range for ultra-low light microscopy [2], UV fluorescence light detection and ranging (LiDAR) and UV-Raman LiDAR (~355nm-532nm) [3, 4], fluorescence lifetime imaging microscopy (~400nm-580nm) [5], positron emission tomography (PET) scanners for diagnostics and medical monitoring (~360-505nm belonging to the peak wavelength of the generated scintillation light in a scintillator) [6], time-of-flight (TOF) UV spectroscopy, and many other biological identification systems [7, 8].

The improvement of detection efficiency in UV wavelength regime for Si-based detectors suffers from a shallow absorption depth (less than ~500nm in the UV spectral range below 450nm).

Under frontside illumination, the UV detection efficiency can be improved in a more appropriate way by exploiting an ultra-shallow junction with a proper space charge region width, in turn leading to acceptable leakage current, breakdown voltage, and dark count rate (DCR). In particular, an optimum ultra-shallow junction based on p^+-n structure has been developed by the implementation of pure boron (PureB) for the UV wavelength regime from 2nm to 400nm [9, 10].

Under backside illumination, the improvement of UV detection efficiency encounters challenges to minimize the diffusion region related to the distance from the backside silicon surface to the edge of the space-charge region (or drift region) towards the frontside. To improve this requires exploiting either a thin silicon body and a deeper junction, or a deeper space-charge region to extend the drift region close to the surface on the backside [11, 12]. However, the realization of these structures based on a bulk silicon substrate suffers from the difficulties of forming a proper deep junction and a backside thinning process without creating defects in the silicon device layer. Therefore, the improvement of BSI (i.e. backside illumination) SPADs in UV spectral range still cannot be sufficiently carried out based on the bulk silicon substrate.

For further improving UV sensitivity in BSI SPADs, the use of SOI technology to realize the BSI SPAD on a thin silicon body, stacked on a buried oxide layer (BOX), has indicated a

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higher near-UV and blue sensitivity with a good DCR value compared to the state-of-the-art [13-15]. A recent development of BSI SPAD consisting of 1.5µm-thin silicon body fabricated in standard SOI CMOS technology presented a photon detection probability (PDP) of ~17.5% at a wavelength of 400nm and a maximum PDP of 26% at a peak wavelength of 500nm with a DCR value of 396.1cps/µm^2 at 3V excess bias voltage upon room temperature [15].

The BSI SPADs fabricated in SOI CMOS technology take advantage of high-quality fabrication process for both the ultrathin SPAD feature and the integrated electronic interface for readout and data processing, by implementing an advanced three-dimensional (3D)-stacked technology with less design complexity and process difficulty, compared to the design and the 3D-bonding process based on a bulk Si-wafer [7].

Furthermore, the 3D-stacking techniques, highly demanded in BSI SPADs, open the possibility of independent process and design developments for the SPADs on a top tier and for the electronic interface in a bottom tier, for their respective optimizations. This approach can outstandingly improve the fill factor (FF) towards more than 70% due to the metal free surface on the backside, a photon detection probability (PDP), a decrease of DCR, as well as a lower power consumption owing to the optimized thin SPAD on the top tier and the smaller technology nodes in the bottom tier [7, 11, 15].

Besides, an ultra-thin Si-based SPAD could enable its integration with a CMOS circuitry on a flexible substrate by post-processing transfer. Flexible SPADs appear appropriate for applications such as wearable or implantable chronic biomedical monitoring devices or retinal prosthesis [7, 16, 17].

In this paper, we introduce the world's thinnest BSI SPAD (to date) with a silicon body thickness of 650nm fabricated in CMOS-compatible SOI technology. This BSI SPAD presents the highest detection efficiency in UV spectral range (at a peak wavelength of 423nm) among other existing Si-based BSI SPADs thanks to its ultrathin silicon body and well-defined doping profile, consisting of a gradient p-well for contributing to the higher avalanche probability of the generated electrons under backside illumination in Geiger mode. Besides, this gradient p-well doping profile provides a strong built-in electric field (~8.8×10^5V/cm) at n^{++}/p-well junction inside the multiplication region. Preliminary static performance of this structure measured under frontside illumination have been reported in [18] and is extended here as follows.

The peak PDP of 69.51% measured in the proposed BSI SPAD is shifted towards 423nm, while the peak PDP value in other recent development of UV-enhanced SOI BSI SPAD were shifted down to 500nm only [15].

Furthermore, our proposed ultrathin SOI BSI SPAD minimizes the measured leakage current, DCR, correlated noise, and secondary effects in the avalanche process in Geiger mode. Such performance is achieved thanks to the implementation of ultrathin silicon body and the immunity of the thin silicon layer over a buried oxide layer from any degradation effect caused by the backside thinning and etching process of the bulk silicon substrate.

Through this paper, section II describes the proposed BSI SPAD structure, and the TCAD simulation studies and analyses. The optimization of the doping profiles and diode structure is carried out using the simulation of the fabrication process consisting of several processing steps of thermal SiO_2 growth, ion implantation, and annealing in SILVACO Athena. The figures of merit of the simulated device are studied using SILVACO Atlas. Section III discusses (A) the fabricated device together with the measured static performance under BSI, (B) functional analysis of PDP as well as temperature variations of DCR and breakdown voltage and (C) a performance comparison of the proposed ultrathin BSI SPAD with the state-of-the-art.

II. Device Structure and Simulation Analysis

Fig. 1 depicts a 3D schematic structure of the two neighbor BSI SPADs based on a shared p-well consisting of a gradient profile fabricated on a SOI membrane with the cross-section view of an individual SPAD.

The photogenerated electron-hole pairs are contributing to impact ionization mechanism and avalanche multiplication in Geiger mode. The avalanche probability of generated carriers, which is involved in PDP in Geiger mode, depends on the location of photogenerated carriers and the electric field distribution [19]. Due to the larger impact ionization coefficient of electrons compared to holes, the formation of p-well in the proposed BSI SPAD is superior for maximizing avalanche probability of electrons in the space charge region and enhancing PDP. A gradient profile in p-well will provide a higher electric field at n^{++}/p junction to initiate impact ionization mechanism.

The design of square-shaped BSI SPAD with a total area of 55µm×29µm consists of an effective active area of 13µm×13µm based on n^{++}/p-well junction, an effective guard ring width of 1.5µm based on a n-well, a distance of 3µm between guard ring (GR) and anode, and an anode width of 7µm.

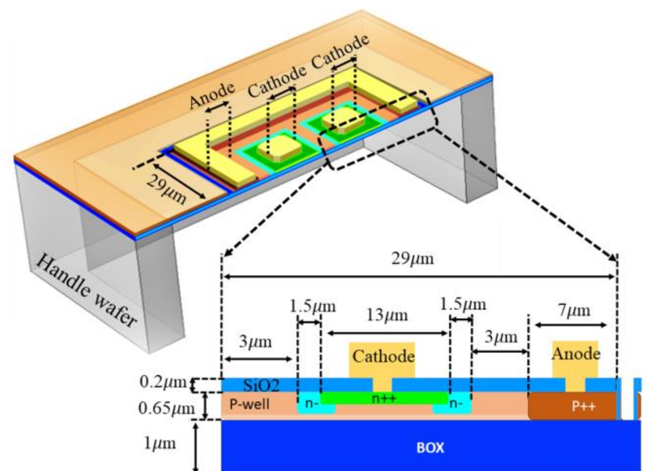

Fig. 1. 3D-schematic structure of the BSI SPAD based on SOI technology with a close-up view of cross section.

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The fill factor of the dual-SPAD device with the mentioned design parameters is 32.1%. In the fill factor calculation, the total active area per pixel involving guard ring under backside illumination is 16μm×16μm. The guard ring is included, since this SPAD is under backside illumination, and our simulations show significant avalanche probability values in the guard ring (see Fig.3). The value of photon detection efficiency (PDE), here, is still limited by the low fill factor parameter. This is due to the considered design limitations induced by the need to keep sufficient safety margins for the fabrication process (e.g. lithography resolution, minimum contact holes size, misalignment, and etching process) in our university cleanroom.

A remarkable improvement in fill factor, up to more than 64% can be realized by modifying the design parameters considering a smaller node technology and decreasing the distance between guard ring and anode, as well as reducing the anode width, down to 1μm. In this first attempt, we focus on realizing a BSI SPAD based on an ultrathin silicon layer of 650nm for enhancing the detection efficiency in UV spectrum instead of maximizing fill factor.

Wafer-level fabrication process is initially performed on a SOI wafer with n-type 700nm-thick silicon layer on a 1000nm-BOX. The final SPAD thickness of 650nm is achieved after successive four cycles of ~27nm top-Si thermal oxidation, four steps of ion implantation with different parameters and dopants, and subsequent SiO_2 etching, to build up the Si-based SPAD.

Fig. 2 (a) shows a cross section of the designed SPAD consisting of the final doping profile simulated in SILVACO (Athena). The parameters of boron-ion implantation for forming the p-well are defined by a dose of 4×10^{13}cm^{-2} and energy (E) of 20keV, while for the p^{++} region (anode), the dose is increased to 5×10^{15}cm^{-2}. The two ion implantation steps of arsenic for forming n^-/GR and n^{++} regions are performed at a dose of 1.3×10^{13}cm^{-2} (E=60keV) and a dose of 5×10^{15}cm^{-2} (E=20keV), respectively. Arsenic dopants take advantage of lower segregation and pile-up problems compared to Boron dopants to avoid degrading the Si/oxide interface. A further improvement of the quality of that interface is obtained by removing the SiO_2 layer that was used for arsenic implantation and re-growing a CMOS-grade dry thermal SiO_2 layer with subsequent thermal annealing under nitrogen and oxygen. The gradient profile for the p-well is formed through the dopant diffusion during the three steps of thermal SiO_2 growth at 950ºC in the rest of the fabrication process [18]. This modified doping profile provides a high built-in electric field of ~8.8×10^5V/cm at breakdown voltage to initiate a high impact ionization rate in Geiger mode. A guard ring (GR) is formed by introducing n-well with a space-charge region depth of ~200nm and a total width of 3μm, while a width of 1.5μm in n-well is overlapping with n^{++} region to prevent the premature edge breakdown.

The simulated dark I-V curve shows a breakdown voltage of 8.5V at room temperature (Fig.2 (b)). Several mechanisms of Auger recombination, Shockley-Read-Hall (SRH) generation/recombination, trap-assisted generation, and band-to-band tunneling are considered in the simulated model. An activation energy of 0.55 eV was obtained when simulating the temperature dependence of the dark current at 4V and the slope of the Arrhenius plot from room temperature to 60ºC.

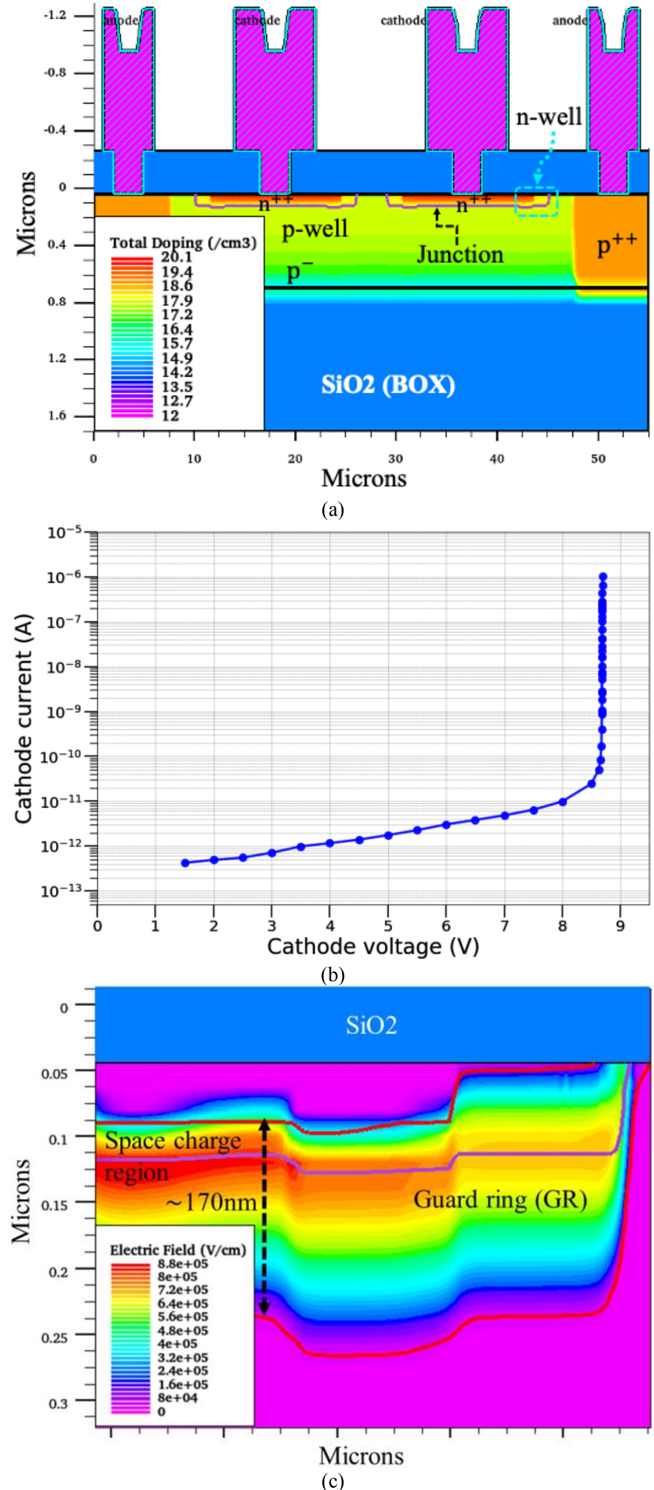

Fig. 2. (a) Two-dimensional (2D) simulated structure of the BSI SPAD, (b) simulated dark I-V curve at room temperature, and (c) simulated electric field at breakdown voltage of 8.5V with a junction depth of ~75nm (violet line) and a space charge region depth of ~170nm (red line).

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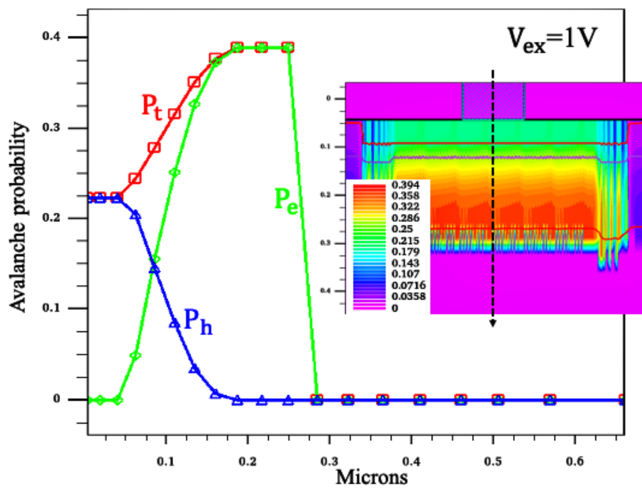

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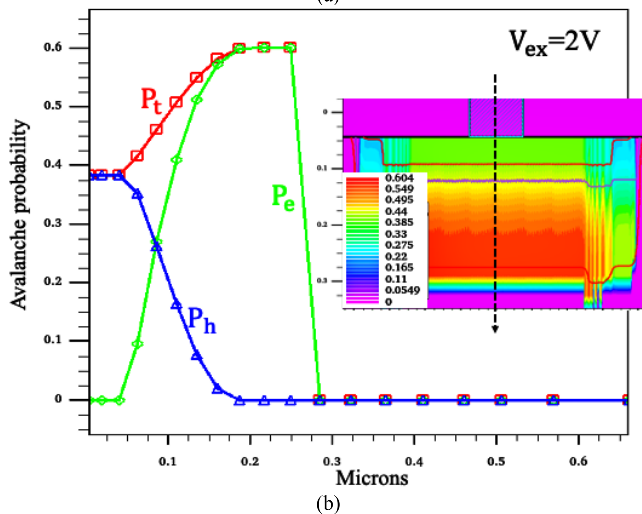

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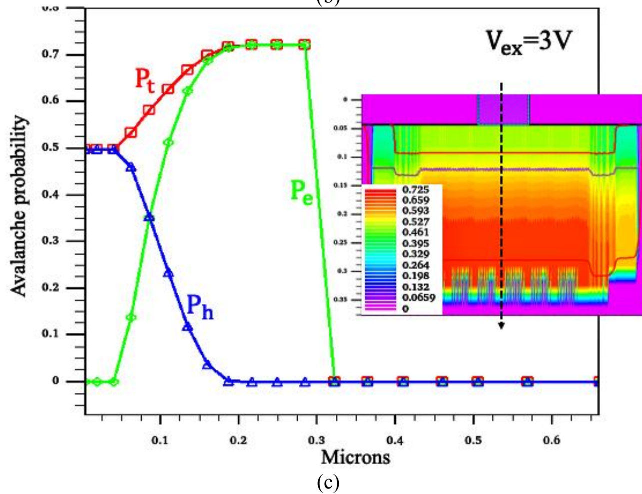

(c)

Fig. 3. Simulated electron (P_e), hole (P_h), and total (P_t) avalanche probabilities across the BSI SPAD depth at the excess bias voltages of (a) 1V, (b) 2V, and (c) 3V in Geiger mode. The 2D-distribution of the total avalanche probabilities in the space charge region are shown in the inset.

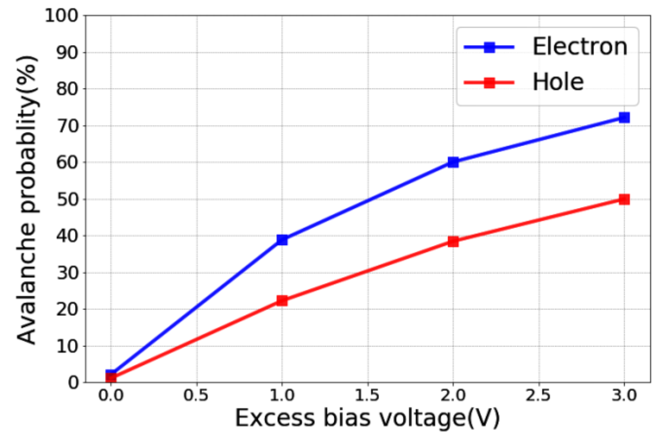

Fig. 4. The maximum avalanche probabilities of electron and hole in the space charge region as a function of excess bias voltage.

This value of activation energy shows a higher contribution of trap-assisted generation than of thermal processes.

Fig.2 (c) depicts the electric field profile at the breakdown voltage of 8.5V at room temperature (RT). The n^{++}/p-well junction depth from top side and the depth of depleted space-charge region (at breakdown voltage) are ~75nm and ~170nm, respectively.

Fig. 3 represents the simulated avalanche probabilities for electrons, holes, and total electron-hole pairs across the depth at 1V, 2V, and 3V excess bias voltages (i.e. V_{ex} over 8.5 V) at RT. The maximum avalanche probability of electron occurs at the edge of p-side space charge region that plays a major role in the calculation of PDP for the proposed BSI SPAD. The maximum simulated avalanche probabilities for electrons and holes in space charge region as a function of excess bias voltage is plotted in Fig. 4.

III. Experiments and Discussion

A. Fabrication

Fig. 5 shows the microscopy images of the fabricated two neighbor BSI SPADs based on a shared p-well as depicted in Fig. 1. After performing the four steps of doping and thermal oxidation of the top Si layer as explained in the last section, the subsequent process is finalized as follows:

- A silicon dry etching process is performed from frontside down to the BOX to realize a trench around the two neighbor SPADs.
- 200nm-SiO_2 plasma enhanced chemical vapor deposition (PECVD) is used as an intermediate layer for contact holes definition by SiO_2-etching.
- Annealing is carried out under oxygen at 700ºC to minimize the surface recombination rate at the interface of Si-SiO_2.
- Al (with 1% Si) is sputtered and patterned for the contacts and metal interconnects.
- The frontside process is finalized by the deposition of 300nm-SiO_2 (PECVD) for the passivation and then, annealing under forming gas at 432ºC during 30min for silicidation in the interface of Al(1%Si) and Si layer. A frontside micrograph of the fabricated SPADs is illustrated in Fig. 5(a).

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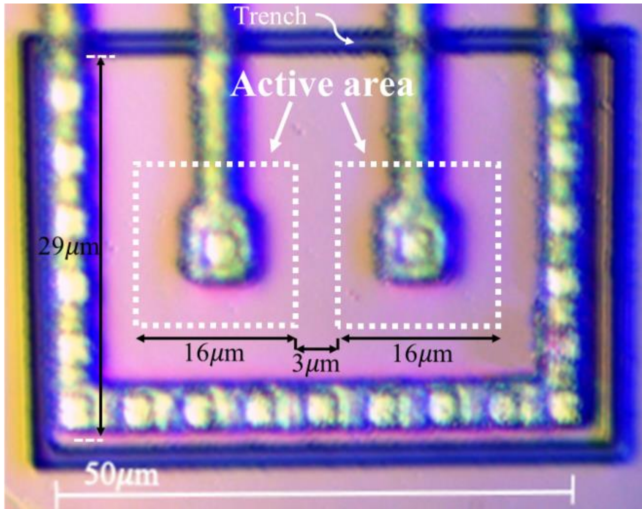

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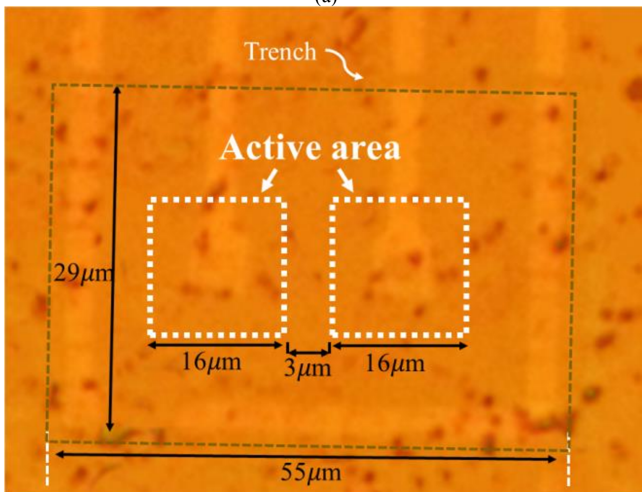

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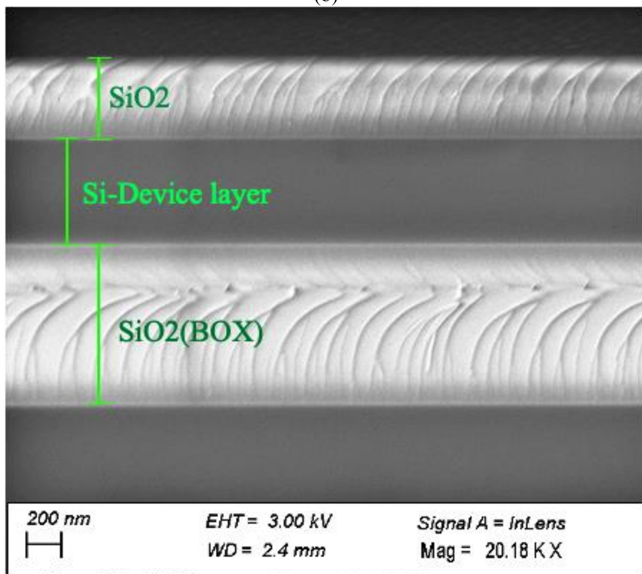

(c)

Fig. 5. The microscope images of BSI SPAD based on SOI technology involving (a) a micrograph of frontside and (b) a micrograph of backside together with (c) a SEM image of cross section.

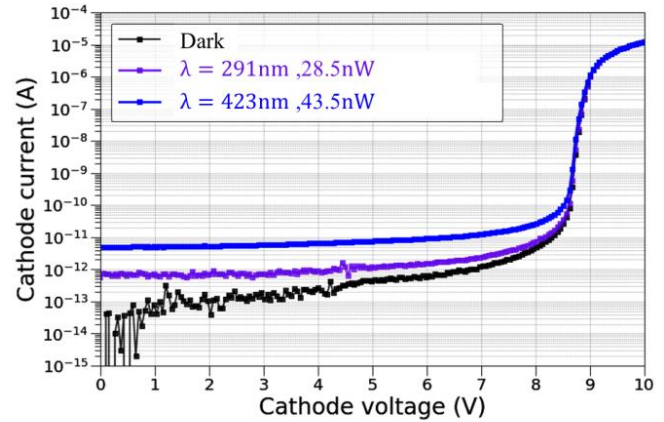

Fig. 6. Current-voltage (I-V) measurement in the dark and under low light power at the wavelengths of 291nm and 423nm at room temperature.

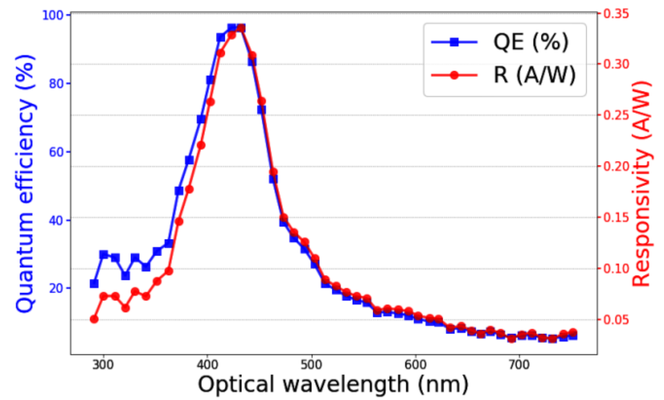

Fig. 7. Quantum efficiency (QE) and responsivity of (R) of the BSI in the spectral range from 291 to 751nm at 4V reverse bias upon room temperature.

The backside process is performed on the handle silicon wafer for realizing the membrane as follows:

- A thinning of the handle silicon layer down to ~248µm is carried out using a grinding process.
- The membrane is patterned using backside photoalignment of an aluminum hard mask, followed by a XeF_2 gas etching of the remaining silicon substrate towards the BOX.

Fig.5(b) shows a backside micrograph of BSI SPADs. A scanning electron microscope (SEM) image of cross section view of the implemented layers is also shown in Fig.5(c).

B. *Measurements*

The measurements are individually performed on each SPAD. The measured current-voltage (I-V) curves in the dark and under back side illumination with a low light power of 28.5nW at a wavelength of 291nm and a light power of 43.5nW at a wavelength of 423nm are presented in Fig. 6. The measured dark I-V curve compared to the simulated ones fairly match. According to the I-V curves, the BSI SPAD achieves a low dark current on the order of 0.1pA where gain is equal one (M=1) under static conditions and a remarkable low breakdown voltage of 8.5V at room temperature.

Fig. 7 shows the measurement of the quantum efficiency (QE) and the responsivity of the SPAD under backside

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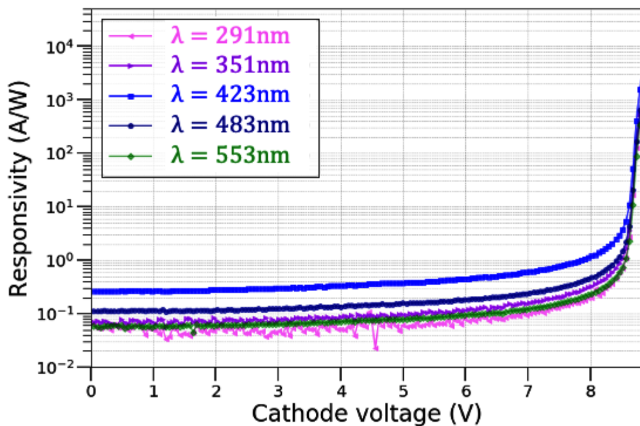

Fig. 8. Photoresponsivity as a function of reverse bias in the spectral range from 291nm to 553nm.

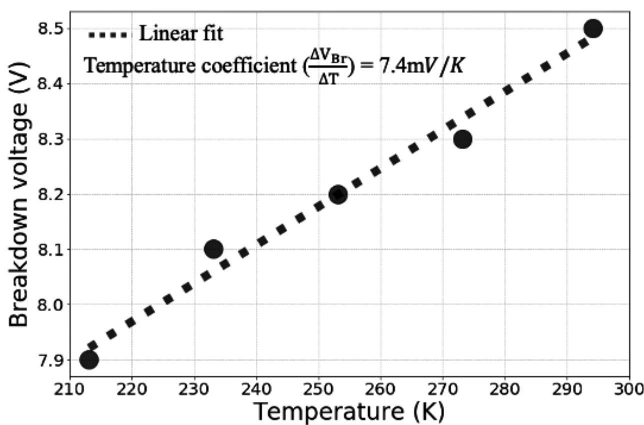

Fig.9. Breakdown voltage versus temperature with a temperature coefficient of 7.4mV/K.

illumination in the wavelength range from 291nm to 751nm, below breakdown voltage, i.e. at 4V, where the gain value is equal to one (M=1).

In this ultrathin BSI SPAD, a maximum QE of 96.41%, corresponding to a photoresponsivity of 0.3 A/W, is achieved at a wavelength of 423nm.

This BSI SPAD enables an outstanding enhancement of UV sensitivity in the shorter wavelengths by achieving a quantum efficiency of 21.6%, corresponding to a responsivity of 0.05A/W, at a wavelength of 291nm.

In comparison to the reported QE and responsivity under frontside illumination in [18], the sensitivity in deep UV-C under backside illumination is degraded. This is due to the influence of thicker SiO_2 (BOX~1000nm) in the illuminated side and the absorption of deep UV-C photons through a distance lower than ~5nm (for the wavelengths below 300nm) inside the diffusion region from backside, which is far from the edge of drift region. For the same reason, the maximum QE and responsivity at the wavelength of 420nm under backside illumination (using monochromator) are comparable to the peak QE and responsivity at the wavelength of 400nm under frontside illumination (using normal LED), corresponding to a similar absorption in the space charge region. Under backside illumination, the responsivities at the longer wavelength up to 751nm are smaller than the values obtained under frontside illumination. The higher detection efficiency under frontside illumination for longer wavelength is obtained due to the formation of the thin silicon body of the SPAD between SiO2 on top and thick buried SiO_2 (BOX) over the handle silicon substrate on the bottom that can act as a reflector [18]. However, under backside illumination, the detection efficiency for longer wavelength regime towards 751nm suffers from the low light absorption in the thin silicon body of SPAD alone.

It is still possible to improve, partially, the detection efficiency within deep UV-C by implementing a modified thickness of SiO_2 (BOX) or utilizing other proper anti-reflection layers on the backside [20], as well as further thinning the Si layer or forming a wider space charge region close to the backside surface.

Fig. 8 shows the details for the responsivity of the BSI SPAD as a function of reverse voltage in the spectral range from 291nm to 553nm. The static reverse bias voltage is swept towards 8.8V above breakdown. The increase of responsivities close to breakdown voltage relates to the value of the gain (M~10 at 8.46V) in a linear avalanche mode. In Geiger mode after breakdown voltage, the increase of the responsivity corresponds to a gain value of ~5.3×10^3 at 8.8V.

The variation of breakdown voltage as a function of temperature is depicted in Fig. 9. The breakdown voltage is shifted towards lower value (7.9V) when decreasing the temperature (213.15K) as caused by the increase of ionization rate. Furthermore, the optical phonon scattering rate decreases when reducing the temperature, resulting in the requirements of lower energy and lower bias voltage to initiate avalanche phenomenon in Geiger mode [11]. The temperature dependency of the breakdown voltage is defined in terms of its temperature coefficient of 7.4mV/K.

In Geiger mode, the DCR measurement of the integrated SPAD is carried out using an external PC25 readout circuit and Agilent oscilloscope (1GHz-bandwidth, 4GSa/s) for pulse counting. In the PC25 printed circuit board from Amptek, a A225 charge sensitive amplifier and shaping amplifier, a A206 voltage amplifier and discriminator, and a 500kOhm quench resistor are connected to the cathode of the BSI SPAD. The BSI SPAD is also placed inside an electrostatic shielded dark chamber, which has a functionality to control the temperature down to -60ºC (213.15K). Fig. 10 displays typical sample measurements of dark pulse traces at an excess bias voltage of 1V during 1ms under the temperatures of 213.15K and 273.15K. These pulses consist of primary noise and correlated noise (i.e. afterpulsing and secondary noises). Slow passive quenching is noted in the proposed device. This requires further optimization of the readout circuit to overcome the by-pass capacitance limitations.

We next analyze the physical origins of the DRC using the relative trends, with excess voltage and temperature, of the rough count rates estimated by counting on the oscilloscope.

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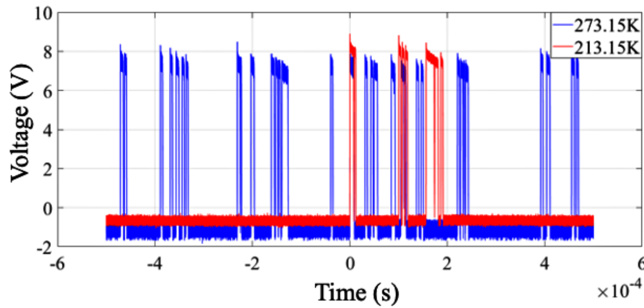
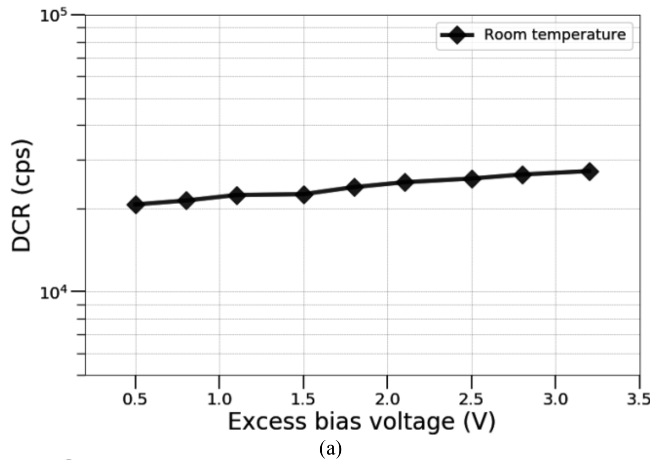


Fig. 10. Total Dark pulse counting under the temperatures of 213.15K and 273.15K at an excess bias voltage of 1V.



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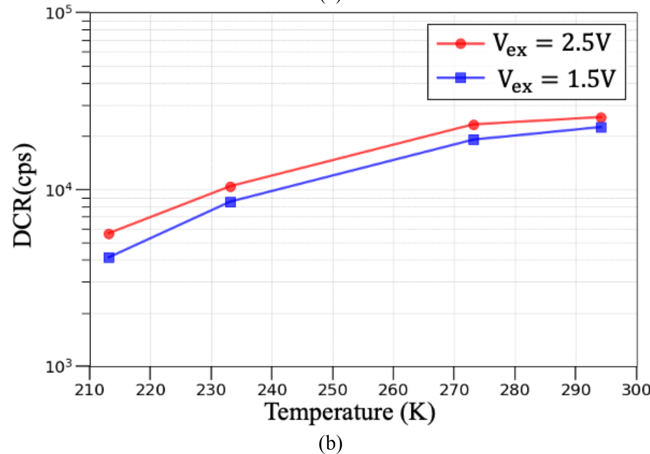

(b)

Fig.11. (a) DCR as a function of excess bias voltage at room temperature, (b) DCR as a function of temperature at the excess bias voltages of 1.5V and 2.5V.

In Geiger mode, the DCR records a triggered avalanche process initiated by the contribution of (i) intrinsic thermal generation of carriers, (ii) Shockley-Read-Hall (SRH) generation or trap-assisted generation of minority carriers in the space charge region, or (iii) band-to-band tunneling [14, 21,22].

The DCR variation as a function of voltage and temperature is studied to obtain a deep insight on the dominant physical mechanisms involved in the DCR by extracting the activation energy values. In Fig. 11 (a), the DCR variation with the increase of excess

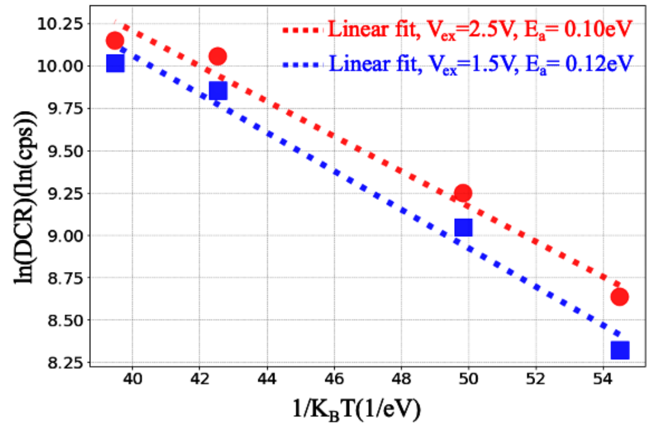

Fig. 12. Arrhenius plots of the DCR at the excess bias voltages of 1.5V and 2.5V.

bias voltage at room temperature shows a weak exponential dependency. This behavior can be related to a dominant contribution of trap-assisted process and lower band-to-band tunneling noise [21]. The DCR values at the excess bias voltages of 1.5V and 2.5V are 22.5kcps (133.1cps/μm^2) and 25.62kcps (151.6cps/μm^2) at room temperature, respectively.

On the contrary, Fig. 11 (b) shows a low dependency of DCR on the temperature variation and slightly higher dependency on excess bias voltages of 1.5V and 2.5V at the lower temperatures. In this trend, the contribution of band-to-band tunneling in the DCR starts to prevail at lower temperature [21, 22]. This phenomenon is also clarified with the low activation energies (E_a) of 0.12 and 0.10 eV for the respective excess bias voltages of 1.5V and 2.5V, extracted from Arrhenius plot in Fig. 12.

Furthermore, the activation energy is reduced at a higher excess bias voltage of 2.5V, since the contribution of band-to-band tunneling against the excess bias voltage under low temperatures is increased [21]. Although band-to-band tunneling becomes a main DCR source at lower temperature, the contribution of trap-assisted phenomena remains dominant at room temperature.

In Fig. 13, we have tried to separate the primary pulses from the afterpulsing, at 3V excess bias voltage under room temperature, using the 1ms time traces with ~6μs dead time defined by our external set-up by extracting and fitting the pulse widths. However, it suffers from the formation of wide digital pulses due to slow quenching and high by-pass capacitor in non-optimized readout circuit. The Gaussian fit in Fig.13 shows the DCR probability by counting the most probable pulses. The part of histogram with the wider width shows afterpulsing probability. The uncertainty compared to fitting is due to the set-up limitation.

Finally, the PDP in the BSI SPAD is extracted from the quantum efficiency multiplied by the avalanche probability. PDE can also be calculated by considering the fill factor (32.1%). Fig. 14 gives the PDP of the BSI SPAD in the spectral range from 291nm to 751nm. A peak PDP of 69.51% (equal to PDE of 22.13%) is achieved at a wavelength of 423nm for the

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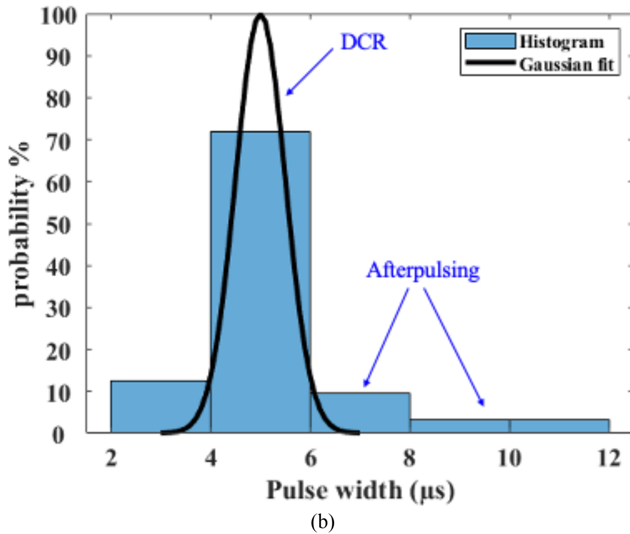

(b)

Fig.13. Histogram of pulse widths at 3V excess bias voltage under room temperature with ~6μs dead time.

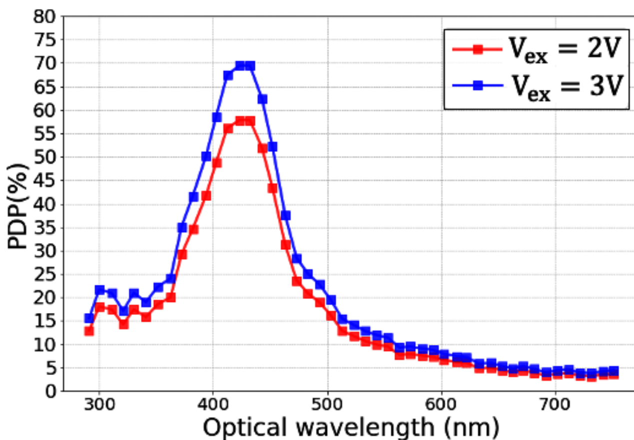

Fig. 14. PDP as a function of wavelength for the excess bias voltages of 2V and 3V at room temperature.

excess bias voltage of 3V.

This PDE can be improved to more than ~45% by exploiting standard CMOS technology and a smaller node SOI technology in order to increase the fill factor (beyond 64%, as discussed in Section II). This BSI SPAD still indicates a PDP of 15.56% at a wavelength of 291nm. Therefore, the ultrathin BSI SPAD achieves an outstanding expansion of UV-sensitivity down to UV-B among all other reported Si- based BSI SPADs.

For the longer wavelengths (>500nm) in visible (or even near infrared spectral range), since the absorption depth in silicon is higher than 1μm, which is beyond the 650nm-thin silicon body in the BSI SPAD, the sensitivity is degraded. The sensitivity in this spectral range could be partially improved by exploiting a metallic reflector on the frontside to increase the photons absorption in the thin silicon device layer.

C. Discussion

Table I describes a final performance comparison of the 650nm-thin BSI SPAD with the state-of-the-art. The SPAD of [11] with a 3μm-thick silicon body fabricated in 45nm CMOS technology presents a better PDP at a peak wavelength of 600nm due to the implementation of advanced CMOS technology, a wider space-charge region, and a high-quality thinning back side process. However, it suffers from a low sensitivity in the UV spectral range with a UV detection wavelength limited to 400nm. The performance impact of exploiting CMOS circuitry is presented in the 1.5μm-thin SPAD fabricated in SOI technology in [13]. In this approach, towards a flexible structure, a higher PDP value under UV wavelengths is achieved by integrating CMOS circuitry, even though this shows a higher breakdown voltage.

The higher peak PDP in the 1.5μm-thin SPADs of [15] (with a higher fill factor compared to the flexible SPADs) fabricated in 140nm SOI CMOS technology, is obtained in the shorter wavelength of 500nm. This BSI SPAD indicates a lower breakdown voltage (11.3V) with regards to the previous ones. The BSI SPADs in [14, 15] are characterized under the shortest wavelength of 400nm. The BSI SPAD with a 650nm-thin silicon body fabricated in SOI technology exhibits the lowest breakdown voltage of 8.5 V with an impressive peak PDP that is shifting down to 423nm and a minimum detectable wavelength of 291nm, without using an advanced CMOS technology and integrated CMOS circuitry. This low breakdown voltage is favorably required for low voltage systems and mobile devices. Besides, this device shows a low DCR at room temperature, thanks to the ultrathin silicon layer consisting of shallow junction, a gradient doping level in p-well in order to build up a high electric field at the junction close to the frontside surface and lower doping level towards the backside, and a CMOS-grade high-quality Si/oxide interface. Presently, the use of a non-optimized external read-out interface with high by-pass capacitor and passive quenching resistor introduces a deadtime limitation. Nevertheless, DCR and tunneling noise in shallow junction could also be higher than for a deeper junction.

Our BSI SPAD process and design appear compatible with most CMOS processes used for analog applications. In a future work, this could be completed with an integrated passive quench resistor, in an array to form a silicon photomultiplier (SiPM) for applications in the UV spectral range and under low light level (a few photons).

For the single photon detection and time-resolved applications, further improvement is required by integrating a dedicated CMOS interface circuitry and further time response measurements to evaluate timing jitter parameters under a suitable pulsed light source.

Here, as a first attempt, we focused on the feasibility of realizing a UV-enhanced BSI SPAD on a sub-micron (650nm) silicon layer and obtained the proof of increasing UV sensitivity under low light level in the presented thin structure.

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TABLE I
AN OVERVIEW ON THE PERFORMANCE COMPARISON WITH SILICON BASED BSI SPADS

	Technology Si-Thick.	pn junction GR structure	V_{Br} (V)	V_{Ex} (V)	DCR (cps/μm²) at RT[a]	Fill factor	PDP at peek wavelength	PDP at 423nm	PDP at Min. detectable wavelength
[11]	45nm CIS ~3μm	p⁺/deep n-well p-well GR[a]	28.5	2.5	55.4	60.5%	31.8% at 600nm	~5%	~3% at 400nm
[13]	Flex. SOI[b] 1.5μm	n⁺/p virtual-GR	17.2	1.5	3500 (Min.) 6300 (Max.)	n.a.	6% at ~560nm	~2%	~2% at ~423nm
[13]	Flex. SOI CMOS[c] 1.5μm	n⁺/p virtual-GR	26.5	1.5	4300	10%	12.5% at ~465nm	~11.2%	~11% at ~400nm
[14]	140nm SOI CMOS 1.5μm	p⁺/n-well p-well GR	11.3	3	240	~36%	25.4% at 490nm	~21%	~20% at 400nm
[15]	140nm SOI CMOS 1.5μm	p⁺/n-well p-well GR	11.3	3	396.1	n.a.	26.4% at 500nm	~21%	~17.5%> at 400nm>
This work	**SOI[d] 0.65μm**	**n⁺/p-well n-well GR**	**8.5**	**3**	**156.8**	**32.1%[e]**	**69.51% at 423nm**	**69.51%**	**15.56% at 291nm**

[a] RT: Room temperature, GR: Guard ring.
[b] The trench isolated SPAD based on SOI technology without implementing CMOS transistor fabrication process.
[c] Flexible CMOS SPAD.
[d] Without implementing standard CMOS technology and CMOS circuitry.
[e] Fill factor value for dual-SPAD device based on a shared p-well

IV. CONCLUSION

We demonstrated (to date) the world's thinnest (650nm) BSI SPAD consisting of n^{++}/p-well junction and a square-shaped active area of 16μm×16μm based on SOI technology with high CMOS compatibility, which enables the exploitation of 3D-stacking approach for integrating with CMOS circuitry. The figures of merit were studied under both static characterization and functional characterization in Geiger mode. Under static conditions, this SPAD demonstrates a low dark current (on the order of 0.1pA at M=1) and a low breakdown voltage of 8.5V at room temperature. In addition, a maximum quantum efficiency of 96.41% (corresponding to a responsivity of 0.3 A/W) is achieved at a wavelength of 423nm. Under functional characterization in Geiger mode, a low DCR of 156.8cps/μm² has been measured at an excess bias voltage of 3V at room temperature. A maximum PDP of 69.51% (PDE=22.31%) is achieved at the same excess bias by considering an avalanche probability of 72.1% for electrons and a fill factor of 32.1%. Besides, this BSI SPAD proves an outstanding UV-detection efficiency down to 291nm.

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