Control of sputtered VO_2 thin film grain size through O_2 concentration

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Vanadium dioxide (VO_2) thin films have the interesting property to undergo a transition from insulator to metallic state (IMT) around a temperature of ~68°C (Fig. 1a). When patterned into micro-scale two-terminal (2T) devices (Fig. 1b), this hysteretic transition can be triggered through Joule heating by applying a voltage V_{IMT} across the obtained VO_2 resistance (Fig. 1c). This enables the design of analog neuron units for neuromorphic applications, such as spiking neural networks. Even more recently, VO_2 peculiar physical properties have been exploited to demonstrate stochastic neurons [1], as well as neurons sensitive to RF and visible radiations [2].

In order to limit the power consumption of such devices, threshold voltage reduction is achieved through downscaling of the VO_2 channel length down to a few hundreds of nanometers. Since this scale becomes comparable with the grain size of the polycrystalline VO_2 films, individual grain dynamics come into play, inducing cycle-to-cycle variations in the device resistance and threshold voltage V_{IMT} [3]. Controlling grain size could thus allow to control device stochasticity depending on the application requirement: e.g., small grains for minimized stochasticity in sensory neurons; larger grains of tunable size to produce the desired level of stochasticity in stochastic neurons. This principle has however still to be demonstrated experimentally.

In this objective, this work demonstrates two different process routes to tune the grain size of VO_2 thin films, and investigates their respective impacts on the electrical properties of these films. The samples were prepared on SiO_2/Si substrates by room temperature DC reactive sputtering from a metallic Vanadium target using an Ar/O_2 plasma, followed by subsequent annealing in an Ar atmosphere. Both oxygen concentration during sputtering step ($[O_2]$) and annealing temperature (T_{anneal}) were varied, with process parameters for these parametric studies detailed in Table 1. The stoichiometry of the films was determined using RAMAN spectroscopy, revealing a large O_2 range (from 9 % to 15 %) yielding the VO_2 phase. Regarding annealing conditions, a minimal temperature of 400 °C was necessary to trigger crystallization.

Annealing temperature and O_2 concentration both show to be effective parameters to tune grain size, from respectively 30 to 90 nm for T_{anneal} ranging from 400°C to 600°C, and 20 to 50 nm for $[O_2]$ ranging from 9% to 15% (Fig. 2). While the first phenomenon is known and explained by the increase of surface diffusion rate with temperature, the second result is rather new, possibly explained by the reduced probability of particles chemisorption due to sub-stoichiometry of the films with lower oxygen content. This phenomenon is accompanied by an increase in oxygen vacancies, deduced from their effects measured on the temperature-resistivity hysteresis (Fig. 3a). Indeed, oxygen vacancies act as unintentional carriers hence reducing film resistivity; they also behave as nucleation centers for the insulator-to-metal transition, thus lowering the transition temperature. Annealing temperature also allows to tune these parameters (Fig. 3b), but to a lesser extent: the effect seems to saturate above 500°C. By optimizing the O_2 content, we reached a high resistivity ratio with order of magnitude comparable with the highest literature values for SiO_2/Si substrates [4][5] (Table 2). Interestingly, we discovered that O_2 content can also be used as a mean to tune the thin film residual stress, as it introduces compressive stress compensating the tensile stress resulting from thermal mismatch (Fig. 4).

In conclusion, we propose oxygen concentration during the sputtering step as a new way to control grain size in VO_2 thin films on CMOS compatible substrates, accompanied by wide tuning possibilities of the temperature-resistivity hysteresis profile as well as residual stress. We make the hypothesis that these effects are attributed to the presence of oxygen vacancies. Ongoing work includes two types of characterization on 2T devices with different O_2 content (hence grain size and oxygen vacancies): (1) cycle-to-cycle variability study the impact of grain size on stochasticity; (2) endurance tests to determine the maximum number of thermal/electrical cycles the devices can undergo before failure. Indeed, oxygen vacancies have recently been associated with permanent transition to metallic state (hence electrical failure) [6], and their impact should thus be investigated to get a full picture of the possible trade-offs between device stochasticity, endurance, and electrical/thermal transition properties.

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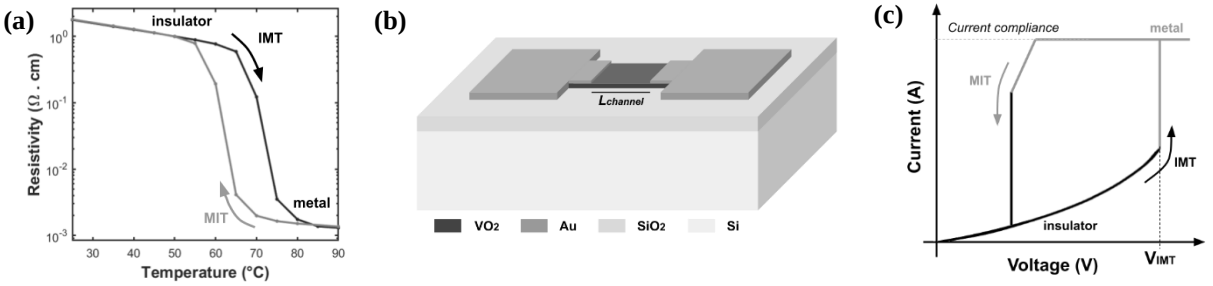


Figure 1. (a) Measured temperature-resistivity hysteresis of our base case VO_2 thin film **(b)** Typical 2T device with micro-scale VO_2 channel (not to scale). **(c)** Typical cycle of a two-terminal device I-V hysteresis. Current compliance is commonly set to protect device from overheating at high current.

Base case

	Substrate	SiO_2 200 nm (thermally grown) / Si
Sputtering	**Pressure**	5 mTorr
	Power	200 W
	Atmosphere	O_2 12.5 %, Ar 87.5 % Total gas flow 50 sccm
	Temperature	Room temperature
	Film thickness	160 nm
Anneal	**Duration**	30 min ramp + 60 min
	Pressure	0.2 mbar
	Temperature	500 °C

Parametric study

[O2]	7%, 9%, 12.5%, 15%, 16%
T_{anneal}	300°C, 400°C, 500°C, 600°C

Table 1. Process parameters for the reference case, and parametric study

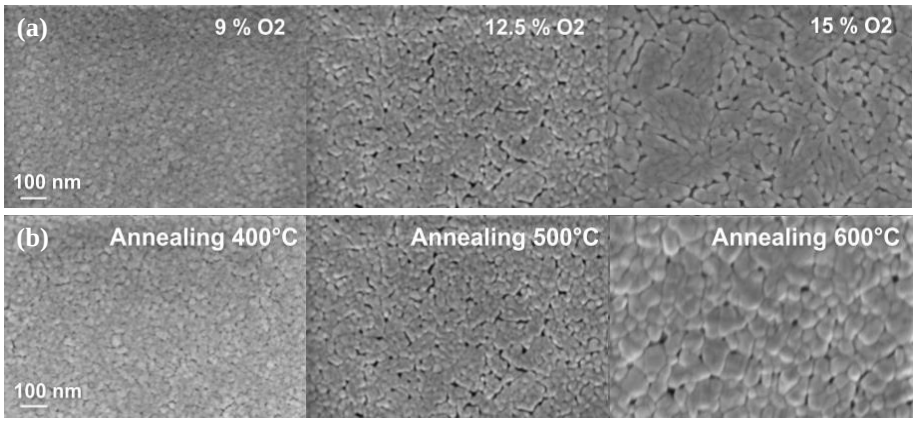
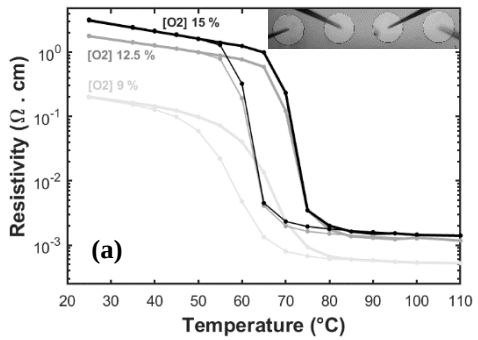


Figure 2. SEM measurements showing grain size evolution with **(a)** Oxygen concentration $[O_2]$ and **(b)** Annealing temperature T_{anneal}



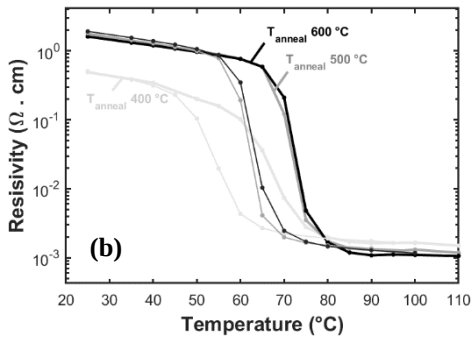


Figure 3. Temperature-resistivity profile evolution with **(a)** O_2 concentration and **(b)** annealing temperature. Resistivity has been extracted by < 100 µA current 4-point probe measurement after Ni/Au contacts evaporation (see inset)

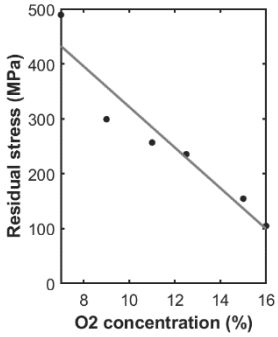


Figure 4. Variation of film residual stress with $[O_2]$

		Sputtering step					*Annealing step*					*Film characterization*			
Reference	**Resistivity ratio**	**Deposition technique**	**Target**	**Deposition pressure**	**Atmosphere**	**Tempe-rature**	**Annea-ling ?**	**Tempe-rature**	**Dura-tion**	**Annealing pressure**	**Atmo-sphere**	**Contact**	**Measurement type**	**Grain size**	**Thick-ness**
This work	2300	**DC sputtering**	V	5 mTorr	O_2 15%, Ar 75%	R.T.	Yes	500 °C	1h	0.2 mbar	Ar 30 sccm	Ni, Au	4 point probe	50 nm	150 nm
Lin 2017 [4]	3700	**Sputtering**	/	/	/	500 - 600 °C	/	/	/	/	/	Ti, Au	/	/	200 nm
Jung 2016 [5]	5700	**RF sputtering**	VO2	6 mTorr	Ar	500 °C	Yes	500 °C	40 min	6 mTorr	O_2 1 sccm	/	4 point probe	298 nm	110 nm

Table 2. Comparison of best state of the art resistivity ratio of VO_2 films sputtered on SiO_2/Si substrates