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SUBSTRATE-RELATED RF PERFORMANCE OF TRAP-RICH HIGH-RESISTIVITY SOI WAFERS

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*To my parents,
and to my wife*

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ABSTRACT

High-Resistivity (HR) Silicon-on-Insulator (SOI) technology is currently addressing mobile challenges allowing heterogeneous integration on a single chip for RF, mixed-signal and SoC applications. HR-SOI substrate decreases RF losses and substrate coupling enabling the integration of high performance passive on-chip components. Nevertheless, it is known that a highly conductive inversion/accumulation layer beneath the BOX degrades the high resistivity properties of the handle wafer, thus increases RF losses, non-linearity behaviour and coupling through the substrate. Engineered trap-rich HR-SOI substrate is well placed to recover the high resistivity properties of the handle wafer enhancing its RF performance in terms of linearity, reduction of losses and coupling effects.

In this thesis, based on wideband electrical measurements the crosstalk of HR-Si substrate with and without a trap-rich layer has been modelled. It has been demonstrated that the quasi-lossless trap-rich (TR) HR-Si substrate can be described by a purely capacitive network. A photo-conductive CPW RF switch structure has been designed and characterized. Thanks to the trapping layer surrounding the active area of the optical RF switches a drastic reduction of the optical crosstalk effect due to the lateral photo-generation in HR-Si substrate is achieved. Static and RF performances of passive and active fully depleted SOI MOSFETs have been characterized on Smart-Cut HR-SOI and TR-SOI (commercially named as Enhanced Signal Integrity, eSI) wafers manufactured by Soitec, Bernin, France. Small- and large-signal measurements indicate a significant improvement in linearity, reduction of RF losses and crosstalk, as well as much larger Q factor for thick-metal spiral inductors on trap-rich substrate. It has been demonstrated that the introduction of trap-rich layer underneath the BOX does not alter the DC and RF performances of SOI CMOS transistors. Moreover, the digital substrate noise is reduced by more than 25 dB on TR-SOI wafer compared with HR-SOI. Temperature measurements of TR-SOI substrate have shown that intrinsic free carriers thermo-generated inside the HR Si substrate degrade its RF performance above 125 °C. The generation of traps in the Si substrate volume is required to keep a quasi-lossless Si-based substrate at higher temperature. Porous silicon demonstrated its efficiency over a wide temperature range, from 25 °C up to 175 °C. Based on all these experiments and simulations, trap-rich Si-based substrate concept paves the way for more integration of mixed signal, digital, analog and photonic devices on a single chip.

ACRONYMS

3G	Third Generation of mobile telephony
4G	Fourth Generation of mobile telephony
5G	Fifth Generation of mobile telephony
AC	Alternative current
BESOI	Bonded and Etched-Back Silicon-on-Insulator
BOX	Buried oxide
BPF	Band-pass Filter
BT	Body-Tied
CLK	Clock
CPW	Coplanar Waveguide
CMOS	Complementary metal-oxide semiconductor
CZ	Czoralchsky
DIBL	Drain-induced barrier lowering
DT	Dynamic Threshold
DSN	Digital Substrate Noise
DC	Direct current
DoS	Density of States
DTI	Deep Trench Isolation
DUT	Device Under Test
EDGE	Enhanced Data GSM Environment
ELO	Epitaxial Lateral Overgrowth
ELTRAN	Epitaxial Layer Transfer
FB	Floating-Body
FBE	Floating Body Effects
FD	Fully-Depleted
FD SOI	Fully Depleted Silicon-on-Insulator
FIPOS	Full Isolation by Porous Oxidized Silicon
FoM	Factor of Merit

FZ	Floating-zone
GeOI	Germanium-on-Insulator
GIDL	Gate Induced Drain Leakage
GPU	Graphics Processing Unit
GSG	Ground-Signal-Ground
GSM	Global System for Mobile Communications
HF	High Frequency
HR	High Resistivity
HR-Si	High Resistivity Silicon
HR-SOI	High Resistivity Silicon-on-Insulator
HV	High Voltage
IDC	International Data Corporation
IMD	Inter-Modulation Distortion
ITRS	International Technology Roadmap for Semiconductors
I/O	Input/Output
IC	Integrated Circuit
ISS	Impedance Standard Substrate
LL	Line-Line calibration technique
LOCOS	Local Oxidation of Silicon
LPCVD	Low-pressure Chemical Vapour Deposition
LPF	Low-pass Filter
LVLP	Low Voltage Low Power
LRM	Load-Reflection-Match calibration technique
LRRM	Load-Reflection-Reflection-Match calibration technique
LSNA	Large-Signal Network Analyzer
MCM	Multi-chip Module
MEMS	Micro-electromechanical systems
MIS	Metal-Insulator-Semiconductor
MHC	Mobile Heterogeneous Computing
MM	More Moore
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Microstrip
MtM	More than Moore

NVNA	Nonlinear Vector Network Analyzer
PD	Partially Depleted Silicon-on-Insulator
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PIC	Photon-Induced Current
POF	Plastic Optical Fiber
PSC	Parasitic Surface Conduction
RF	Radio Frequency
RFFE	Radio Frequency Front-End
RLCG	Equivalent lumped model of a transmission line
RP	Resistivity Profile
RTA	Rapid Thermal Annealing
SIMOX	Separation by Implantation of Oxygen
SiP	Systems-in-Package
SIPOS	Oxygen-doped polycrystalline silicon
SOA	Silicon-on-Anything
SoC	Systems-on-Chip
SOG	Silicon-on-Glass
SOI	Silicon-on-Insulator
SOLT	Short-Open-Load-Thru calibration technique
SON	Silicon-on-Nothing
SOQ	Silicon-on-Quartz
SOS	Silicon-on-Sapphire
STI	Shallow Trench Isolation
TA	Thermal Annealing
TC	Temperature Coefficient
TEM	Transverse Electromagnetic
THD	Total Harmonic Distortion
TMAH	Tetramethylammonium hydroxide
TRL	Tru-Reflection-Load calibration technique
ULP	Ultra-Low Power
UTB SOI	Ultrathin Body Silicon-on-Insulator
UTBB SOI	Ultrathin Body and BOX Silicon-on-Insulator
UWF	Ultra Wide Frequency
VLSI	Very Large Scale Integration

xxx Acronyms

VNA	Vector Network Analyzer
WiFi	Wireless Fidelity

LIST OF SYMBOLS

α	Attenuation constant	$[np/m]$
β	Phase constant	$[rad/m]$
C	Lineic Capacitance	$[F/m]$
C_{air}	Lineic capacitance of a coplanar waveguide surrounded by air	$[F/m]$
C_{CPW}	Lineic capacitance of a coplanar waveguide	$[F/m]$
C_{ox}	Oxide capacitance	$[F/m]$
C_m	Measured lineic capacitance	$[F/m]$
D	Electric displacement field	$[C/m^2]$
D_{vt}	Level of defects density	$[#/cm^3]$
ΔC	Absolute difference of the lineic capacitance of a coplanar waveguide to its mean value	$[F/m]$
ΔG	Absolute difference of the lineic conductance of a coplanar waveguide to its mean value	$[S/m]$
E	Electric field	$[V/m]$
E_g	Silicon band gap	$[ev]$
ε	Complex permittivity	$[F/m]$
ε_0	Vacuum permittivity	$[F/m]$
ε_r	Relative permittivity	$[F/m]$
ε'	Real part of the complex permittivity	$[F/m]$
ε''	Imaginary part of the complex permittivity	$[F/m]$
f_1	First cut-off frequency of crosstalk test structure on SOI	$[Hz]$
f_2	Second cut-off frequency of crosstalk test structure on SOI	$[Hz]$

f_b	Relaxation frequency of majority carriers (in inversion) [Hz]	
f_e	Dielectric relaxation frequency	[Hz]
f_m	Maximum oscillation frequency	[Hz]
f_s	Relaxation frequency of interfacial polarization (in accumulation)	[Hz]
f_t	cut-off frequency at the maximum current gain	[Hz]
G	Lineic Conductance	[S/m]
G_m	Measured lineic conductance	[S/m]
γ	Complex propagation constant	[—]
Γ	Reflection coefficient	[—]
H_2	Second Harmonic component	[dBm]
H_3	Third Harmonic component	[dBm]
I_{DD}	Supply current	[A]
J	Electric current density	[A/m ²]
L	Lineic Inductance	[H/m]
λC	Maximum excursion of the lineic capacitance of a coplanar waveguide with DC voltage	[F/m]
λG	Maximum excursion of the lineic conductance of a coplanar waveguide with DC voltage	[S/m]
MAG	Maximul available gain	
μ	Complex permeability	[H/m]
μ_0	Vacuum permeability	[H/m]
μ_n	Electron mobility	[cm ² /(V · s)]
μ_p	Hole mobility	[cm ² /(V · s)]
μ_r	Relative permeability	[H/m]
n	Electron concentration	[#/cm ³]
N_a	Acceptor concetration	[#/cm ³]
N_d	Donor concetration	[#/cm ³]
n_i	Intrinsic concentration	[#/cm ³]

$\nabla \cdot$	Divergence operator	$[/m]$
ω	Angular frequency	$[rad/s]$
p	Hole concentration	$[#/cm^3]$
ϕ_F	Fermi level	$[ev]$
ϕ_t	Thermal voltage	$[V]$
Ψ_{MS}	Metal-to-Semiconductor contact potential	$[V]$
Ψ_{ox}	Potential drop across the oxide	$[V]$
Ψ_S	Surface potential	$[V]$
q	Charge of an electron	$[C]$
Q_{ox}	Total charge in the oxide	$[C]$
Q_f	Density of interface fixed charges in the oxide	$[#/cm^2]$
Q_G	Charge at the gate electrode of the MOS capacitance	$[C]$
Q_S	Charge in the semiconductor under the oxide	$[C]$
R	Lineic Resistance	$[\Omega \cdot m]$
ρ	Electrical resistivity	$[\Omega \cdot m]$
ρ_{eff}	Effective resistivity	$[\Omega \cdot m]$
S	Scattering matrix	$[dB]$
S	Width of the slot between coplanar conductors of a coplanar waveguide	$[m]$
σ	Electrical conductivity	$[S/m]$
SS	Subthreshold slope	$[mV/V]$
t	Metal thickness	$[m]$
t_{inv}	Thickness of the (strong) inversion layer	$[m]$
t_{ox}	Oxide thickness	$[m]$
t_{weak}	Thickness limit of the weak inversion	$[m]$
t_p	Thickness of Psi layer	$[m]$
$\tan\delta$	Loss tangent	$[-]$
V_{DD}	Supply voltage	$[V]$
V_{FB}	Flat-band voltage	$[V]$

V_{th}	threshold voltage	[V]
V_b	Applied bias voltage	[V]
W	Width of the central conductor of a coplanar waveguide	[m]
W_f^m	Metal work function	[eV]
W_f^{Si}	Silicon work function	[eV]
W_g	Width of the coplanar ground conductor of a coplanar waveguide	[m]
W_W	Width of the trap-rich trench for substrate crosstalk reduction	[m]
Y	Admittance matrix	[S]
Z	Impedance matrix	[Ω]
Z_0	Characteristic impedance	[Ω]
Z_L	Impedance of transmission line	[Ω]

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CHAPTER 1

INTRODUCTION

Connected mobile devices are becoming a strategic imperative in order to remain attractive, improve efficiency and competitive for advanced electronic applications. The wireless revolution where Laptops, Smartphone's, tablets, TVs, vehicles and enterprises are connected in a cloud style environment makes possible communication anywhere at any time. Recent developments in wireless communications with the emergence of advanced radio-frequency standard such as LTE, LTE-A and 5 G have brought numerous challenges. The most critical challenge is to provide higher levels of integration with more power efficiency and cost-effective solutions on the same-chip. In parallel to the development of nanometer CMOS as well as beyond-CMOS device technologies for switching, memory and analog functions, the increasing need to integrate various (heterogeneous) technologies (e.g. RF communication, power control, passive components, sensors, actuators) helps to migrate from the system board-level into the system-in- package (SiP) or to the system-on- chip (SoC). In fact, mobile System-on-Chip (SoC) with heterogeneous integration of multiple technologies has truly revolutionized the semiconductor industry [1]. This trend relies on the integration of “More Moore” (MM) devices (mainly silicon technology scaling) with “More than Moore” (MtM) elements that add new functionalities (non-CMOS) that do not typically scale or behave according to “Moore’s Law” [2, 3] as can be depicted in Fig. 1.1.

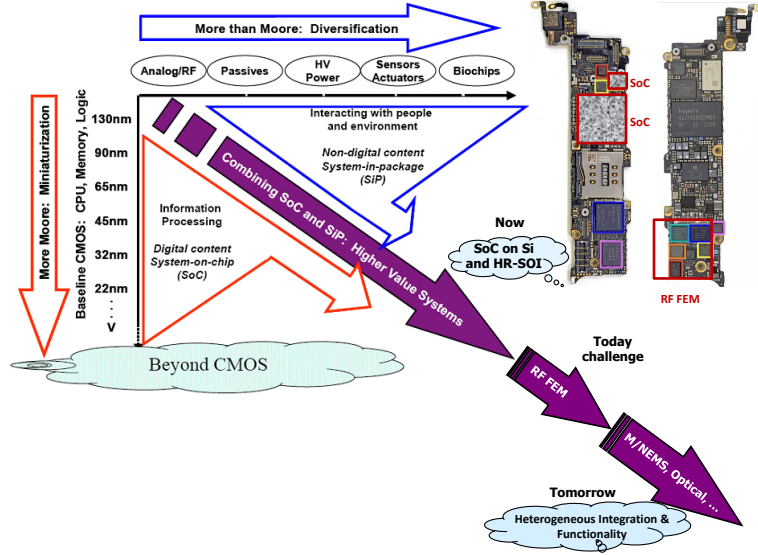


Fig. 1.1: Combined need of miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”) [3, 4].

1.1 SUBSTRATE TECHNOLOGIES FOR RF APPLICATIONS

In microelectronics, photonics, opto-electronics, high frequency or high power device applications, selecting the right semiconductor substrate technology can provide a strategic advantage by achieving higher applications performance. Materials such as gallium arsenide (GaAs), alumina, SOS have traditionally been the substrate of choice for microwave and (radio-frequency) RF applications. However, the large scale of commercial RF applications, such as cellular communication require substrates that are low loss, low cost, easy to manufacture and capable of being integrated with digital, and RF MEMS technologies. As CMOS technology continues to scale down allowing operation cut-off frequency f_t close to 500 GHz for n-MOSFETs [5], it provides the opportunity to integrate RF System-on-chip applications (SoC) [6] that contain digital, analog and RF functions on the same chip. Although silicon is a very mature technology, low-resistivity silicon substrate has not been used as microwave substrate because its extremely high dielectric loss which limit the integration of high quality passive components. The bulk Si solution implementation requires complex processing like triple wells and deep isolation trenches.

1.1.1 SOI technology

Silicon-on-insulator (SOI) technology has been developed in the 1960-1970s. It provides complete oxide isolation from the handle silicon substrate offering high speed, reduction of leakage currents and power consumption [7]. There are several methods for fabrication of SOI wafers. Oxygen implantation into silicon (SIMOX) [8, 9] or bond/etch back (BESOI) [10, 11] have gained early acceptance in the market. Epitaxy layer transfer (ELTRAN) [12], and single layer transfer are the two most critical processes for substrate engineering that allow the tailoring of the composite substrate to the application. Unibond Smart-CutTM process is the dominant method for thin layer transfer and SOI fabrication [13]. This technique starts with an thermal oxidized Si bulk substrate (donor substrate). Then a splitting region within the donor substrate (oxidized Si bulk substrate) by ion implantation (e.g. H^+ or He^+) is defined. The latter allows for transferring a thin film to the handle wafer by means of bonding followed by splitting. Unibond Smart-Cut process can be used to create a thin layer of any semiconductor material on top of an insulator.

The first SOI substrate was the Silicon-on-Sapphire (SOS) which used the alumina (Al_2O_3) as an insulator [14]. SOS substrates are well suited for RF applications and co-integration of digital and RF functions to produce highly programmable system [15].

1.1.2 HR-SOI advantages for RF applications

The integration of high quality passive components in standard bulk silicon technology is not obvious. It is well known that passive components integrated in standard silicon technologies suffer from high substrate losses. Both active devices and passive components RF performance are affected by the losses in the conductive silicon substrate, particularly at high frequencies. The degree of those losses depends on the resistivity of the silicon and on the thickness of the dielectric isolation. Increasing the resistivity will reduce the substrate losses and parasitic coupling, thus increase the quality factor of the integrated passive components. Since SOI technology is fully compatible with high resistivity (HR) substrate without inducing any impact on latch up or isolation, high performance passive components can be achieved on SOI. The presence of the buried oxide layer not only reduces the junction capacitance but also offers the opportunity of using high resistivity substrate to reduce substrate related RF losses and coupling.

Today, substrate resistivity values higher than $10 \text{ k}\Omega.cm$ can be achieved and it has been shown experimentally in [16] that dielectric losses associated with silicon substrates become negligible when its nominal resistivity is as high as $3 \text{ k}\Omega.cm$.

With the recent advance and decreasing cost of SOI substrates, SOI is becoming a mainstream technology for high performance RF switches. High performance

antenna switches have already been integrated on SOI [17, 18] and more than 65 % of substrates used in fabricating handset switches are SOI based [19]. The feasibility of SOI power amplifiers has also been reported very recently [20]. HR-SOI technology has recently come abroad to address the integration of multi-standard RF front end modules (FEM) on the same chip, since it offers the highest possible degree of integration and a cost effective approach [21].

1.2 SUMMARY OF PREVIOUS WORK AND CONTRIBUTIONS

Although, HR-SOI has demonstrated considerable reduction of substrate losses and crosstalk [22], it is known that HR-SOI handle wafer suffers from a parasitic surface conduction effect (PSC) [23]. The presence of fixed oxide charges at the SiO_2/Si interface creates an accumulation/inversion high conductive layer which degrades high resistivity properties of the handle wafer, increases its substrate losses and crosstalk. In his PhD thesis [24] D. Lederer evaluated the RF performances of oxidized high resistivity silicon substrate and developed a figure of merit (FoM) which account for wafer inhomogeneities. The proposed effective resistivity ρ_{eff} [25] parameter correspond to substrate resistivity sensed by a coplanar wave-guide structure. As previously mentioned, HR-SOI wafers are strongly affected by parasitic surface conduction (PSC) effect which drastically reduces their effective resistivity ρ_{eff} [25] at least one order of magnitude lower than the nominal wafer resistivity ($\approx 10 \text{ k}\Omega\cdot\text{cm}$) as seen in Fig. 1.2.

Several technological solutions have been proposed in the literature to overcome this issue [23, 26, 27]. HR-Si wafer passivated using a trap-rich layer underneath the oxide drastically reduces substrate RF losses allowing the handle wafer to recover its high resistivity properties as can be seen in Fig. 1.2.

In addition to the effective resistivity FoM to compare different Si-based substrate RF performance by means of their inhomogeneous conductivity properties, RF non-linear behaviour was addressed by C. Roda Neve in his PhD thesis [28]. Typically non-linearity behaviour is known to be generated from active devices. However, it has been demonstrated that the substrate itself introduces harmonic distortions which can be much higher than those of active devices or RF switches [29]. Large-signal measurement using passive components such as CPW lines or crosstalk structure on trap-rich passivation layer underneath the oxide layer proved that harmonics levels are significantly reduced below the wireless communication systems as depicted in Fig. 1.3.

1.3 SCOPE OF THIS WORK

As illustrated in Fig. 1.4 improving substrate RF performance allows to integrate diverse functions, such as high quality passive elements, active devices, optically controlled devices and RF MEMS structures on the same chip. The research objectives of this dissertation are to complement previous work and

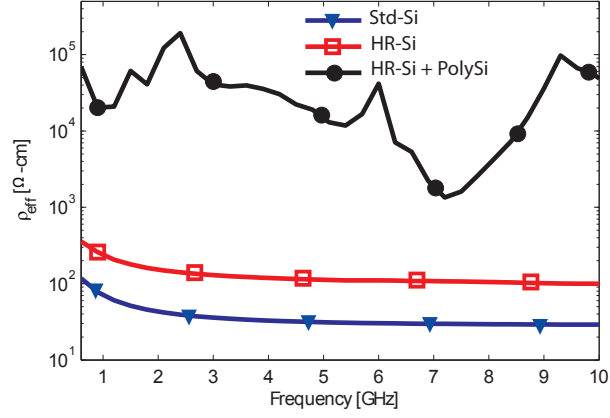


Fig. 1.2: Measured effective resistivity on Std-Si, HR-Si and HR-Si + PolySi ($t_{ox}=50$ nm (thermal oxide), $t_{PolySi}=287$ nm) [27].

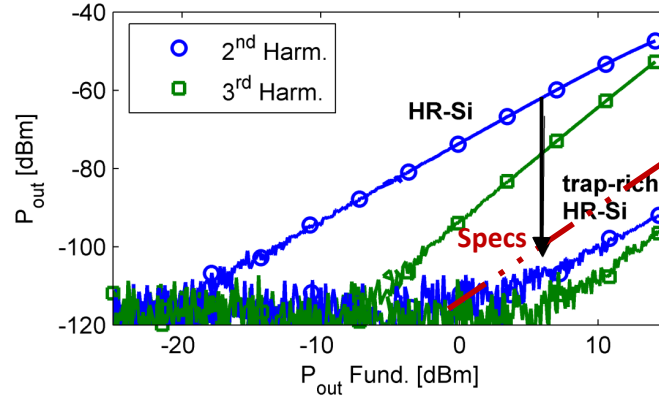


Fig. 1.3: Measured harmonic distortion components H2 and H3 of a 2146- μm -long CPW line on HR-Si ($\rho_{Si} > 5$ k $\Omega\cdot\text{cm}$) without and with trap-rich PolySi layer [29, 30].

investigate RF performance of the trap-rich HR-SOI (TR-SOI) technology and its suitability to co-integrate on-chip passive elements and active devices for RF front end blocks and system-on-chip applications. A detailed description of the used wafers list for each chapter is presented in Annexe A.

Chapter 2 will address the electrical substrate coupling effect and its reduction using a trap-rich passivation layer. The substrate resistivity profile was investigated using a simple MOS structure to analyze the PSC effect and how it was reduced using high density of traps at the SiO_2/Si interface. Based on physical simulations and ultra wideband electrical measurements of a crosstalk-test structure lying on oxidized HR-Si wafer with and without trap-rich passivation layer an equivalent circuit model was developed. The latter take into account the parasitic surface conduction effect that occurs at the substrate surface. It has been demonstrated that the quasi-lossless trap-rich (TR) HR-Si substrate can be described by a purely capacitive network.

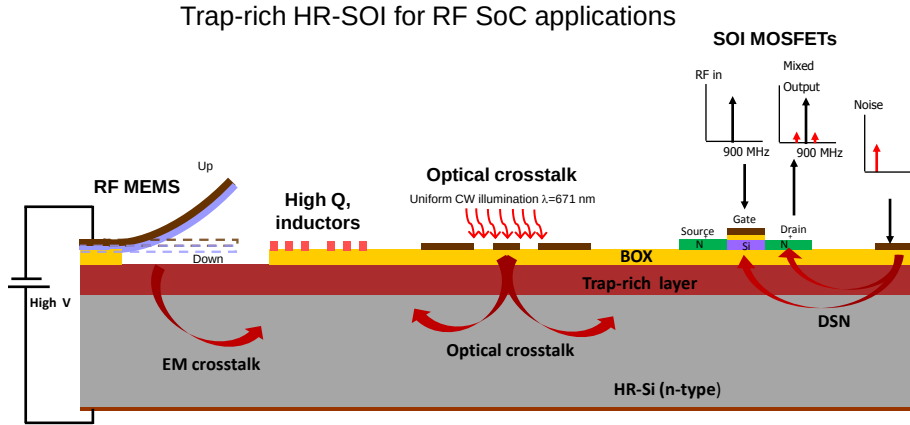


Fig. 1.4: RF System-on-Chip on TR-SOI.

In chapter 3, a photo-conductive CPW RF switch structure has been designed and characterized on oxidized HR-Si substrate with and without a trap-rich passivation layer. A well-controlled process was developed to locally etch the polysilicon window only from the restricted photoconductive area of the CPW photo-induced switch. Thanks to the trapping layer surrounding the active area of the optical RF switches a drastic reduction of the optical crosstalk effect due to the lateral photo-generation in HR-Si substrate is achieved.

While chapter 2 and 3 focus on electrical and optical crosstalk on trap-rich HR-Si substrate, chapter 4 deals with DC and RF performances of passive and active devices on commercial 200 mm HR-SOI and TR-SOI wafers (commercially named as Enhanced Signal Integrity, eSI) manufactured by Soitec, Bernin, France. Small- and large-signal measurements indicate a significant improvement in linearity, reduction of RF losses and crosstalk, as well as much larger Q factor for thick-metal spiral inductors on trap-rich HR-SOI substrate. It has been demonstrated that the introduction of trap-rich layer underneath the BOX does not alter the DC and RF performances of FD SOI CMOS transistors. Moreover, the digital substrate noise (DSN) was investigated on HR- and TR-SOI wafers. Digital switching noise was injected in the vicinity of SOI MOSFETs and the mixed output spectrum signal at the drain port quantify the coupled signal through the common substrate.

In chapter 5 the impact of temperature on trap-rich HR-SOI wafers was investigated by means of physical Atlas simulations, small- and large-signal measurements for a wide temperature range from -120°C up to 255°C . The trapping capabilities of trap-rich HR-Si and porous Si wafers are characterized using small- and large-signal measurements at high temperature and compared with their respective counterpart HR-Si and std-Si substrates, respectively.

RF MEMS tunable low-pass filter and patch antenna were designed and fabricated on top of HR-Si and trap-rich HR-Si substrates using a low complexity fabrication process (see Annexe B). Experimental and simulation results demonstrate that the important insertion loss for low-pass filter originates from the PSC occurring at the SiO_2/Si interface. The introduction of a trap-rich passivation layer at the SiO_2/Si interface is a promising solution to improve the quality of RF-MEMS integrated on Si substrate.

A general conclusion of this thesis is presented in chapter 6 and perspectives that highlight the efficiency of TR-SOI technology for co-integration of mixed signal, digital, analog and photonic devices on a single chip are discussed.

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CHAPTER 2

ULTRA-WIDE FREQUENCY RANGE CHARACTERIZATION AND MODELLING OF SUBSTRATE CROSSTALK ON TRAP-RICH HR-SI WAFERS

WITH ultrawideband (UWB) technology emerging in commercial applications, low power, high integration and low cost UWB ICs have attracted significant development resources. Silicon technology is the centrepiece on the semiconductor industry and has a large production scale. With the scaling of CMOS technologies and tremendous improvements in RF characteristics such as f_t and f_{max} of CMOS devices, there has been a huge trend to design RF CMOS devices and circuits in CMOS technology. Highly integrated CMOS transceiver is obviously a candidate for low-cost UWB products. Therefore, CMOS technology shows its capability for the co-integration of digital blocks with high-performance RF analog devices on the same silicon substrate for System-on-Chip (SoC) applications [1–3]. However, cost reduction and higher performances obtained from the development of a single chip solution have to face a significant undesired coupling effect and substrate losses that can degrade the performance of RF mixed-signal and complex SoC circuits. One of the main issues to make RF mixed signal integrated circuits is the much lower substrate resistivity in standard CMOS processing which limited the integration of high-quality passive elements, compared with semi-insulating GaAs. Moreover, integration of digital blocks generate a switching digital noise that can be easily injected into and propagate through the lossy silicon substrate, and thus degrades the performance of the sensitive analog and RF integrated circuits (ICs) or even causes failure of the system.

High performance SoC applications impose stringent requirement on the substrate characteristics. An ideal substrate should be good thermal conductor and provide good isolation for digital switching noise (preferably < -100 dB). Among the numerous wireless standards, ultra wideband (UWB) systems face many design and technological challenges since it operates at high frequencies and over a wide frequency band (3.1 to 10.6 GHz). Such systems are more sensitive to substrate noise which mostly originates from the synchronization clock (500 kHz, 3 MHz, 10 MHz, 100 MHz, etc.) and the high speed digital circuits. Switching noise of such digital circuits propagates through the substrate and affects the different parts of the wideband system such as low noise amplifier (LNA) [4], UWB RF filters [5] and voltage controlled oscillator (VCO) [6].

The effect of substrate parasitics on insertion loss (IL) of CMOS T/R switch was highlighted by Huang [7], and low IL designs were demonstrated at 900 MHz as well as at 2.4 GHz [8]. Among the many applications enabled by SoC building blocks are reconfigurable RF systems that benefit from co-integration of RF MEMS devices with CMOS integrated circuits. Although they offer high performance in a modular fashion, they still suffer from substrate coupling and crosstalk effect [9].

Digitally oriented bulk CMOS process typically rely on low resistivity substrate in order to minimize the latch-up considerations. The resulting conductive losses in monolithic inductors, transmission lines and other high-frequency circuits are usually considered to be excessive for RF applications, and so lightly doped silicon substrates are more typically used in both CMOS and BiCMOS approaches for RF SoC applications. High-resistivity silicon (HR-Si) has recently drawn increased attention for the integration of radio frequency (RF) [1, 2] and millimetre wave [3] integrated circuits on silicon substrates. In fact, the use of high resistivity silicon substrate has been proposed as an attractive material for co-integration of RF and mixed-mode signal systems [10]. It exhibits excellent RF properties with effective resistivity values of at least 3 k Ω .cm [11], and it is now widely available for industrial scale production. Other more exotic approaches improving substrate resistivity or isolation that have been proposed include the use of silicon-on-insulator (SOI) [12], silicon-on-sapphire (SOS) [13], silicon-on-anything (SOA) [14], porous silicon [15] and bulk micromachining [16]. HR-Si substrate is fully compatible with Silicon-on-Insulator (SOI) technologies, and high resistivity SOI (HR-SOI) wafer is nowadays presented as a mature and low cost technology for high-performance mixed-mode integrated systems. However, the main challenge in using HR-SOI, or as soon as an oxide layer is deposited or grown on top of a HR-Si substrate, is to conserve the high-resistivity characteristics of the substrate. Indeed, the fixed oxide charges (Q_{ox}) at the SiO_2/Si interface attract free mobile carriers at the top surface of the Si creating a highly conductive layer underneath the oxide, which degrades the effective resistivity of the substrate. The reduction of the substrate effective resistivity will translate to an increase of the coplanar wave-guide (CPW) transmission line RF losses and an increase of the parasitic coupling (crosstalk) between devices and integrated circuits lying on the same Si substrate [17]. Fortunately, such parasitic surface

conduction (PSC) effect can be effectively overcome by introducing a high density of traps near the insulating oxide. The traps capture the free carriers, thereby enabling the substrate to recover its nominal resistivity value and stabilizing the whole wafer surface. Several techniques can be used to introduce a trap-rich layer at the SiO_2/Si interface, such as ion implantation [18], and the deposition of a layer of amorphous silicon (α -Si) [19] or polycrystalline silicon (PolySi) [20] between the HR-Si handle substrate and the oxide layer. A comparison between the different passivation techniques is given by Chao-Jung et al. in [21]. To assess the substrate losses and coupling mechanisms, and how technological solutions can improve the performance of RF, mixed-mode applications and SoC, an accurate model of the substrate coupling, or crosstalk, mechanism becomes fundamental. Such model must be based on physical understanding of current flow paths in the silicon substrate. It should also cover the widest possible frequency range in order to provide a useful tool for the diversity of applications that can be found in current and future SoCs, from analog to digital, including MEMS and optoelectronic devices. Although the crosstalk dependence on substrate resistivity and separation between devices was presented by Raskin et al. in [22], neither the crosstalk behaviour below 100 MHz nor the impact of PSC and its reduction by the introduction of trap-rich layer were studied.

In this chapter, we investigate over a wide frequency range, from 100 kHz to tens of GHz, the substrate crosstalk in Si-based substrates, with focus on HR-Si substrates, showing the PSC effect and its reduction using a trap-rich layer. To that purpose we use finite-element numerical 2D-simulations from Atlas SILVACO and measurements done on crosstalk test structures fabricated on different Si substrates. The dependence of crosstalk on the Si resistivity, and on the distance separating the noisy aggressor and the victim are then investigated. Simulations and measurements to assess the impact of PSC on substrate crosstalk, and its reduction using a high trap-rich polysilicon (PolySi) layer are presented after. An equivalent lumped element electrical circuit, valid for frequencies starting from 100 kHz, is proposed before concluding.

2.1 SUBSTRATE COUPLING IN SI AND SOI-LIKE SUBSTRATES

Substrate coupling is the process whereby a parasitic current flow in the substrate electrically couples devices in different parts of the circuit, or circuits in different parts of the system due to the presence of conductive and capacitive path in the silicon substrate [23]. As previously mentioned HR-SOI technology has demonstrated its potentialities to reduce substrate coupling effect for mixed-signal high frequency applications. Reducing the coupling for SOI silicon substrate is strongly dependent on semiconductor doping, fixed charges in the oxide and the density of traps at the interface SiO_2/Si . This corresponds to reducing the effective substrate resistivity that leads to considerable substrate losses and, thus, to excessive attenuation of integrated transmission lines [11, 19], reduced

quality factors of on-chip inductors [10] and increase in crosstalk [20, 22]. At first, a qualitative analysis of the substrate electrical behaviour that corresponds the charges distribution in the SOI substrate was investigated through Atlas from SILVACO numerical simulation. The fundamental mechanisms of carrier's transport in a SOI capacitive structure are described using the most popular C-V characteristics. The resistivity profile is also used to get more insight about charges distribution and help to develop the correspondent equivalent circuit model.

2.1.1 Silicon substrate characterization and parasitic surface conduction (PSC) effect

The C-V MOS capacitor characteristics are well known in the literature to analyze the semiconductor substrate and oxide properties. This device is the favourable test structure for studying the substrate behaviour and mechanisms that will affect the coupling through the substrate. The equivalent capacitance per unit length is presented in Fig. 2.1, where the steady state of the carrier distribution in the cross-section of a MOS capacitor for a p-type Si substrate is shown. The quasi-static C-V characteristic of the MOS structure provides a

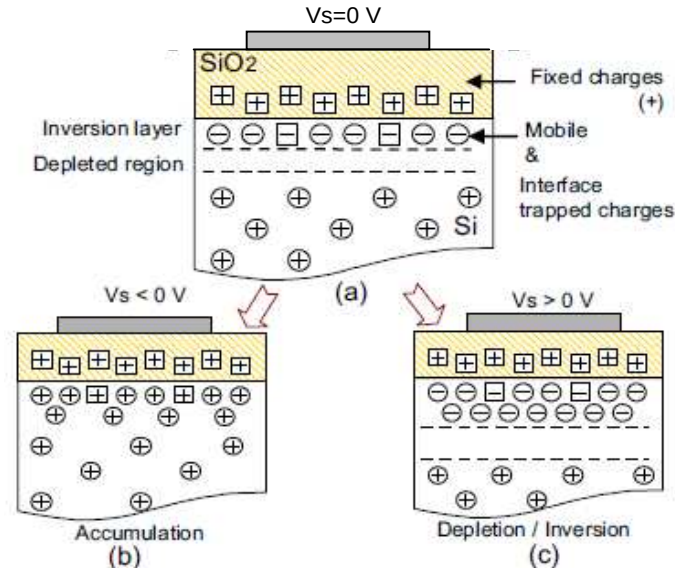


Fig. 2.1: Cross section of a MOS p-type capacitor structure under (a) zero, (b) negative, and (c) positive bias voltages [24].

better understanding of capacitance variation for different substrate properties. We simulate the C-V curve of a MOS capacitor, shown in Fig. 2.2 (a), using

Atlas software by SILVACO. It consists of a 145 nm-thick oxide and a 300 μm -thick Si substrate, using aluminium for the top and back electrodes (see Fig. 2.2 (b)). As expected, the minimum capacitance value (C_{min}) is higher for the standard Si due to the larger depletion region in the case of HR-Si. The introduction of a typical value of fixed oxide charges ($Q_{ox} = 10^{11} \text{cm}^{-2}$) produces an almost identical shift of the flat band voltage (V_{FB}), and a very slightly reduction of C_{min} for both substrates resistivity. As the applied DC voltage changes from -5 to 5 V, the MOS structure mode of operation changes from accumulation to depletion and inversion. The MOS capacitance equivalent circuit at low frequency depends on the carrier's concentration at the SiO_2/Si interface. With no applied voltages on a p-type substrate, holes represent the majority carriers in the valence band. For zero voltage ($V_{GB} = 0\text{V}$) the presence of fixed oxide charges in the oxide layer induces a weak inversion layer and a small depletion zone. When a negative voltage is applied in between the top metal and the semiconductor, more holes will accumulate at the interface oxide-p-type silicon substrate. At a strong accumulation operation mode the oxide capacitance value (C_{ox}) is depicted. The value of the oxide fixed charges density using the shift in the flat band voltage between the ideal simulated curve with $Q_{ox} = 0$ and when $Q_{ox} = 10^{11} \text{cm}^{-2}$.

When a positive voltage V_{GB} is slightly higher than V_{FB} , the majority carriers are driven away from the semiconductor-oxide interface, leaving it depleted from holes. This area acts as a dielectric and the total capacitance value correspond to the oxide capacitance in series with the depletion capacitance. As the voltage increases, the depletion region moves away from the metal surface, increasing the effective thickness of the dielectric between metal and the Si substrate, thereby reducing the capacitance. The changes of the depletion capacitance C_d versus the applied V_s voltage can be explained by the increase of the depletion region depth (t_d).

As the front applied voltage increases beyond the flat-band voltage, minority electrons carriers are attracted to the oxide/silicon interface. The electrons at the interface create a weak inversion layer, because the minority carriers density is lower than the initial doping substrate density (N_A), and the surface potential $\Psi_s \ll 2 \cdot \phi_F$. Keeping V_{GB} increasing over the flat band voltage, the density of electron increases and the equivalent C_i capacitance exceed the depletion capacitance C_d , most available minority carriers are in the inversion layer and further increase of the V_{GB} do not further deplete the semiconductor. The depletion region reaches a maximum depth and the total capacitance corresponds to the series combination of oxide capacitance C_{ox} and inversion capacitance C_i .

In all cases, a low resistivity layer appears at the SiO_2/Si interface, separated by a depletion zone from the nominal Si when inversion occurs. Such low-resistivity layer depends on the quantity of fixed oxide charges, the nominal resistivity and

type of the Si substrate.

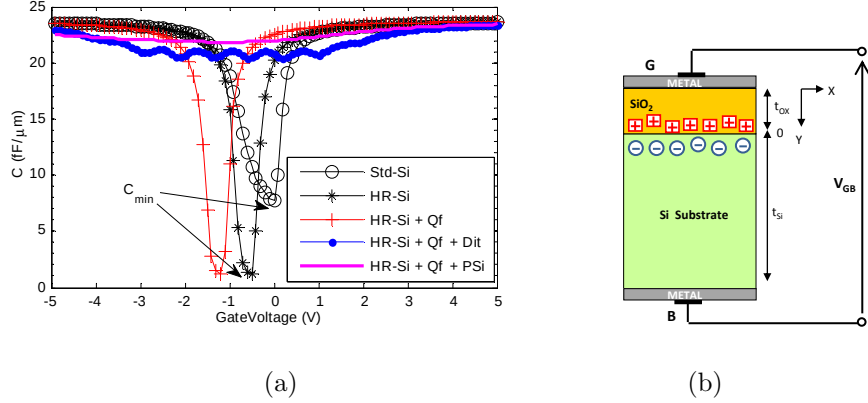


Fig. 2.2: (a) Simulated C-V curves at 1 Hz for a standard (std) and high resistivity (HR-Si : 5 kΩ-cm) p-type silicon substrate, with and without a trap-rich layer, (b) Multilayer MOS structure

Oxidized HR-Si substrate is known to suffer from Parasitic surface conduction effect (PSC) and resistivity degradation near the insulating oxide [25, 26]. Indeed, the existence of fixed oxide charges (Q_{ox}) within the SiO_2/Si interface creates a non-homogeneous surface conduction layer all over the wafer by attracting free carriers at the HR-Si surface, hence creating an inversion/accumulation zone, reducing the effective resistivity, and increasing RF losses and substrate crosstalk. To get more physical insight about the impact of PSC on the effective resistivity of the silicon substrate, numerical simulations have been run to extract the resistivity profile along the semiconductor depth as shown in Fig. 2.3. The electrical resistivity is defined using electrons and holes concentration and their corresponding mobilities, as given by the following relation (Eq. 2.1):

$$\rho(x, y) = \frac{1}{\sigma(x, y)} = \frac{1}{q(p(x, y) \cdot \mu_p(x, y) + n(x, y) \cdot \mu_n(x, y))}, \quad (2.1)$$

where q is the charge of an electron, n and p , μ_n and μ_p the electron and hole concentration and mobility, respectively.

Because of the metal-semiconductor work-function difference and the fixed oxide charges the inversion layer right underneath the oxide drastically decreases the resistivity of the substrate over a depth of approximately 3 μm . Such parasitic conduction effect can be efficiently reduced by introducing a high density of traps near the insulating oxide as detailed in following section.

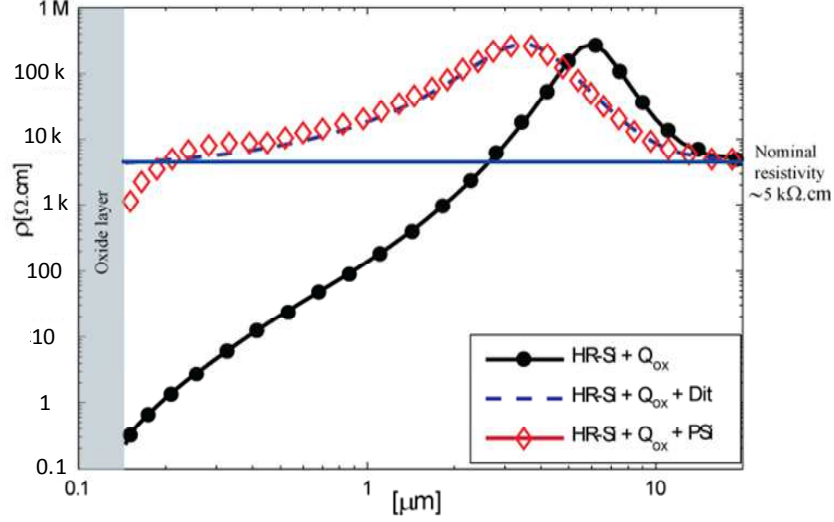


Fig. 2.3: Simulated resistivity vs. substrate depth for p-type 5 kΩ.cm HR-Si substrates, without ($Q_{ox} = 10^{11} \text{ cm}^{-2}$, $D_{it} = 0$) and with a trap-rich layer ($Q_{ox} = 10^{11} \text{ cm}^{-2}$ and $D_{it} = 10^{11} / \text{cm}^2 / \text{eV}$), at $V_{GB} = 0 \text{ V}$.

2.1.2 Crosstalk structure

The experimental crosstalk test structure consists of two identical metallic taps, embedded in a coplanar structure for RF-probe measurements, which represent respectively the noisy aggressor and the victim, as shown in Fig. 2.4. The 1 μm-thick aluminium (Al) crosstalk test structure lies on a substrate composed of a 145 nm-thick oxide, a 725 μm-thick silicon substrate of various resistivities and a 0.5 μm-thick Al back metallization. The rectangular metallic pad size is of 50 μm x 150 μm and they are spaced by 50 μm. Small-signal power transfer between both pads (S_{21} scattering parameter) is measured on-wafer from 100 kHz up to 4 GHz using a Rohde-Schwarz ZVR vector network analyzer that presents an extremely low noise floor level, lower than -130 dBm.

2.1.3 Influence of silicon substrate resistivity

The first set of measurements presented in Fig. 2.5 shows the isolation between the two metallic pads on standard resistivity Si substrate ($\rho = 20 \Omega \cdot \text{cm}$) and high resistivity Si substrate ($\rho > 1 \text{ k} \Omega \cdot \text{cm}$).

The use of SOI in combination with HR-Si considerably reduces substrate crosstalk below 10 GHz, compared to standard SOI. Measured crosstalk characteristic for a standard resistivity Si substrate of $\rho = 20 \Omega \cdot \text{cm}$ perfectly corresponds to the analysis proposed in [22]. It presents two inflection points noted f_1 and f_2 , a 40 dB/dec slope at low frequencies (below f_1) related to the 145

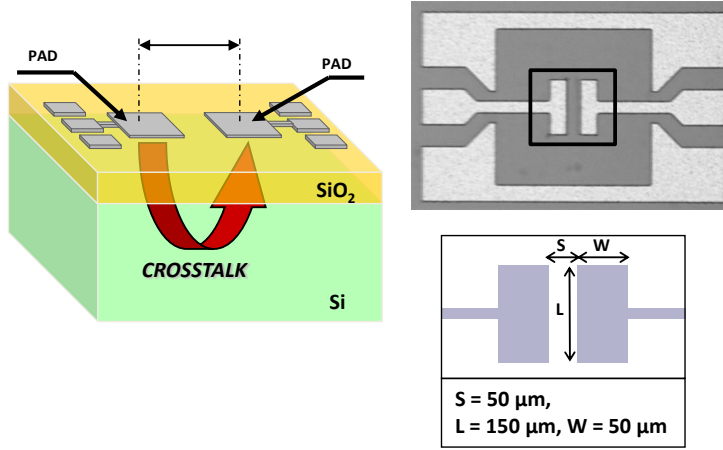


Fig. 2.4: Cross section and layout of the crosstalk test structure.

nm oxide and a slope of 20 dB/dec at high frequencies (above f_2) illustrating the capacitive coupling. However, measurements performed on HR-Si substrate below 10 MHz indicate that the S_{21} coupling parameter does not present a slope of 40 dB/dec as theoretically predicted in [19] but a slope of about 20 dB/dec.

In order to understand this abnormal or at least unpredicted behaviour at low frequencies, the crosstalk for a HR-Si substrate of $\rho = 5 \text{ k}\Omega\cdot\text{cm}$ has been simulated with Atlas numerical software. As predicted by the lumped equivalent circuit proposed in [22], simulations show a 40 dB/dec slope below f_1 in the case of HR-Si substrate. However, when fixed charges (Q_{ox}) at the oxide-substrate interface are introduced, and thus the PSC effect is considered, the low frequency slope of S_{21} is indeed close to 20 dB/dec as shown in Fig. 2.6. This behaviour cannot be modelled by the equivalent electrical circuit proposed in [22] as it will be discussed after.

2.1.4 Influence of the distance between the noisy aggressor and the victim

Crosstalk structures composed of two metallic pads spaced by different distances d have been measured and results are presented in Fig. 2.7. At a frequency of 10 MHz the crosstalk decreases from -60 dB to -70 dB when the spacing distance d increases from 50 to 150 μm . We observe a dependence of the crosstalk on spacing as described in [22], i.e. increasing the distance between the sensitive and noisy devices shifts downward the crosstalk characteristic. Similarly to Fig. 2.6, the S_{21} parameter presents a slope of 20 dB/dec below f_1 . However, it is worth

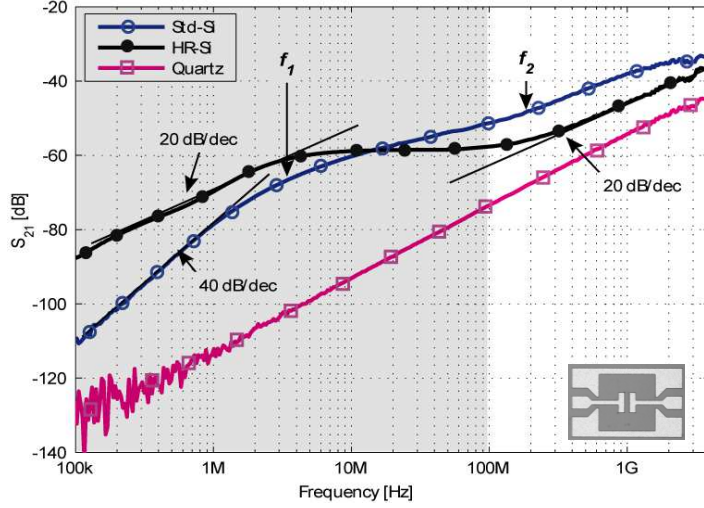


Fig. 2.5: Measured S_{21} parameters on Std ($\rho = 20 \Omega\cdot\text{cm}$) and HR ($\rho > 5 \text{ k}\Omega\cdot\text{cm}$) Silicon and quartz substrates. In the case of the Si substrates, the metallic pads and CPW feed lines are isolated from the substrate with a 145 nm-thick SiO_2 layer. The grey area extending from 100 kHz until 100 MHz highlights the frequency band which was not experimentally studied in [22].

noting that the crosstalk level is unchanged for the 3 values of d for frequencies lower than 300 kHz. This can be linked to the PSC effect, and more exactly to the presence of the inversion layer underneath the oxide layer. The independence of the substrate coupling with the distance has also been observed over a wide frequency band from 10 MHz to 10 GHz in the case of heavily-doped buried layer Bulk CMOS technology in [17]. Noise at low frequencies can have impact on victims far away from the aggressor. This could be an important drawback for SoC where low power digital circuits and MEMS actuators [9] operating at low frequencies, tens and hundreds of kHz, share the same substrate than high-speed memories, wireless and power handling circuit. Due to the substrate crosstalk at low frequencies, some systems could not be integrated into the same chip, but should have to be fabricated on a different substrate or chip, that corresponds to a System-in-Package (SiP) approach, and with a consequently increase of the cost per system.

2.2 SUBSTRATE TECHNOLOGY FOR CROSSTALK REDUCTION

A major problem for co-integration of analog front-end and digital baseband processing circuits of communication systems onto the same chip is the switching digital noise or unwanted signals that propagate through the common substrate

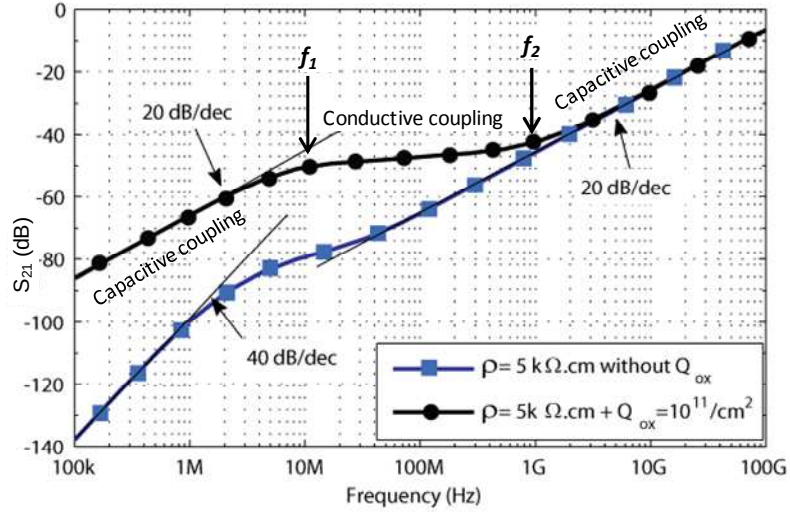


Fig. 2.6: Simulated crosstalk into HR-Si substrate with and without fixed charges ($Q_{ox} = 10^{11} \text{ cm}^{-2}$).

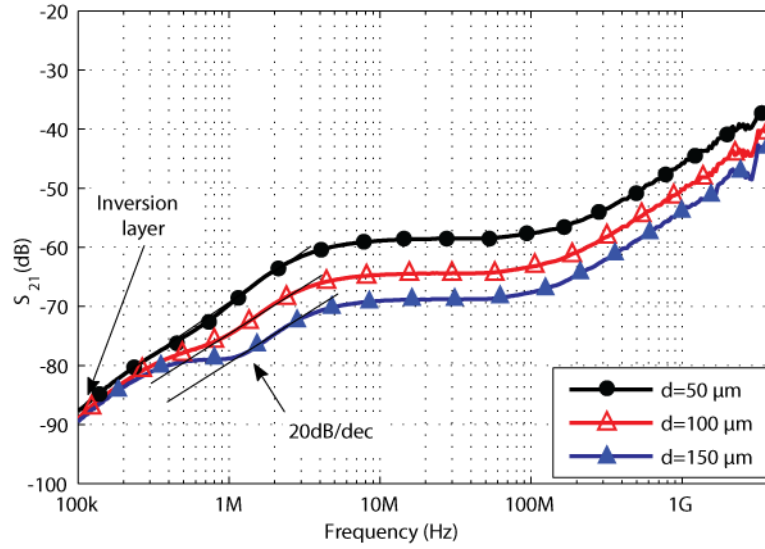


Fig. 2.7: Measured crosstalk on HR-Si substrate as a function of the distance between the two metallic pads.

degrading the performance of the analog circuits [6]. This parasitic current flow in the substrate electrically couples devices in different parts of the circuit or parts of the system due to the presence of conductive and capacitive path in the silicon substrate [23]. The three basic mechanisms governing substrate coupling are injection mainly by the digital circuitry, propagation through the common substrate and detection by the victim analog and RF devices as illustrated in Fig. 2.8. The injected signals are transmitted through the substrate by its equivalent resistances and parallel capacitances.

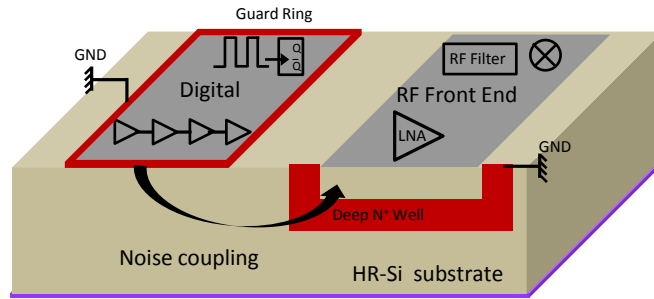


Fig. 2.8: RF and digital circuit on the same chip, isolation techniques.

2.2.1 Substrate isolation techniques

The selection and implementation of the right isolation techniques on the sensitivity circuitry, accounting for the frequency characteristics of each noise source, becomes one of the key factors that allows silicon success for RF SoC applications.

A variety of techniques to decrease the effects of substrate noise have been proposed and studied. These techniques include choices for the manufacturing technology, the substrate thickness and doping concentrations, the physical separation between noise aggressors and victims, the placement of substrate contacts, guard rings, and deep N^+ wells [27].

The simple way to deal with substrate coupling is to physically isolate the noise source and victims by placing them furthest away from each other. The simplest method is the distance isolation [3] as previously show in Fig. 2.7, where the crosstalk is reduced by more than 10 dB when the distance increases from 50 to 150 μm .

The most popular and straightforward way to shield analog circuits and improve device isolation is the use of grounded guard rings that surround the sensitive active devices. Guard rings are passive isolation structures which prevent sub-

strate noise currents reaching the analog circuitry [28] as shown in Fig. 2.8. This is due to that a guard band works as a low impedance path to ground. The effectiveness of this technique depends on the width of the guard ring, substrate resistivity, and the inductance between the guard ring and ground. In general, the isolation improves with increasing spacing, guard ring width, and substrate resistivity.

A further improvement in isolation can be achieved through the use of a deep low-resistivity n-well placed underneath the circuit block and connected to the AC ground, it acts as an effective shield to signal injected from nearby sources [29]. Another method is to increase the resistivity of a silicon substrate [30], thereby attenuating signals that leak from digital circuits through the substrate. Various new schemes have been explored to suppress substrate noise coupling between circuit elements, such as a bulk micromachining process used to create localized region on a silicon wafer where the silicon substrate is locally thinned from the backside using anisotropic etching and coated with an Al metal backside ground plane [31]. In [32] a porous silicon (PSi) trench was used to provide RF isolation between circuits. Another approach comes with the emerging SOI technologies for mixed-signal and RF applications [33]. The buried oxide layer in SOI offers superior DC/low frequency isolation in conjunction with more compact integration of active devices. At high frequencies, however, signal isolation in SOI is known to vanish [22] as the buried oxide becomes capacitively transparent to RF/microwave signals. Although, SOI technology open the way to use high resistivity substrates, it was mentioned that oxidized HR-Si wafer resistivity decreases and then the handle wafer loses its high resistivity properties. Different passivation techniques were proposed in literature to improve oxidized HR-Si RF performance by introducing a high density of traps. Next section will investigate polysilicon passivation technique to allow recovering nominal high resistivity properties of the wafer.

2.2.2 Introduction of a trap-rich layer at the SiO_2/Si interface

The highly conductive thin layer (PSC) at the SiO_2/Si which originates from the positive fixed charges inside the oxide layer or the biasing of the interconnection lines strongly degrades the substrate crosstalk characteristics over a wide frequency band. This issue can be overcome by introducing a trap-rich layer between the oxide and the HR-Si substrate which captures the free carriers and locally depletes the HR-Si substrate [24].

The presence of a high density of traps is modelled in two different ways. A first approach considers the introduction of a high enough density of traps (D_{it}) at the SiO_2/Si interface to overcome the PSC effect. These interface defect traps defined at discrete energy levels within the bandgap of the Si substrate exchange charge with the conduction and valence bands through the emissions and recombination of electrons. Two types of trap have been defined: donor-like traps below the semiconductor neutrality Fermi level and acceptor-like traps above the Fermi level. A donor-like trap is positively charged and therefore

can only capture an electron whereas acceptor-like trap is negatively charged and therefore may only emit electron. Simulated parameters for interface defect traps used in Atlas [34] for better qualitative description of carriers trapping to overcome the effect parasitic surface conduction effect are summarized in table 2.1

Parameters	Description	Values	Units
Donor	Donor-type trap level		
Acceptor	Acceptor-type trap level		
DEGEN.FAC	Degeneracy factor of the trap level used to calculate the density	2	
Density	Maximum density of states of the trap level	10^{11}	cm^{-2}
E.Level	Energy of the discrete trap level. It is equal to the energy distance between conductances band and trap level for acceptor trap, and to energy distance between trap level and valence band for donor trap.	0.1, 0.2, 0.3	eV
SIGN	Capture cross section of the trap level for electrons	2.84×10^{14}	cm^{-2}
SIGP	Capture cross section of the trap level for holes	2.85×10^{15}	cm^{-2}

Table 2.1.: Interface defect traps parameters used in Atlas Simulations

The second approach consists in placing a thin polysilicon layer of 300 nm-thick just underneath the SiO_2 layer. The high density of grain boundaries in the polysilicon layer provides a large number of surface and volumetric traps. The total density of states DoS g_E within the defined polysilicon is composed by the sum of two exponential tails distribution near the conduction (acceptor-like) and valence (donor-like) bands and two deep levels with Gaussian distribution (one acceptor-like and the other donor-like) [34]. The expression of the total energy distribution is given by:

$$\begin{aligned}
 g(E) = & NTA \exp\left(\frac{E - E_c}{WTA}\right) + NTD \exp\left(\frac{E_v - E}{WTD}\right) \\
 & + NGA \exp\left(-\left(\frac{EGA - E}{WGA}\right)^2\right) \\
 & + NGD \exp\left(-\left(\frac{E - EGD}{WGD}\right)^2\right),
 \end{aligned} \tag{2.2}$$

where E represents the trap energy, E_c is the conduction band energy, E_v is the valence band energy and the subscripts (T, G, A, D) stand for tail, Gaussian (deep level), acceptor and donor states, respectively.

To favour the trap mechanism, the defects distribution in the Si band-gap was mainly considered to be a tail distribution rather than a Gaussian distribution. Typical polysilicon parameters that provide better qualitative description are summarized in table 2.2.

Parameters	Description	Values	Units
mun	Electrons mobility	300	cm ² /Vs
mup	Holes mobility	30	cm ² /Vs
NTA	Density of acceptor-like states in the tail distribution at the conduction band edge.	10 ²¹	cm ⁻³ /eV
NTD	Density of donor-like states in the tail distribution at the valence band edge	10 ²¹	cm ⁻³ /eV
WTA	Characteristic decay energy for the tail distribution of acceptor-like states	0.033	eV
WTD	Characteristic decay energy for the tail distribution of donor-like states	0.049	eV
NGA	Total density of acceptor-like states in a Gaussian distribution	1.5×10 ¹⁷	cm ⁻³
NGD	Total density of donor-like states in a Gaussian distribution	1.5×10 ¹⁷	cm ⁻³
EGA	Energy that corresponds to the Gaussian distribution peak for acceptor-like states. This energy is measured from the conduction band edge	0.62	eV
EGD	Energy that corresponds to the Gaussian distribution peak for donor-like states. This energy is measured from the valence band edge.	0.78	eV
WGA	characteristic decay energy for a Gaussian distribution of acceptor-like states	0.15	eV
WGD	characteristic decay energy for a Gaussian distribution of donor-like states	0.15	eV

Table 2.2.: Polysilicon parameters used in Atlas Simulations

The simulated C-V characteristics in Fig.2.2 for both standard and high-resistivity resistivity values show the effect of the traps which strongly increases the semiconductor capacitance in series with the BOX capacitance, hence the total MOS capacitance tends to the BOX capacitance over the entire bias range. The simulated resistivity profile below one of the metallic pads of the crosstalk structure, biased at zero DC voltage ($V_{GB}=0V$), is shown in Fig. 2.3. We observe that, in both cases, the high resistivity value is recovered at the top surface of the substrate and a buried depletion region is created before reaching the nominal resistivity of the HR-Si substrate, i.e. 5 k Ω .cm for the simulated case, at a depth larger than 10 μ m.

Fig. 2.9 shows the simulated crosstalk response between both metallic pads for an oxidized HR-Si with and without the introduction of a 300 nm-thick PolySi layer, acting as a trap-rich layer, at the SiO_2 /Si substrate interface. These results clearly show the efficiency of the PolySi layer to minimize the noise coupling. We observe a reduction of more than 20 and 35 dB at, respectively, 100 kHz and 10 MHz. Basically, thanks to the PolySi layer the intrinsic high resistivity properties of the HR-Si are recovered, i.e. the impact of Q_{ox} and thus PSC is cancelled out. This tremendous improvement is also experimentally demonstrated in Fig.2.10 with the introduction of a 300 nm-thick undoped PolySi layer. Actually, the trap-rich HR-Si substrate behaves as a lossless substrate (purely capacitive coupling) over nearly the whole measurement frequency range. Indeed, S_{21} parameter shows a 20 dB/dec dependence over the whole frequency band above

1 MHz, similar to the quartz substrate. It is worth noting that the 40 dB/dec slope of S_{21} parameter below f_1 , theoretically predicted in [22], is recovered for HR-Si substrate (Figs. 2.4 and 2.6) thanks to the introduction of a trap rich layer underneath the oxide. Besides, the introduction of a trap-rich layer provides a better isolation than guard ring or metal Faraday cages [17].

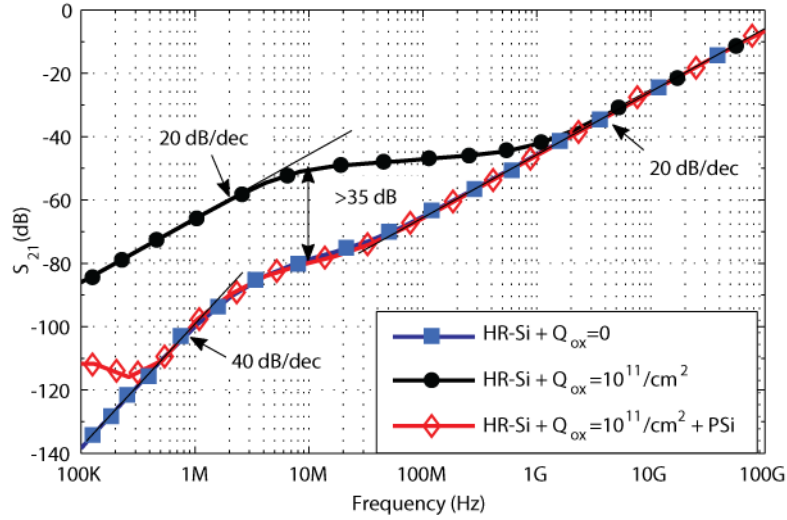


Fig. 2.9: Simulated crosstalk on HR-Si substrate without and with Q_{ox} and in presence of a trap-rich polysilicon layer of 300 nm-thick for a pads distance $d = 50 \mu\text{m}$.

2.2.3 Polysilicon (PSi) layer thickness

To provide a high density of traps between the Si substrate and the oxide, we deposited a layer of polycrystalline silicon (PolySi) by means of a low pressure chemical vapour deposition (LPCVD) at 625°C at 1.08 mTor. The resulting wafer followed a PECVD oxidation to obtain the desired 3000 nm-thick SiO_2 on top of the PolySi layer. The high density of traps are formed at the grain boundaries, thus the uniformity of grain size and its typical columnar grain microstructure [11] determine the efficiency of the deposited trap-rich layer to reduce the PSC effect. The numerous traps created by silicon dangling bonds in PolySi are able to absorb the free carriers attracted at the SiO_2/Si interface and greatly reduce substrate losses. Fig. 2.11 displays the crosstalk response between both metallic pads for deposited PolySi layers ranging from 76 up to 435 nm. The direct relationship between the crosstalk reduction and the PolySi thickness is clearly observed. A thickness of 435 nm is needed to approach the crosstalk behaviour of a lossless Si substrate. The critical thickness to get rid of the PSC

effect will depend on the PolySi grain size as experimentally demonstrated in [11]. PolySi layer characterized by small grains, such as crystallized amorphous silicon [11], provides an efficient trap-rich layer already for a thickness of 280 nm.

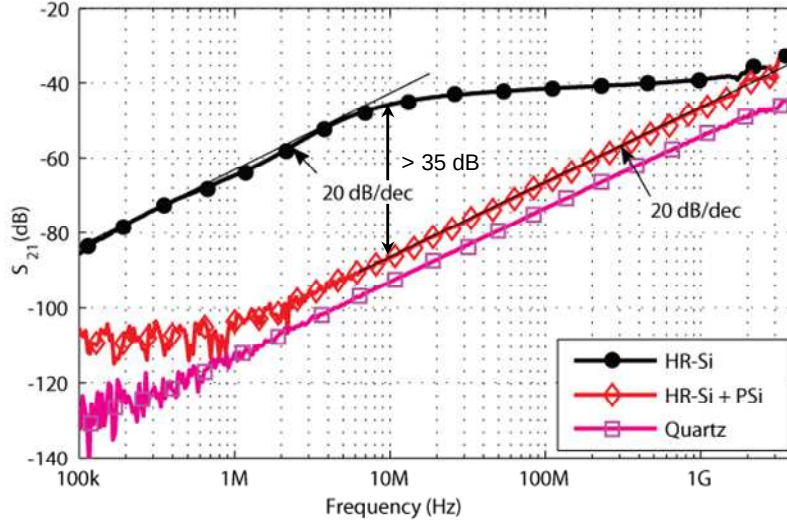


Fig. 2.10: Measured S_{21} response on quartz and HR-Si substrates with and without 300 nm-thick polysilicon layer.

2.3 CROSSTALK MODELLING

With a high level of integration in system-on-chip applications, it is mandatory to incorporate substrate coupling into the compact models in order to properly simulate the wideband electrical behaviour of integrated circuits. Moreover, the development of a lumped elements equivalent circuit for substrate crosstalk provides a precious tool to deeper understand the physical coupling mechanisms and to predict the efficiency of various crosstalk reduction techniques. A new lumped elements equivalent circuit is proposed hereafter to describe the PSC effect and its reduction by the introduction of a trap-rich PolySi layer. Simulations using this model over a wide frequency band are compared with measurements to validate the approach.

2.3.1 Equivalent circuit including PSC effect

As shown in Fig. 2.6, a typical crosstalk versus frequency curve is subdivided into three regions separated by two characteristic frequencies, f_1 and f_2 . The frequency at which the capacitance starts to play a role is the transition frequency,

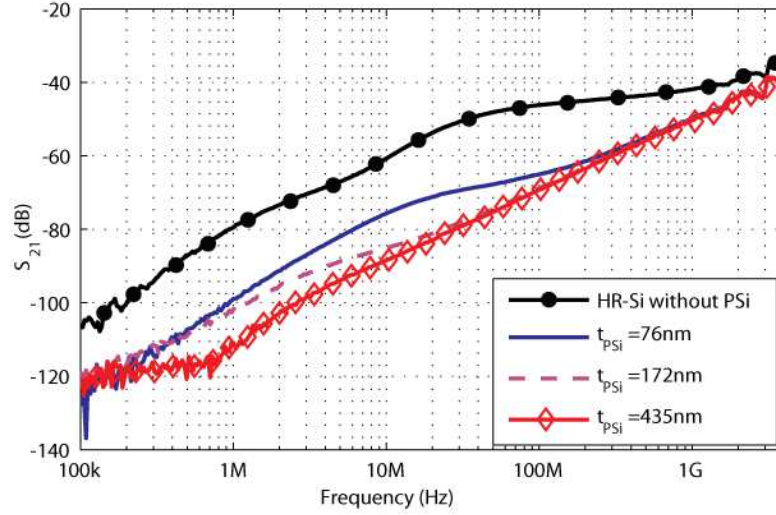


Fig. 2.11: Dependence of crosstalk on the polysilicon layer thickness for a HR-Si substrate ($d = 50 \mu\text{m}$).

which is also determined by the resistivity that depends on the doping level.

At low frequencies the oxide capacitance dominates and the first region defined by the transition frequency f_1 is characterized by a 40 dB slope without the effect of the parasitic surface conduction effect as in [22] and by 20 dB slope when it is included. At medium frequencies, a conductive layer is defined by the two transition frequencies f_1 and f_2 which are defined respectively by the substrate resistance R_{Si2} between the top and bottom of the substrate and the R_{Si1} which define the conductive coupling between the two metallic pads as shown in the equivalent lumped circuit in Fig. 2.12 similarly to the model presented in [22]. The increase of the oxide thickness reduces the low frequency coupling as it was previously investigated in [35] that is why the SOI CMOS technology is a viable solution compare to bulk CMOS technology from the substrate crosstalk point of view.

When including the PSC effect the lumped elements equivalent circuit modelling the coupling between two metallic pads of same size lying on an oxidized HR-Si substrate is shown in Fig. 2.13. The capacitances noted C_1 represent the coupling between the metallic pads and the SiO_2/Si substrate interface, R_2 , C_2 , the resistive and capacitive coupling between each pad and the wafer backside metallization, and R_3 , C_3 the resistive and capacitive coupling path between both metallic pads through the silicon substrate. The analytical expressions of those lumped elements are given hereafter.

$$C_1 = K_1 \cdot \frac{\epsilon_0 \cdot \epsilon_{ox} \cdot A_{pad}}{t_{ox}} \quad (2.3)$$

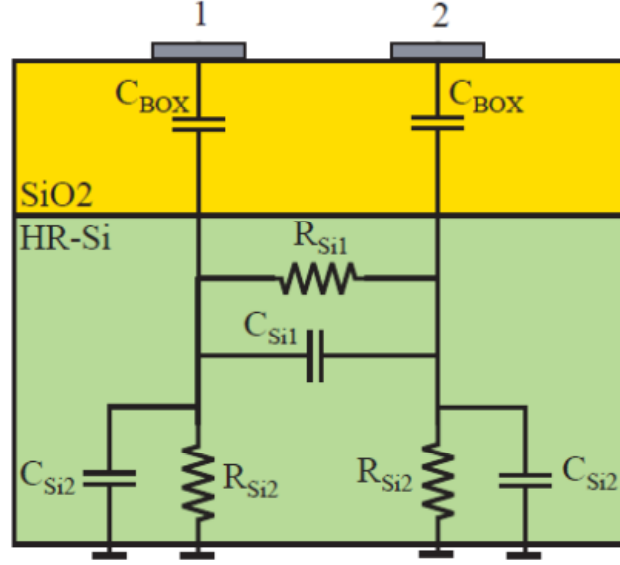


Fig. 2.12: Equivalent lumped elements of substrate crosstalk on oxidized high resistivity Si substrate.

where ϵ_0 , ϵ_{ox} , t_{ox} and A_{pad} , are, respectively, the absolute permittivity (vacuum), oxide relative permittivity, the thickness of the oxide layer, the area of the metallic pad, and K_1 is a fringing factor accounting for the fringing field effects. For identical pads with an area of $A_{pad} = W \times L = 50 \mu\text{m} \times 150 \mu\text{m}$, the expressions of R_2 and C_2 derived from [22], are given by:

$$R_2 = \left[K_2 \cdot \frac{\sigma_{Si} \cdot A_{pad}}{t_{Si}} \right]^{-1} \quad (2.4)$$

$$C_2 = K_2 \cdot \frac{\epsilon_0 \cdot \epsilon_{Si} \cdot A_{pad}}{t_{Si}} \quad (2.5)$$

The rectangular pads presents equal width $W = 50 \mu\text{m}$ and located at a spacing distance $d = 100 \mu\text{m}$. The capacitance C_3 and resistance R_3 between the two are calculated using the following expressions [22, 36]: ,

$$R_3 = \left[K_3 \cdot \frac{\sigma_{Si} \cdot \pi}{4 \cdot \ln \left[\frac{\pi(d-W)}{W+t} + 1 \right]} \cdot W \right]^{-1} \quad (2.6)$$

$$C_3 = K_3 \cdot \frac{\pi \cdot \epsilon_0 \cdot (\epsilon_{Si} + 1)}{4 \cdot \ln \left[\frac{\pi(d-W)}{W+t} + 1 \right]} \cdot W \quad (2.7)$$

where ϵ_{Si} , σ_{Si} , and t_{Si} are, respectively, the relative permittivity, the conductivity and the thickness of silicon substrate. t is the thickness of the metallic

conductor ($t_{Al} = 1 \mu m$), and K_2 and K_3 are the fringing factor coefficients and their expressions are given in [22].

In order to introduce the impact of PSC, the formed highly conductive layer is modelled by the inversion resistance R_{inv} (Eq. 2.8) [37] underneath which there is a depletion region that can be described by its depletion capacitance C_d (Eq. 2.9) where $X_{d,max}$ is the maximum depletion depth expressed by Eq. 2.10. Where ρ_{inv} , t_{inv} , d , N_A , n_i et K are the resistivity and thickness of the inversion layer, the spacing distance between each metallic pad, the acceptors concentration, the intrinsic carrier density and a fringing factor, respectively.

$$R_{inv} = K \cdot \frac{\rho_{inv} \cdot d}{W \times t_{inv}} \quad (2.8)$$

$$C_d = K \cdot \frac{\varepsilon_0 \cdot \varepsilon_{Si}}{X_{d,max}} \cdot A_{pad} \quad (2.9)$$

$$X_{d,max} = \sqrt{\frac{4 \cdot \varepsilon_0 \cdot \varepsilon_{Si} \cdot \ln\left(\frac{N_A}{n_i}\right)}{q^2 \cdot N_A}} \quad (2.10)$$

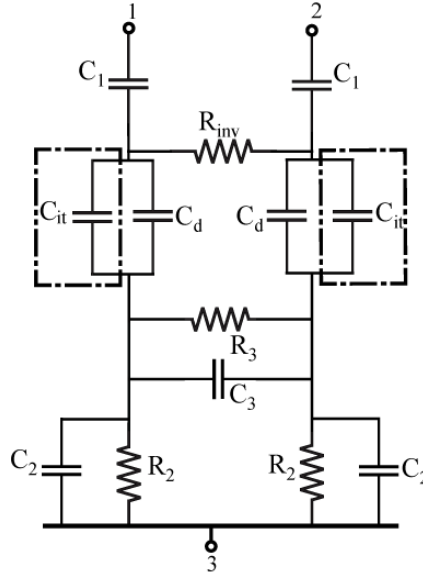


Fig. 2.13: Lumped element electrical equivalent circuit for substrate crosstalk modelling considering the presence the PSC effect (R_{inv}) and trap-rich layer (C_{it}). The values introduced in the PSC lumped model are: $C1 = 1.4$ pF, $Cd = 80$ fF, $R_{inv} = 0.09$ M Ω , $R3 = 0.6$ M Ω , $C3 = 9.6$ fF, $R2 = 5$ M Ω , $C2 = 1.04$ fF, and for the PSi lumped model: $C1 = 1.4$ pF, $Cd = 4$ fF, $C_{it} = 18$ fF, $R_{inv} = 17$ M Ω , $R3 = 0.6$ M Ω , $C3 = 30$ fF, $R2 = 5$ M Ω , $C2 = 1.04$ fF.

The previous analytical expressions have been used to set initial parameters of the model presented in Fig. 2.13, then the equivalent circuit elements were fitted using ADS software to the measurement results. Based on the equivalent circuit in Fig. 2.13 a quite good agreement was achieved between the measured and simulated data over the entire frequency band as shown in Fig. 2.14. The PSC effect at the SiO_2/Si interface is well described using the lumped elements R_{inv} and C_d , and a typical 20 dB/dec slope is simulated at low frequency for a HR-Si substrate, in agreement with the measurements, contrary to the 40 dB/dec predicted in [22]. It is worth to notice that for d larger than a few hundreds of μm distributed effects into the substrate might impact the crosstalk behaviour over the frequency range. In that case, several lumped elements equivalent circuits must be cascaded to model the propagation of the coupling signal into the substrate. Atlas numerical models take into account those distributed effects along the coupling path in the Si substrate.

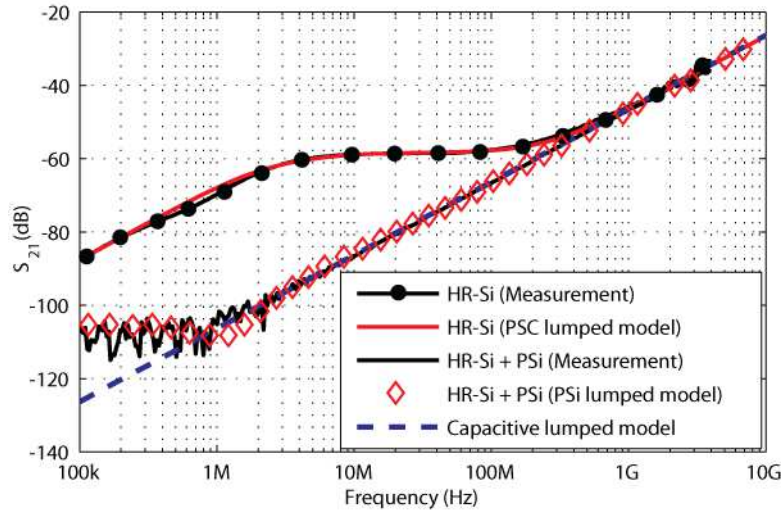


Fig. 2.14: Measured and modelled crosstalk in HR-Si substrate without and with 300 nm-thick polysilicon layer.

2.3.2 Equivalent circuit including a trap-rich layer

The introduction of a trap-rich layer below the oxide has a double effect on the crosstalk equivalent circuit: (1) the increase of the R_{inv} value because of the drastic carrier mobility reduction caused by the trapping mechanisms, and (2) the presence of a parallel capacitance C_{it} (Eq. 2.11) with C_d whose value depends on the trap density of the PolySi layer. The depletion layer depth increases on trap-rich oxidized HR-Si wafer as depicted from the resistivity profile vs. sub-

strate depth in Fig. 2.3, which explain C_d low value. When considering a large value for R_{inv} and C_{it} in the equivalent circuit of Fig. 2.13 (the fitting values are given in the caption of the figure), a typical 20 dB/dec slope crosstalk characteristic can be obtained over the whole frequency band which is in agreement with the measurements. Again, this simple lumped element model demonstrates that minimum crosstalk coupling can be reached over a wide frequency band by the introduction of a trap-rich layer in the case of HR-Si substrate. This is in agreement with the Atlas simulations presented in Section 2.1.1 and Fig. 2.3. Finally, thanks to the introduction of a trap-rich layer, the crosstalk behaviour of a HR-Si substrate can be modelled by a simple capacitive model as presented in Fig. 2.15. This purely capacitive model fits very well with measurements in Fig. 2.14 for frequencies higher than 1 MHz.

$$C_{it} = K \cdot q \cdot D_{it} \cdot A_{pad} \quad (2.11)$$

where q the electron charge, D_{it} the interface traps density extracted from Atlas simulations as previously defined in Section 2.1.1: $D_{it} = 10^{11}/\text{cm}^2/\text{eV}$, K is a filling factor.

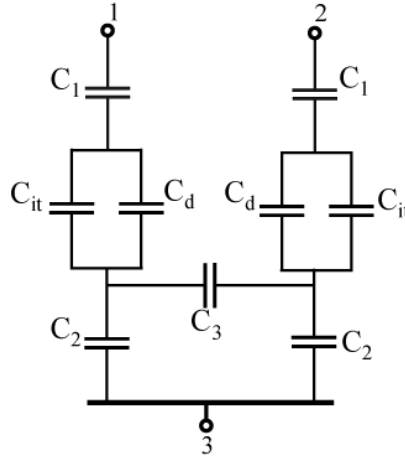


Fig. 2.15: Purely capacitive crosstalk model for the trap-rich HR-Si substrate. The values introduced in the capacitive lumped model are: $C_1 = 1.4$ pF, $C_d = 4$ fF, $C_{it} = 18$ fF, $C_3 = 30$ fF, $C_2 = 1.04$ fF.

2.4 CONCLUSION

In this chapter based on the electrical properties of HR-Si substrates, the crosstalk on Si (and HR-Si) substrates over a wide frequency band has been

analyzed. A standard $C(V)$ characteristics for a simple MOS structure was used to analyse the charge distribution over the oxidized Si substrate. The simulated resistivity profile demonstrate the effect of the highly conductive inversion layer of several microns at the substrate surface. Such parasitic surface effect degrades the high resistivity properties of the handle wafer and increases the coupling through the common substrate.

A lumped element equivalent circuit model from 100 kHz up to several GHz, based on the physical understanding of substrate crosstalk, has been proposed and compared with measurements and numerical simulations. It includes the impact of PSC effect and its reduction thanks to the introduction of trap-rich layer at the oxide-Si substrate interface. It has been proved that the discrepancy between measurements and previous crosstalk models [22] for Si and HR-Si substrates at low frequencies, is due to the presence of a highly conductive layer (PSC) at the Si surface.

The introduction of a trap-rich layer of PolySi has been successfully simulated and compared with crosstalk measurements. It has been proved to be an efficient solution to drastically reduce the crosstalk at frequencies below 10 GHz, to fully leverage the excellent properties of the HR-Si (or HR-SOI) for low loss RF, mixed mode and SoC applications. Thanks to this trap-rich PolySi layer, a purely capacitive lumped equivalent circuit properly describes the quasi-lossless HR-Si substrate. This simple capacitive model can be used by RF designers to build RF, analog and digital devices lying on a PolySi trap-rich HR-Si substrate.

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CHAPTER 3

CPW RF SWITCH AND OPTICAL CROSSTALK ON TRAP-RICH HR-SI SUBSTRATES

THE growing interest in optical control of microwave and millimeter-wave devices and systems was driven by the need of the heterogeneous integrations of digital, analog/RF circuits, RF MEMS structures and optically controlled devices on the same chip [1]. The term "optical control of microwaves" describes such a mechanism where an incident optical signal alters the performance characteristics of a microwave device. One of the means of achieving this is through photo-conductivity. The photo-conductive effect within the semiconductor substrate is the origin of all optically controlled microwave components. Incident optical energy is absorbed in a semiconductor material within a microwave device, thus generating electrical carriers that alters the state of the microwave device. The electron-hole pairs generated in the semiconductor material locally modify the substrate conductivity which leads to a significant change in the propagation of microwave signal. Si-based photonics has gotten considerable expansion and development, and various microwave devices using the photo-conductivity effect have been developed which include photo-induced switches [2], phase shifters, attenuators [3], reconfigurable antenna [4] and optically controlled millimeter-wave filters [5]. In addition to the possibility of co-integration, optical control of microwave circuit has attracted interest largely because of its unique advantages such as fast response, immunity to electromagnetic interferences, high power handling, good isolation between

controlling and controlled devices.

However, due to the inherent optoelectronic properties of semiconductor substrate, the photo-induced carriers are not restricted to the illuminated zone but spread laterally through a large area [6]. Such lateral diffusion of photogenerated carriers can drastically influence the behaviour of neighbour devices and interconnections due to optical crosstalk. In the previous chapter, electromagnetic crosstalk has been investigated over a wide frequency band. Similar to the electrical coupling, optical crosstalk is a critical issue for co-integration of optical controlled devices, digital, analog and RF circuits on the same chip. The reduction of the small-signal electrical crosstalk has been demonstrated with the high resistivity (HR) Silicon-on-Insulator (SOI) technology [7]. However, the RF losses associated with the free carrier accumulation or inversion at the SiO_2/Si interface (parasitic surface conduction) degrade the RF properties of the substrate [8] and lead to the generation of harmonics [9], [10]. It has been shown that those surface parasitic effects can be overcome by using a trap-rich polysilicon layer [8], amorphous silicon layer [11], amorphous silicon followed by Si-crystallization at 900 °C) with rapid thermal annealing (RTA) [12], or by damaging the silicon interface through ion implantation [13]. The trap-rich passivation layer was proven as an efficient technological solution to recover the HR properties of the HR-Si substrate, and to reduce the harmonic distortion originated from the substrate [9], [10], RF losses and electrical crosstalk over a wide frequency range [14].

This chapter aims at covering the efficiency of a polysilicon trap-rich layer to restrict the photo-induced plasma in the active area of the optically modulated coplanar wave-guide (CPW) RF switch and thus drastically reduce the optical crosstalk between other RF switches and CPW interconnection lines lying on the same HR-Si substrate. Following this, we detail CPW optically controlled RF switch operation, photoconductivity profile using theoretical expressions. Efficiency of the optically controlled switch on high resistivity silicon (HR-Si) substrate is then investigated. The lateral diffusion of photogenerated carriers is simulated and measured on HR-Si wafer. A proposed new design for the CPW RF switch is investigated to show the efficiency of the trap-rich passivation layer by reducing the lateral diffusion, while keeping the switching efficiency of the optically controlled device.

3.1 CPW OPTICALLY CONTROLLED RF SWITCH

Research on Si-based optoelectronic devices is stimulated by several developments such as emergence of silicon-on-insulator (SOI) as platform for both photonic integrated circuits and mixed-signal integrated circuits on CMOS technology [15]. Excellent optical properties as well as true compatibility with CMOS integrated circuit technology is highly promising for future low-cost optically controlled and photonic integrated circuits. Actually, it is widely established nowa-

days that SOI technologies are the best candidates for low-power low-voltage mixed signal integration for RF applications [16]. Besides, SOI substrates provide a strong reduction of RF losses and electromagnetic coupling for mixed-signal integration [7]. The great maturity of silicon processing can be applied in many respect to SOI based optically controlled and photonic integrated circuits with very low cost and high level of integration, which certainly enhance heterogeneous integration for RF SoC applications.

The interest in microwave components with tunable switching behaviour has been increasing over the past years. Multi-mode communication applications have become popular and more demanding. The RF front end needs either a multiband or a wideband tunable RF/ microwave devices such as antennas to cover multi-standard operations, tunable power amplifiers to adjust output power in some wireless systems, tunable filters, phase-shifters, oscillator, and so on. A wide range of solutions have been proposed in the literature to provide tunability of RF devices and circuits. Some of them include PIN diodes [17], varactor diodes, or MEMS switches [18]. The main disadvantage of these approaches is the need of specific control voltage lines to tune electro-statically the RF behaviour of the device. It imposes the design of specific voltage control circuitry and the presence of electrical bias lines which may affect the integrity of the RF signal. Another known way to make tunable RF components is by using optoelectronic techniques. Optical control of the various components commonly used in antenna T/R modules such as attenuators [19, 20], tunable filters, switches [21], phase shifters [22] and reconfigurable antenna [4] has been demonstrated.

Several different methods are being used for the optical control of microwave circuits and antennas. They can be broadly classified as direct and indirect control schemes. Some Direct optical control schemes rely on illumination of bulk semiconductor substrates while others involve illumination of semiconductor junction devices such as PIN diodes, FETs and Bipolar transistors. Indirect optical control involves the illumination of a dedicated optical detector that converts the optical control signal into a suitable electrical form, and controls the performance of microwave device.

Photo-conductive switches, where the control of the tunable parameter is done via an off-chip light source that illuminates a defined area, appear as the best alternative to avoid additional circuitry and, in some cases, applied high-voltage values. Moreover, it allows almost perfect thermal and electromagnetic isolation, as well as high-speed modulation. The concept of exploiting optically induced losses in semiconductor substrate to monitor the signal attenuation along a CPW line was firstly reported by Platte in [23]. Sadow and Lee [24] presented measurements of a CPW photoconductive switch fabricated on GaAs substrate showing up to 45 dB of microwave isolation at 1.7 GHz using 143 mW of laser diode power. More recently, a heterostructure light activated microwave photoconductive switch [25] on GaAs substrate combined with a vertical-cavity surface emitting laser by flip-chip bonding technology reported 25 dB insertion loss value at 1 GHz. Canseliet et al. [26] designed an optically controlled microwave switch

on silicon substrate which shows an insertion loss of 15 dB at 20 GHz. Table 3.1 summarizes different microwave switches used for reconfigurable applications.

Ref.	Freq. (GHz)	Insertion loss S_{21} (dB)	Power (mW)
Single PIN diode [17]	5.6	20	-
MEMS RF switches [18]	2	23	-
Heterostructure photoconductive switch [25]	1	25	-
Photoconductive switch [4]	12	15	200
Optically controlled switch [26]	20	15	90
CPW photconductive switch [24]	1.7	45	143
This work on HR-Si	2	18.5	65
	20	50	65
This work on HR-Si + PolySi (window)	2	11	65
	20	25	65

Table 3.1.: Microwave switches used in RF reconfigurable applications

3.1.1 Photo-induced carriers distribution

As the name suggests, photo-conductivity strictly refers to the increase in electrical conductivity of a photoconductive material in response to incident light. The fundamental physical mechanism arising in the optical microwave switch is the photo-generation (electron-hole plasma) within the illuminated semiconductor region when the photon energy is equal or greater than the semiconductor band gap energy. The photo-generated carriers create a highly conductive region at the substrate surface. The basic structure of a CW-mode optically controlled CPW RF switch lying on HR-Si substrate is shown in Fig. 3.1 (a). The charge carriers in the bulk region of the HR-Si film increase the electrical conductivity leading to a smaller shunt resistance as shown in Fig. 3.1(b). Platte in [27] gives a theoretical distribution profile of such photoconductivity process. The basic situation of the optical control of photo-conductivity in optical microwave switches devices illustrates the incident laser radiation which produces an exponential decay of the photo-conductivity according to:

$$\Delta\sigma(y) = \Delta\sigma_s \cdot e^{-\alpha \cdot y} \quad 0 \leq y \leq \infty \quad (3.1)$$

where y is the direction perpendicular to the substrate surface, $\Delta\sigma_s$ the surface photo-conductivity at $y=0$, and α the absorption coefficient or the inverse of the penetration depth which depends on the light wavelength and the semiconductor band-gap energy. For a trap-less material with negligible surface recombination,

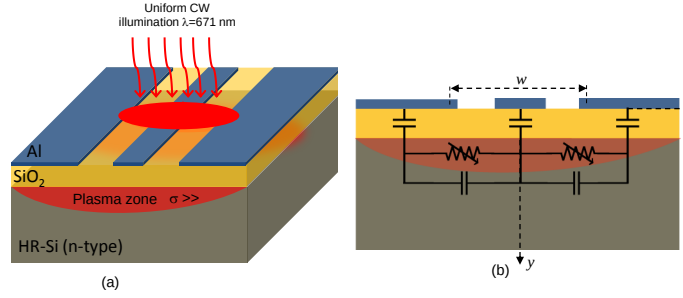


Fig. 3.1: Photo-induced CPW RF switch structure.

the peak value of $\Delta\sigma_s$ can be expressed by:

$$\Delta\sigma_s = \frac{q}{h \cdot c_0} (\mu_n + \mu_p) (1 - R) S \cdot \alpha \cdot \lambda_0 \cdot \tau \frac{P}{A} \quad (3.2)$$

where q is the electronic charge, h the Planck's constant, c_0 the velocity of light in vacuum, μ_n and μ_p are the electron and hole mobilities, respectively, R the surface reflectivity, S the relative spectral response of the semiconductor material exhibiting a peak response at λ_0 , τ the excess carrier lifetime, P the incident peak power and A the illuminated area.

Using a CW-laser irradiance across the irradiated window with a width $W = 400 \mu\text{m}$ and a uniform transversal photoconductivity $\Delta\sigma(y) = \Delta\sigma_{\text{meff}} = \text{constant} = 10 (\Omega \cdot \text{cm})^{-1}$ extracted from Atlas simulations at the maximum illumination power intensity (90 mW), the lateral diffusion-controlled profile of photoconductivity $\Delta\sigma(x)$ [27], [28] is approximately given by:

$$\Delta\sigma(x) = \Delta\sigma_{\text{meff}} \left\{ 1 - e^{-\frac{W}{L_a}} \cosh\left(\frac{x}{L_a}\right) \right\} \quad -\frac{W}{2} \leq x \leq \frac{W}{2} \quad (3.3)$$

$$\Delta\sigma(x) = \Delta\sigma_{\text{meff}} \sinh\left(\frac{W}{2L_a}\right) e^{\frac{x}{L_a}} \quad -\infty \leq x \leq -\frac{W}{2} \quad (3.4)$$

$$\Delta\sigma(x) = \Delta\sigma_{\text{meff}} \sinh\left(\frac{W}{2L_a}\right) e^{-\frac{x}{L_a}} \quad \frac{W}{2} \leq x \leq \infty \quad (3.5)$$

$$L_a = \sqrt{\left[\left(2\mu_n\mu_p\tau k_B \frac{T}{q} \right) (\mu_n + \mu_p) \right]} \quad (3.6)$$

where L_a is the ambipolar diffusion length assumed to be independent of excess carrier density, k_B is Boltzmann's constant and T is the absolute temperature. It is seen from Fig. 3.2 that lateral carrier diffusion into the shaded

semiconductor regions at the ends of the illuminated zone causes an increase the optical crosstalk. Photo-generated carriers in HR-Si substrate with an excess carrier lifetime $\tau = 10^{-4}s$ [28] spread over a large area of the CPW optical switch (several hundreds of microns). Lateral carrier diffusion mechanism causes a high optical crosstalk photo-generation rate. The lateral carriers distribution is mainly controlled by diffusion and is depending on the spot size of the illumination and the ambipolar diffusion length. The ambipolar diffusion length is coupled to the carrier lifetime as in Eq. 3.6. The decrease of the lifetime reduces the diffusion length, and implies a decrease of the excess carrier concentration. This can only be compensated when the generation of excess carriers is increased by illuminating the substrate with a higher optical intensity [29]. To reduce such lateral carriers diffusion we may need to limit the substrate illuminated surface so as to have a higher photoconductivity in a restricted zone and reduced lateral diffusion otherwise. Optical isolation can be achieved by decreasing the lifetime τ to values lower than $10^{-6}s$ [30], [31]. For the shortest life time, the electron concentration nearly equals the doping concentration, which means that the photogenerated carriers are immediately recombined when generated. The alteration of the excess carrier lifetime can be achieved with the introduction of traps and recombination centers in the region where carriers are photo-generated.

3.1.2 Numerical simulations of CPW optical RF switch on HR-Si substrate

2D Atlas SILVACO is a physically based semiconductor device simulator that predicts the electrical behaviour associated with the physical structure under specified biased and illumination conditions. ATLAS achieves this through partitioning the specified device into a two or three-dimensional mesh grid. ATLAS then applies a set of differential equations, based on Maxwell's Laws, to the mesh to simulate the transport of carriers through the structure [32]. Accurate high frequency small-signal Atlas simulations of the coplanar optically controlled structures were investigated. A CPW line with $56\ \mu\text{m}$ for the central conductor, $36\ \mu\text{m}$ for the slots width and $208\ \mu\text{m}$ for the coplanar ground planes is simulated on top of a $4\ \text{k}\Omega\text{-cm}$ high resistivity silicon substrate. The photo-induced plasma volume is simulated under different optical power intensities, using a continuous wave mode laser at a wavelength of $671\ \text{nm}$. The spot laser is positioned $100\ \mu\text{m}$ above the CPW structure with an open window diameter of $400\ \mu\text{m}$. A maximum optical power of $90\ \text{mW}$ is considered with a uniform beam distribution. Figs. 3.3 (a) and 3.3 (b) shows the simulated insertion loss (S_{21}) and reflection coefficient (S_{11}) of the CPW switch under various illuminations. The photo-induced switch performance increases with the light power, reaching $18\ \text{dB}$ and $48\ \text{dB}$ at 2 and $20\ \text{GHz}$, respectively, under $90\ \text{mW}$ optical power. The optically generated carriers within the bulk region of the HR-Si film decrease the high dark-resistivity (Off-state) of the semiconductor causing a transition to the "on-state" of the device.

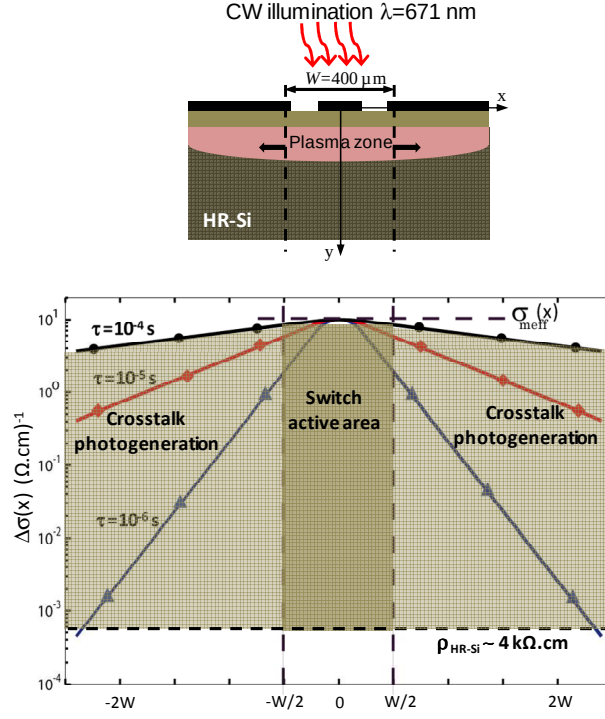


Fig. 3.2: Longitudinal diffusion profile of photoconductivity $\Delta\sigma(x)$ (using Eq. 3.3, 3.4 and 3.5 on HR-Si substrate ($4 \text{ k}\Omega\cdot\text{cm}$), $\mu_n + \mu_p = 1,870 \text{ cm}^2/\text{Vs}$, and $T = 300 \text{ K}$).

3.1.3 CPW RF switch characterization

3.1.3.1 Measurements setup

On-wafer S-parameter measurements were performed with an Anritsu 37269D VNA using SüssTM $150 \mu\text{m}$ |Z| GSG on-wafer RF probes over the frequency range from 40 MHz to 25.5 GHz. A dedicated on-wafer short-open-line-thru (SOLT) calibration technique is used to remove parasitic components such as cables, connectors and other systematic errors. The calibration process aims at moving the measurement reference plane at the VNA to tips of the RF probes. A TRL (thru-Reflect-Line) deembedding technique is then used to remove unwanted parasitics introduced from the CPW RF pads and get the real S-parameters of the DUT. A $8,000 \mu\text{m}$ -long CPW transmission line was illuminated with a continuous wave mode laser diode at a wavelength of 671 nm. The output laser light was coupled into a 2 m-long and $450 \mu\text{m}$ -diameter plastic optical fiber, and the fiber was positioned with a probe-holder above both CPW slots

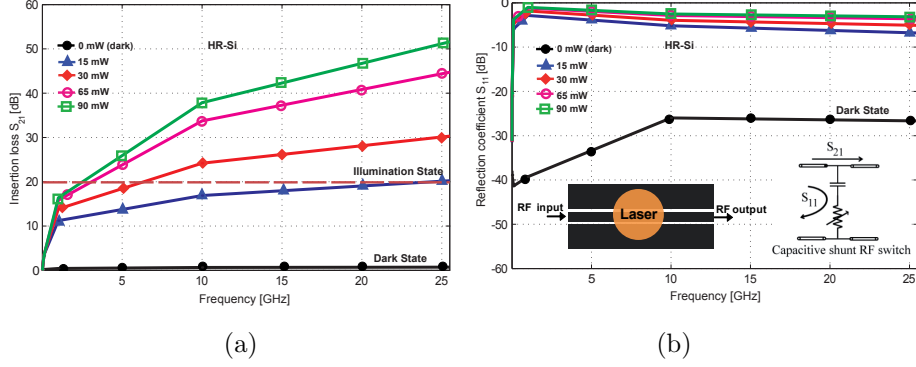


Fig. 3.3: Simulated photo-induced CPW shunt RF switch: (a) insertion loss and (b) reflection coefficient on HR-Si substrate under different illumination power levels.

as illustrated from the schematic of the measurement set-up in Fig. 3.4. When neglecting the light diffraction at the end of the fiber and taking into account the uniform distribution of the beam, the spot size attained was in the order of $400 \times 400 \mu\text{m}$. The illumination intensity is proportional to the applied output power, with a maximum of 90 mW.

The dimensions of the CPW line are the same as in the case of Atlas simulation. HR-Si substrate is used since it has been demonstrated to be an excellent substrate for the CW-mode optically controlled microwave devices with its low loss properties and its long carrier lifetime [33]. The $1 \mu\text{m}$ -thick metallic lines are isolated from the HR-Si substrate by a grown thermal oxide of 50 nm.

3.1.3.2 CPW line and substrate characterization

The characterization of CPW RF switch structure was done by measuring its S-parameters as previously mentioned. The scattering parameters allow to extract the reflection and insertion loss coefficients. Moreover, using solution of wave propagation equations and a transmission line lumped-element equivalent circuit illustrated in Fig. 3.5, electrical properties of the CPW structure and the handle substrate could be extracted. The values of L, C, R and G in the model are inductance per unit length, capacitance per unit length, resistance per unit length and conductance per unit length, respectively. The series inductance represents the self-inductance of the central conductor, C represents the shunt capacitance between conductors, R represents the conductor resistance and G represents the dielectric leakage resistance.

The differential telegraph equations [34] can be solved simultaneously giving the wave solution exponential form as follow:

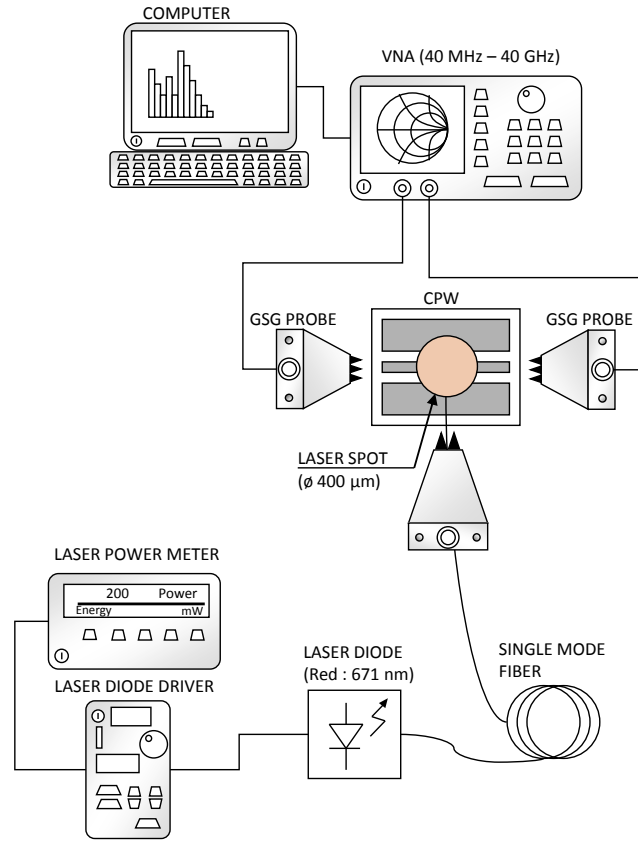


Fig. 3.4: Schematic of the measurement set-up.

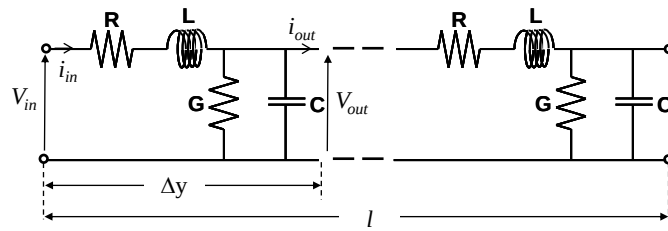


Fig. 3.5: Transmission line distributed lumped-element equivalent circuit

$$V(z) = V_{in}e^{-\gamma z} + V_{out}e^{-\gamma z}, \quad (3.7)$$

$$I(z) = I_{in}e^{-\gamma z} + I_{out}e^{-\gamma z}, \quad (3.8)$$

In the above equations the parameter with γ define the complex *propagation constant* given by:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}, \quad (3.9)$$

where α is the attenuation constant, and β is the phase constant.

From Eqs. 3.7 and 3.8 the characteristic impedance of the transmission line, Z_c , is defined as the ratio between the voltage and current from the time-domain of the differential telegraph equations for a sinusoidal steady-state condition [35]:

$$Z_c = \frac{V_{out}}{i_{out}} = \frac{V_{in}}{i_{in}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (3.10)$$

The R, L, C and G model parameters could be extracted from Eqs. 3.9 and 3.10:

$$R = \Re(\gamma Z_L), \quad (3.11)$$

$$L = \frac{\Im(\gamma Z_L)}{\omega}, \quad (3.12)$$

$$G = \Re\left(\frac{\gamma}{Z_L}\right), \quad (3.13)$$

$$C = \frac{\Im\left(\frac{\gamma}{Z_L}\right)}{\omega} \quad (3.14)$$

At high frequency approximation, (i.e when $\omega L \gg R$ and $\omega C \gg G$), the total losses seen by the transmission line are described by:

$$\alpha_{tot} = \alpha_{cond} + \alpha_{sub} \approx \frac{R}{2} \sqrt{\frac{C}{L}} + \frac{G}{2} \sqrt{\frac{L}{C}} \approx \frac{R}{2Z_c} + \frac{G}{2} Z_c \quad (3.15)$$

where α_{cond} are conductor losses due to the resistivity of the metal and α_{sub} are substrate losses due to the coupling between the line and the substrate. The propagation constant is provided from the de-embedded measured S-parameters of the CPW line, whereas the characteristic impedance is extracted based on Dehan method [36]. Base on the open-method [37] where two step calibrations are provided, on-wafer LRRM (Load-Reflect-Reflect-Much) calibration and TRL (thru-Reflect-Line), the thru is modelled by a shorter transmission line with its own characteristic impedance and propagation constant.

Effective resistivity

There are several material properties which have a major impact on the signal propagation, such as its permeability $\mu = \mu_0 \mu_r$, electrical permittivity $\varepsilon = \varepsilon_0 \varepsilon_r$

and the resistivity $\rho = \frac{1}{\sigma}$.
 where μ_0 and ε_0 are the vacuum permeability and permittivity, respectively.
 Permeability and permittivity are complex numbers and so can be written as:

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' \quad (3.16)$$

$$\mu_r = \mu_r' - j\mu_r'' \quad (3.17)$$

The real parts represents the ability of the substrate material to store electric and magnetic energy while the imaginary part represents losses. The energy loss in a dielectric medium is quantified by the loss tangent ($\tan\delta$) of the dielectric which is defined as the ratio between the imaginary and real parts of the complex permittivity expressed as:

$$\tan\delta = \frac{\omega\varepsilon_r'' + \sigma}{\omega\varepsilon_r'} \approx \frac{\sigma}{\omega\varepsilon_r'} = \frac{1}{\rho\omega\varepsilon_r'} \quad (3.18)$$

where ω is the angular frequency, σ is the electrical conductivity and ρ the electrical resistivity. A dielectric is considered lossless for $\tan\delta < 0.1$, which corresponds to an electrical resistivity of $\rho = 1.5 \text{ k}\Omega\text{-cm}$ for Si (at 1 GHz), and higher resistivity substrates with $\tan\delta < 0.03$ are required for actually wireless systems operating in the GHz range.
 For a coplanar wave guide fabricated on homogeneous dielectric with infinite thickness, the relative effective permittivity of the CPW line without conductor losses is given by:

$$\varepsilon_{r\text{eff}} = \frac{C_{CPW}}{C_{air}} = 1 + q(\varepsilon_r - 1) \quad (3.19)$$

which is the ratio of the actual CPW structure capacitance (C_{CPW}) to the capacitance when the dielectric is replaced by air (C_{air}), and q a filling factor. $q = 0$ if the CPW structure is surrounded by air, and $q = 1$ if all is dielectric. With the previously defined CPW structure dimensions we assume that the semiconductor substrate thickness sufficiently large and hence can be considered infinite. If the following condition is maintained: $h > 2(W + 2S)$, with h equal to the total substrate thickness [35], the quality factor is approximated by 0.5 and the relative effective permittivity is given by:

$$\varepsilon_{r\text{eff}} = \frac{\varepsilon_r + 1}{2} \quad (3.20)$$

Based on the measured S-parameters and once the characteristic impedance of the CPW line is known the RLCG correspondent model is then defined using Eqs. 3.11, 3.12, 3.13 and 3.14 and the substrate resistivity is expressed by [38]:

$$\rho_{sub} = \frac{1}{2} \frac{C_{air}}{\varepsilon_0} \frac{1}{G} \quad (3.21)$$

For non-homogeneous dielectrics stacked in a multilayer configuration *D.Lederer* and *J. – P.Raskin* [39] proposed a new Figure of Merit (FoM) which gives the effective resistivity of the multilayer stacked materials approximated as an homogeneous substrate that have the same losses as the investigated non-homogeneous substrate. The proposed effective resistivity expression is given by:

$$\rho_{eff} = \frac{1}{\sqrt{\varepsilon_{reff}}} \left(\frac{\varepsilon_{reff} - 1}{\varepsilon_{rsi} - 1} \right) \frac{\sqrt{C_{air}}}{\varepsilon_0} \frac{\sqrt{C_m}}{G_m}, \quad (3.22)$$

with ε_{reff} the relative effective permittivity of a CPW line on a lossless substrate extracted using analytical formulas [38].

$$\varepsilon_{reff} = \frac{C_{CPW}}{C_{air}}, \quad (3.23)$$

where C_m and G_m are the capacitance and conductance extracted from the measured propagation constant and characteristic impedance of the CPW line.

3.1.3.3 CPW RF switch measurements on HR-Si

The photo-induced insertion loss and reflection coefficient of the CPW switch on HR-Si substrate under different illumination levels are presented in Fig. 3.6 (a) and 3.6 (b), respectively. When the slots of the CPW line are illuminated with the maximum optical power of 90 mW the signal attenuation becomes in the order of 60 dB at 20 GHz. When illuminated, the dominating CPW transmission line loss is coming from the substrate conductivity going from a low to high values in the plasma region. Such behaviour is well noted by the good qualitative agreement between the simulation results presented in previous paragraph as in Fig. 3.3 (a) and the experimental results shown in Fig. 3.6 (a). At a fixed frequency of 2 GHz the insertion loss increases with the optical power intensity as can be seen in Fig. 3.7 (a). The reflection coefficient is less than -3 dB for frequencies below 5 GHz in combination with an insertion loss higher than 10 dB which means that the RF signal is mainly reflected. The switching mechanism and the influence of the frequency of the RF signal on the absorption or reflective behaviour of the switch were addressed by Roda-Neve in [30]. He demonstrated that for trap-rich HR-Si substrates the mechanism is purely reflective at 1 GHz, while being absorptive at 41 GHz.

The effective resistivity ρ_{eff} of the wafer is extracted from the measurements with the method explained in [39]. As shown in Fig. 3.7 (c), the effective resistivity decreases from 300 Ω -cm in the dark state to less than 10 Ω -cm when the switch area is illuminated with 90 mW power intensity. Such decrease of the effective resistivity corresponds the the high photo-generation rate, i.e. a highly conductive switch active area.

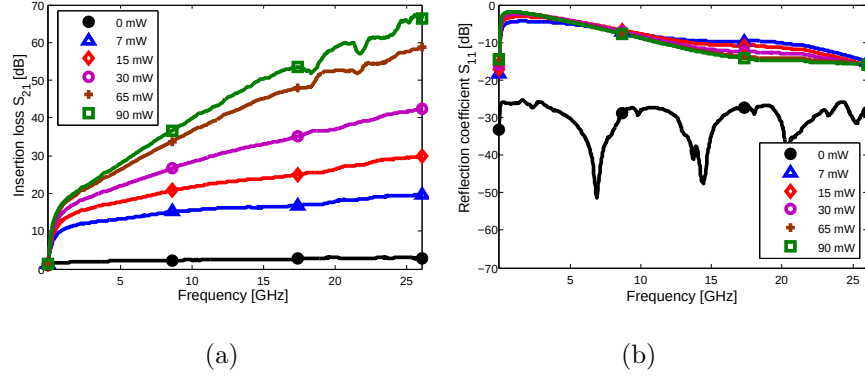


Fig. 3.6: Photo-induced CPW RF switch: measured (a) insertion loss and (b) reflection coefficient on HR-Si substrate under different illumination power levels.

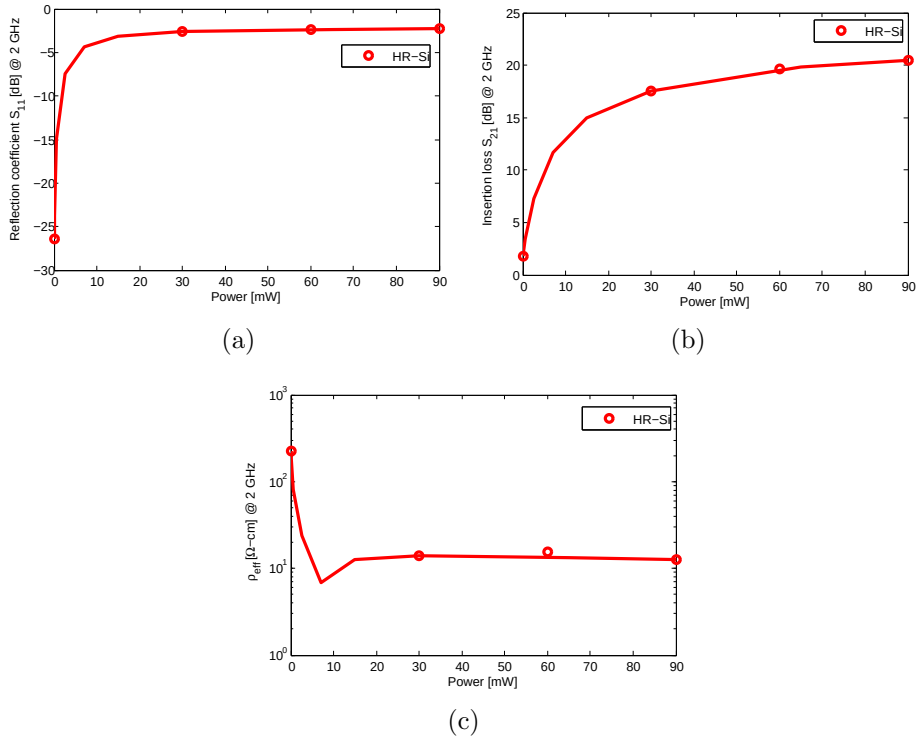


Fig. 3.7: Photo-induced CPW RF switch: measured (a) reflection coefficient, (b) insertion loss and (c) effective resistivity ρ_{eff} on HR-Si substrate @ 2 GHz under different illumination power levels.

3.2 OPTICAL CROSSTALK ISSUE

3.2.1 Optical crosstalk on HR-Si substrate

As previously explained in Section 3.1.1 the photo-induced carriers diffusion spread laterally to large area through the common substrate. These induced carriers may have a major impact on the performance of the neighbour devices. The optical crosstalk measure the variation of the insertion loss of a non-illuminated CPW line structure when its neighbour CPW RF switch is optically controlled using different illumination levels.

In our experiment, we measured the scattering parameters on a 3,385 μm -long CPW line (line B) when illuminating its neighbour line (line A). Fig. 3.8 shows the lateral diffused photo-generated carriers which alter the RF performance of the neighbour device. The attenuation along line B is presented in Fig. 3.9 for different light power levels. It shows an attenuation of more than 26 dB at 20 GHz when the spot light is 600 μm away from the measured CPW line as illustrated in the inset of Fig. 3.9.

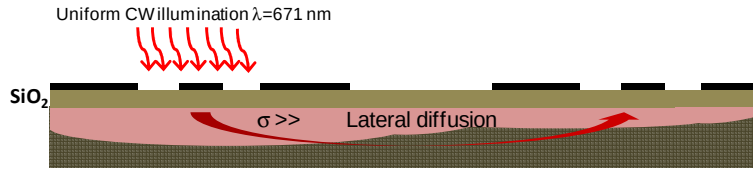


Fig. 3.8: Top view of two neighbour CPW lines lying on the same oxidized HR-Si substrate.

The attenuation is still 13.5 dB when the laser spot is put away at a distance of approximately 800 μm (approximate distance to the RF probe pads) from the CPW line victim. Fig. 3.10 (a) and (b) exhibit the insertion loss and reflection coefficient, respectively, measured on the CPW line RF switch when its neighbour device is illuminated with different power intensity at a frequency of 2 GHz, for an away distance of 600 μm and > 800 μm . It shows that increasing the distance between the two devices reduces the optical crosstalk by more than 5 dB. Moreover, the effective resistivity in Fig. 3.10 (c) doesn't show a big difference when increasing the separation distance between the optically CW-induced device and its neighbour measured line, which tells the lateral diffusion effect. It can be assumed that attenuation is not attributed only to the photo-induced plasma under the spot light but to lateral diffusion in different directions underneath the illuminated area [40]. This optical crosstalk drastically influences other components or interconnections in the neighbourhood of the optically controlled microwave device. To overcome this issue, several techniques have been proposed such as increasing the separation distance between photo-induced devices and

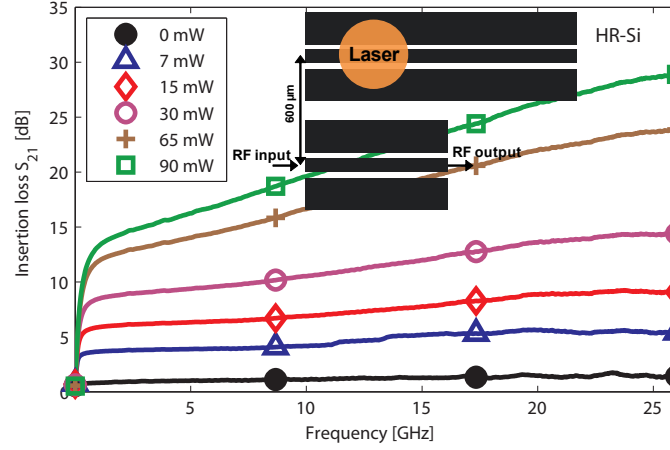


Fig. 3.9: Measured insertion loss along a CPW line 600 μm away from a photo-induced CPW RF switch illuminated under various power.

their victims [41], or using a monolithically integrated metal radiation shield [42]. However, with the downscaling of RF active and passive devices and the urgent need for compact systems a more efficient solution must be proposed.

3.2.2 Reduction of photo-induced carriers on trap-rich HR-Si

The impact of a high density of traps located at the HR-Si substrate and oxide interface on photo-induced carrier recombination has been tested by simulating the attenuation along a CPW line illuminated by various laser power levels. An undoped polysilicon layer (PolySi) of 400 nm-thick including a high density of traps sandwiched between the oxide field layer and the HR-Si substrate has been considered in Atlas simulator to model the trap-rich layer. The simulation of defect states is done by specifying the density of defect states as a combination of exponentially decaying band tail states and Gaussian distribution of midgap states. The optical properties of poly-Si differ from single crystal silicon because of grain boundaries and other structural defects. These defects can lead to states within the bandgap, which act as generation-recombination centers and absorb light with energy less than the bandgap energy. The high density of tail distributed traps ($D_{vt} = 1 \times 10^{17} \text{cm}^{-3}$) at the interface strongly increases the recombination rate of the photo-induced carriers in the Si substrate. As shown in Figs. 3.11 (a) and 3.11 (b) the attenuation and reflection coefficient of the CPW line are only weakly affected by the laser illumination, contrary to the results shown in Fig. 3.6 (a) without a trap-rich layer. It demonstrates the efficiency of an undoped poly-Si layer to vanish the impact of the photo-induced carriers on the Si substrate conductivity.

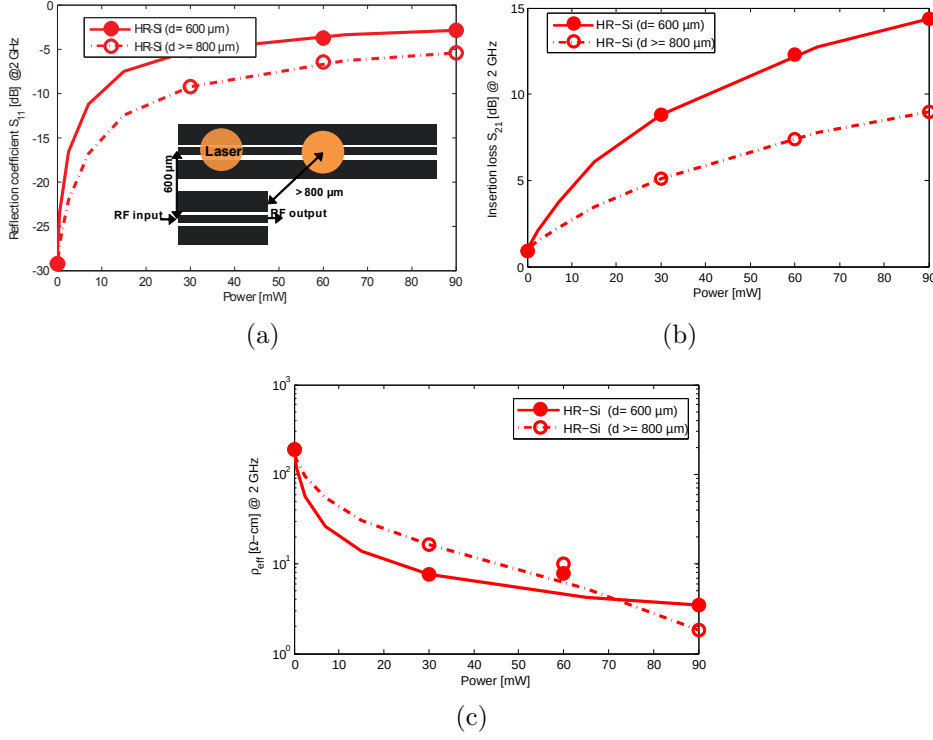


Fig. 3.10: Measured (a) reflection coefficient, (b) insertion loss and (c) effective resistivity ρ_{eff} for a 3,385 μm -long CPW line due to optical crosstalk on HR-Si substrate for different distance @ 2 GHz under different illumination power levels.

The performance of a CPW-based photo-induced switch, fabricated on HR-Si substrate and passivated with a 400 nm trap-rich LPCVD Poly-Si layer underneath a 50 nm-thick oxide layer as shown in the inset of Fig. 3.12 (b), is investigated. It has been demonstrated in [43, 44] that using a trap-rich Poly-Si passivation layer the PSC effect is reduced and the handle wafer recover its nominal intrinsic high resistivity value. In Figs. 3.12 (a) and 3.12 (b) the reflection coefficient and attenuation were measured for a 8,000 μm CPW line having the same dimensions as the simulated device and illuminated with different power intensities. It show that the efficiency of the optically controlled CPW switch is reduced giving a S_{21} value less than 8 dB when illuminated with 90 mW at 20 GHz. The significant reduction of the photoconductivity effect on trap-rich Poly-Si HR-Si substrate is related to the trapping of the photo-induced carriers.

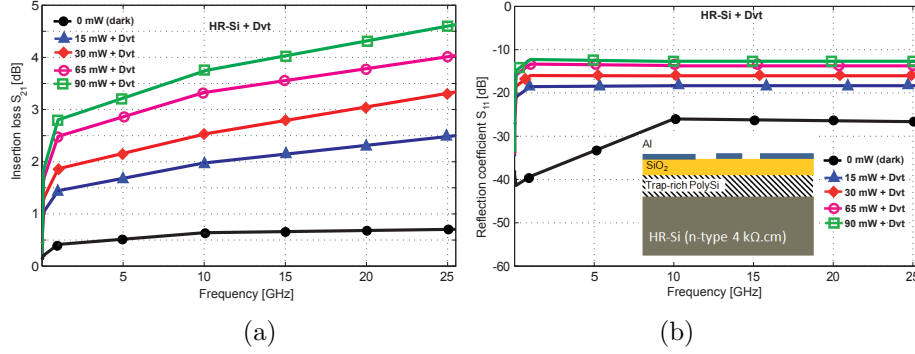


Fig. 3.11: Simulated (a) insertion loss and (b) reflection coefficient of a photo-induced CPW RF switch on HR-Si substrate with high density of volume traps ($D_{vt} = 1 \times 10^{17} \text{ cm}^{-3}$) in an undoped polysilicon layer under different illumination power levels.

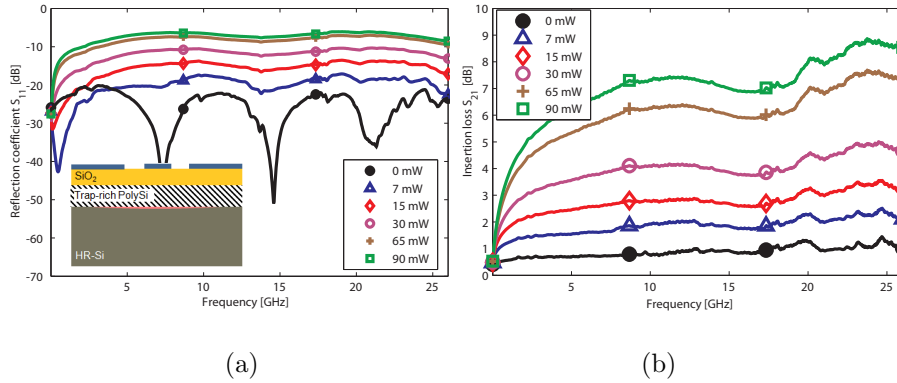


Fig. 3.12: Photo-induced CPW RF switch: measured (a) reflection coefficient and (b) insertion loss on trap-rich HR-Si substrate under different illumination power levels.

Moreover, as expected, the reduction of the optical crosstalk due to the lateral carrier diffusion on trap-rich HR-Si substrate is fully achieved as shown in Figs. 3.13 (a) and 3.13 (b) where almost all the impact of illumination has vanished due to the high density of traps in the passivation polysilicon layer. The measured attenuation values are lower than 0.5 dB at 20 GHz as shown in Fig. 3.13 (b). The trap-rich layer has efficiently absorbed the photo-induced carriers and the CPW line behaves like a non-illuminated device at the maximum optical power intensity (90 mW). Therefore, this technological solution has a great interest to reduce the optical crosstalk between devices lying on the same chip. However, as demonstrated in Fig. 3.12 (b), a trap-rich layer totally reduces the efficiency of

the photo-induced switch and the behaviour of any optically controlled devices on such trap-rich HR-Si substrate. The trap-rich poly-Si material should be etched only from the restricted photoconductive area of the CPW photo-induced switch. A proposed new design was previously developed in [44] which limits the substrate illuminated surface so as to have a higher photoconductivity in a restricted zone and reduced lateral diffusion otherwise using a high traps density outside the switch area as show in Fig. 3.14.

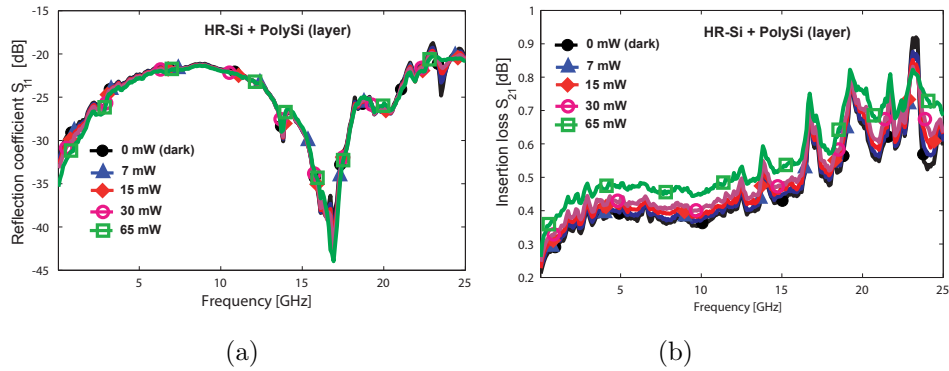


Fig. 3.13: Measured (a) reflection coefficient and (b) insertion loss along a CPW line 600 μm away from a photo-induced CPW RF switch on trap-rich HR-Si substrate illuminated under various power levels.

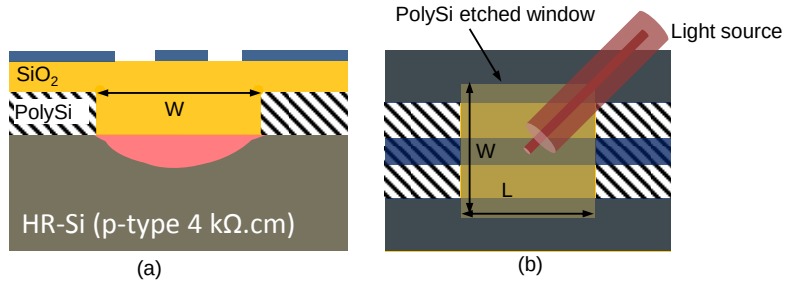


Fig. 3.14: Optically controlled CPW RF switch on trap-rich HR-Si (a) Cross section and (b) top view.

3.3 NEW DESIGNED CPW PHOTO-INDUCED SWITCH ON TRAP-RICH HR-SI WAFER

3.3.1 Fabrication process

An optimal design was developed in [44] where the photo-induced plasma will be restricted to a limited area as shown in Fig. 3.14. It consists of a CPW line on top of oxidized HR-Si substrate with trap-rich passivation layer which locally etched away in the active photo-induced optically controlled switch. A 525 μm -thick HR-Si substrate (4 $\text{k}\Omega\text{-cm}$) is used for each sample. The trap-rich layer surrounds the active area of each CPW RF switch. Different dimensions of the switch lateral active area are investigated ; i.e. the area where the trap-rich layer is excluded. A high quality HR-Si / oxide interface in the active region of the switch is required to conserve weak surface recombination and thus assure a high photo-induced surface conductivity. To avoid the degradation of the interface between the HR-Si substrate and the oxide insulating layer during the local removal of the PolySi layer as experienced in [41],[45] , a first 50 nm-thick oxide layer is thermally grown on top of the HR-Si substrate as presented in the process steps in Fig. 3.15 (a) and patterned to only cover the active region of the switch (Fig. 3.15 (b)). A 400 nm-thick polysilicon layer (PolySi) with a typical columnar structure [46] is deposited by low-pressure chemical vapor deposition (LPCVD) as shown in Fig. 3.15 (c). Patterning of PolySi layer by reactive ion etch with SiCl_4 is made to define the restricted switch active area 3.15 (d). A TMAH etching technique was used in [44] to remove the poly-Si material from active area window, but such technique introduces defaults at the Si surface which act as traps for the photo-induced carriers. The proposed dry etching method will limit the etching poly-Si windows without degrading the performance of the HR-Si substrate. A second 50 nm-thick thermal oxide is grown all over the wafer as in Fig. 3.15 (e) for the isolation of CPW line from the Si substrate. Front-side 1 μm -thick aluminum is evaporated in e-gun vacuum system and patterned to define the final CPW structure shown in Fig. 3.15 (f). The designed window dimensions in the PolySi layer must be determined to reach the highest CPW RF switch performance at the lowest optical power level and at the same time guarantee a drastic reduction of the optical crosstalk with the neighbour RF switches, interconnections and other integrated devices.

3.3.2 Optically controlled CPW RF switch and crosstalk reduction on trap-rich HR-Si substrate

By locally removing the trap-rich layer in a known volume, a reduction of transmission RF losses and optical crosstalk is assured without degrading the performance of the optically controlled CPW RF switch. Regarding the photo-induced switch performance for different active area dimensions, it was observed that increasing the switch area increases the photo-induced attenuation as developed in [47]. The attenuation and reflection coefficient of the RF switch

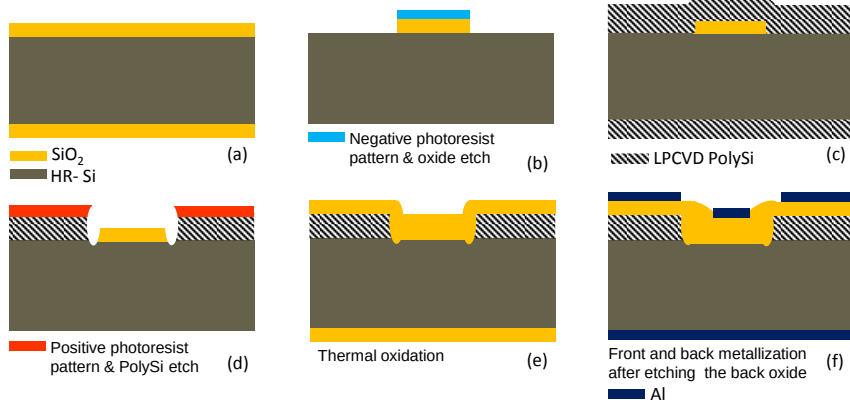


Fig. 3.15: Process steps for trap-rich HR-Si optically controlled CPW RF switch.

of active area of $400 \times 400 \mu\text{m}$ (etched PolySi window which corresponds to the total laser spot size giving the maximum illuminated semiconductor surface) are presented in Figs. 3.16 (a) and (b), respectively. An attenuation of 22 dB at 20 GHz for an optical power of 90 mW is achieved. This value can be compared with the 55 dB attenuation in the case of RF switch built on top of a HR-Si substrate presented in Fig. 3.6 (a). The reduced switching efficiency of the RF switch lying on a locally passivated trap-rich PolySi layer HR-Si substrate is directly related to the restricted active area of the RF switch, i.e. $400 \times 400 \mu\text{m}$.

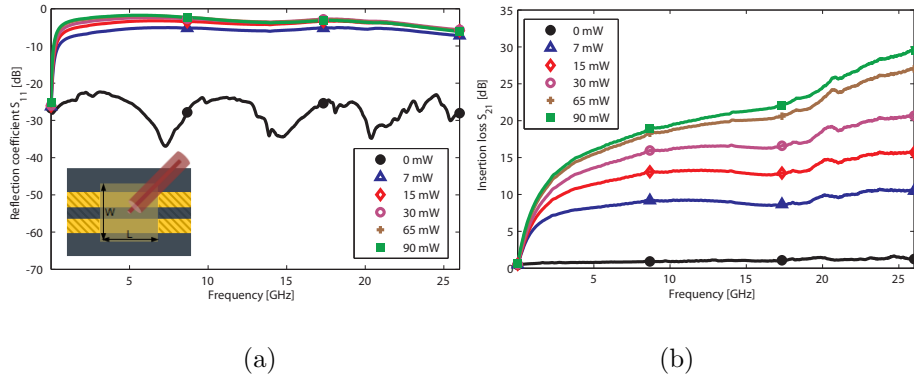


Fig. 3.16: Measured (a) reflection coefficient and (b) insertion loss of a Photo-induced CPW RF switch with etched trap-rich window on HR-Si substrate under different illumination power levels.

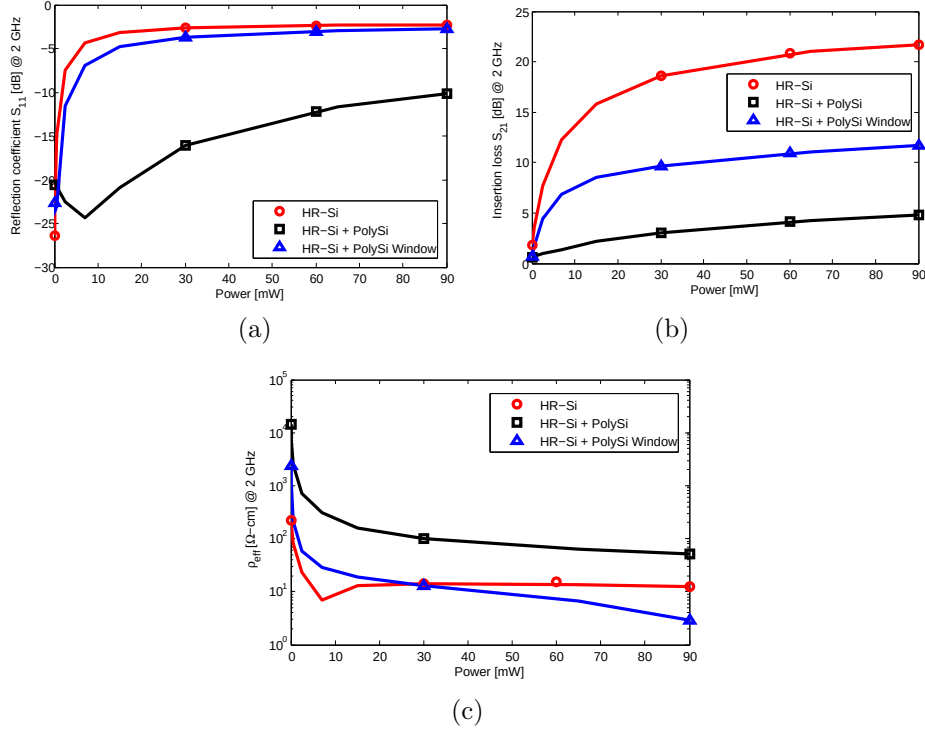


Fig. 3.17: Measured (a) reflection coefficient, (b) insertion loss and (c) effective resistivity ρ_{eff} on HR-Si, trap-rich HR-Si and etched window trap-rich HR-Si substrates @ 2 GHz under different illumination power levels.

Measurements of the reflection coefficient and insertion loss in Figs. 3.17 (a) and (b) respectively, compare the efficiency of the photo-induced optically controlled switch on three different wafers. As depicted in Fig. 3.17 (b) the high density of traps reduces the photoconductivity effect on HR-Si trap-rich poly-Si, whereas the photo-induced switch performance increases using a designed etched window (HR-Si poly-Si window) and on HR-Si substrates, reaching almost 12 dB and 25 dB at 2 GHz, respectively. The extracted effective resistivity ρ_{eff} over the optical power intensity at a fixed frequency of 2 GHz in Fig. 3.17 (c) decreases to values lower than 10 Ω -cm on HR-Si and HR-Si poly-Si window at the highest 90 mW power intensity.

The dimension of the etched window must be determined in order to maintain the efficiency of the switch at the lowest optical power intensity and reduced optical crosstalk level. As simulated in [44] to increase the switch efficiency it is necessary either to increase the power density or the illuminated switch

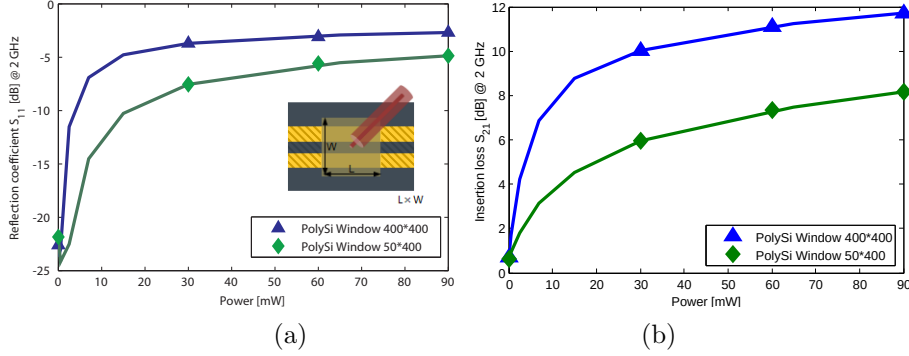


Fig. 3.18: Optically controlled CPW RF switch measured (a) reflection coefficient and (b) insertion loss @ 2 GHz for different windows dimension on trap-rich HR-Si.

area. Fig. 3.18 (a) and (b) compare the reflection coefficient and insertion loss, respectively for two investigated window dimensions. The lateral switch area of $400 \times 400 \mu\text{m}$ shows higher attenuation level compared to a window of $50 \times 400 \mu\text{m}$.

The photo-generation is mainly confined to the active area of the CPW switch (the etched window in the PolySi layer) and the lateral diffusion of photo-induced carriers is drastically reduced due to the high recombination rate in the trap-rich PolySi layer.

An efficient optical crosstalk reduction is reached with the designed structure without degrading the efficiency of the optically controlled CPW RF switch comparing with results in [40] where TMAH etching technique introduces traps on the HR-Si surface and thus degrades the optical switch performance. The reflection coefficient and attenuation values presented in Figs. 3.19 (a) and 3.19 (b), respectively, are measured on a CPW line spaced by $600 \mu\text{m}$ from the active area of neighbour illuminated RF switch. An optical reduction of more than 25 dB is achieved at a power illumination of 90 mW when comparing the attenuation values on HR-Si substrate in Fig. 3.9 and RF switch surrounded by a trap-rich layer in Fig. 3.19 (b).

The variation of the reflection coefficient and insertion loss over the optical power intensity is plotted in Fig. 3.20 (a) and (b), respectively, for a two separation distance of $600 \mu\text{m}$ and $d > 800 \mu\text{m}$. Even increasing the separation distance between the optically controlled devices and its neighbours, the optical coupling on HR-Si substrate still at higher level in particular cases when considering the co-integration of CMOS miniature devices. The trap-rich technological solution with a designed windows to restrict the photo-induced switch area provides better optical isolation and could be considered as promote substrate for the

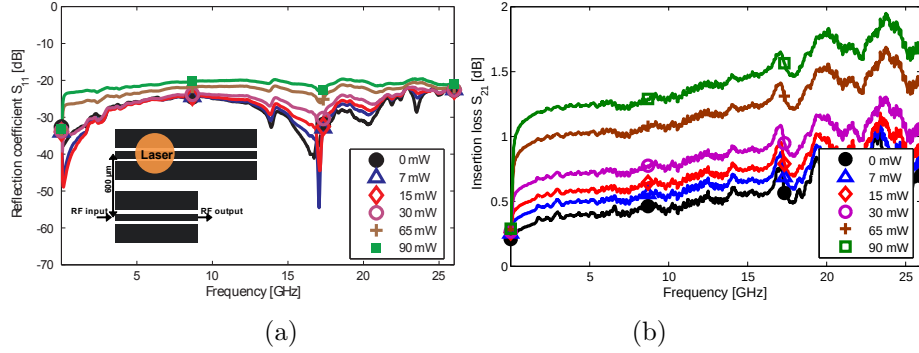


Fig. 3.19: Measured CPW line (a) reflection coefficient and (b) insertion loss on trap-rich HR-Si substrate when a neighbour optically controlled RF CPW switch is illuminated at different power levels.

co-integration of RF CMOS and optically controlled devices on the same chip.

3.4 SUBSTRATE NON LINEAR CHARACTERIZATION USING CPW LINE STRUCTURE

Radio-frequency characterization of passive devices is provided using small-signal measurement setup with an input power of 0 dB. However, as previously investigated by Roda-Neve [44] oxidized HR-Si substrate electrical properties are highly dependent on the applied bias voltage which have a major impact on the charge distribution inside the substrate and thus on its resistivity profile. Based on the variation of the substrate electrical properties with time due to either voltage biasing or a large-signal operation, the RF device behaviour is then consider non-linear. Using a large-signal Network analyzer a characterization setup was used to measure the amplitude and phase of the generated harmonics of the transmitted and reflected waves [9].

The measurements of RF components non-linearity behaviour such as RF switches, passive or active devices under a large signal operation have been developed using a commonly FoM which expect the total harmonic distortion (THD) and inter-modulation distortion (IMD) [48]. Base on a 4-port Agilent PNA-X vector network analyze (VNA) on-wafer non-linear characterization setup was implemented by Roda-Neve [44] using adapted measurement equipments to accurately measure the generation of harmonics due to HR-Si substrate non-linearity behaviour [10]. A large 900 MHz signal (which correspond to GSM fundamental frequency) with input power ranging from -25 to 15 dBm was used as the fundamental tone injected in the input of the CPW line. The frequency spectrum in Fig. 3.21 shows two harmonic components added to the fundamental tone. The

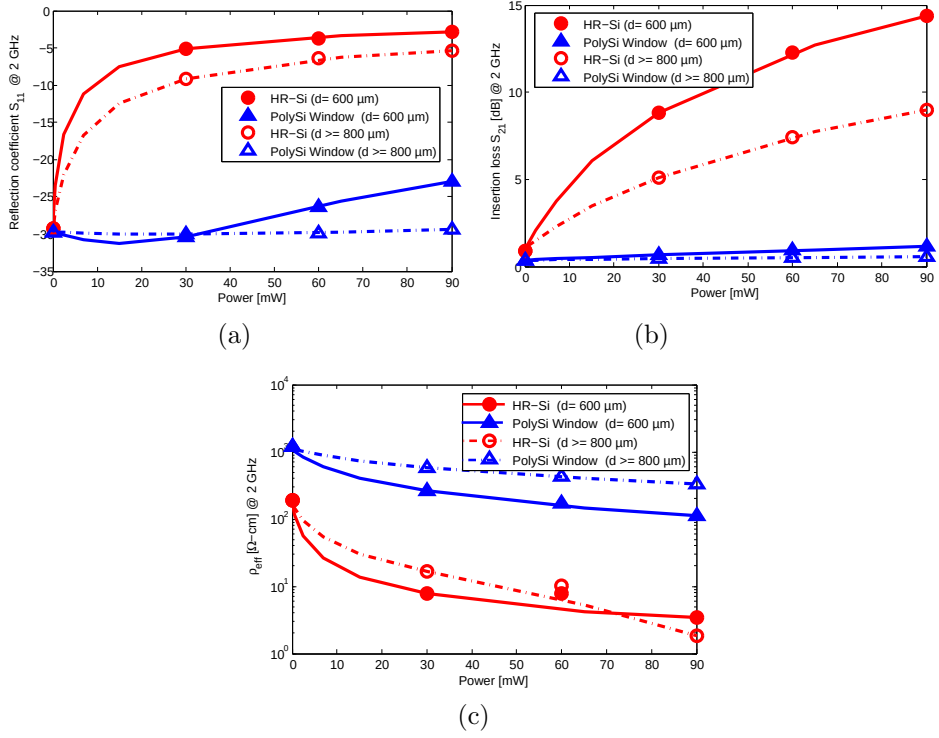


Fig. 3.20: Measured (a) reflection coefficient, (b) insertion loss and (c) effective resistivity ρ_{eff} for a 3,385 μm -long CPW line on HR-Si and etched trap-rich window substrates for different distance @ 2 GHz under different illumination power levels.

output power of each frequency component was measured when a 50Ω load is placed at the correspondent output port. The distortion level is quantified using a total harmonic distortion (THD) which is equal to the ratio between the integrated power of all harmonics and the measured power at the fundamental tone. If the harmonic level of a certain frequency is at least 10 dB higher than the others, THD can be approximated by the output level of such harmonic order. Such is the case of the measured non-linearities coming from the substrate where the 2^{nd} harmonic distortion level is the highest.

In this section we used a non-linearity characterization setup where the PNA-X configuration allows to measure, at the same time, the harmonic distortion and the S-parameters of the CPW lines under different illumination power levels as shown in Fig. 3.22.

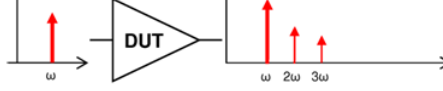


Fig. 3.21: Frequency spectrum of a non-linear system for a one tone input signal.

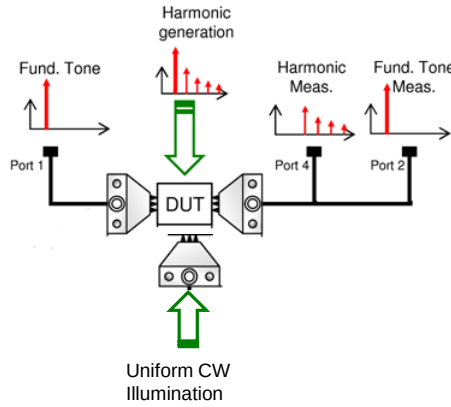


Fig. 3.22: Schematic of harmonic distortion characterization setup under different illumination levels.

3.4.1 Substrate non-linearity of a CPW RF switch at the dark state

The non-linear performance of HR-Si, HR-Si + PolySi and HR-Si + Window polySi substrate were measured for a 871 μm -length CPW line and Fig. 3.23 shows the 2nd and 3rd harmonic distortion levels without illumination (dark state). CPW line on oxidized HR-Si wafer present a significant harmonic distortion levels of -60 dBm at an input power level of 15 dBm. The distortion is mainly governed by the 2nd harmonic component at 1.8 GHz. The harmonic distortion specifications for RF switches is approximated to -70 dBc at an input power of 35 dBm [49, 50]. Therefore, the HR-Si substrate is not suited for the fabrication of RF switches, non-linear RF devices and circuits (PA, LNA, ...) with low harmonics specifications.

The substrate non-linearity measured on HR-Si + PolySi substrate is only -95 dBm at an input power of 15 dBm, more than 35 dB lower than its initial HR-Si wafer without trap-rich passivation layer and lower than RF switches specification by more than 20 dB.

The proposed configuration for the CPW RF switch with the etched polySi window at the active photo-induced region show a reduction of harmonic distortion by more than 10 dB compare to CPW RF switch on HR-Si as depicted in Fig. 3.23. Such non-linearity level is high enough to introduce more

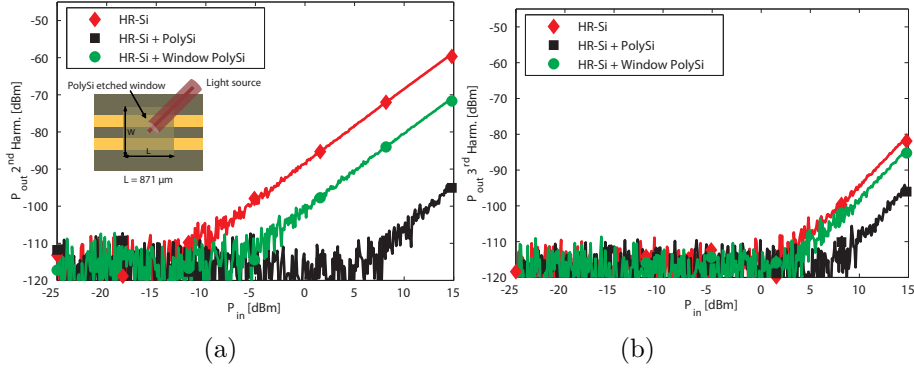


Fig. 3.23: Measured (a) 2^{nd} and (b) 3^{rd} harmonic distortion of a $871 \mu\text{m}$ -length CPW line on HR-Si, HR-Si + PolySi and HR-Si + Window PolySi substrates at the dark state.

non-linearity behaviour coming only from the substrate.

3.4.2 Substrate non-linearity of a CPW RF switch under different illumination levels

Regarding the non-linearity behaviour on the investigated substrate under different illumination levels, Fig. 3.24 illustrates the measured 2^{nd} and 3^{rd} harmonic distortions due to the optical crosstalk on HR-Si handle substrate. The input large-signal was injected at the input of a CPW RF switch ($871 \mu\text{m}$ -length) when its neighbour was illuminated ($1571 \mu\text{m}$ -length) with different power levels. The distance between the two CPW line structures is approximated to $700 \mu\text{m}$. It can be observed that the 2^{nd} HD on oxidized HR-Si wafer is sufficiently high and illumination effect does not add more non-linearity.

Using a passivation polysilicon layer underneath the oxide layer, the high density of traps literally capture the photogenerated carriers. Although, it increases with the illumination power, the 2^{nd} harmonic distortion level remains below -70 dBm at the maximum power intensity of 90 mW as depicted in Fig. 3.24 (a). However, for the CPW RF switch configuration with an etched polySi window the substrate non-linearity increases with illumination and it becomes as high as that on oxidized HR-Si wafer as seen in Fig. 3.26 (a).

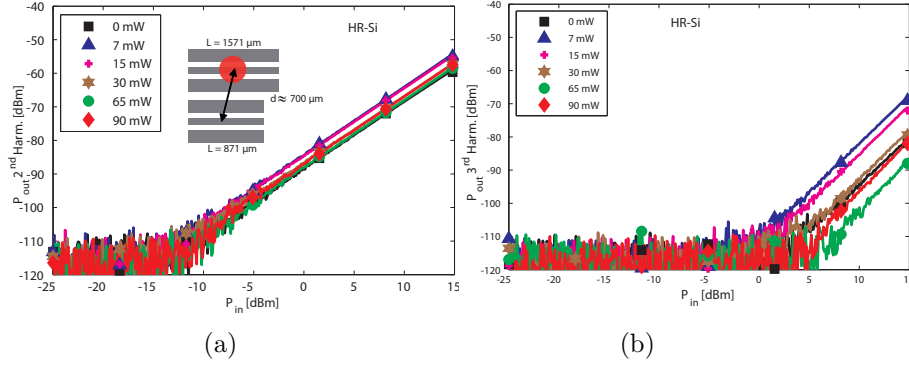


Fig. 3.24: Measured (a) 2^{nd} and (b) 3^{rd} harmonic distortion of a $871 \mu\text{m}$ -long CPW line on HR-Si substrate at different illumination levels.

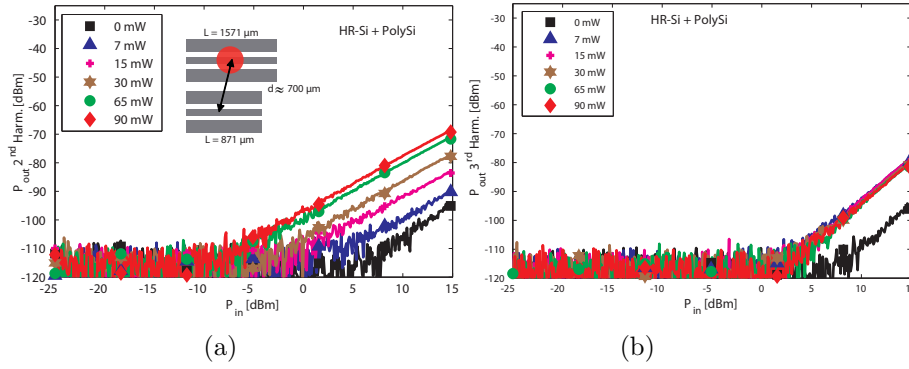


Fig. 3.25: Measured (a) 2^{nd} and (b) 3^{rd} harmonic distortion of a $871 \mu\text{m}$ -long CPW line on HR-Si + PolySi substrate at different illumination levels.

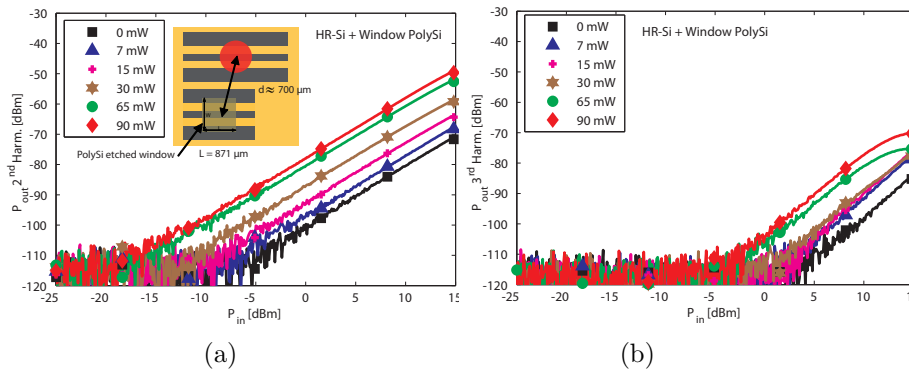


Fig. 3.26: Measured (a) 2^{nd} and (b) 3^{rd} harmonic distortion of a $871 \mu\text{m}$ -long CPW line on HR-Si + Window PolySi substrate at different illumination levels.

3.5 CONCLUSION

In this chapter we have investigated the performance of CW-mode optically controlled microwave switch on silicon substrate. The main advantages of this optically controlled device are i) a low optical control power ii) simplicity of fabrication and compatibility with standard CMOS process iii) inherent isolation between control and driven signals. For all these reasons, this opto-microwave CPW RF switch may find applications in tunable RF devices and circuits such as tunable filters, reconfigurable antennas. The designed CPW RF switches on HR-Si substrate with and without etched polySi window provide higher switching efficiency at low optical power at a frequency of 20 GHz compare with Canseliet et al. [26] as depicted in table 3.1. Although, the implemented switches on HR-Si substrate show good switching efficiency but they suffer from the spread of the photo-generated excess carriers over a large distance which drastically influences the behaviour and performance of neighbour interconnections and devices. By introducing a trap-rich polysilicon layer sandwiched between the oxide layer and the HR-Si substrate, it has been found that the optical crosstalk is drastically reduced thanks to the high recombination rate in the PolySi layer. A well-controlled process was developed to locally etch the polysilicon window. Depending on the application, the dimensions of the trap-rich free area; i.e. where a highly photo-conductive region is wanted, must be optimized in order to assure the good performance of the optically controlled RF device under low optical power and simultaneously minimize the optical crosstalk between the different components of an integrated System-on-Chip (SoC).

Using the effective resistivity and harmonic distortions FoMs it was demonstrated that the passivated trap-rich HR-Si substrate allows to recovers the high resistivity properties of oxidized HR-Si wafer and reduces its non-linear behaviour by more than 50 %. The new designed CPW RF switch with a locally etched polySi window reduces the optical crosstalk as well as the non-linearity coming from the substrate thanks to the trap-rich layer.

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CHAPTER 4

SOI CMOS TECHNOLOGY ON COMMERCIAL 200 MM TR-SOI SUBSTRATES: RF PERFORMANCE AND DIGITAL SUBSTRATE NOISE

HR-SOI substrate is today considered as the mainstream technology option for the integration of RF System-on-Chip (SoC) due to its capability to deliver very competitive performance while offering great flexibility to integrate more functionality and providing lower cost solution compared with GaAs PHEMT and SOS technologies. Recent studies have reported the integration of antenna switches [1–3] and power amplifiers [4] on HR-SOI substrate. It was also shown that the availability of high performances passive components enables the integration of filters and diplexers which are massively used in multi-standard RF front end modules [5]. Even though HR-SOI substrate meets most of the requirements for the integration of RF front-end modules, it is known that it suffers from surface conduction effect underneath the BOX and degradation of its nominal resistivity. It has been previously shown using coplanar wave-guides (CPWs) that the transverse electric field through the SiO_2/Si interface induces a surface carrier channel of accumulation or an inversion highly conductive layer [6, 7]. Such parasitic surface conduction (PSC) effect reduces the effective resistivity of HR-Si handle wafer by more than one order of magnitude [8], increases substrate RF losses and crosstalk [9]. In addition, the non-linear behaviour of HR-Si substrate increases due to PSC effect and the generated harmonics by the passive components can have higher power levels than those from RF switches or other active devices fabricated on HR-SOI [10]. Various

technological solutions have been developed to reduce these parasitic effects and enhance the HR properties of the Si substrate. The introduction of a trap-rich layer has been proved as the most effective technique while being compatible with industrial SOI wafer fabrication and with the important thermal budget of standard CMOS process [9]. The numerous traps created by silicon dangling bonds in the trap-rich layer capture the free carriers at the SiO_2/Si interface, thereby enabling the substrate to recover its nominal resistivity, linearity, eliminating the DC dependency [10, 11], and leading to a substantial reduction of RF losses and crosstalk [12]. In this chapter we investigate the static and RF performances of passive and active fully-depleted (FD) SOI MOSFETs fabricated using a standard CMOS process on top of either HR-SOI or TR-SOI UNIBOND wafer both provided by Soitec. Fig. 4.1 shows an image of the 200 mm $\varnothing$ processed SOI wafer where it highlights the designed passive (CPW lines and crosstalk structure) and active devices (FD SOI MOSFET's). The RF losses and substrate non-linearity are analyzed using CPWs lines and crosstalk structures. DC and RF performances of FD SOI MOSFET and the digital substrate noise effect on RF performance of the measured transistors are investigated when a digital noise signal is injected in its vicinity.

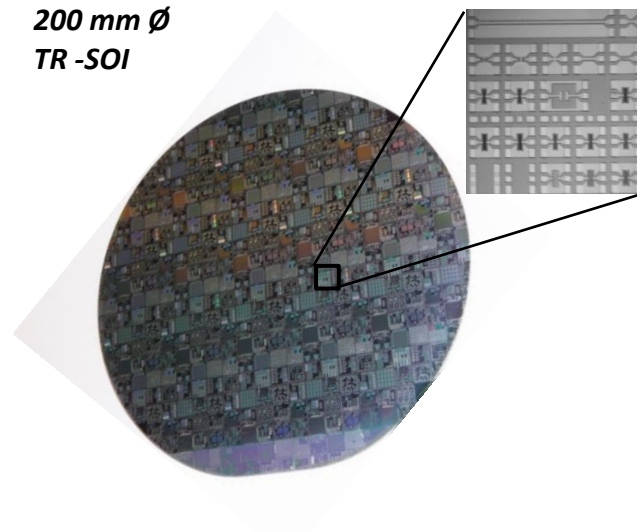


Fig. 4.1: Image of the processed SOI wafer: highlight characterized passive and active devices.

4.1 RF PERFORMANCE OF CPW LINES AND INDUCTORS ON TR-SOI

4.1.1 CPW Line RF Performance on commercial TR-SOI wafers

The passivation efficiency of trap-rich TR-SOI substrates was investigated on commercial 200 mm HR-SOI wafers for passive and active devices fabricated using a standard SOI CMOS process [13]. A coplanar waveguide structure is used to investigate RF substrate losses and non-linearity behaviour. Indeed, among the integrated passive elements, coplanar structures are quite sensitive to substrate effects at the SiO_2/Si interface [14]. The cross section of the CPW line on HR-SOI and TR-SOI substrates are illustrated in Fig. 4.2. Its dimensions are $38\ \mu m$ (Wc), $18\ (S)$, $213\ (Wg)$ for, respectively, the width of the central conductor, the slot space and the planar ground planes.

On-wafer small- and large-signal measurements of the CPW line were per-

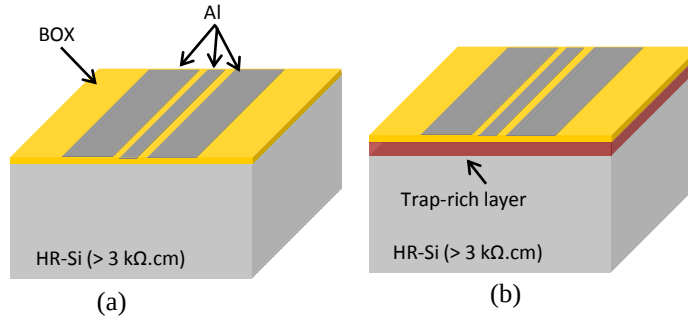


Fig. 4.2: Cross-section of CPW line on (a) HR-SOI and (b) TR-SOI substrates.

formed using a dedicated setup [10] based in an Agilent 4 Ports PNA-X vector network analyzer. The RF measurements were carried up to 10 GHz and the RF substrate losses as well as the effective resistivity (ρ_{eff}) of the wafers were extracted from the measured S-parameters using the method depicted in [8]. CPW lines on TR-SOI wafers present extremely low attenuation level (< 0.2 dB/mm) being close to those of CPW made on SOS or quartz, where losses are mainly governed by conductor losses as presented in [15]. Fig. 4.3 shows the excellent RF lossless TR-SOI compared with HR-SOI and quartz handle wafers. In fact, the extracted effective resistivity in Fig. 4.4 confirms the true high resistivity ($> 3\ k\Omega.cm$) up to 5 GHz of the wafer compared with only $200\ \Omega.cm$ for the oxidized HR-SOI substrate. A degradation of ρ_{eff} (4 times lower) was observed for the HR-SOI wafer after CMOS process. When we talk about CMOS process, we refer to the different classical fabrication steps for building up a MOS transistor such as gate oxide growth, ion implantation to define the doping profile of the channel, gate material deposition and patterning, source

and drain implantation, the different metallization steps, etc. These different steps introduce a thermal budget which could affect the carrier distribution in the TR-SOI and HR-SOI wafers, the traps density and defects at the different interfaces, etc. The extracted effective resistivity in Fig. 4.4 show that the introduced trap-rich layer (TR SOI wafer) underneath the oxide layer stabilizes the whole wafer and almost no variation is measured for the extracted effective resistivity for the TR SOI wafer before and after CMOS process. Whereas we can observe a clear reduction of the extracted effective resistivity after CMOS processing for the HR SOI wafers. The droop and overshoot around 3 GHz is mainly related to error of probing contact on that device. Such low effective resistivity of HR-SOI without the trap-rich passivation layer is explained by the presence of a highly conductive inversion layer underneath the oxide layer.

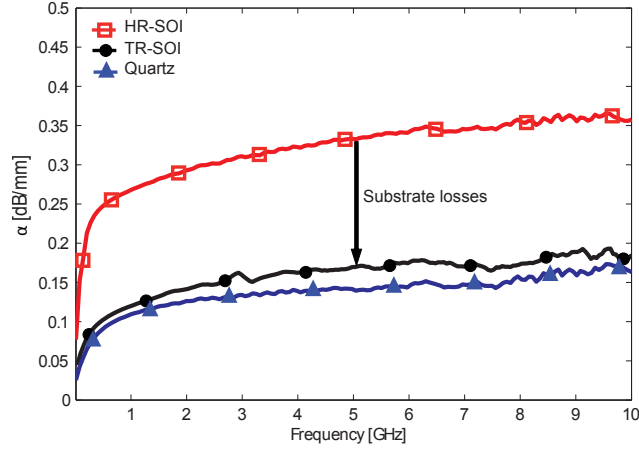


Fig. 4.3: Measured Attenuation vs. frequency of a CPW line on HR-SOI, TR-SOI and quartz substrates.

Regarding their linear behaviour, the 2^{nd} and 3^{rd} harmonics of a 900 MHz fundamental signal with an input power of +25 dBm at the output of a 2,000 μm -long CPW line on both HR-SOI and TR-SOI substrates are shown in Fig. 4.5. The non-linear distortion phenomena seen in microwave devices and circuits is mainly quantified using the total harmonic distortion (THD FoM) figure of merit, which is defined as the ratio of the total output powers of all generated harmonics to the measured power at the fundamental frequency. The THD can be approximated to the harmonic distortion level 10 dB higher to the other frequency generated harmonics, As explained in Section 3.4.

A reduction by more than 25 and 35 dB is depicted on TR-SOI for respectively, the 2^{nd} and 3^{rd} distortion levels. The HR-SOI non-linear behaviour is mainly due to the modulated charge density at the SiO_2/Si interface. The parasitic surface

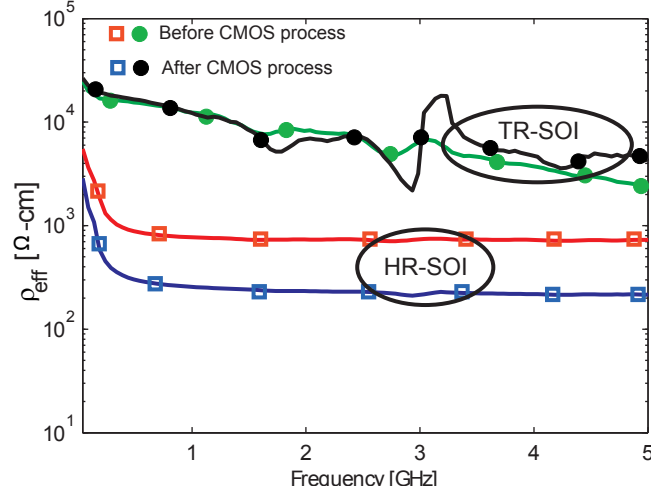


Fig. 4.4: Measured Effective resistivity on HR-SOI and TR-SOI before and after CMOS process.

electron inversion layer change the distribution of free carriers inside the silicon substrate, thereby modulate its correspondent non-linear capacitance and conductance [16]. The handle wafer becomes highly dependent on bias voltages [11] applied on the CPW lines. The DC voltage changes the carrier's distribution at the SiO_2/Si interface and thus modulates the effective resistivity of the substrate and increases the harmonic levels. With a trap-rich layer underneath the oxide a total independence from DC applied voltage is achieved as previously investigated in [10, 11], it corresponds to an ideal HR-SOI substrate, i.e. not suffering from the parasitic surface conduction effect. The high ρ_{eff} and linear behaviour of the TR-SOI wafer makes it a viable substrate solution for RF integrated SoC applications.

4.1.2 Inductors on TR-SOI

Passive elements such as inductors, capacitors and interconnection transmission lines, cover a large area on the chip of the front-end modules (FEM). The performance of the latter is highly affected by their correspondent quality factors, RF losses and linearity which are key factors for the whole system. The focus is put on high quality on-chip inductors as they are critical components and widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers and low noise amplifiers. Therefore, there is an increasing demand to design high quality factor inductors to minimize RF power loss, phase noise and DC power consumption.

In this research high quality factor inductors were fabricated on HR-Si wafers

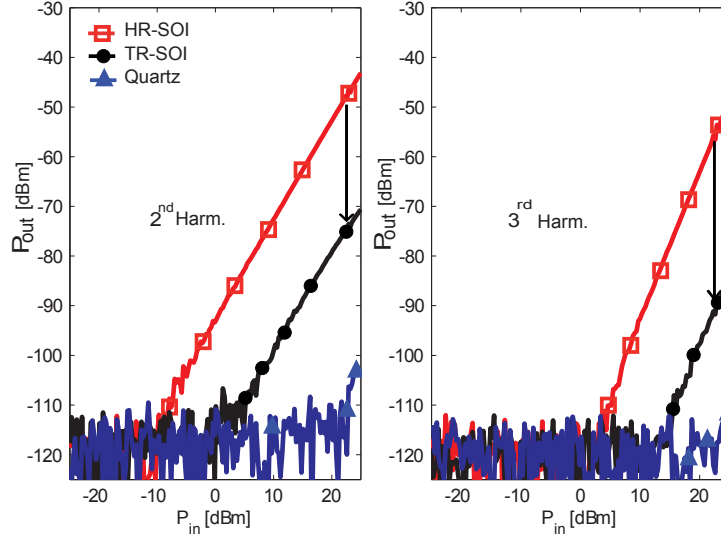


Fig. 4.5: Measured 2nd and 3rd harmonic power levels of a CPW line on HR-SOI, TR-SOI and quartz substrates.

with and without a passivation trap-rich layer using a multimetal surface micro-machining process at the University of Michigan [17]. The detailed specifications of each substrate are outlined in table 4.1. Trap-rich polysilicon (PolySi) and amorphous layers (α -Si) were deposited by LPCVD deposition technique on a HR-Si 10 k Ω .cm (TR-10k) at 625 °C and HR-Si 4 k Ω .cm (TR-4k) at 525 °C, respectively. The α -Si layer was then crystallized using rapid thermal annealing (RTA) at 900 °C for 120 s. On all wafers, a 150 nm-thick thermal oxide layer was grown at 950 °C partially consuming the trap-rich layer. The resulting passivation layer thickness is 330 and 360 nm for TR-10k (PSi) and TR-4k (α -Si), respectively.

The designed inductors involve two thick electroplated metal layers as described by the process flow in Fig. 4.6. A 5 μ m Au and a 35 μ m-thick Cu stacked structural and underpass metal layers were used to further reduce conductor losses (highest Q at the inductor operating frequency), and thus observe the effect the trap-rich layer.

The impact of the passivation polysilicon layer on the Q factor and non-linear behaviour of 2 nH single-turn circular inductor is investigated. The inductor is designed to have its peak Q at frequency beyond 2.5 GHz as shown in Fig. 4.7 (a) with the dimension depicted in its inset. The measurement results on the trap-rich HR-Si in Fig. 4.7 (b) show a much higher Q compared with the standard HR-Si when a thick Cu layer is used. The maximum Q on 10 k Ω .cm trap-rich HR-Si is more than 60 at 2.73 GHz while it is only 35 at 1 GHz on standard

Wafers	Thermal oxide : t_{SiO_2} (nm)	Trap-rich		Si		
		Type	Thickness (nm)	Type	Thickness (μm)	ρ ($\Omega\cdot\text{cm}$)
HR-4k	150			P	725	> 4 k
HR-10k	150			N	725	> 10 k
TR-4k	150	LPCVD α -Si	360	P	725	> 4 k
TR-10k	150	LPCVD PolySi	330	N	725	> 10 k

Table 4.1.: HR-Si substrates specifications.

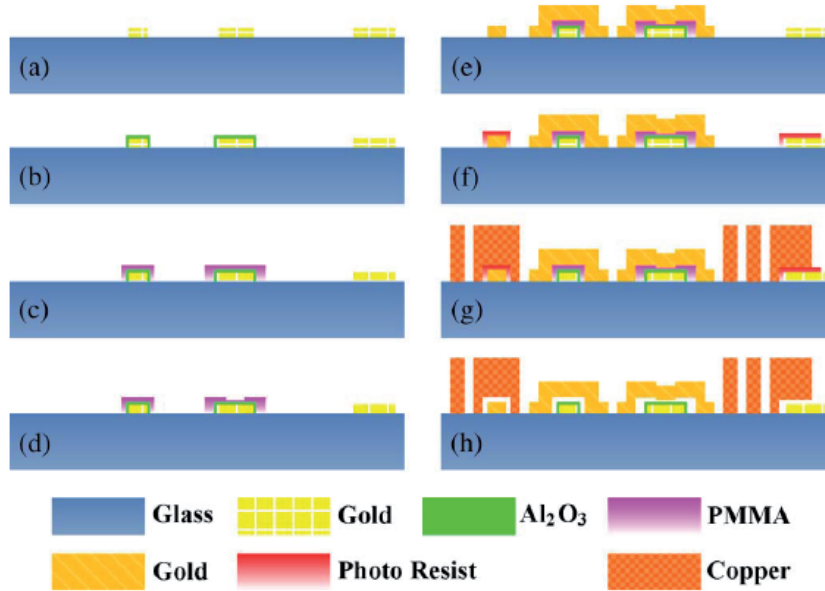


Fig. 4.6: Fabrication process flow: (a) Au lift-off, (b) Al_2O_3 deposition, (c) PMMA patterning, (d) PMMA thinning, (e) Au electroplating, (f) S1813 lithography, (g) Cu electroplating, (h) release in acetone followed by CPD. [17].

HR-Si.

Inserting patterned ground shield [18] or a trenched silicon island [19] beneath the inductor have been reported to have a significant improvement on the inductor's performance. Due to substantial reduction of substrate RF losses and parasitic coupling, the measured quality factor on trap-rich HR-Si substrate with

a thick Cu layer exhibits Q values similar in range than reported for inductors fabricated on CMOS-grade trench silicon substrate [19]. Using a patterned ground shield technique [18], not only the inductor quality factor improvement is not as significant compare with those fabricated on trap-rich HR-Si or trench silicon substrate, but also the compromise to produce high resonance frequency and relatively high quality factor inductors.

As previously mentioned the inductor elements cover a large area within the

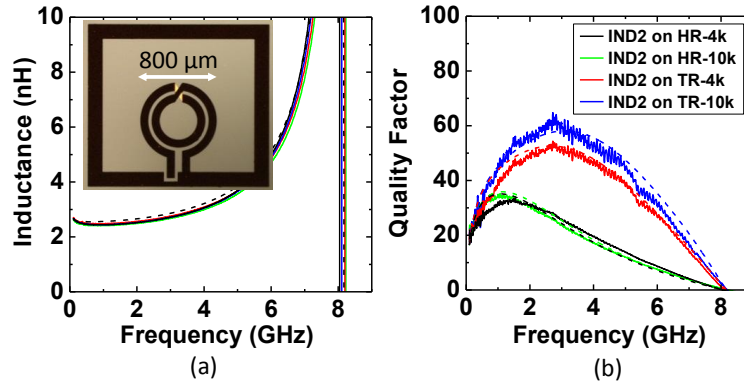


Fig. 4.7: Measured (a) inductance (inset: microscope image of the inductor) and (b) Q of 2 nH_{IND} on HR-Si and TR-Si (the dashed line is the simulation result using the lumped element model [20]).

integrated RF circuits and thus substrate non-linearity is mainly sensed through such large passive elements surface. To that end the inductor non-linear behaviour was investigated through the measurement of the output power at the second and third order harmonics (HD2 and HD3) on HR-Si wafers with and without a trap-rich layer for different fundamental input frequencies, 900 MHz, 2 GHz and 4 GHz. Higher harmonic levels are depicted on HR-Si wafer compared to passivated trap-rich HR-Si when the fundamental RF frequency is close to the inductor operation frequency, which corresponds to the maximum quality factor value. Fig. 4.9 (a) shows HD2 level at -90 dBm and HD3 close to the noise floor level when an input fundamental frequency is 900 MHz on both wafers. The non-linear behaviour increases on HR-Si substrate when the input fundamental frequency increases to 2 and 4 GHz as shown in Figs. 4.9 (b) and (c). The passivated trap-rich layer reduced the effect of the parasitic surface conduction (PSC) effect at the SiO_2/Si interface and thus maintains low harmonic levels over the whole frequency range on both TR-10k and TR-4k wafers. These results correlate with the measured quality factor, i.e. reduction of harmonics with the increase of the quality factor.

The PSC effect as well as the trap-rich layer on HR-Si substrate were previously investigated and modelled in chapter 2 and the complete inductor equivalent lumped elements is shown in Fig. 4.8. The inductor parasitic lumped elements

derived from the skin and proximity effect are described by the L_{S1} , R_{S1} , R_{S2} elements. C_p represents the parasitic capacitance due to the overpass and underpass layers in multi-turn inductors [20].

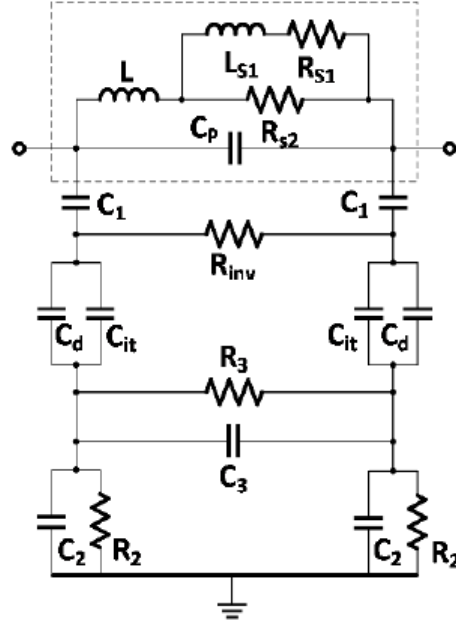


Fig. 4.8: Lumped elements model of an inductor on trap-rich on HR-Si substrate.

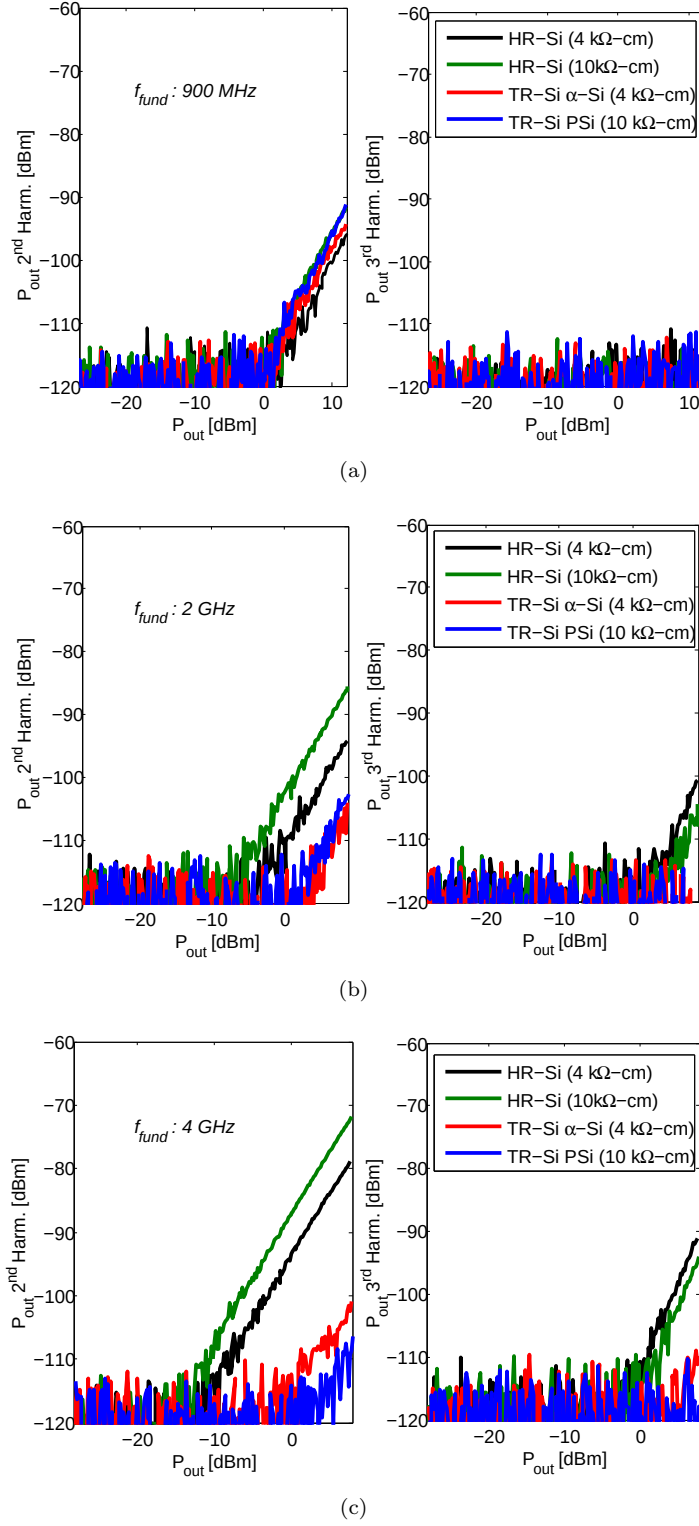


Fig. 4.9: Measured harmonic distortions of $2nH$ inductor @ different fundamental tones (a) 900 MHz, (b) 2 GHz and (c) 4 GHz on HR-Si, amorphous trap-rich HR-Si (TR α -Si) and polySi trap-rich HR-Si (TR PSi).

4.2 FD SOI MOSFET DC AND RF CHARACTERISTICS

Fully-depleted (FD) SOI NMOSFETs are designed using a standard $1\ \mu\text{m}$ SOI CMOS process and fabricated in the Winfab clean-room at UCL [13]. N-channel SOI MOSFETs with gate lengths of 1.5, 2 and $3\ \mu\text{m}$, finger width (W_f) of 10, 20, 30 and $40\ \mu\text{m}$, with 20 parallel fingers are studied. The RF test structures employ a multi-finger gate layout to minimize gate resistance. Multi-finger devices are used and embedded in coplanar waveguide (CPW) access pads for performing RF characterization. In this section we focus on FD SOI MOSFETs with $2\ \mu\text{m}$ gate length (L) with 20 gate fingers of $20\ \mu\text{m}$ gate width each (W). The number of 20 fingers is mainly designed to minimize series resistance in the gate and S/D contacts. Whereas, the gate finger width of $20\ \mu\text{m}$ for a channel length of $2\ \mu\text{m}$ is optimum to maximize the RF cut-off frequency of the transistor. Both intrinsic ($10^{15}\ \text{at}/\text{cm}^3$, named NiN) and standard boron implantation ($4 \times 10^{16}\ \text{at}/\text{cm}^3$, NP2N) are considered for the channel doping. The cross section of the tested nMOS transistors is shown in Fig. 4.10 having 400 nm-thick BOX, 80 nm-thick thin active silicon film and 25 nm-thick gate oxide, all lying on HR-Si handle substrate ($> 3\ \text{k}\Omega\cdot\text{cm}$) and HR-Si substrate passivated by a $2\ \mu\text{m}$ trap-rich layer. DC and RF measurements were performed on 18 dies for both HR-SOI and TR-SOI wafers.

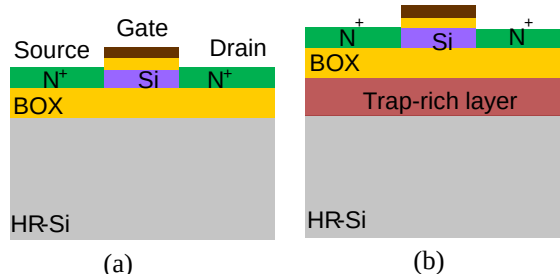


Fig. 4.10: Cross-section of the FD SOI MOSFET transistors on (a) HR-SOI and (b) TR-SOI wafers.

4.2.1 DC characterization and parameters extraction

4.2.1.1 Threshold voltage (V_{th})

Threshold voltage is one of the most important and valuable parameters for DC characterization, device modelling and device engineering of any technology node. For a MOSFET transistor it is used to distinguish the gate voltage at which the transition between weak and strong inversion occurs in the MOSFETs channel. The threshold voltage can be either positive or negative, depending on the doping concentration and the material used to form the gate electrode. If the threshold voltage is negative the n-channel MOSFET is a depletion-mode

device (such as intrinsic doping NiN devices in this work); if it is positive, the device is an enhancement-mode MOSFET (i.e. NP2N standard doping transistors). Depletion-mode devices will have an inversion layer when the gate voltage is equal to zero. Enhancement-mode devices require an applied positive gate voltage to create the inversion layer.

The analytical expression of the threshold voltage for a fully depleted SOI MOSFET is given by [21, 22]:

$$V_{th}^f = V_{FB}^f + 2\Phi_F - \frac{Q_b}{2C_{OX}} - (V_{BG} - V_{FB}^b - 2\Phi_F + \frac{Q_b}{2C_{BOX}}) \cdot \frac{C_{Si}C_{BOX}}{C_{OX}(C_{Si} + C_{BOX})} \quad (4.1)$$

where V_{th}^f and V_{BG} are the front threshold and back-gate voltages, V_{FB}^f and V_{FB}^b are the front and back gate flatband voltages, C_{OX} , C_{BOX} and C_{Si} are front and back gate oxide and depleted silicon-film capacitances, respectively. Q_b is the charge density in the depleted silicon film given by:

$$Q_b = +qN_A T_{Si} \quad (4.2)$$

for n-channel devices where N_A is the p-type body doping concentration and T_{Si} is the SOI-film thickness.

Since the buried oxide thickness is in the range of 400 nm, the silicon film-thickness is under 100 nm, and $\epsilon_{Si}/\epsilon_{OX}=11.8/3.9$, $C_{Si} \gg C_{BOX}$, we have

$$\frac{C_{Si}C_{BOX}}{C_{OX}(C_{Si} + C_{BOX})} \simeq \frac{C_{BOX}}{C_{OX}} \quad (4.3)$$

Equation 4.1 can be written for an n-channel SOI MOSFET

$$V_{th}^f = V_{FB}^f + 2\Phi_F - (V_{BG} - V_{FB}^b - 2\Phi_F) \cdot \frac{C_{BOX}}{C_{OX}} + \frac{qN_A T_{Si}}{C_{OX}} \quad (4.4)$$

For non-fully depleted silicon film or $T_{Si} > X_{dmax}$ the threshold voltage is given by

$$V_{th}^f = V_{FB}^f + 2\Phi_F + \frac{qN_A X_{dmax}}{C_{OX}} \quad (4.5)$$

where

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (4.6)$$

is the flat band voltage,

$$\Phi_F = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) \quad (4.7)$$

is the Fermi potential, and

$$x_{dmax} = \sqrt{\frac{4\epsilon_{si}\Phi_F}{qN_a}} \quad (4.8)$$

is the maximum depletion width.

In this work, V_{th} is extracted from $I_D(V_G)$ curves measured in the linear regime ($V_{DS} = 50$ mV) using the second derivative method [23]. The second derivative of the drain current with respect to gate voltage is calculated using Eq. 4.9

$$\frac{d^2 I_D}{d^2 V_G} = \frac{dg_m}{dV_G} \quad (4.9)$$

The maximum of the second derivative is then found and the corresponding V_G is taken as V_{th} as shown in Fig. 4.11.

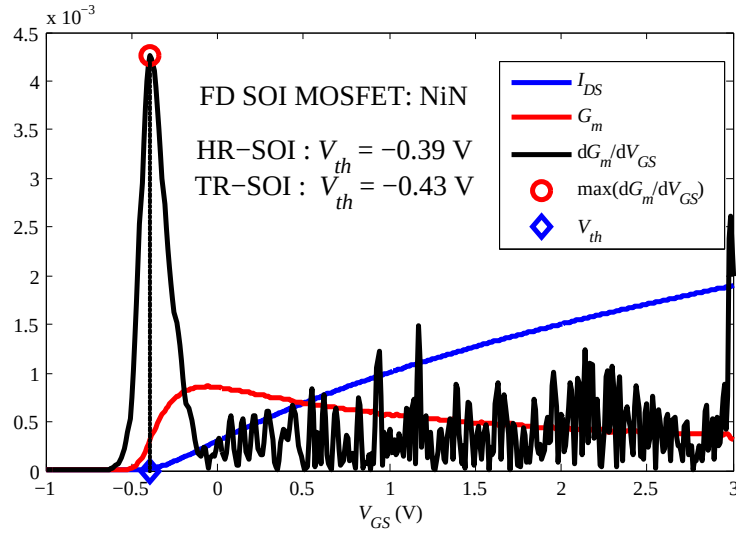


Fig. 4.11: Experimental result showing dg_m/dV_G method as a function of gate voltage to extract threshold voltage at low $V_d = 50$ mV for NiN FD SOI MOSFETs with $L = 2\mu\text{m}$, $W = 20\mu\text{m}$ and $N_f = 20$. The g_m and dg_m/dV_G are normalized to their maximum peaks.

In Fig. 4.12 the distribution of the extracted V_{th} for both intrinsic NiN and standard NP2N doped transistors is presented. Based on statistical measurement of 18 devices on each wafer, i.e. HR-SOI and TR-SOI, the observed variation is mainly related to the process variability. The mean values of the extracted V_{th} for the 18 devices (for the NiN doped transistors) are quite similar for both technologies, i.e. -0.39 and -0.43 V, respectively. We claim that the introduced trap-rich layer underneath the BOX does not affect the DC and RF performance of active devices. The V_{th} variation for the NP2N doping transistors on both HR-SOI and TR-SOI have relatively the same tendency (close to 0.22 V).

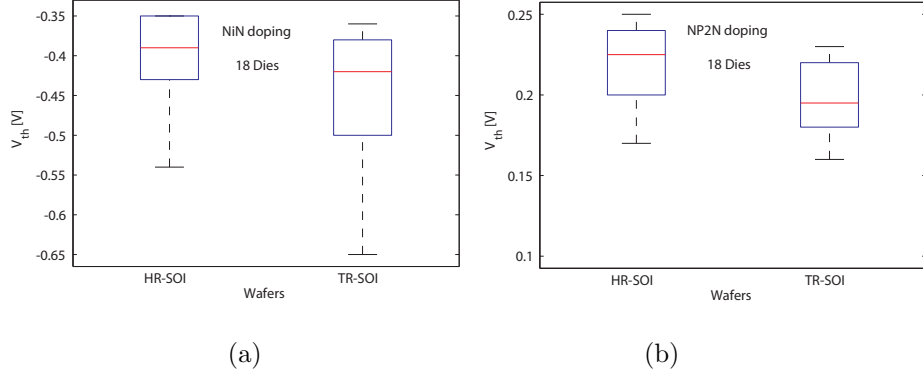


Fig. 4.12: V_{th} distribution for (a) NiN and (b) NP2N FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

4.2.1.2 The current-voltage $I_D(V_G)$ characteristics and Transconductance (g_m)

The current-voltage $I_D(V_G)$ characteristics is an essential way to study and extract different DC characterization parameters for a MOSFET transistors. The normalized $\text{Log}I_D(V_{GT})$ and $g_m(V_{GT})$ curves recorded for 2 μm -long FD SOI nMOS are presented in Fig. 4.13. The results outline similar DC behaviour on both wafers, for both channel doping levels NiN and NP2N FD SOI MOSFETs. The saturation drain current for a fully depleted SOI MOSFET transistor takes place when $V_D \gg (V_G - V_{th}) = V_{GT}$, and I_{Dsat} is given by [22]:

$$I_{Dsat} = \frac{\mu_n C_{OX}}{1 + \frac{C_{Si} C_{BOX}}{C_{OX}(C_{Si} + C_{BOX})}} \frac{W}{L} \frac{(V_G - V_{th})^2}{2} \quad (4.10)$$

where C_{OX} , C_{BOX} , C_{Si} , are the front and back oxide and depleted silicon-film capacitances, respectively. The body factor for fully depleted devices under depleted back interface conditions is given by:

$$n = 1 + \frac{C_{Si} C_{BOX}}{C_{OX}(C_{Si} + C_{BOX})} = 1 + \alpha \quad (4.11)$$

The body factor quantify the coupling efficiency between the front-gate voltage and the channel. The closer n to unity, the sharper is the transition between off- and on-states of the transistor.

As previously mentioned since $C_{Si} \gg C_{BOX}$, the buried oxide thickness is in the range of 400 nm and the gate oxide thickness is only 25 nm the body factor could be approximated to 1 and I_{Dsat} equation can be written:

$$I_{Dsat} = \frac{\mu_n C_{OX}}{1 + \alpha} \frac{W}{L} \frac{(V_G - V_{th})^2}{2} = \mu_n C_{OX} \frac{W}{L} \frac{V_{GT}^2}{2} \quad (4.12)$$

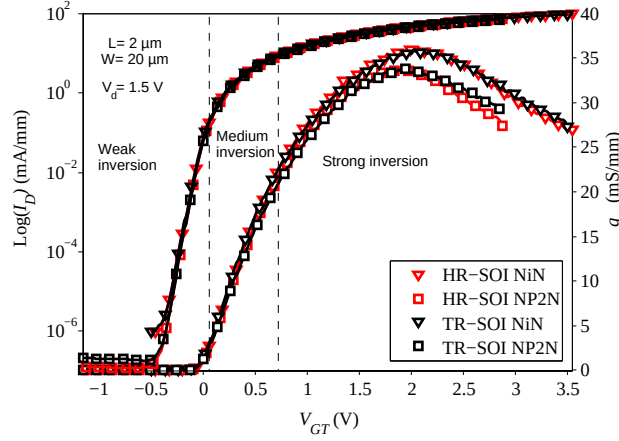


Fig. 4.13: Normalized $\text{Log}I_D(V_{GT})$ and $g_m(V_{GT})$ characteristics at $V_D = 1.5$ V for NP2N and NiN FD SOI MOSFETs with $L = 2\mu\text{m}$, $W = 20\mu\text{m}$ and $N_f = 20$ on HR-SOI and TR-SOI substrates.

The transconductance of a MOSFETs is a measurement of effectiveness of the control of the drain current by the gate voltage and corresponding to the first derivative of the drain current I_D with respect to the V_G (Eq. 4.8).

$$g_m = \frac{dI_D}{dV_G} \quad (4.13)$$

In a thin-film, fully-depleted SOI MOSFETs, the transconductance can be obtained as follows:

$$g_m = \frac{dI_{Dsat}}{dV_G} = \frac{W\mu_{eff}C_{OX}}{n.L}(V_G - V_{th}) = \frac{W\mu_{eff}C_{OX}}{L}V_{GT} \quad (4.14)$$

where W is the width, L the gate length, L_{eff} the effective carrier mobility and C_{OX} the front gate oxide capacitance.

From the transconductance versus gate voltage characteristics in Fig. 4.13, it is possible to extract various electrical and technological parameters such as threshold voltage, carrier mobility, etc. The variation of the normalized $I_D(V_{GT})$ and $g_m(V_{GT})$ in Fig. 4.14 show relatively the same tendency on 18 dies for NiN FD transistors on both HR-SOI and TR-SOI substrates.

The maximum transconductance (g_{mmax}) is a useful information for analog and RF figures-of merits and can be translated into how fast the transistor perform. Figure 4.15 shows the distribution of the extracted g_{mmax} for NiN and NP2N FD transistors on both HR-SOI and TR-SOI substrates, which are quietly in the same range.

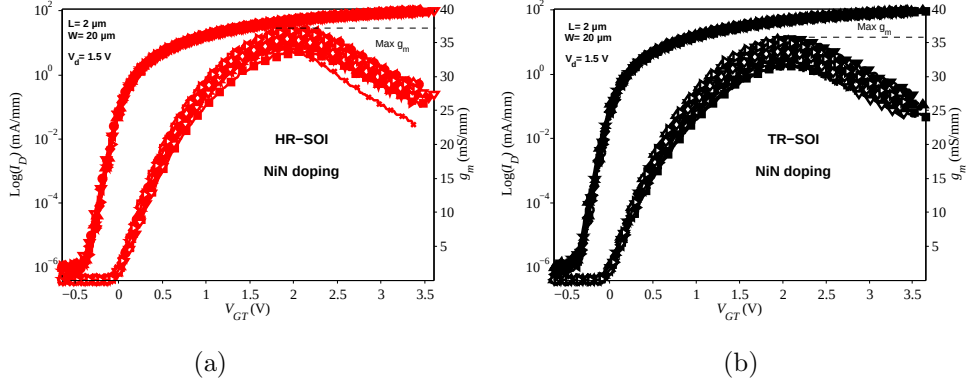


Fig. 4.14: Variation of the normalized $I_D(V_{GT})$ and $g_m(V_{GT})$ for NiN FD SOI MOSFETs from 18 dies on (a) HR-SOI and (b) TR-SOI wafers.

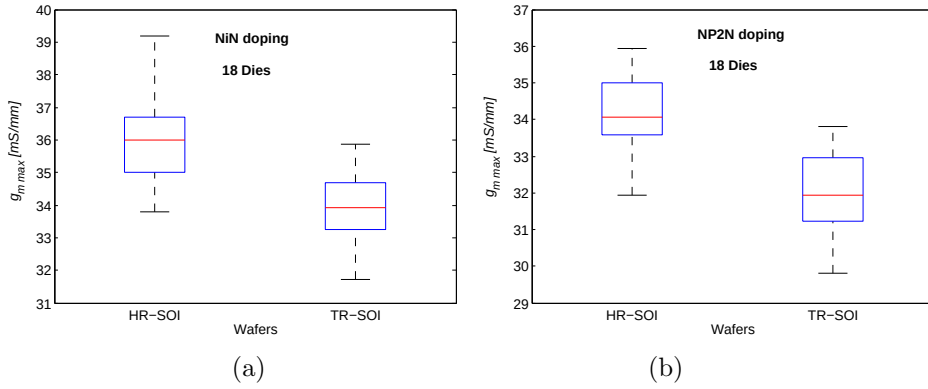


Fig. 4.15: g_{mmax} distribution for NP2N and NiN FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

4.2.1.3 Subthreshold slope (SS)

In weak inversion the drain current depends exponentially on gate and drain voltages. By taking the slope of the straight line at this regime based on $dV_G/d\log(I_D)$ (hence the inverse of $d\log(I_D)/dV_G$) as depicted in Fig. 4.16 the sharpness of the current transition from off-state to on-state can be determined [24]. Lower value of the 'subthreshold slope' or 'subthreshold swing' implies more efficient and rapid switching of the devices. It is defined as the change in gate voltage required to produce a decade change in drain current and given by :

$$SS = \frac{\partial V_G}{\partial \log(I_D)} = n \frac{kT}{q} \ln(10) \quad (4.15)$$

where k is the Boltzmann constant, T is the temperature, and q is the charge of the electron.

Theoretically, the lowest possible value is 60 mV/decade, which is reached when $n \approx 1$. Practically, values around 65 mV/decade can be obtained for long fully depleted devices at room temperature. The extracted subthreshold slope for the investigated NiN and NP2N FD SOI MOSFETs on both HR-SOI and TR-SOI substrates are quite similar as depicted in Fig. 4.16. The variation of the subthreshold slope for the measured NiN and NP2N transistors of 18 dies on both HR-SOI and TR-SOI wafers are shown in Fig. 4.17 (a) and (b), respectively.

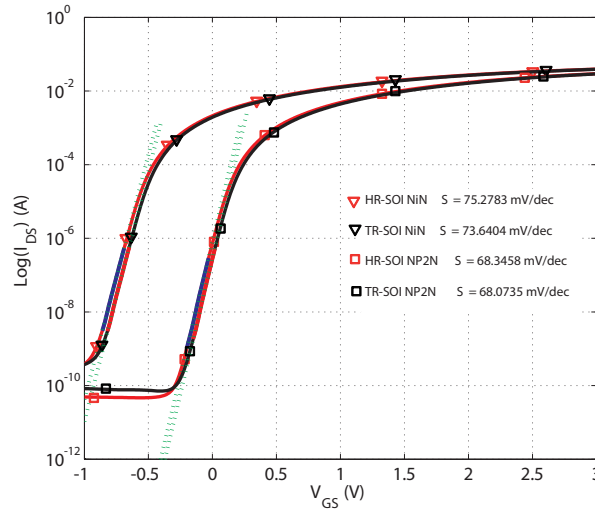


Fig. 4.16: Experimental result showing the extraction of SS from drain current in log scale at $V_d = 50$ mV for NiN and NP2N FD SOI MOSFETs on HR-SOI and TR-SOI wafers.

4.2.1.4 Drain-induced barrier lowering (DIBL)

Drain-induced barrier lowering (DIBL) occurs when the depletion regions of the drain and the source interact with each other near the channel surface to lower the source potential barrier [25, 26]. When a high drain voltage is applied to a short-channel device, it lowers the barrier height, resulting in further decrease of the threshold voltage [13]. The source then injects carriers into the channel surface (independent of gate voltage). DIBL is enhanced at high drain voltages and shorter channel lengths. DIBL can be extracted as the shift of V_G with V_D ($DIBL = \frac{\Delta V_G}{\Delta V_D}$) at constant normalized drain current (i.e. $I_{Dnorm} = I_D/(W/L)$) of 10^{-7} A). Alternatively DIBL can be defined as a V_{th} shift due to the variation in drain voltage ($DIBL = \frac{\Delta V_{th}}{\Delta V_D}$) [27]. The subthreshold curves are steep as shown in Fig. 4.16 and DIBL (Drain Induced Barrier Lowering) effects are very slight.

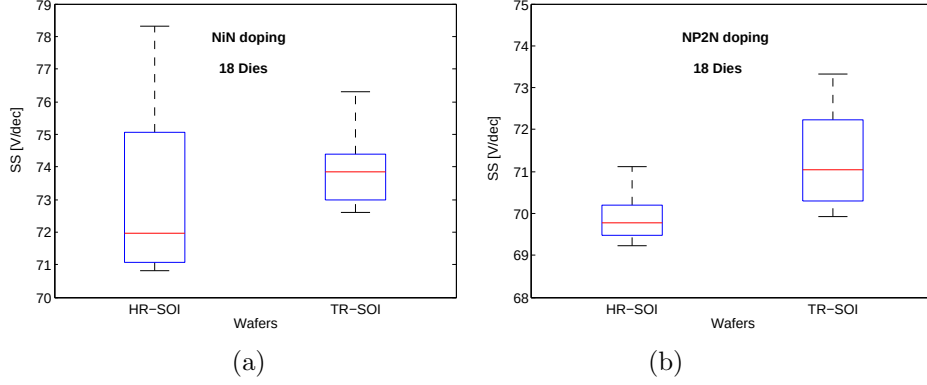


Fig. 4.17: Subthreshold slope distribution for NP2N and NiN FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

Figure 4.18 (a) and (b) shows the distribution of the extracted DIBL values for the measured NiN and NP2N FD SOI MOSFETs, respectively, from the 18 dies on each HR-SOI and TR-SOI wafers. The average values of the extracted DIBL are relatively similar on both substrates for each NiN and NP2N doping profiles 13.5 and 14.2 mV/V, respectively.

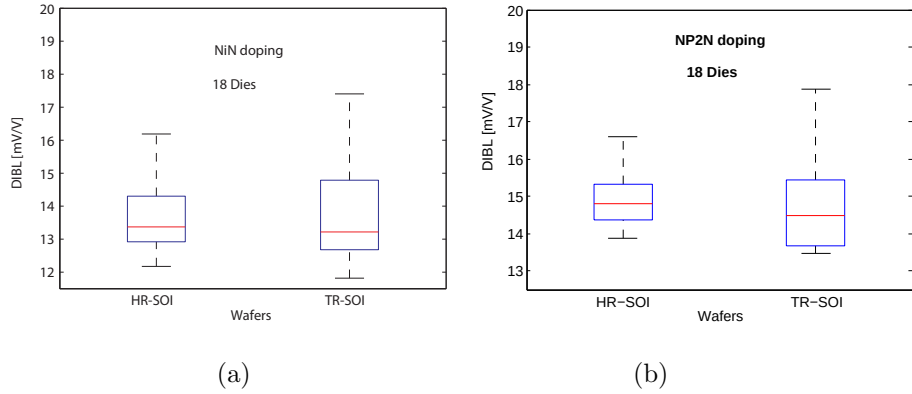


Fig. 4.18: DIBL distribution for (a) NiN and (b) NP2N FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

4.2.1.5 Transconductance-to-current ratio (g_m/I_D)

The ratio of transconductance to drain current (g_m/I_D) is a very important figure of merit for analog circuits [28–30]. It occurs in the formula for the DC

gain of a MOSFET:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta V_{in}}{g_d} \frac{g_m}{\Delta V_{in}} = \frac{g_m}{g_d} = \frac{g_m}{I_D} \cdot V_{EA} \quad (4.16)$$

where g_d is output conductance and V_{EA} is Early voltage. It is known that the maximum performance of analog devices may be obtained for the largest gain, which means the largest g_m/I_D ratio. This condition appears in weak inversion for MOSFET transistors [24]. The value of g_m/I_D can be rewritten as:

$$\frac{g_m}{I_D} = \frac{dI_D}{I_D dV_G} = \frac{\ln(10)}{SS} = \frac{q}{nkT} \quad (4.17)$$

A previously defined, the body factor n is a measure of the ideality of the coupling between the gate voltage and the channel surface potential. Typical values of n are in the range of 1.05 to 1.1 for FD SOI MOSFETs [22].

To fairly compare all types of transistors on both wafers and to eliminate the impact of threshold voltage variations, we extracted in Fig. 4.19 g_m/I_D over $I_D/(W/L)$. The low body effect coefficient for FD SOI devices allows for obtaining almost identical high values of g_m/I_D (35 V^{-1}) on both HR-SOI and TR-SOI technologies.

In strong inversion, for long-channel devices, g_m/I_D becomes:

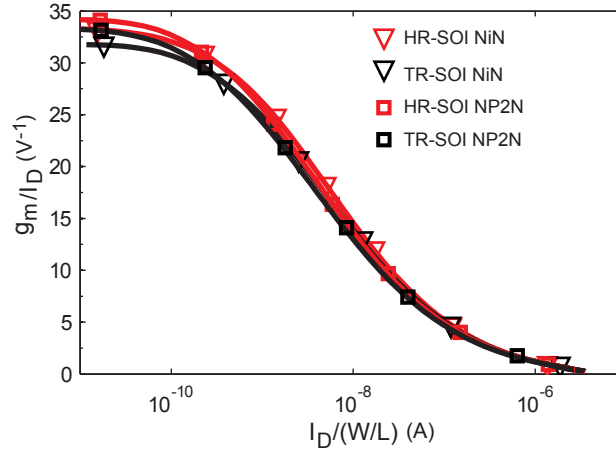


Fig. 4.19: g_m/I_D ratio versus $I_D/(W/L)$ at $V_D = 1.5 \text{ V}$, for NP2N and NiN FD SOI MOSFETs on HR-SOI and TR-SOI substrates.

$$\frac{g_m}{I_D} = \sqrt{\frac{2\mu_0 C_{OX} W/L}{n \cdot I_D}} \quad (4.18)$$

These different DC extracted parameters suggest that trap-rich passivation layer does not impact the DC behaviour of the studied long channel FD SOI

MOSFETs. The measured MOS transistors are pretty large and thus they feature a large contact area with the BOX. But even for such a wide transistors, the traps underneath the BOX do not impact the transistor behaviour.

4.2.2 High frequency performance

High frequency measurements have been performed from 0.04 to 40 GHz using Anritsu 37369A in combination with HP4145A. The S-parameters plans correspond to the active part of the device and defined using a two-steps calibration procedure. First, an off-wafer LRRM (Load-Reflection-Reflection-Match) calibration technique defines the reference planes at the probe tips. Then, the CPW accesses embedding the device are deduced using a dedicated on-wafer open test structure as shown in Fig. 4.20. The open de-embedding method requires a dedicated dummy structure manufactured in the same chip as the DUT. The measured S-parameters of the open structure is converted to Y-parameters Y_{Open} and then subtracted from the total Y-parameters Y_{Total} ($Y_{DUT} = Y_{Total} - Y_{Open}$) [31]. The de-embedded DUT Y-parameters Y_{DUT} is then converted to other representation suitable for the extraction of different RF parameters.

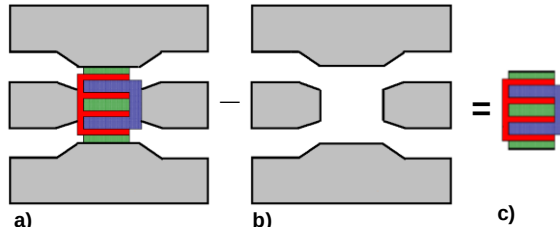


Fig. 4.20: Schematic illustration of de-embedding methods a) complete structure b) open structure c) DUT transistor.

The RF behaviour of a transistor is usually characterized by two key parameters, the current gain cut-off frequency f_T and the power gain cut-off frequency f_{max} [32], extracted from measured data after the de-embedding step. The Current gain cut-off frequency is also known as unity current gain frequency defined as the frequency at which the short circuit current $|H_{21}|$ is equal to unity. It is extracted from the x-axis intersection of an extrapolated -20 dB/dec line on the curve of the current gain $|H_{21}|$ versus frequency as depicted in Fig. 4.21. The current gain $|H_{21}|$ can be expressed by :

$$|H_{21}| = \frac{|Y_{21}|}{|Y_{11}|} \quad (4.19)$$

It can also be calculated from the measured S parameters using:

$$|H_{21}| = \frac{|-2S_{21}|}{|(1-S_{11})(1+S_{22})+S_{12}S_{21}|} \quad (4.20)$$

Fig. 4.21 presents the expected H_{21} which shows excellent similarity, respectively, for the NiN and NP2N FD SOI MOSFETs on both wafers. The current gain was extracted at the bias voltages condition giving the maximum of g_m , i.e. $V_{GS}=1.5$ V, and $V_{GS}=2$ V for NiN and NP2N transistors, respectively and $V_{DS}=1.5$ V in both cases. These curves demonstrate that substantially high RF performance of FD SOI MOSFET can be achieved on TR-SOI wafers.

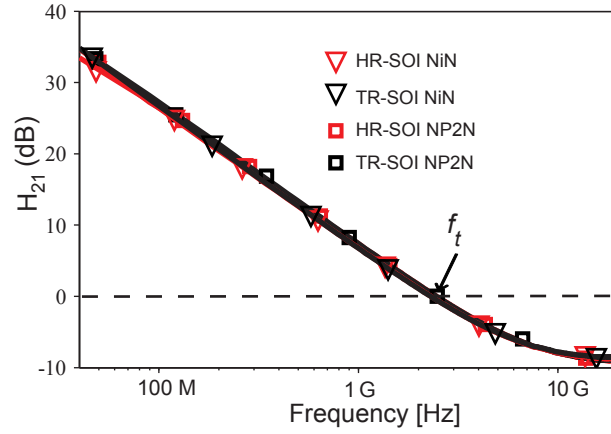


Fig. 4.21: Current gain measured for NiN (at) and NP2N (at) FD SOI MOSFETs on HR-SOI and trap-rich HR-SOI substrates.

Based on the small-signal equivalent circuit in Fig. 4.25, the current gain cut-off frequency f_T can be obtained analytically from:

$$f_T = \frac{\Re(Y_{21})}{2\pi\Im(Y_{11}/\omega)} \quad (4.21)$$

where $\Re(Y_{21})$ is mainly a function of the gate transconductance and $\Im(Y_{11})$ is directly related to the total gate capacitance, thus f_T can be expressed by:

$$f_T = \frac{g_m}{2\pi C_{gg}} \quad (4.22)$$

where C_{gg} is the total gate capacitance, i.e. the sum of gate-to-source and gate-to-drain capacitances ($C_{gg} = C_{gs} + C_{gd}$).

The influence of parasitic capacitances and resistances to the current gain cut-off

frequency can be detailed using the following expression of f_T [33, 34]:

$$f_T \approx \frac{g_m}{2\pi C_{gs}} \frac{1}{(1 + \frac{C_{gd}}{C_{gs}}) + (R_s + R_d)(\frac{C_{gd}}{C_{gs}}(g_m + g_d) + g_d)} \quad (4.23)$$

Equation 4.23 highlighted the importance of the ratio g_m/g_d and C_{gs}/C_{gd} whose high values enhance the cut-off frequency f_T . Figure 4.22 shows cut-off frequency f_T versus V_G , respectively for NiN and NP2N FD SOI MOSFETs on both wafers. A slightly shift down of f_T is seen on TR-SOI compared to the values on HR-SOI, which could be related to the higher values of access resistance R_d as shown in Fig. 4.26. The variability of the extracted f_T from 18 dies on each HR-SOI and TR-SOI wafers, respectively, for NiN and NP2N transistors is presented in Fig. 4.23, which show a slightly higher f_T values on HR-SOI wafers. Again, the observed variation is mainly related to our academic process variability.

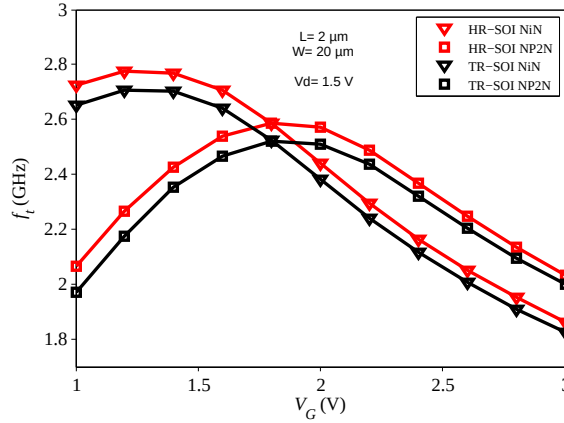


Fig. 4.22: Current gain cut off frequency f_T as function of V_G measured for NiN and NP2N FD SOI MOSFETs on HR-SOI and TR-SOI substrates.

The maximum oscillation frequency f_{max} is defined as the frequency at which the power gain equal to unity, i.e. the device still provides power in a stable operation. The Maximum Available Gain (MAG) as a function of S-parameter can be expressed by:

$$MAG = \frac{|S_{21}|}{|S_{11}|} (k - \sqrt{k^2 - 1}) \quad (4.24)$$

where k is the Rollet's stability factor defined by:

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}||S_{21}|} \quad (4.25)$$

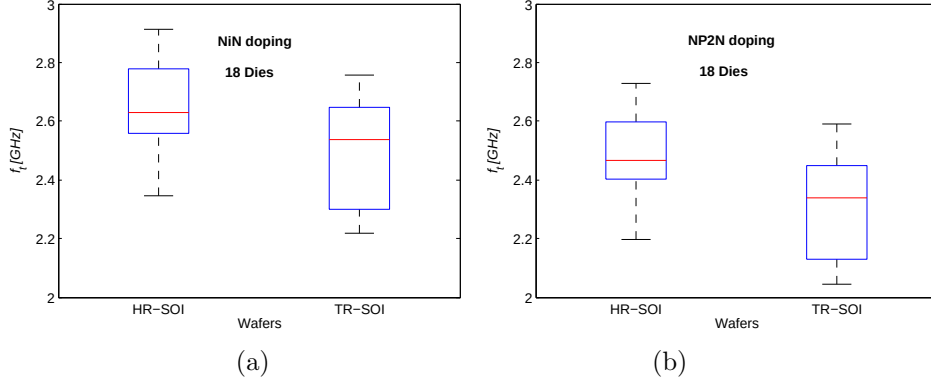


Fig. 4.23: Cut off frequency f_T distribution for NiN and NP2N FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

with $\Delta = S_{11}S_{22} - S_{21}S_{12}$. The maximum available gain definition is only valid in the case of a stable device, i.e. $k > 1$. Another approach to extract f_{max} is using the unilateral gain (ULG) which is defined as the maximal available gain of a device when the stability is ensured by using a lossless feedback network to cancel the reverse transmission of the device. This gain is defined as:

$$ULG = \frac{1}{2} \cdot \frac{|S_{21}|^2}{k|S_{12}| - \Re(S_{21})} \quad (4.26)$$

It is interesting to point out that ULG and MAG present similar values [35] if the definition of ULG and MAG is taken at intersection cross at 0 dB. From the simplified small signal equivalent circuit, the maximum oscillation frequency is given by the following relation [33, 36]:

$$f_{max} \approx \frac{g_m}{4\pi C_{gs}} \frac{1}{(1 + \frac{C_{gd}}{C_{gs}}) \sqrt{g_d(R_g + R_s) + \frac{1}{2} \frac{C_{gd}}{C_{gs}} (R_s g_m + \frac{C_{gd}}{C_{gs}})}} \quad (4.27)$$

Ideally f_{max} has direct correlation with f_T . Nevertheless, gate resistance R_g has a tremendous effect on f_{max} and it depends on process conditions and topology of the transistors. In this work, we used the MAG definition extrapolated to cross at 0 dB. Figure 4.24 illustrates the distribution of the extracted f_{max} respectively for NiN and NP2N devices from 18 dies on each HR-SOI and TR-SOI substrates. It can be seen that f_{max} increases on TR-SOI wafer for both NiN and NP2N doping transistors which could be related to the decrease of C_{ds} as depicted in Fig. 4.28.

4.2.3 Small signal equivalent circuit model parameters

S-parameters measurements were carried out using an Anritsu vector network analyzer from 40 MHz upto 40 GHz, on the different FD SOI MOSFETs on

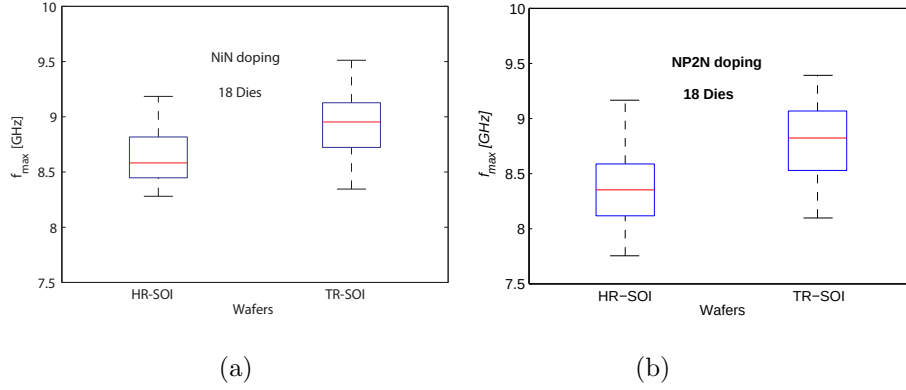


Fig. 4.24: Maximum oscillation frequency f_{max} distribution for (a) NiN and (b) NP2N FD SOI MOSFETs from 18 dies on each HR-SOI and TR-SOI wafers.

both HR-SOI and TR-SOI wafers. Two different sets of data in cold FET and saturation conditions are used after a de-embedding procedure to extract the extrinsic and intrinsic parameters as in the small signal equivalent circuit model in Fig. 4.25. The cold bias condition settle a drain voltage equal to zero and gate voltage is biased from -1 to 3 V.

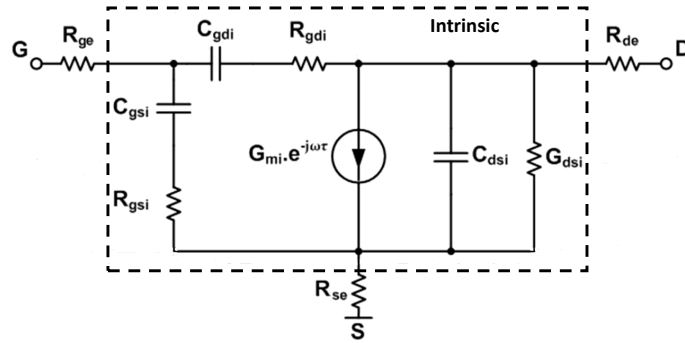


Fig. 4.25: Small signal equivalent circuit model used for modelling the parasitic resistances and capacitances with separating block between extrinsic (denoted as “e”) and intrinsic (denoted as “i”).

Extrinsic resistances

In Fig. 4.25 the dotted box differentiates between the intrinsic (active zone) and extrinsic (outside) elements of a typical equivalent circuit for a MOSFET transistor [36, 37]. The parasitic extrinsic resistances (R_{se} , R_{de} , (being the source

and drain resistances) include metallic losses and contacts resistances between the metal and the source and drain implants. The gate resistance R_{ge} includes the resistance of gate fingers and metallic lines that connect the gate fingers together to the reference plane [35]. The extraction of the intrinsic elements from the S-parameters is very sensitive to the values of the extracted extrinsic resistances. The extraction of these extrinsic resistances is achieved using the coldFET method proposed by Bracale et al. [38] and reviewed by Tinoco et al. [37] to provide an ideal value of the parasitic resistances extracted over a wide frequency range. The method is based on inversion-regime, where the transistor is extracted at $V_{GS} > V_{th}$. These parasitic resistances can be extracted from the approximation in Eq. 4.28 to 4.30 [39, 40]:

$$\Re(Z_{11} - Z_{12}) = R_g - \frac{1}{4g_{ds}} \quad (4.28)$$

$$\Re(Z_{22} - Z_{12}) = R_d + \frac{1}{g_{ds}} \quad (4.29)$$

$$\Re(Z_{12}) = R_s + \frac{1}{2g_{ds}} \quad (4.30)$$

Since MOSFETs channel conductance, g_d is proportional to $(V_G - V_{th})$, the extrinsic resistances can be obtained with a simple linear regression as a function of term $(1/(V_G - V_{th}))$. For symmetrical devices for source and drain, one should find R_s and R_d nearly equal to each other. Fig. 4.26 shows the extracted extrinsic elements for the measured FD SOI MOSFETs with an NP2N channel doping profile as function of the gate width W and gate length L . R_g , R_d and R_s are quite similar when comparing both HR-SOI and TR-SOI technologies. The slight variation of R_g could be related the process conditions and transistors topology rather than the substrate properties.

Intrinsic parameters

The dotted box in Fig. 4.25 illustrates the intrinsic part of the small signal equivalent circuit of the MOSFET transistor almost related to the active area of the device. The extractions of the intrinsic Z-parameter elements (Z_{int}) can be obtained from the subtraction of the extracted extrinsic resistances from the measured Z-parameters (Z_{ext}) using the following relation

$$|Z_{in}| = |Z_{ext}| - \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \quad (4.31)$$

As depicted from the equivalent circuit model in Fig. 4.25, the intrinsic elements contain three capacitances C_{gs} , C_{gd} and C_{ds} (being the total gate-to-source, gate-to-drain and drain-to-source capacitances, respectively). These intrinsic capacitances can be extracted either when the transistor is operated in the on-state, or in the off-state. The latter, outline the deep depletion regime of the transistor, i.e negative value of V_{GS} and $V_{DS} = 0V$. The direct extraction method introduced by Raskin et al. in [36] is then applied. Under this bias

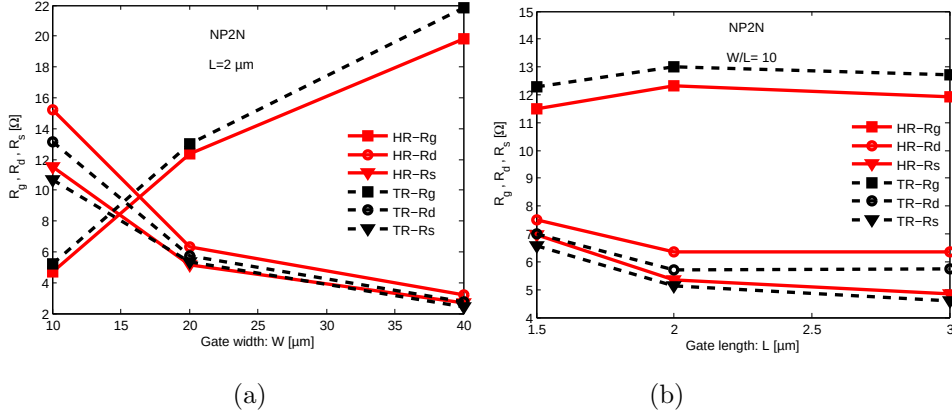


Fig. 4.26: Variation of the extrinsic elements, R_g , R_d and R_s , for an NP2N doping SOI MOSFET (a) over gate width W , and (b) over gate length L .

condition, the gate transconductance and output conductance of the transistor are negligible. The drain and source capacitances should theoretically result in almost similar values as a result of symmetrical transistor operations in off-state condition. C_{gs} and C_{gd} in the off-state contain the contribution fringing capacitances, overlap capacitances, and the body depletion capacitances [31].

For on-state, the transistor is biased in saturation and strong inversion regime i.e. $V_{DS} = 1.5V$ and V_{GS} is at the bias point of interest, $V_{GS} > V_{th}$. The gate transconductance and output conductance are extracted at this condition as the transistor in the on-state condition. The capacitances extracted at this regime correspond to the total capacitances i.e. C_{gs} , C_{gd} and C_{ds} . The extraction of both off- and on-state elements was performed using direct extraction method [36]. The different parameters are obtained from the transformed Z_{int} to Y-parameters and are given by:

$$C_{gd} = -\frac{\Im(Y_{12})}{2\pi f} \quad (4.32)$$

$$C_{gs} = \frac{\Im(Y_{11}) + \Im(Y_{12})}{2\pi f} \quad (4.33)$$

$$C_{ds} = \frac{\Im(Y_{22}) + \Im(Y_{12})}{2\pi f} \quad (4.34)$$

$$g_m = |Y_{21} - Y_{12}| \quad (4.35)$$

$$g_d = \Re(Y_{22}) \quad (4.36)$$

Fig. 4.28 illustrates the extracted intrinsic capacitances as function of gate width W and length L for NP2N doping profile FD SOI MOSFETs. C_{gs} and C_{gd} show almost similar extracted value on both HR-SOI and TR-SOI technologies, whereas, C_{ds} is more than 15% lower on TR-SOI.

Table 4.2 summarizes the extracted extrinsic and intrinsic parameters for the different FD SOI MOSFETs measured on both HR-SOI and TR-SOI wafers. The intrinsic transconductance G_{mi} and conductance G_{dsi} extracted values are quite similar on both technologies.

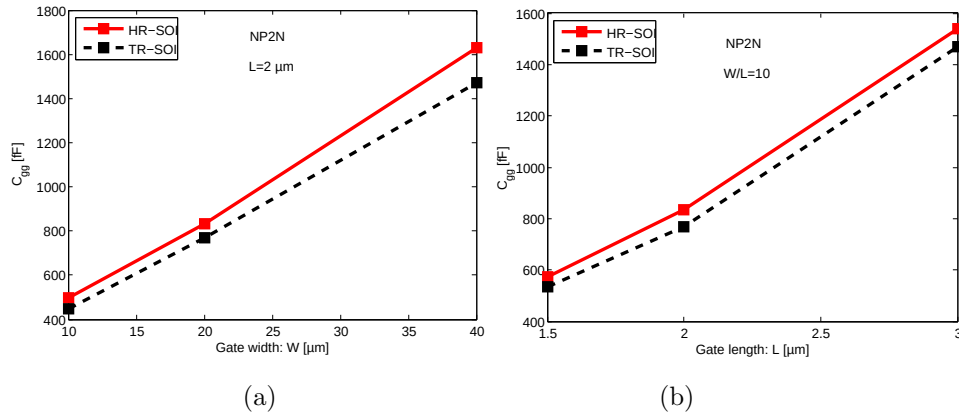


Fig. 4.27: Variation of the intrinsic parameter C_{gg} for an NP2N doping SOI MOSFET (a) over gate width W , and (b) over gate length L .

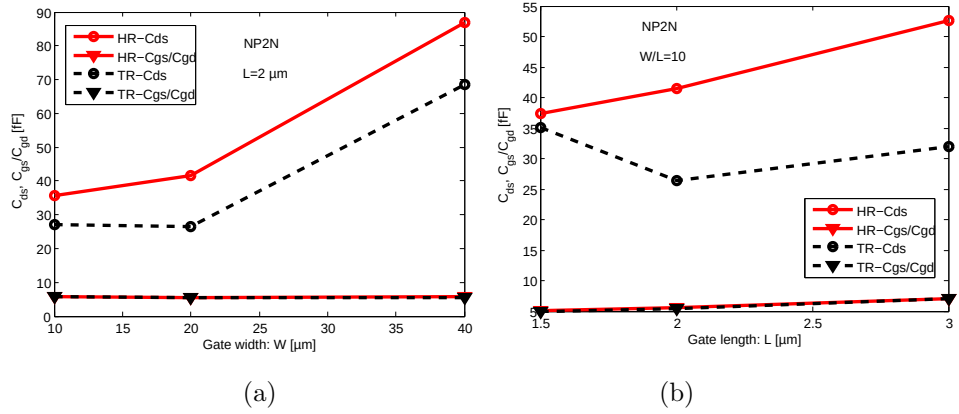


Fig. 4.28: Variation of the intrinsic parameters C_{gs}/C_{gd} for an NP2N doping SOI MOSFET (a) over gate width W , and (b) over gate length L .

Extrinsic and Intrinsic equivalent circuit model parameters

wafer	Doping	Lg (μm)	W (μm)	Rg (Ω)	Rd (Ω)	Rs (Ω)	Rsd (Ω)	Cgs (ff)	Cgd (ff)	Cgg (ff)	Cgs / Cgd	Cds (ff)	Rgsi (Ω)	Rgdi (Ω)	Gdsi (ms)	Gmi (ms)	Gmi/Gdsi	tau
HR-SOI	NP2N	1,5	15	11,9	6,37	4,83	11,2	477	95	572	5,02	37,4	9,31	42,2	0,513	8,95	17,44	10,8
HR-SOI	NiN	1,5	15	12,7	6,54	4,81	11,35	524	102	626	5,13	38,9	5,88	37,4	1,29	12,6	9,76	8,16
HR-SOI	NP2N	2	40	19,8	3,22	2,7	5,92	1390	243	1630	5,72	86,9	7,98	40,4	1,06	19,7	18,58	15,8
HR-SOI	NP2N	2	20	12,3	6,35	5,34	11,69	707	127	834	5,57	41,5	10,7	39,2	0,259	9,2	35,52	16,5
HR-SOI	NiN	2	20	13,3	5,81	4,71	10,52	813	143	956	5,68	38,2	6,14	32,3	1,07	13,8	12,89	11,2
HR-SOI	NP2N	2	10	4,68	15,2	11,5	26,7	424	72,4	496	5,85	35,8	16,7	118	0,347	4,55	13,11	14,5
HR-SOI	NP2N	3	30	11,5	7,5	6,96	14,46	1350	193	1540	6,99	52,7	12,8	48,4	0,229	9,85	43,01	30,8
HR-SOI	NiN	3	30	12,4	5,71	5,1	10,81	1570	226	1800	6,94	45,9	7,46	43,4	1,11	16,5	14,87	18,6
TR-SOI	NP2N	1,5	15	12,7	5,75	4,6	10,35	445	89	534	5,00	35	9,8	30,4	0,6	9	15	11,1
TR-SOI	NiN	1,5	15	13,7	6,19	4,76	10,95	483	96,2	579	5,02	34,5	5,79	26,5	1,3	12,2	9,38	8,38
TR-SOI	NP2N	2	40	21,9	2,74	2,44	5,18	1250	223	1470	5,60	68,4	7,03	18,6	1,07	22,2	20,74	15,4
TR-SOI	NP2N	2	20	13	5,71	5,14	10,85	648	119	767	5,44	26,4	12,3	42	0,479	9	18,78	15,9
TR-SOI	NiN	2	20	14,3	5,33	4,57	9,9	752	137	889	5,49	35,1	6,13	23,9	1,38	14,2	10,29	10,9
TR-SOI	NP2N	2	10	5,2	13,1	10,7	23,8	384	65	449	5,90	27	17	72,5	0,16	4,5	28,12	16,5
TR-SOI	NP2N	3	30	12,3	7	6,58	13,58	1290	181	1470	7,12	32	13,1	34,9	0,387	10	25,84	29,7
TR-SOI	NiN	3	30	12,9	5,5	5,04	10,54	1480	215	1700	6,88	41	7,63	32,8	1,2	16,3	13,58	18,7

Table 4.2.: Summary of the extracted extrinsic and intrinsic equivalent circuit parameters for the investigated FD SOI MOSFETs on HR-SOI and TR-SOI technologies.

4.3 SUBSTRATE CROSSTALK AND DIGITAL SUBSTRATE NOISE ISSUES

Reduction of the coupling through the substrate and isolation are critical areas of concern for RF SoC applications. SOI CMOS technology has stimulated the trend to integrate RF analog circuits with baseband digital circuitry onto silicon substrate. However, hybrid systems fabricated on Si based substrates suffer from substrate coupling due to the impact of digital switching noise. Voltage variations into silicon substrate propagate to the area of sensitive analog/RF circuits and interfere with their operation [41]. The degree of coupling among various silicon process depends on device type (passive elements, nMOS, pMOS, ...) and wafer type/structure (bulk, SOI, ...) [42]. Isolation between analog and digital parts with guard rings [43], metal Faraday cages [44], buried layers or deep n-well trenches and separation of the supply nets are methods to reduce coupling mechanisms through the common substrate [45, 46].

4.3.1 Substrate crosstalk on TR-SOI

The experimental crosstalk structure used to investigate substrate coupling consists of two identical metallic pads embedded in a coplanar structure for RF probe measurements, which represent the noisy aggressor and the victim, as shown in the insight of Fig. 4.29. The rectangular metallic pad size is of $50\text{ }\mu\text{m}$ (W) $\times$ $150\text{ }\mu\text{m}$ (L), and they are spaced by $50\text{ }\mu\text{m}$ (S). The efficiency of the TR-SOI is assessed by measuring the crosstalk level (S_{21}) in the frequency range of 10 MHz up to 25 GHz. A pure capacitive coupling is depicted in Fig. 4.29 for TR-SOI with a characteristic 20 dB/dec slope over the whole frequency range. A reduction by more than 15 dB is observed at 100 MHz for TR-SOI at 0 V compared with the HR-SOI counterpart where conductive effects in the substrate associated with parasitic surface conduction at the SiO_2/Si interface increases RF substrate losses. Such highly conductive layer underneath the BOX was modelled by an inversion resistance on p-type oxidized HR-Si substrate as in Section 2.3.1. The crosstalk level decreases for negative bias as a deep depletion is formed below the BOX, whereas it is enhanced and exhibits higher cut-off frequency for positive bias where the accumulation increases below the oxide. Such bias dependency is totally suppressed on TR-SOI wafer, thanks to the high density of traps which stabilize the whole wafer and show a pure capacitive coupling behaviour over the measurable frequency range [12]. As previously investigated in Chapter 2 in Section 2.3.2, the trap-rich HR-Si substrate can really be considered as lossless Si-based substrate and was modelled by a simple pure capacitive network.

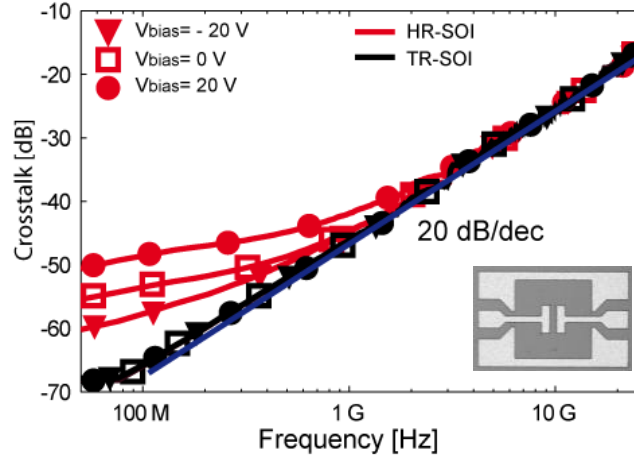


Fig. 4.29: Measured crosstalk vs frequency on HR-SOI and TR-SOI substrates under different front bias conditions.

4.3.2 Impact of Digital substrate noise on FD SOI MOSFET RF performances

Design of mixed-signal ICs and SoC applications suppose the resolution of coupling challenges of the significant digital switching noise which is injected into and propagate through the shared substrate degrading the performance of analog/ RF blocks. The generated digital noise expands from few hundreds of kHz to several MHz, corresponding to multiples of the clock signal. The distribution of the clock peaks current generates a considerable amount of the substrate noise strongly coupled via junction capacitances and capacitive coupling between source/drain, the back gate node and the substrate. The propagation of substrate noise through HR-SOI and TR-SOI is investigated by measuring the frequency spectra at the MOSFET's drain when a clock noise is injected in the vicinity of the transistors via a metallic pad 350 μm away from the device.

The test structure consists of a metallic pads located at a fixed distance from a intrinsic doped (NiN) FD SOI n-MOSFET (see Fig. 4.30). The 350 μm distance between the noise injection RF pads and the transistor was calculated based on the minimum distance, fixed by the design rules to separate two orthogonal RF pads, which is 200 μm for our 3-port RF measurement setup. The on-wafer measurements were performed using a Cascade Probe station with an Agilent E8267D RF generator which provide a 900 MHz RF input signal at -7 dBm and Agilent E4440A spectrum analyzer connected to the drain output port. The measurements of the digital substrate noise were performed in the saturation regime ($V_{GS} = 2$ V, and $V_{DS} = 1.5$ V). We consider such region as the “on state” of the transistor which gives the maximum of g_m and thus the highest f_T .

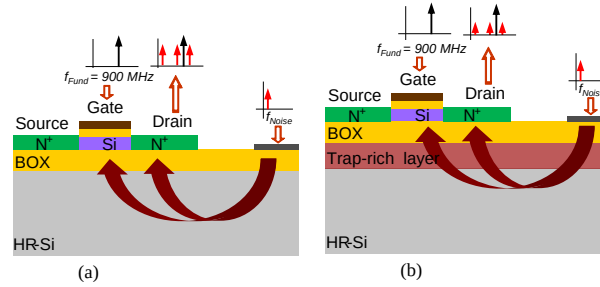


Fig. 4.30: Cross-section of the FD SOI MOSFET transistors with noise pad on (a) HR-SOI and (b) TR-SOI wafers.

The conclusions are the same if the transistor is biased in linear regime.

A Keithley K2636A pulse source-meter generates either digital or sinusoidal 5 V peak-to-peak AC signal as shown in the setup Fig. 4.31. A DC voltage source-meter was coupled via a bias T with $V_{DC} = -10$ V to set a deep depletion region underneath the BOX.

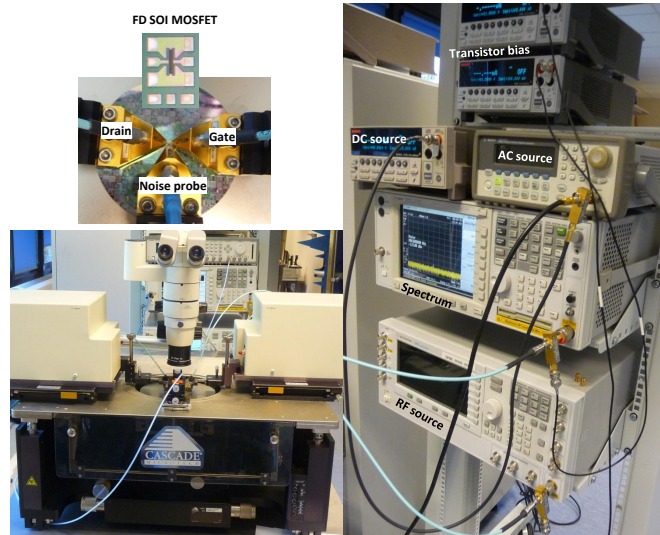


Fig. 4.31: On wafer probe station with substrate noise injection setup.

Firstly we considered only the digital or sinusoidal noise source injected via a coplanar RF probe, and we measured the spectrum of the transmitted noise

signal at the drain node. The transistor is biased at saturation whereas the RF input signal is turned OFF.

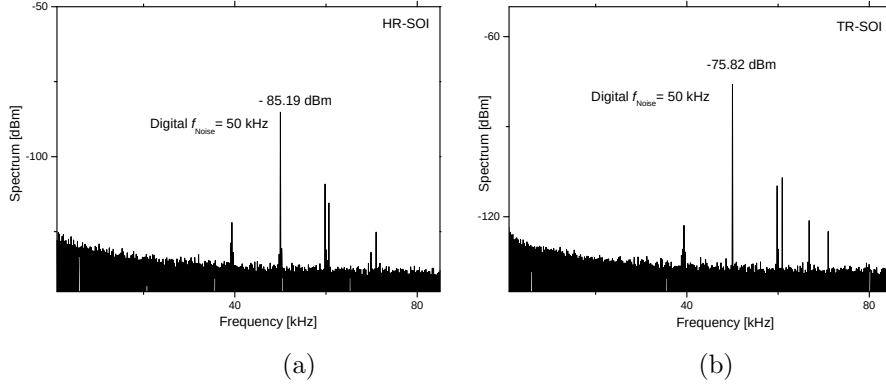


Fig. 4.32: Frequency spectrum of measured digital noise signal on (a) HR-SOI and (b) TR-SOI substrates at clock frequencies of 50 KHz.

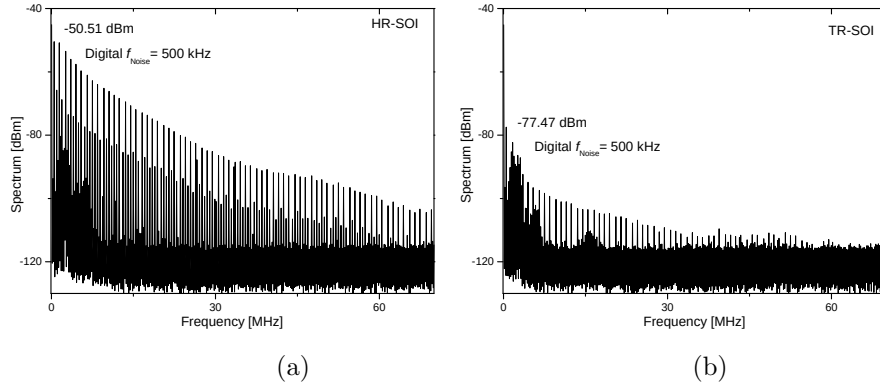


Fig. 4.33: Frequency spectrum of measured digital noise signal on (a) HR-SOI and (b) TR-SOI substrates at clock frequencies of 500 kHz.

Fig. 4.33 shows the directly coupled digital noise signal when the RF input signal is OFF. A clock noise frequency of 500 kHz (5 V peak-to-peak) is injected through the noise RF pads faraway 350 μm from the transistor. The recorded output spectrum is measured at the drain port of the transistor. Although it was expected that at such low frequencies the BOX layer of the SOI technology provides a high isolation level, the presence of highly conductive surface layer at the BOX/HR-SOI interface leads to coupling and propagation of the large noise signal. However, in the case of TR-SOI wafer in Fig. 4.33 (b) the directly coupled

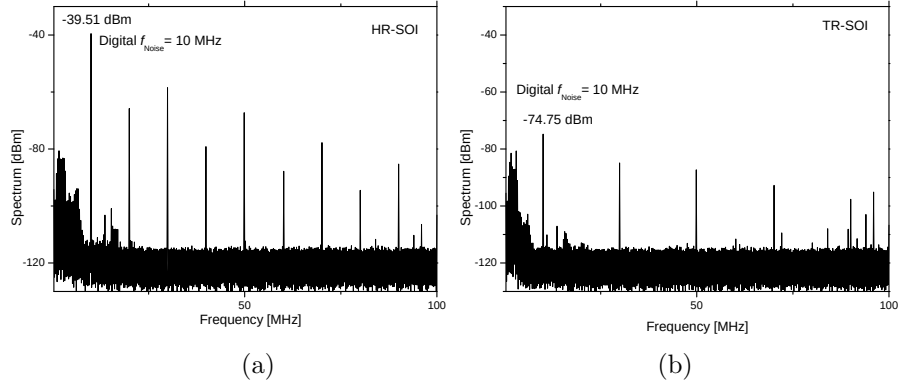


Fig. 4.34: Frequency spectrum of measured digital noise signal on (a) HR-SOI and (b) TR-SOI substrates at clock frequencies of 10 MHz.

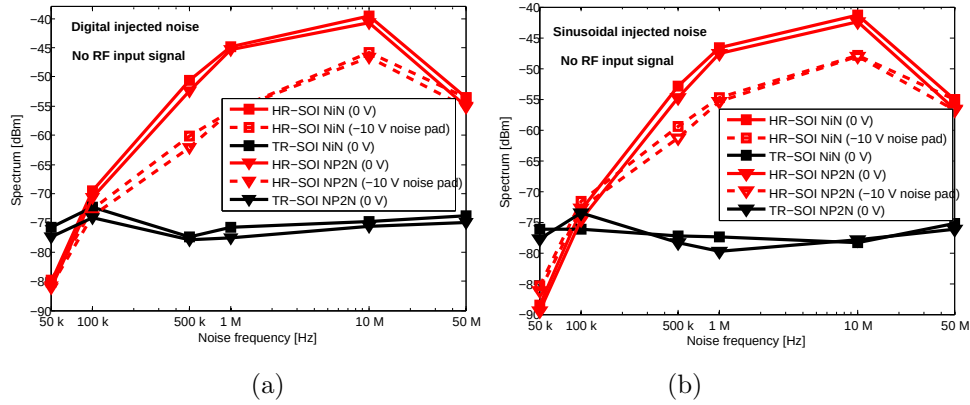


Fig. 4.35: Power levels of the digital (a) and sinusoidal (b) noise frequencies injected nearby NiN and NP2N FD SOI MOSFETs on both HR-SOI and TR-SOI wafers when RF input signal is OFF.

noise is highly reduced. The largest noise peak at 500 kHz is -50.51 dBm whereas it is reduced to -77.47 dBm on TR-SOI. The power level of the coupled noise is reduced by more than 25 dBm when the square noise frequency varies from 500 kHz up to 50 MHz as depicted in 4.35, (a) for digital and (b) for sinusoidal noise sources. A deep depletion is formed under the BOX when a negative DC bias is added to the clock frequency, therefore the coupled noise decreases by 10 dBm comparing to its level at 0 V which is in good correlation with previous results using a passive crosstalk structure (as observed in Fig. 4.29).

It is interesting to note that the magnitude of the noise coupling depends on the distance between the noise source (aggressor) and the victim. However, the main

purpose of our analysis was to evaluate the relative impact of the trap rich layer on the substrate noise coupling. The comparison between the values obtained with HR SOI and TR SOI is of interest, knowing that the absolute values will vary with the distance between the noise injection RF pads and the transistor.

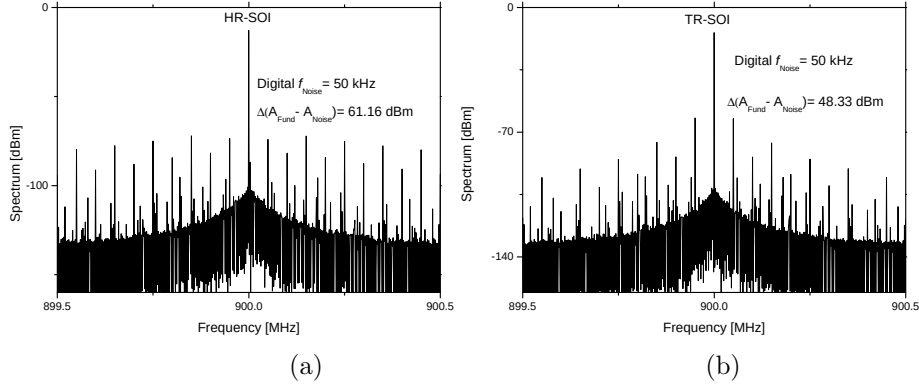


Fig. 4.36: Output spectrum around 900 MHz for FD SOI MOSFET on (a) HR-SOI and (b) TR-SOI when noise frequency of 50 kHz is injected.

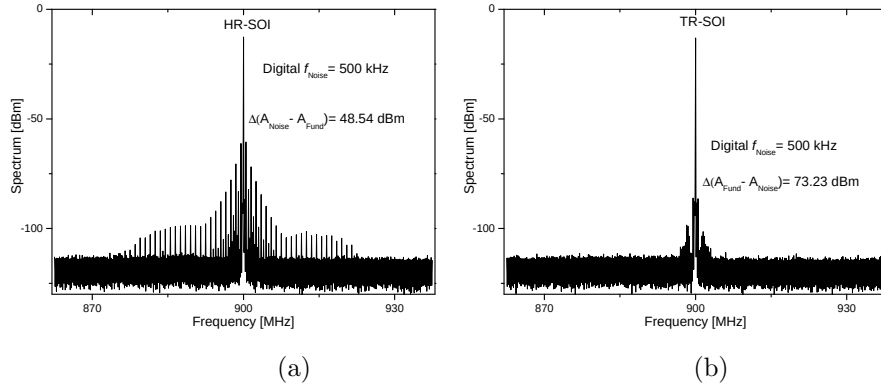


Fig. 4.37: Output spectrum around 900 MHz for FD SOI MOSFET on (a) HR-SOI and (b) TR-SOI when noise frequency of 500 kHz is injected.

The digital substrate switching noise generates a mixing product with a fundamental f_c input RF signal applied at the gate of the transistor. The injected digital noise near to the active device generates N harmonics $f_c - N \times f_{noise}$ and $f_c + N \times f_{noise}$ as shown in Fig. 4.34. By measuring the difference between the fundamental 900 MHz input signal amplitude and the injected noise amplitude Fig. 4.37 shows a reduction by more than 25 dB on the TR-SOI wafer compared

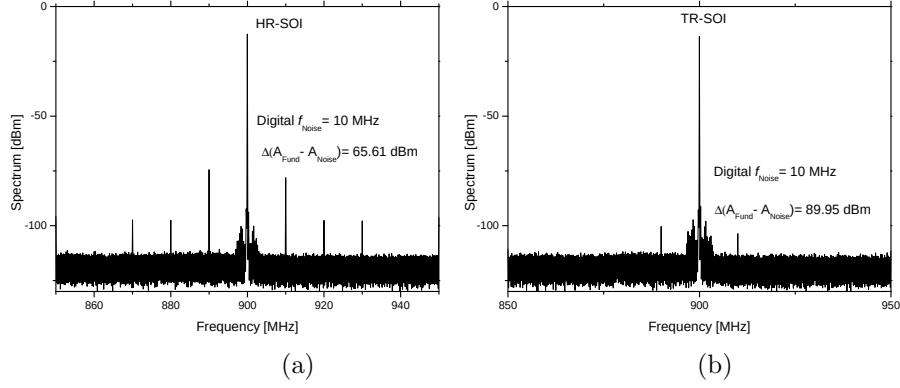


Fig. 4.38: Output spectrum around 900 MHz for FD SOI MOSFET on HR-SOI (a) and TR-SOI (b) when noise frequency of 10 MHz is injected.

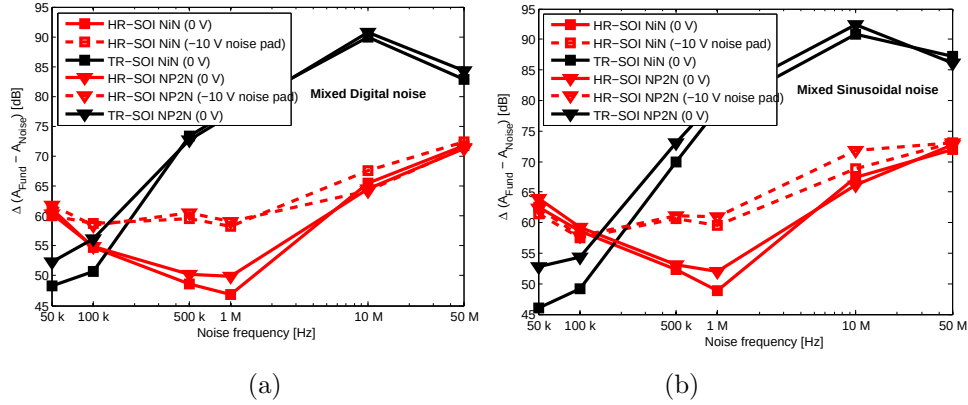


Fig. 4.39: Power level differences between RF input 900 MHz and f_{Noise} amplitudes on HR-SOI and TR-SOI wafers at each noise frequency (a) mixed digital noise and (b) mixed sinusoidal noise.

to its initial HR-SOI counterpart when a 500 kHz square signal of 5 V peak-to-peaks is injected. The generation of these mixed products of the RF input and noise signal at the drain output node can be explained by the substrate noise coupled at the back-gate of the FD SOI transistor which modulates its active zone.

The detected mixed noise level over a clock frequency range from 50 kHz up to 50 MHz is reduced by more than 20 dB as shown in Fig. 4.39 which confirms the efficiency of the commercially available TR-SOI substrate to reduce the switching noise between digital and analog/RF blocks on the same chip. However, at low noise frequencies below 200 kHz the coupled signal is much higher on TR-SOI

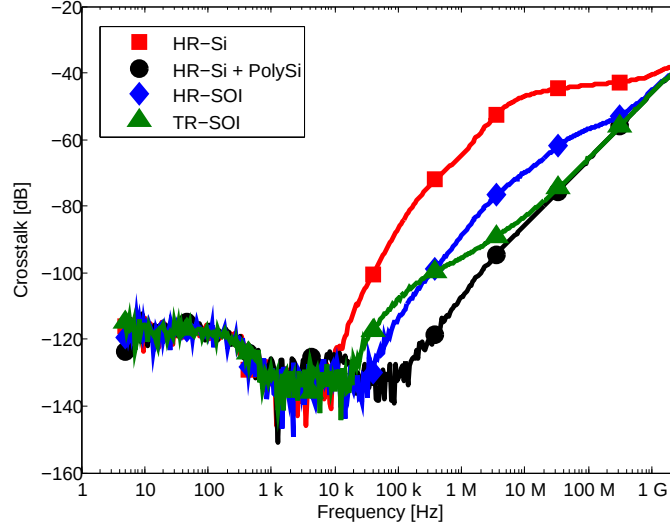


Fig. 4.40: Low frequency measured crosstalk on HR-SOI and TR-SOI substrates.

than in HR-SOI. Such results correlate with crosstalk measurement in Fig. 4.40 where the trap-rich passivated wafer show a conductive behaviour with a cut-off frequency close to 200 kHz. While the buried oxide layer is supposed to provide good isolation and reduced crosstalk on both SOI wafers, it is seen that TR-SOI add a resistive behaviour at low frequencies. However, this conductive behaviour at lower frequencies was not depicted on HR-Si wafer passivated using a trap-rich polysilicon layer deposited by LPCVD technique at 625 °C. We claim that the trapping capabilities of TR-SOI wafers is reduced due to the thermal budget of SOI CMOS smart-Cut process where the different annealing steps could affect the trap-rich layer topology and thus reducing its traps density.

4.4 CONCLUSIONS

By comparing RF performance of HR-SOI and TR-SOI technologies we aim to show the improvement in terms of insertion loss reduction for CWP lines, electrical crosstalk and linearity of the silicon-based substrates. In fact, measurement results indicate a significant improvement such as reduced substrate RF losses by more than 0.3 dB/mm on TR-SOI wafer compare with HR-SOI. The correlation between the substrate effective resistivity and the generated harmonic distortion along a CPW line demonstrated the efficiency of a TR-SOI substrate as a viable solution for RF front modules integration. Passive elements including inductors, capacitors, filters and interconnections are essential in integrated RF FEM. As such passive element occupy substantial area, it is

critical to reduce losses, non-linearity and substrate coupling that degrade RF performance of these passive components. The non-linearity of the substrate sensed through a thick-metal spiral inductor structure was investigated. Small- and large-signal measurement indicate a significant improvement in the quality factor as well as reduction of the non-linearity behaviour on trap-rich passivated wafer compare to its HR-Si counterpart. Such improvement enables to build high performance matching networks, couplers and active circuits such a VCO and multi-band power amplifiers on top of quasi-lossless TR-SOI substrate.

The excellent matching between the experimental static and RF characteristics of measured FD SOI MOSFETs on top of HR-SOI and TR-SOI wafers clearly demonstrate that it does not alter the DC or RF behaviour of SOI MOS transistors. The main variation of V_{th} , g_{mmax} , and f_T more related to the process variability rather than the presence of traps underneath the BOX.

Using UCL academic CMOS process we only designed n-type fully depleted (FD) MOSFET to check the CMOS compatibility and performance of active devices on TR-SOI wafers. Actually, we are currently investigating commercial n-type and p-type MOS devices with different gate geometries (gate length from 0.26 to 1 μm and gate width from 2 to 10 μm). The preliminary results confirm that the transistor behaviour (n- or p-type) is not affected by the presence of traps underneath the BOX.

As the trap-rich introduced layer is deposited underneath the BOX, to further stabilize the whole handle substrate, reducing the BOX thickness has no significant effect on the measured substrate losses as previously investigated in Roda-Neve PhD thesis [47]. However, the coupling effect and the substrate non-linearity increase when the oxide thickness is scaled down. On another hand, it would be interesting to note that thanks to the thin BOX, the back-gate control schemes has demonstrated a tremendous improvement in ultra-thin silicon thick (UTB SOI) and thin buried oxide SOI (UTBB SOI) devices [24]. The trap-rich technology enables the integration of a localized doped silicon film underneath the buried oxide that can be used as back-gate control of UTBB transistors.

The efficiency of TR-SOI to reduce substrate crosstalk and digital switching noise is demonstrated. A reduction by more than 15 dB is achieved at 100 MHz for TR-SOI compare with HR-SOI in terms of substrate crosstalk. The trap-rich HR-Si substrate can really be considered as lossless Si-based substrate with RF performance comparable to GaAs and sapphire types of substrates.

With its linear behaviour and an adequate level of isolation, TR-SOI technology could be considered as an excellent solution for integration of highly performance passive elements, analog/RF and digital circuits in RF FEM for SoC applications.

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CHAPTER 5

EFFECT OF TEMPERATURE ON RF PERFORMANCES OF HR-SI, TRAP-RICH HR-SI, HR-SOI, TR-SOI AND POROUS SI BASED SUBSTRATES

THE evolutionary demand to co-integrate complex high-speed digital circuits with high performance RF analog and RF MEMS devices on the same chip have resulted in the need to develop CMOS compatible substrate technology. In addition there is a concerted efforts and research to develop wireless sensors that operate in harsh environment for monitoring electric machinery, automotive, aerospace engine monitoring [1, 2]. These systems will utilize robust and efficient high power devices that are operable over an extended temperature range (-55°C to 200°C). For most the commercially available Si-based integrated circuits the maximum rated ambient temperature is 85°C which is sufficient for portable, communication and computing product applications. Military and automotive applications are typically rated to 125°C [3]. High temperature effects in bulk CMOS technology is a major concern due to leakage current that contribute to higher junction temperature. As digital and RF/analog blocks are built on the same substrate the interconnection temperature and power dissipation increase. Buried insulator layer in Silicon-on-Insulator technology greatly reduces the leakage path associated with the drain and source p-n junctions and extend the operating temperature in the range of 300°C [4, 5]. SOI structure provides also improved latch-up immunity which increases the reliability of the circuit operation at higher temperature. Another major advantage of SOI over bulk-Si technology as was already mentioned in the first chapter is its compati-

bility with high-resistivity substrates.

The previous chapter has described RF losses, non-linearity and substrate coupling effects on commercially available [6] HR-SOI and trap-rich SOI (TR-SOI) wafers before and after CMOS process.

In this chapter focus is put on low and high temperature effects on the RF performance of Si-based substrates. Table 5.1 summarizes the different investigated substrates through this chapter. In the first section, substrate RF losses, non-linearity and crosstalk on oxidized n-type HR-Si and trap-rich HR-Si wafers are investigated by means of experimental and simulation results over a large temperature range from -120°C upto 255°C , and compared with lossless quartz substrate used as a reference. Next, the RF performance as function of temperature of commercial n-type HR-SOI and TR-SOI wafers which received a standard clean-room process [7] are compared with oxidized HR-Si wafers with and without a passivation polysilicon layer. Then, we aim to investigate the RF properties of HR-SOI and TR-SOI substrates after a standard CMOS process at extreme temperature operation. As already mentioned in the previous chapter, the trap-rich HR-SOI technology is compatible with the CMOS process thermal budget. The efficiency of TR-SOI technology will be investigated by means of experimental small and large-signal measurement at low and high temperature. Another CMOS compatible substrate that consists of locally grown thick porous Si (PSi) on bulk standard Si wafers is described in the last section of this chapter. Small and large-signal high frequency measurements as function of high temperature on trap-rich HR-Si, porous Si substrates are compared with their corresponding initial HR-Si and standard-Si substrates, respectively.

5.1 RF CHARACTERIZATION OF HR-SI AND TRAP-RICH HR-SI SUBSTRATE AT AMBIENT TEMPERATURE

5.1.1 Substrate losses and non-linearity

The first three wafers in Table 5.1 were processed using a standard clean room process. A set of CPW lines with characteristic impedance of $50\ \Omega$ were fabricated on top of oxidized HR-Si substrate ($4\ \text{k}\Omega\cdot\text{cm}$), with and without a passivation polysilicon layer as shown in Fig. 5.1. The 400 nm-thick trap-rich layer was fabricated by low-pressure-chemical-vapour-deposition (LPCVD) at 625°C . A 50 nm-thick oxide layer was grown on top of the Si wafers by wet thermal oxidation at 950°C . RF performance of these oxidized HR-Si and HR-Si + PolySi wafers will be compared with a reference quartz lossless and linear substrate. The strip, slot and planar ground widths of the $1\ \mu\text{m}$ -thick aluminium CPW lines were 26, 12 and $208\ \mu\text{m}$, respectively.

On-wafer RF small-signal measurements were made using an Agilent PNA-X vector network analyzer [8] from 10 MHz up to 26.5 GHz. A set of a specific de-embedding structures are used for accurate device parameters extractions. The attenuation and effective resistivity of the investigated substrates are

Wafers	Thermal oxide thickness t_{SiO_2} (nm)	Trap-rich		Maximum annealing Temperature	PSi thickness (μm)	Si		
		Type	Thickness (nm)			Type	Thickness (μm)	ρ ($\Omega\cdot\text{cm}$)
HR-Si	50			950 °C		N	525	> 4 k
HR-Si + PolySi	50	LPCVD PolySi	400	950 °C		N	525	> 4 k
Quartz	750 μm							
HR-SOI without CMOS	400			Smart Cut™ thermal budget		N	725	> 3 k
TR-SOI without CMOS	400	Not Available	2000	Smart Cut™ thermal budget		N	725	> 3 k
HR-SOI after CMOS	400			CMOS process thermal budget		N	725	> 3 k
TR-SOI after CMOS	400	Not Available	2000	CMOS process thermal budget		N	725	> 3 k
Std-Si	500			950 °C		P	525	0.005
HR-Si	500			950 °C		N	515	> 4 k
HR-Si + PolySi	500	LPCVD PolySi	500	950 °C		N	515	> 4 k
Porous Si (PSi)	500			950 °C	200	P	525	0.005

Table 5.1.: Investigated wafers description, thickness and type of layers.

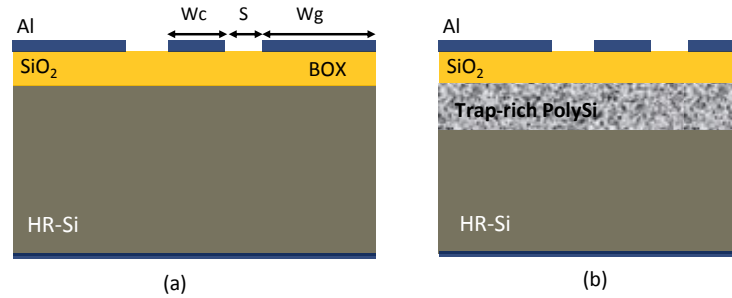


Fig. 5.1: Schematic of a CPW transmission line fabricated on (a) a HR-Si and (b) Trap-Rich Si substrates.

extracted from the measured S-parameters using the method described in [9]. Fig. 5.2 (a) shows the measured attenuation of a 2,146 μm -long CPW line at room temperature and zero bias, on top of HR-Si, trap-rich HR-Si and quartz substrates. The passivated HR-Si + PolySi wafer shows the lowest attenuation level. The CPW lineic losses are reduced by more than 0.3 dB/mm at 5 GHz on trap-rich HR-Si compare with the initial HR-Si handle wafer. The substrate losses are reduced when a highly density of traps freezes the excess carriers

attracted at the top of Si surface by the positively charged fixed oxide charges. The same CPW line structure was simulated using 2D physics ATLAS Silvaco simulator [10] on n-type HR-Si with nominal resistivity $\rho = 4k\Omega\text{.cm}$ (defined by a donor doping value $N_d = 1.1 \times 10^{12}/\text{cm}^3$). As was investigated in Lederer [11] and Roda-Neve [12] PhD thesis, the oxide charges located at the Si-SiO₂ interface are the main contributors to the creation of an accumulation or inversion layer below the oxide, depending on the type of the Si substrate. A fixed charge density of $Q_f = 10^{11}/\text{cm}^2$ is considered in our simulations which create an non-homogeneous highly conductive accumulation layer that describes the parasitic conduction effect on oxidized HR-Si substrate. The introduction of high density of traps was simulated using two different ways. The first approach considers the introduction of high-enough density of interface traps $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$ to overcome the parasitic surface effect. Interface defect traps are activated at a discrete energy levels within the bandgap of the semiconductor Si substrate. The second approach consists on introducing a 400 nm-thick PolySilicon layer where an energy distribution of defect states in the bandgap of the polysilicon material is defined. The defect states within the polysilicon layer are defined by the sum of two exponential tail distributions near the conduction and valence bands and two deep levels with Gaussian distribution [10]. Typical polysilicon parameters that provide better qualitative description are summarized in Table 5.2.

Using AC analysis in Atlas simulator the capacitance and conductance data are calculated. The attenuation, characteristic impedance of the CPW line and the effective resistivity are then extracted using RLCG model as explain in Chapter 3. Simulated CPW lines attenuation in Fig. 5.2 (b) shows a reduction by more than 50 % when interface traps or polysilicon layer with defect states is introduced underneath the oxide layer.

The extracted effective resistivity ρ_{eff} sensed by the CPW line from measurement and simulation results fall down to less than 200 $\Omega\text{.cm}$ on oxidized HR-Si substrate compared with its initial nominal 4 k $\Omega\text{.cm}$ resistivity as shown in Fig. 5.3 (a) and (b), respectively. Such reduction of the effective resistivity is mainly caused by the highly conductive accumulation layer at the Si-SiO₂ interface simulated by the introduction of fixed charges density Q_f . As explained in Section 2.2 the accumulation layer underneath the oxide drastically decreases the resistivity of the substrate and spreads over a depth of approximately 3 μm . The results presented in Fig. 5.3 clearly indicate that thanks to the introduction of a high density of interface traps or defect states formed in the polysilicon layer the nominal high resistivity of the initial HR-Si wafer is fully recovered.

The characterization of the non-linear properties of HR-Si with and without the passivation layer and quartz substrates is achieved using an one-tone characterization setup based on a 4-port Agilent PNA-X vector network analyzer (VNA). An input 900 MHz signal with a power level from -25 to 25 dBm is

Parameters	Description	Values	Units
mun	Electrons mobility	300	cm^2/Vs
mup	Holes mobility	30	cm^2/Vs
NTA	Density of acceptor-like states in the tail distribution at the conduction band edge.	10^{21}	cm^{-3}/eV
NTD	Density of donor-like states in the tail distribution at the valence band edge	10^{21}	cm^{-3}/eV
WTA	Characteristic decay energy for the tail distribution of acceptor-like states	0.033	eV
WTD	Characteristic decay energy for the tail distribution of donor-like states	0.049	eV
NGA	Total density of acceptor-like states in a Gaussian distribution	1.5×10^{17}	cm^{-3}
NGD	Total density of donor-like states in a Gaussian distribution	1.5×10^{17}	cm^{-3}
EGA	Energy that corresponds to the Gaussian distribution peak for acceptor-like states. This energy is measured from the conduction band edge	0.62	eV
EGD	Energy that corresponds to the Gaussian distribution peak for donor-like states. This energy is measured from the valence band edge.	0.78	eV
WGA	characteristic decay energy for a Gaussian distribution of acceptor-like states	0.15	eV
WGD	characteristic decay energy for a Gaussian distribution of donor-like states	0.15	eV

Table 5.2.: Polysilicon parameters used in Atlas simulator.

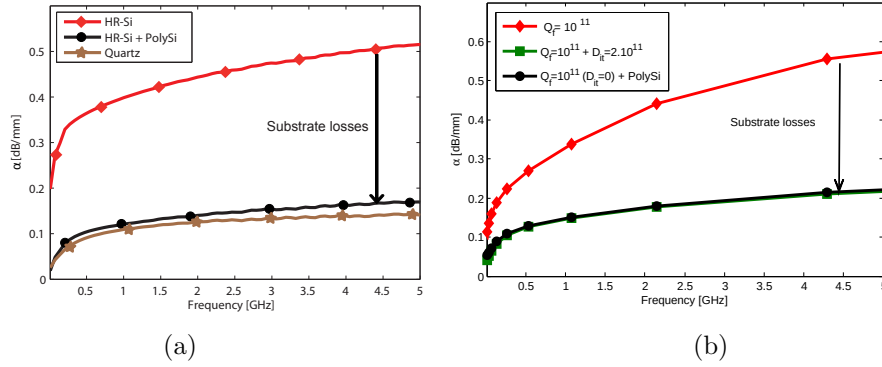


Fig. 5.2: (a) Measured CPW lines lineic losses on HR-Si, HR-Si + 400 nm-thick PolySi and quartz substrates, (b) Simulated CPW lines lineic losses on HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$), HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$, HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + 400 nm-thick PolySi substrates at ambient temperature.

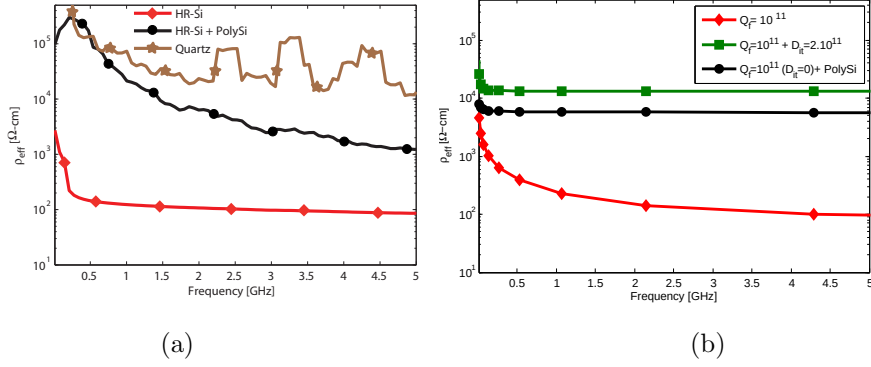


Fig. 5.3: (a) Measured effective Si resistivity of CPW lines on HR-Si, HR-Si + 400 nm-thick PolySi and quartz substrates, (b) Simulated effective Si resistivity of CPW lines on HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$), HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2 \cdot 10^{11}/\text{cm}^2/\text{eV}$, HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + 400 nm-thick PolySi substrates at ambient temperature.

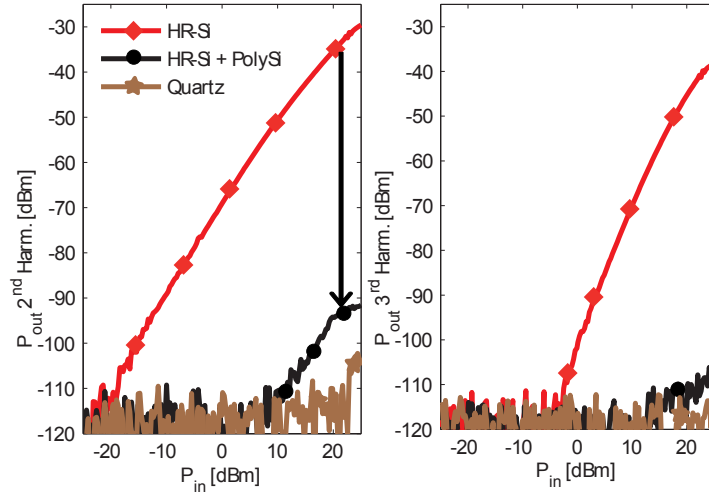


Fig. 5.4: Harmonic distortion for a input signal at 900 MHz of a 2,146 μm -long CPW line on HR-Si, HR-Si + 400nm-thick PolySi and quartz substrates at ambient temperature.

injected into the CPW line and the output generated harmonics are detected. Fig. 5.4 shows the 2nd and 3rd harmonic distortions which correspond to the levels of signal power at 2nd and 3rd times of the fundamental signal frequency

generated due to non-linearity of the substrate. CPW lines on oxidized HR-Si wafer present significant harmonic level, -30 dBm at an input power of + 25 dBm. The 2nd harmonic distortion on the passivated wafer is reduced by more than 60 dB at + 25 dBm compare with the non passivated HR-Si substrate as depicted in Fig. 5.4. The introduction of the trap-rich passivation layer reduces the CPW line losses and harmonic distortions, fully recovering the HR-Si characteristics of the substrate.

5.1.2 Substrate crosstalk on HR-Si and HR-Si + PolySi wafers at ambient temperature

The experimental crosstalk test structure consists of two identical rectangular metallic pads ($50 \times 150 \mu\text{m}$) spaced by $50 \mu\text{m}$ and embedded in a coplanar structure for RF probe measurement as shown in the inset of Fig. 5.5 (a). The coupled electrical signal through the common substrate is assessed by measuring the crosstalk level (S_{21}). As previously investigated in Chapter 2 the substrate crosstalk behaviour was modelled by a lumped equivalent circuit where the S_{21} curves on oxidized HR-Si wafer presents a conductive and capacitive coupling zones above 10 MHz as show in Fig. 5.5 (a). A flat response zone describes the conductive behaviour at the Si-SiO₂ interface as demonstrated by simulating the same crosstalk structure on oxidized HR-Si substrate when including a certain density of oxide charges $Q_f = 10^{11}/\text{cm}^2$ as shown in Fig. 5.5 (b). As previously obtained from small-signal measurement using CPW lines, the low extracted effective resistivity on oxidized HR-Si substrate confirms the impact of the highly conductive accumulation layer underneath the oxide to increase the substrate coupling effect. The reduction of the crosstalk levels is achieved by the introduction of interface traps or defect states in a 400 nm-thick polysilicon layer. Measurement and simulation results presented in Fig. 5.5 (a) and (b), respectively, show a pure capacitive coupling with a characteristic of 20 dB/dec slope over the whole frequency range [13], similarly to the lossless reference quartz wafer. The crosstalk is further reduced due to the lower dielectric constant of quartz (3.7). Indeed, to further reduce the substrate coupling effect at higher frequencies other substrates with lower permittivity than that of Si should be used. The passivated HR-Si handle wafer was modelled by a simple capacitive lumped equivalent model as described in Section 2.3.2. We note that the fluctuations in the measurement results on passivated HR-Si and quartz wafers are mainly related to the experimental setup errors at frequencies below 40 MHz.

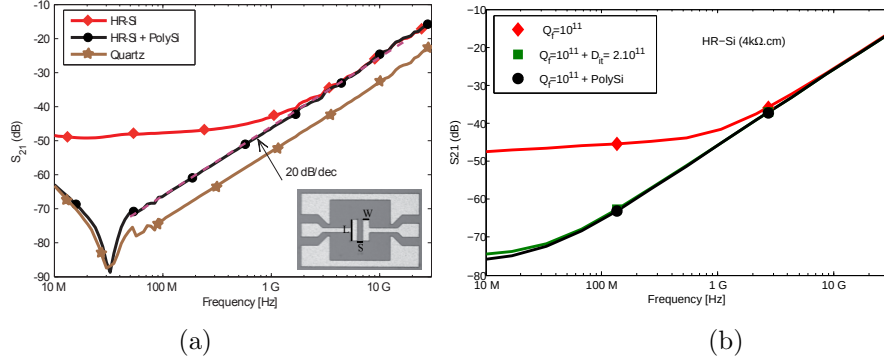


Fig. 5.5: (a) Measured Substrate crosstalk on HR-Si, HR-Si + 400nm-thick PolySi and quartz substrates, (b) Simulated Substrate crosstalk on HR-Si (4 kΩ.cm, $Q_f = 10^{11}/cm^2$), HR-Si (4 kΩ.cm, $Q_f = 10^{11}/cm^2$) + $D_{it} = 2.10^{11}/cm^2/eV$, HR-Si (4 kΩ.cm, $Q_f = 10^{11}/cm^2$) + 400 nm-thick PolySi substrates at ambient temperature.

5.2 HR-SI, TRAP-RICH HR-SI AND QUARTZ SUBSTRATES RF PERFORMANCE AT LOW AND HIGH TEMPERATURES

The influence of temperature on the lineic CPW lines losses, effective resistivity and non-linearity behaviour of HR-Si substrate with and without passivation polysilicon layer can be used to expect the RF performance of these substrates for high temperature RF applications. To this end, small and large signal measurements were performed on oxidized HR-Si, passivated HR-Si and quartz substrates as function of temperature and on wafer measurements were made over the temperature range from -120°C upto 255°C .

For high temperature control a Temptronics 8-inch thermo-chuck is provided (see Fig. 5.6). Ground-signal-ground (GSG) ($150\ \mu\text{m}$ -pitch) high frequency Z probes from SüssTM are used for signal measurements over the temperature range from 25°C upto 255°C . The wafer chuck is set to the desired temperature and held constant for 15 min to allow the substrate to be at a uniform temperature. A thru-reflect-line (TRL) [14, 15] calibration is performed at each temperature to eliminate the pad parasitics and obtain the intrinsic S-parameters of the DUT.

A cryogenic LakeShore Model CRX-4K on wafer probe station is used to measure large and small-signal RF characteristics of passive CPW lines and crosstalk structures. Fig. 5.7 shows the cryogenic measurement setup, where we used nitrogen to cooldown the temperature at -120°C .



Fig. 5.6: On-wafer probing with Temptronics High Temperature control station.

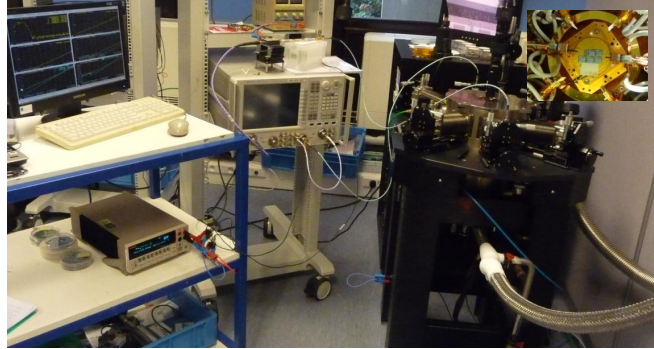


Fig. 5.7: Cryogenic measurement setup.

5.2.1 Substrate losses, effective resistivity and non-linearity variation with temperature

The variation of the lineic losses at 5 GHz for a temperature range from -120°C to 255°C is represented in Fig. 5.8 (a). The results of 2 D numerical simulations in Fig. 5.8 (b) on HR-Si ($4\text{ k}\Omega\cdot\text{cm}$) that include a constant fixed charge density of $Q_f = 10^{11}/\text{cm}^2$ with and without an interface traps density are in good agreement with measurement results.

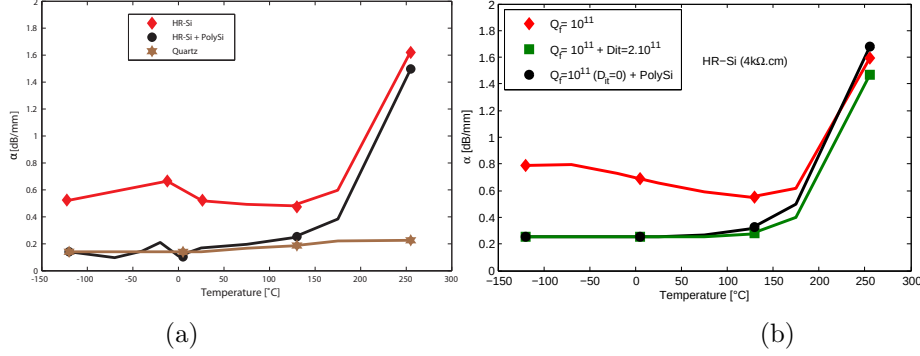


Fig. 5.8: (a) Measured variation of lineic losses at 5 GHz of a 2,146 μm -long CPW line on HR-Si, HR-Si + 400nm-thick PolySi and quartz substrates, (b) Simulated variation of lineic losses at 5 GHz of a 2,146 μm -long CPW line on HR-Si (4 k Ω .cm, $Q_f = 10^{11}/\text{cm}^2$), HR-Si (4 k Ω .cm, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2 \cdot 10^{11}/\text{cm}^2/\text{eV}$, HR-Si (4 k Ω .cm, $Q_f = 10^{11}/\text{cm}^2$) + 400 nm-thick PolySi substrates with temperature.

The losses increase with respect to temperature due to the increase of intrinsic carriers $n_i(T)$ in the substrate as shown in equation 5.1. Where E_g is the silicon band gap, k is Boltzmann's constant and q is the electron charge.

$$n_i(T) = 3.3 \times 10^{15} T^{\frac{3}{2}} \exp\left(-\frac{E_g}{2kT}\right) \quad (5.1)$$

The majority carriers concentration given by the equation 5.2, indicate that the majority carriers density is defined by the doping level at lower temperatures, whereas at certain high temperature value it becomes equal to n_i (increasing function of T) leading to silicon intrinsic properties [16].

$$n = n_i \exp\left(\frac{q\phi_F}{kT}\right) = \frac{N_d + \sqrt{(N_d)^2 + 4n_i^2}}{2} \quad (5.2)$$

As the temperature increases the impact of the interface traps is lowered. In fact, lineic losses of the CPW line on the trap-rich substrate is as lower as 0.3 dB/mm up to 175 °C, while it increases rapidly for higher temperatures. The trap-rich passivation layer is efficient for trapping the mobile carriers generated at the Si/SiO₂ interface and not in the substrate volume. The trapping capabilities of the passivated HR-Si substrate are maintained when handle wafer is cooled down, whereas for oxidized HR-Si substrate an increase RF losses is depicted which can be explained by an increase of carriers mobility at cryogenic temperatures.

The effect of low and high temperature on HR-Si and HR-Si + PolySi substrates as function of frequency are shown in Fig. 5.9 and Fig. 5.10, respectively.

Both HR-Si and HR-Si + PolySi show a slight increase of CPW lineic losses upto 175 °C. Beyond this temperature both wafers behave as low resistivity substrate with high RF losses because of the increase of the mobile carriers density.

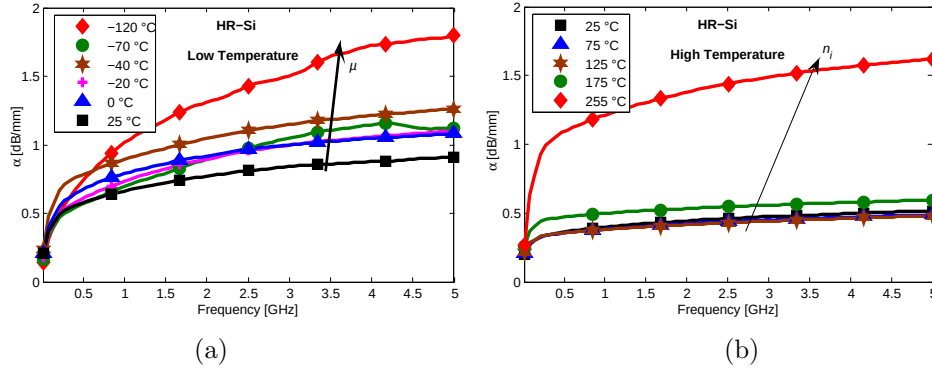


Fig. 5.9: Measured lineic losses of a 2,146 μm -long CPW line on HR-Si substrate (a) at low temperature and (b) at high temperature.

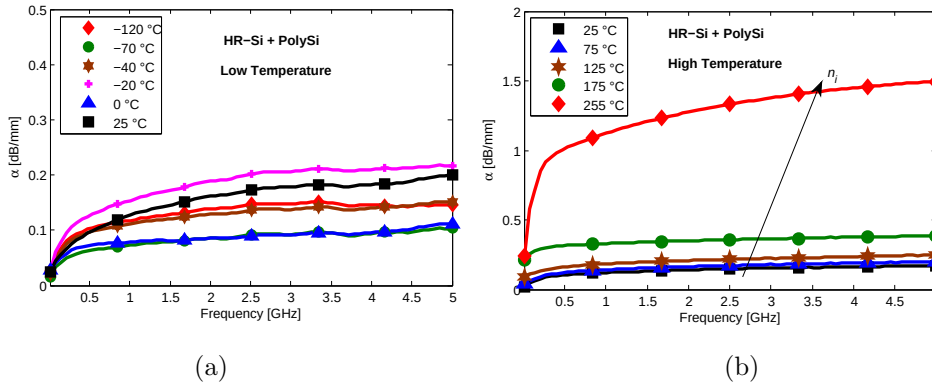


Fig. 5.10: Measured lineic losses of a 2,146 μm -long CPW line on HR-Si + 400nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

The measured lineic losses on quartz wafer in Fig. 5.11 outlines the increase of conductor losses with temperature, which increases the total lineic losses of the CPW line.

The simulated lineic losses on HR-Si at low and high temperature conditions as function of frequency, when considering a fixed charge density of $Q_f = 10^{11}/\text{cm}^2$, in Fig. 5.12 is in perfect agreement with measurements shown in Fig. 5.9. Nevertheless, when introducing a high density of interface traps $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$,

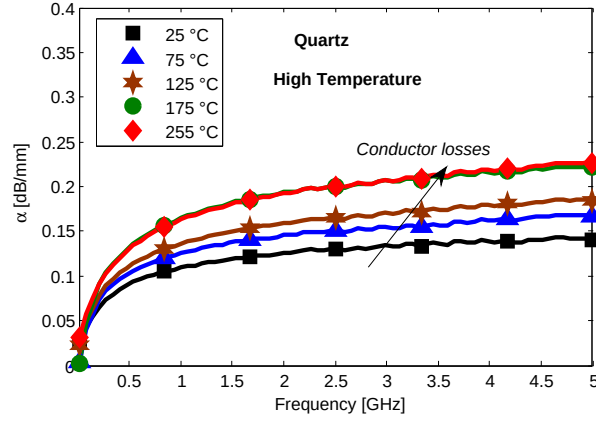


Fig. 5.11: Measured lineic losses of a 2,146 μm -long CPW line on quartz substrate at high temperature.

or considering a 400 nm-thick polysilicon layer, only high temperature condition has an impact on carriers distributions and trapping properties as displayed in Fig. 5.13 and 5.14, respectively. Substrate losses increases beyond 175 °C, as depicted from measurement results and was mainly attributed to the increase of substrate carriers concentration.

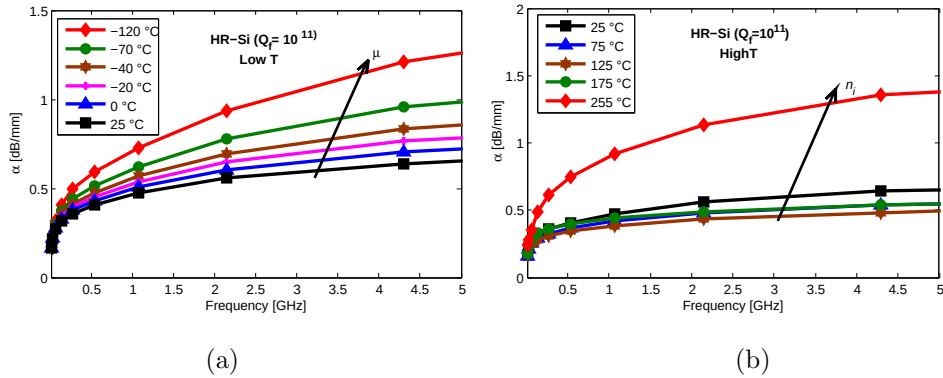


Fig. 5.12: Simulated lineic losses of a 2,146 μm -long CPW line on HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) substrate (a) at low temperature and (b) at high temperature.

The extracted effective resistivity from measurement and simulations results on the investigated substrates in Fig. 5.15 (a) and (b), respectively, show a good agreement. Indeed, ρ_{eff} on HR-Si wafer without polySi exhibits lower values either at high temperature or at low temperature going down from 207 $\Omega\cdot\text{cm}$ at

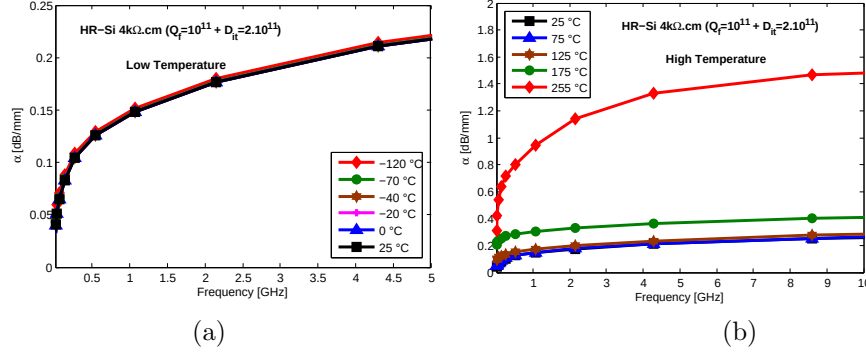


Fig. 5.13: Simulated lineic losses of a 2,146 μm -long CPW line on HR-Si (4 $\text{k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$ substrate (a) at low temperature and (b) at high temperature.

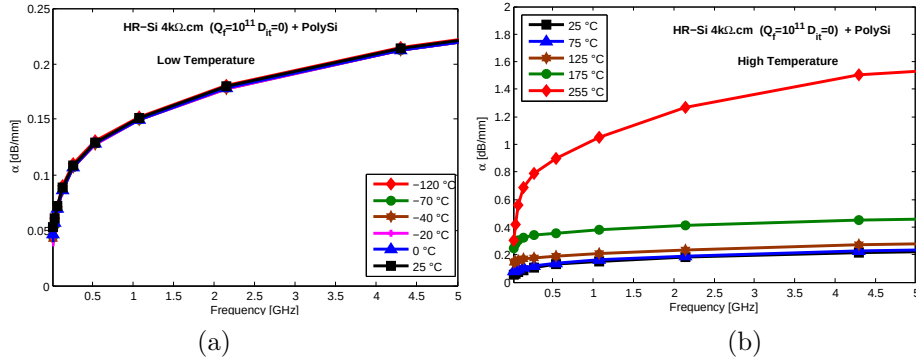


Fig. 5.14: Simulated lineic losses of a 2,146 μm -long CPW line on HR-Si (4 $\text{k}\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$, $D_{it} = 0$) + 400 nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

ambient temperature to less than 20 $\Omega\cdot\text{cm}$ at -120°C and 255°C as can be seen in Fig. 5.16 (a) and (b), respectively. Such reduced effective resistivity is mainly related to the increase of carriers inside the substrate at higher temperature [17], whereas the mobility increases at lower temperature. The effective resistivity and thus substrate RF losses become independent on the doping level of the handle wafer. These measured results are in good agreement with simulated effective resistivity at low and high temperature conditions on HR-Si substrate considering the effect of a fixed charge density and without interface traps as observed in Fig. 5.18 (a) and (b), respectively.

The trap-rich passivated substrates effective resistivity remains as high as 1 $\text{k}\Omega\cdot\text{cm}$ (i.e., the substrate remains quasi-lossless) for lower temperature condi-

tions from -120°C upto 135°C which suggests that the efficiency of the introduced high density of interface traps is enough to maintain the high resistivity properties of the trap-rich HR-Si wafer. As the temperature increases beyond 135°C the effective resistivity decreases to the intrinsic properties of the Si substrate as depicted in Fig. 5.17 (a) and (b), respectively. Simulated effective resistivity on oxidized HR-Si with a trap-rich layer was achieved by considering two methods, one using a high density of interface traps and the second by simulating a 400 nm-thick trap-rich polysilicon layer underneath the oxide. A high and low temperature, the two methods qualitatively agree with the measurement results as can seen in Fig. 5.19 when considering interface traps and in Fig. 5.20 simulating a trap-rich polysilicon layer.

The high resistivity observed on passivated wafer is explained by the trapping of most of mobile carriers at grain boundaries, leaving few of them to contribute to the conduction. As the temperature increases, the number of trapped carriers does not increase appreciably resulting in sharp reduction in effective resistivity. The electrical conduction properties in polycrystalline silicon is influenced by carrier trapping at the grain boundaries [18]. Indeed, the high concentration of defects and dangling bonds at the grain boundaries provides a high density of trapping states that creates a potential barriers which impede the transport of free carriers between the grains.

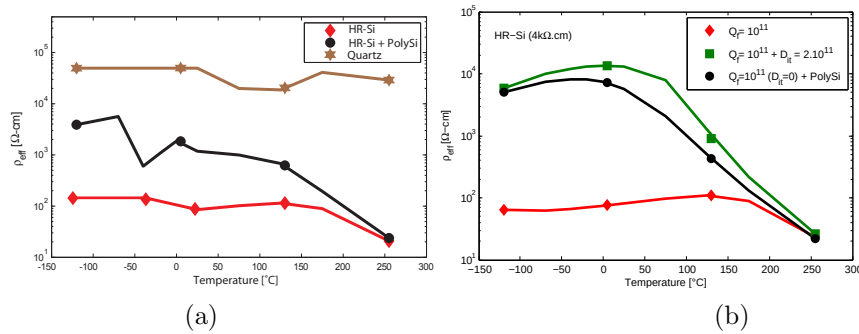


Fig. 5.15: (a) Measured variation of the effective resistivity at 5 GHz of a 2,146 μm -long CPW line on HR-Si, HR-Si + 400 nm-thick PolySi and quartz substrates, (b) Simulated variation of the effective resistivity at 5 GHz of a 2,146 μm -long CPW line on HR-Si (4 k $\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$), HR-Si (4 k $\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$, HR-Si (4 k $\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + 400 nm-thick PolySi substrates with temperature.

To further analyze the electrical and physical behaviour of oxidized HR-Si substrates with and without trap-rich passivation layer as function of temperature effect, a simple MOS structure was simulated using Atlas simulator. The multilayer structure consists of a 50 nm-thick oxide layer on top of 300 μm -thick HR-Si substrate and top and back aluminium bias electrodes as seen in the inset

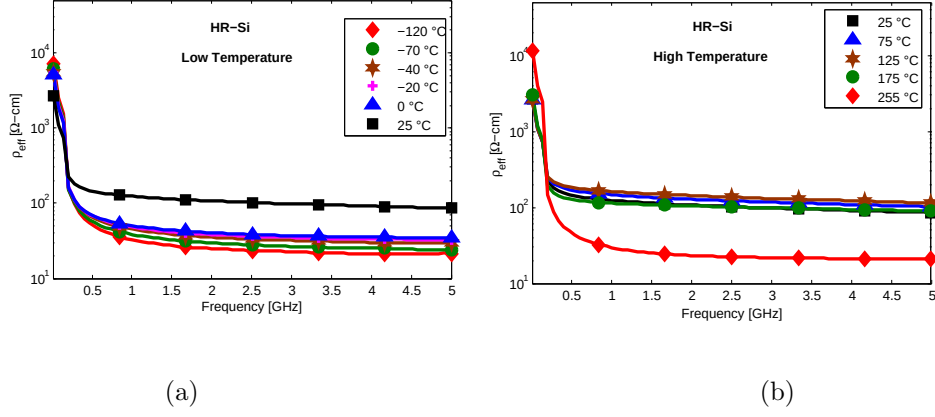


Fig. 5.16: Measured effective resistivity of a 2,146 μm -long CPW line on HR-Si substrate (a) at low temperature and (b) at high temperature.

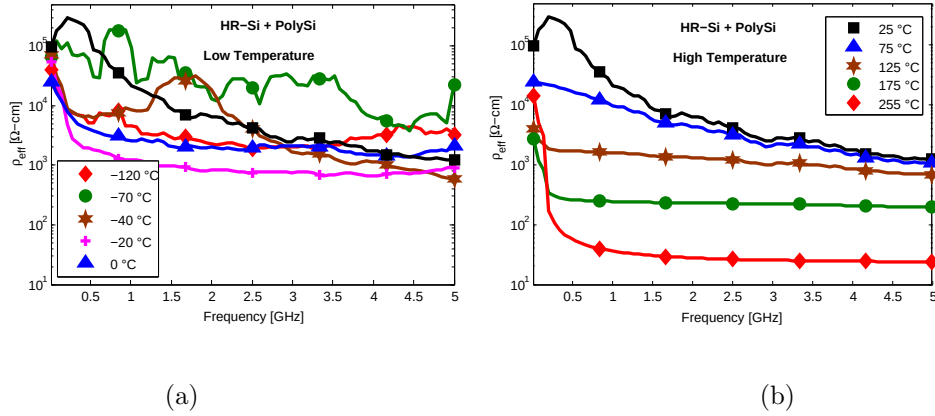


Fig. 5.17: Measured effective resistivity of a 2,146 μm -long CPW line on HR-Si + 400 nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

of Fig. 5.21. The n-type doping value of $N_d = 1.1 \times 10^{12}/\text{cm}^3$ correspond to a resistivity of 4 $\text{k}\Omega.\text{cm}$. The resistivity profile versus depth of the substrate is extracted using the equation 5.3.

$$\rho(x, y) = \frac{1}{\sigma(x, y)} = \frac{1}{q(p(x, y) \cdot \mu_p(x, y) + n(x, y) \cdot \mu_n(x, y))}, \quad (5.3)$$

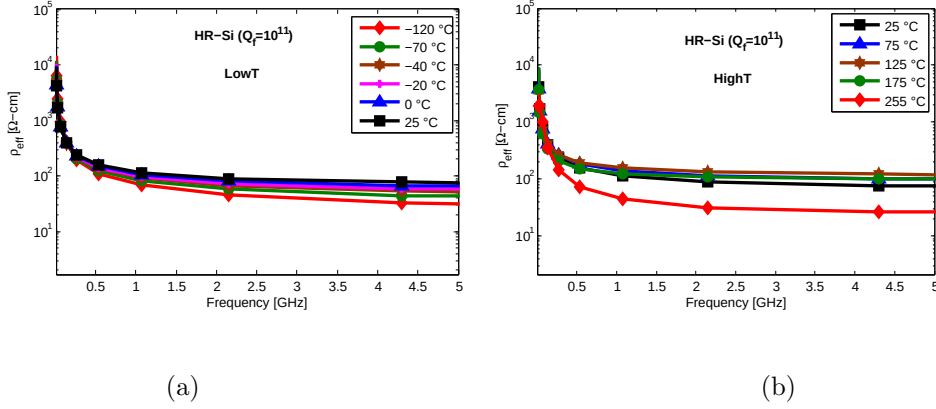


Fig. 5.18: Simulated effective resistivity of a 2,146 μm -long CPW line on HR-Si (4 k $\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) substrate (a) at low temperature and (b) at high temperature.

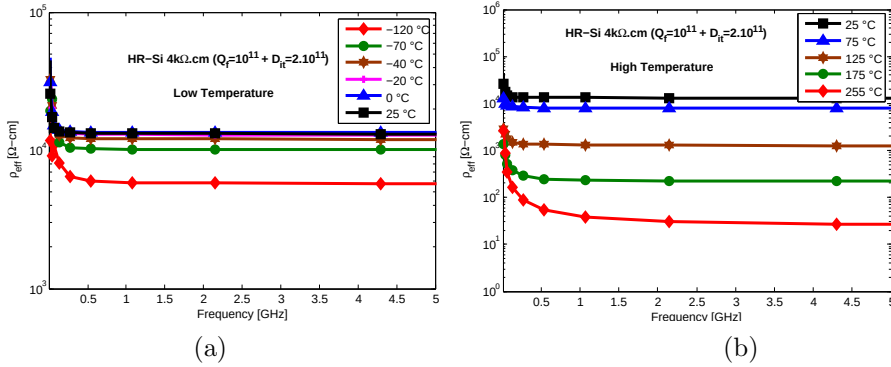


Fig. 5.19: Simulated effective resistivity of a 2,146 μm -long CPW line on HR-Si (4 k $\Omega\cdot\text{cm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$ substrate (a) at low temperature and (b) at high temperature.

where q is the electron charge, n and p , μ_n and μ_p the electron and hole concentration and mobility, respectively.

Because of the metal-semiconductor work-function difference and the fixed oxide charges ($Q_f = 10^{11}/\text{cm}^2$) the accumulation layer underneath the oxide drastically decreases the resistivity of the substrate over a depth of approximately 10 μm . Due to this parasitic surface conduction effect the resistivity at the substrate surface drops down to less than 10 $\Omega\cdot\text{cm}$ at ambient temperature. Fig. 5.21 (a) and (b), show the extracted resistivity vs. substrate depth at low and high temperature conditions, respectively on oxidized HR-Si substrate without interface

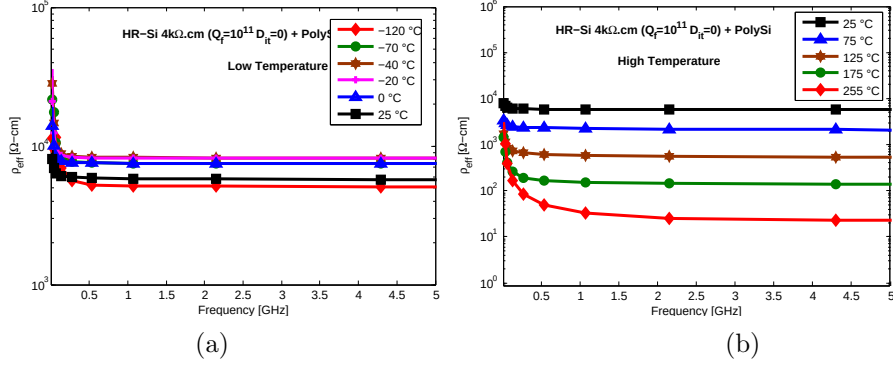


Fig. 5.20: Simulated effective resistivity of a 2,146 μm -long CPW line on HR-Si (4 k $\Omega \cdot \text{cm}$, $Q_f = 10^{11}/\text{cm}^2$, $D_{it} = 0$) + 400 nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

traps ($D_{it} = 0$). It can be seen that at cryogenic temperatures the resistivity is slowly decreased, both at the SiO_2/Si interface ($Y_I = 0.1 \mu\text{m}$) or in the substrate volume ($Y_V = 100 \mu\text{m}$), due to the increase of carriers mobility as depicted in Fig. 5.23 (b).

As the temperature increases beyond 175 °C the bulk resistivity drops to less than 200 $\Omega \cdot \text{cm}$ as can be observed in Fig. 5.21 (b), and also the depletion width underneath the oxide layer decreases due to the increment of intrinsic carrier concentration (presented in Fig. 5.23 (a)). These results are in good agreement with previous measurements and simulations of the CPW line structure on oxidized HR-Si substrate without passivation trap-rich layer.

To overcome the effect of the conductive layer underneath the oxide, a high

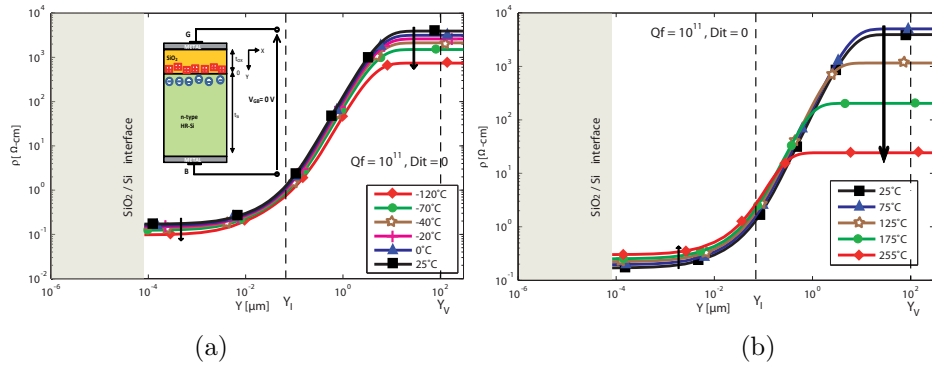


Fig. 5.21: Simulated resistivity vs. substrate depth for n-type HR-Si substrate (4 k $\Omega \cdot \text{cm}$, $t_{ox} = 50 \text{ nm}$, $Q_f = 10^{11}/\text{cm}^2$) (a) at low temperature and (b) at high temperature.

enough density of traps ($D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$) is introduced to completely absorb the accumulation layer, thereby enabling the substrate to recover its nominal resistivity. At lower temperature conditions, the increase of substrate resistivity (presented in Fig. 5.22 (a)) is directly related to the absorption of free carriers at the SiO_2/Si interface, where it can be seen that carriers concentration shown in Fig. 5.23 (b) drops when higher trap densities are present at the substrate surface ($Y_I = 0.1 \mu\text{m}$).

When the temperature increases the trap-rich passivated substrate resistivity decreases as shown in Fig. 5.22 (b). This is a direct consequence of the intrinsic carrier concentration increase inside the substrate (presented in Fig. 5.23 (a)). Even if the trap-rich passivation layer is efficient for trapping mobile carriers at the SiO_2/Si interface and not in the substrate volume, oxidized HR-Si substrate with or without traps density becomes intrinsic at higher temperature beyond 175°C . These results agree with the increased substrate losses and decreased effective resistivity extracted from CPW line characterization.

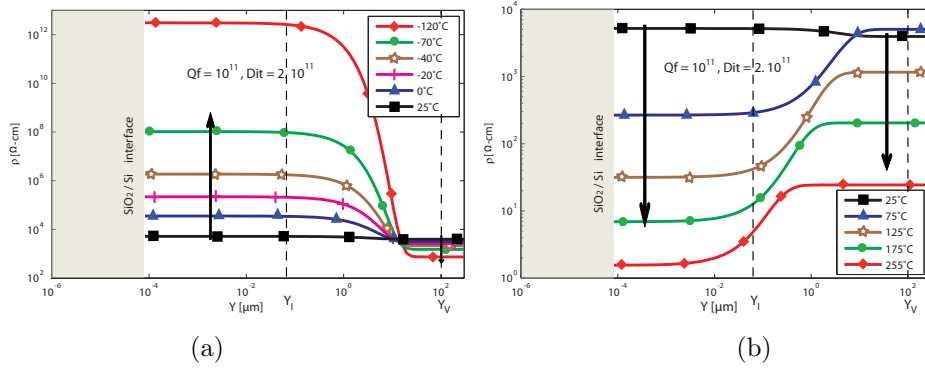


Fig. 5.22: Simulated resistivity vs. substrate depth for n-type HR-Si substrate ($4 \text{ k}\Omega\cdot\text{cm}$, $t_{ox} = 50 \text{ nm}$, $Q_f = 10^{11}/\text{cm}^2$) + $D_{it} = 2.10^{11}/\text{cm}^2/\text{eV}$ (a) at low temperature and (b) at high temperature.

Regarding the non-linear behaviour of the investigated substrates with temperature, harmonic distortion measurements were made for a fundamental tone at 900 MHz and input power sweep from -25 to 25 dBm. CPW lines on oxidized HR-Si substrate present significant 2^{nd} and 3^{rd} harmonic distortion levels at ambient temperature, but a slight variation with temperature is depicted in Fig. 5.24 (a) and (b), respectively. The variation of 2^{nd} harmonic distortion as function input power at low and high temperature is very small as presented in Fig. 5.25 (a) and (b), respectively. In correlation with measurements and simulations of the effective resistivity variation with temperature, the oxidized HR-Si wafer is considered as lossy and non-linear substrate due to the conduction effect at the Si-SiO₂ interface.

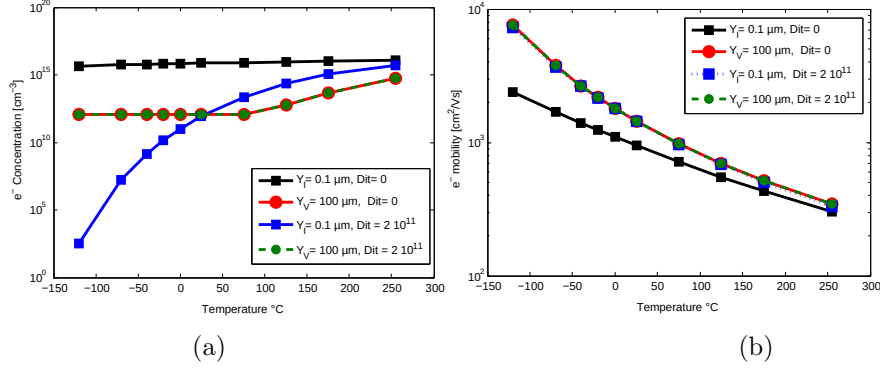


Fig. 5.23: Simulated (a) electron concentration and (b) electron mobility vs. temperature : at the SiO_2/Si interface ($Y_I = 0.1 \mu\text{m}$) and at the substrate volume ($Y_V = 100 \mu\text{m}$), for n-type HR-Si ($4 \text{ k}\Omega\cdot\text{cm}$, $t_{ox} = 50 \text{ nm}$, $Q_f = 10^{11}/\text{cm}^2$) without ($D_{it} = 0$) and with interface traps ($D_{it} = 2 \cdot 10^{11}/\text{cm}^2/\text{eV}$).

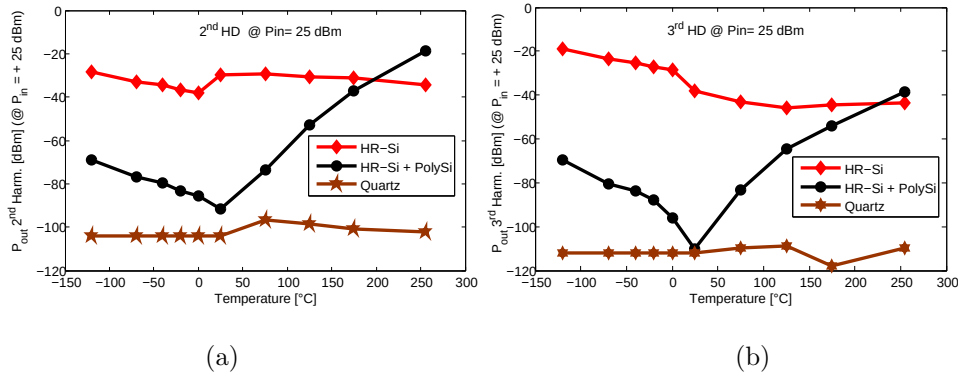


Fig. 5.24: Variation of (a) 2nd and (b) 3rd harmonic distortions with temperature of a 2,146 μm -long CPW line on the investigated substrates.

From Fig. 5.24 (a) and (b) both 2nd and 3rd harmonic distortions increase when temperature raise up or cool down on trap-rich HR-Si wafer. Although, the trap-rich passivation solution recovers the high resistivity properties and reduce the non-linearity behaviour of HR-Si wafer by more than 50 dB at ambient temperature, the trapping mechanisms inside the polysilicon layer are highly dependent on high temperature condition.

The variation of 2nd harmonic distortion as function of input power at low and high temperature on trap-rich HR-Si wafer is shown in Fig. 5.26 (a) and (b), respectively. It can be seen that higher temperature increases carriers distribution inside the substrate and thus its non-linearity.

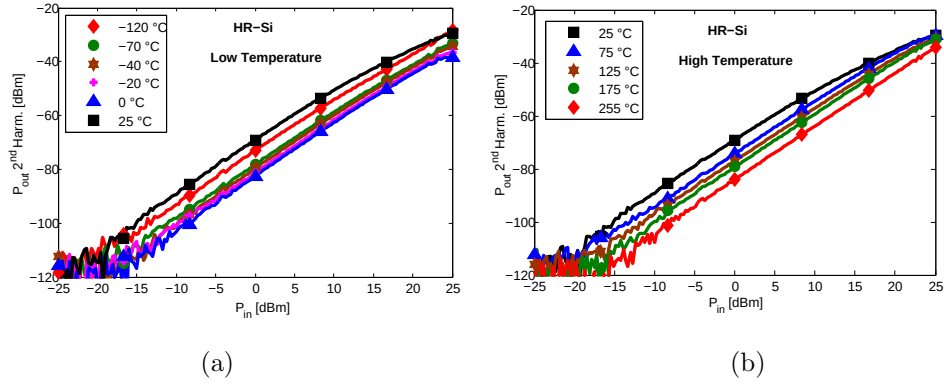


Fig. 5.25: Measured 2nd harmonic distortion of a 2,146 μm -long CPW line on HR-Si substrate (a) at low temperature and (b) at high temperature.

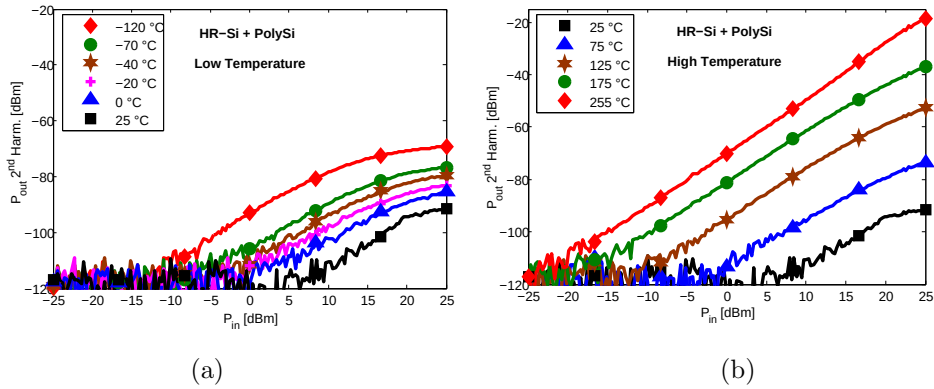


Fig. 5.26: Measured 2nd harmonic distortion of a 2,146 μm -long CPW line on HR-Si + 400nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

5.2.2 Effect of temperature on HR-Si and trap-rich HR-Si substrates crosstalk

Fig. 5.27 (a) and (b) displays the effect of low and high temperature, respectively, on substrate coupling in oxidized HR-Si wafer. The figure outlines that substrate crosstalk is temperature dependent. In fact, as the number of intrinsic carriers increases at high temperature more free carriers contribute to the conduction path between the two rectangular taps. A highly conductive flat zone describes the resistive effect associated to the substrate resistances.

Due to their high resistivity characteristics the trap-rich HR-Si exhibits a pure capacitive coupling behaviour into the substrate. With the increased temperature up to 175 °C a strong resistive coupling path occurs accurate and the efficiency of trap-rich layer is degraded as depicted in Fig. 5.28 (b). As the effective resistivity decreases at higher temperature lower than 20 $\Omega.cm$ as previously shown in Fig. 5.17 (b) the substrate coupling effect on the trap-rich passivated substrate is almost similar to the crosstalk levels on top of oxidized HR-Si wafer. As expected from CPW line measurements, the trap-rich HR-Si coupling effect exhibit no dependence with respect to the low temperature variation as presented in Fig. 5.28 (a) where a pure capacitive coupling behaviour is clearly obtained.

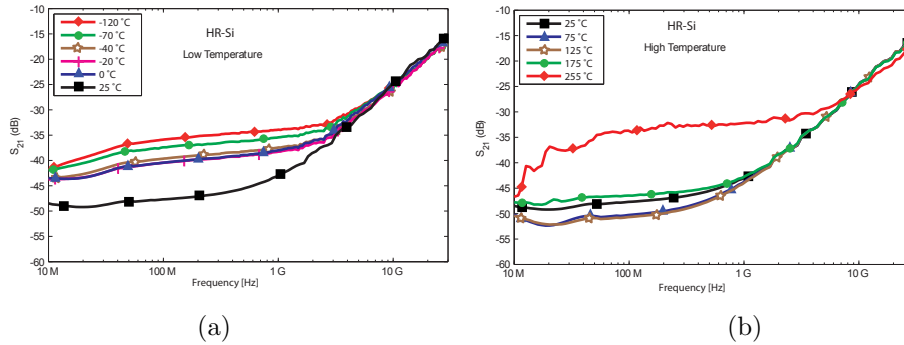


Fig. 5.27: Measured substrate crosstalk on HR-Si substrate (a) at low temperature and (b) at high temperature.

5.3 RF CHARACTERIZATION OF COMMERCIAL HR-SOI AND TR-SOI WAFERS WITHOUT CMOS PROCESS COMPARED TO HR-SI AND TRAP-RICH HR-SI WITH TEMPERATURE

It was demonstrated in the previous section by means of measurements and simulations that particularly high temperature condition degrades drastically the RF performance of passivated trap-rich HR-Si wafer. HR-SOI substrates are equivalent to the oxidized HR-Si wafers, where they share almost the same multilayer stack configuration. Moreover, on HR-SOI structure the fixed

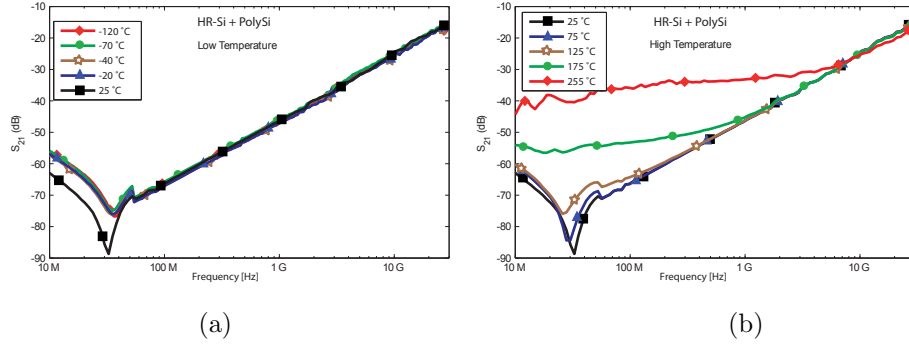


Fig. 5.28: Measured substrate crosstalk on HR-Si + 400 nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

charges in buried oxide layer (BOX) lead to a significantly high parasitic surface conduction effect at the Si-SiO₂ interface as that occurs in oxidized HR-Si substrate. However, the HR-SOI wafer provided using a smart-cut process [19] involves several annealing and bonding steps that can eventually introduce contaminants or defects at the bonding interface. A 400 nm-thick buried oxide layer is thermally grown for HR-SOI and trap-rich-SOI (TR-SOI) wafers, which corresponds to the typical value used in industrial manufacturers for RF communication systems. The thin top active silicon film is removed using TMAH (tetramethylammonium hydroxide) etching technique (10 % at 85 °C during 60 s) [20], prior to the metallization of CPW lines.

In this section, we intend to compare the effect of temperature on RF performance of oxidized HR-Si with commercial HR-SOI wafers with and without trap-rich passivation layer. All compared wafers were processed using a standard clean room process with 1 μ m-thick Al metallization and are defined as follow:

- . HR-Si: 50 nm-thick thermal oxide on top of HR-Si (4 k Ω .cm) handle substrate,
- . HR-Si + PolySi: 50 nm-thick thermal oxide + 400 nm-thick LPCVD polysilicon on top of HR-Si (4 k Ω .cm),
- . HR-SOI without CMOS: HR-SOI commercial wafer (> 3 k Ω .cm) with 400 nm-thick BOX,
- . TR-SOI without CMOS: TR-SOI commercial wafer (> 3 k Ω .cm) + 2 μ m-thick trap-rich layer with 400 nm-thick BOX.

5.3.1 RF characterization of the investigated wafers at ambient temperature

Firstly, the small and large signal measurements on the investigated substrates are compared at ambient temperature. The attenuation and effective resistivity of 2,146 μ m-long CPW line with dimensions $W = 26 \mu$ m, $S = 12 \mu$ m, and $W_g =$

208 μm are shown in Fig. 5.29 (a) and (b), respectively. Although, their initial nominal resistivity is in the same order of magnitude, substrate losses on the oxidized HR-Si is much more higher than that of the HR-SOI wafer. The thin 50 nm-thick oxide layer used in the case of oxidized HR-Si wafer with a high density of oxide charges may increase the surface conduction and thus decrease proportionally the surface resistivity. It is clear that the parasitic surface conduction effect at the Si-SiO₂ interface degrades significantly the HR properties of the oxidized HR-Si substrate leading to an effective resistivity lower than 100 $\Omega\cdot\text{cm}$ as shown in Fig. 5.29 (b). In the case of HR-SOI wafer, the quality of the grown 400 nm-thick thermal oxide was improved after the different annealing steps of the smart-cut SOI process [21]. Moreover, the fabrication steps of the latter process may introduce defects and contaminants at the bonding interfaces [22] which slow down the conductive effect at the Si-SiO₂ interface and thus increase the effective resistivity of the whole wafer.

The highly non-linear behaviour of the oxidized HR-Si wafer compared with the HR-SOI substrate shown from the 2nd and 3rd harmonic distortions in Fig. 5.30 confirms the previous results. In fact, the distortion due to the substrate non-linearities increases with the decrease of the effective resistivity extracted from the small-signal measurements. The 2nd harmonic level is 20 dB higher in the case of the oxidized HR-Si which tells us about the spatial charges distribution and thus the electric field variation inside the substrate that can be translated to a non-linear equivalent substrate conductance and capacitance of the CPW line.

The introduction of a trap-rich passivation layer reduces the PSC effect and stabilizes the whole HR-Si and HR-SOI wafers in terms of high resistivity and lowering the harmonic distortion generation. Indeed, Fig. 5.29 (a) and (b) display that HR properties of oxidized HR-Si and HR-SOI wafers are recovered and $\rho_{eff} > 3 \text{ k}\Omega\cdot\text{cm}$ at 5 GHz on TR-SOI wafer is achieved. The 2nd harmonic distortion decreases by more than 55 and 35 dB, respectively, on trap-rich HR-Si and TR-SOI wafers compared with their initial HR-Si and HR-SOI substrate. Although a thicker 2 μm -thick trap-rich layer was used for the TR-SOI wafer compared with only 400 nm-thick LPCVD polysilicon on trap-rich HR-Si wafer, substrate losses and non-linearities on the latter are the lowest. Several factors can influence the trapping capabilities of the trap-rich passivation layer, starting from the deposition techniques and post-annealing steps that impact its morphological characteristics [23]. As the traps are mostly formed at the grain boundaries where they are associated with silicon dangling bonds, the grain boundary surface has to be maximized to achieve a high trap density. Trap-rich layer with uniform small grain size and columnar structure [24] have been proven to efficiently recover the nominal resistivity of HR-Si substrate with $\rho > 5 \text{ k}\Omega\cdot\text{cm}$.

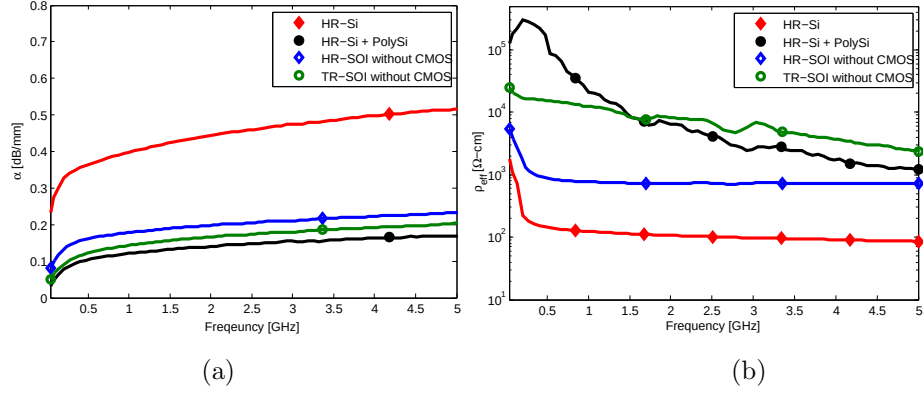


Fig. 5.29: Measured (a) CPW lines lineic losses and (b) effective resistivity on HR-Si, HR-Si + 400 nm-thick PolySi, HR-SOI and TR-SOI without CMOS process substrates at ambient temperature.

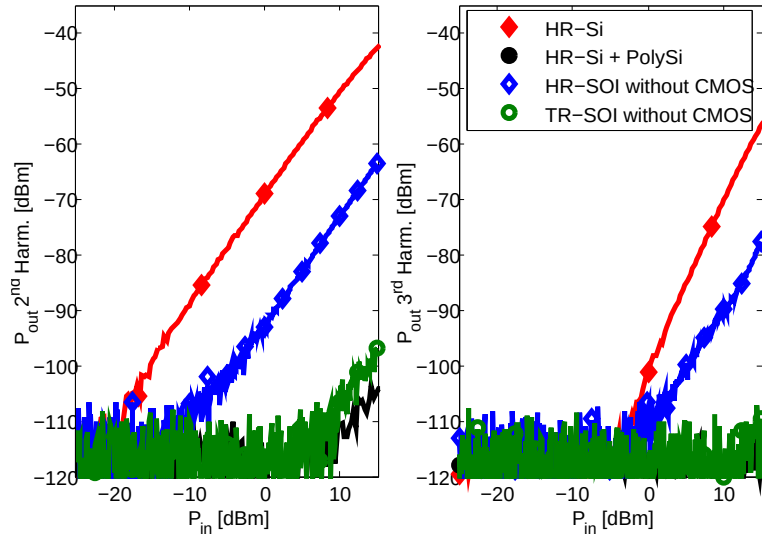


Fig. 5.30: Harmonic distortion for a input signal at 900 MHz of a 2,146 μ m-long CPW line on HR-Si, HR-Si + 400 nm-thick PolySi, HR-SOI and TR-SOI without CMOS process substrates at ambient temperature.

5.3.2 RF characterization of the investigated substrates with temperature

The capability of SOI CMOS technology to operate at large temperature range from -55°C to a practical limit of approximately 300°C has been demonstrated [25] as the best compromise for low power consumption, low leakage current, bet-

ter isolation and higher integration. This section intends to compare temperature effect on RF performance of trap-rich HR-Si and HR-SOI wafers. As previously mentioned, all wafers received a standard clean room process to pattern CPW line structures. Two different setups were used to measure small and large-signal data at low and high temperatures. Fig. 5.31 (a) and (b) display the variation of CPW line lineic losses and effective resistivity as function of temperature extracted at a constant frequency (5 GHz). Both trap-rich HR-Si and TR-SOI wafers exhibit the lowest RF losses below 175 °C (Fig. 5.29 (a)), whereas the effective resistivity is maintained higher than 1 k $\Omega.cm$ upto 125 °C (Fig. 5.31 (b)). Although, the trap-rich HR-Si wafer presents a 400 nm-thick LPCVD polysilicon passivation layer compare with 2 μm -thick trap-rich layer used for the TR-SOI wafer, the measured CPW lineic losses are slightly higher on the latter. The high annealing temperature (1,100 °C) used through the Smart-Cut SOI process [19] assures a high quality thermal oxide, whereas it regenerates partially the crystalline properties of the deposited trap-rich layer and thus reduces its trapping capability. As the temperature increases, the effective resistivity is lowered similarly on both wafers due to the increase of intrinsic carriers inside the substrate as previously explained.

Regarding non-linear behaviour of the investigated substrates, the measured 2nd

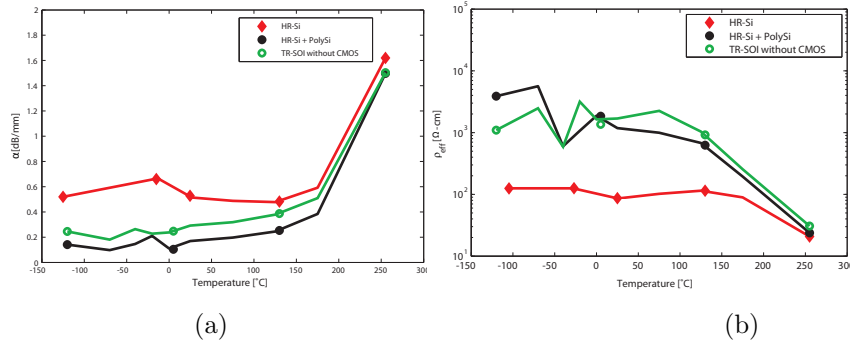


Fig. 5.31: Variation of (a) CPW lines lineic losses and (b) effective resistivity at 5 GHz of a 2,146 μm -long CPW line on HR-Si, HR-Si + 400 nm-thick PolySi, HR-SOI and TR-SOI without CMOS process substrates with temperature.

and 3rd harmonic distortion levels as function of temperature at an input power of 15 dBm in Fig. 5.32 (a) and (b) outline that substrate distortion increases at extreme temperature operation. The substrate distortion is mainly governed by the 2nd harmonic component at 1.8 GHz. From Fig. 5.32 (a), it can be observed that the harmonic distortion levels on trap-rich HR-Si and TR-SOI wafers is lower than harmonic distortion specification for RF switches [26] in the temperature range from -75 °C up to 135 °C. In correlation with previously shown effective resistivity and CPW line lineic losses variation with increased temperature, the non-linearity of the substrate increases on both trap-rich HR-Si and

TR-SOI wafers. The lower harmonic distortion levels on TR-SOI wafer compare with the trap-rich HR-Si could be related to thinner oxide layer in the case of oxidized HR-Si substrate (50 nm instead of 400 nm in the case of HR-SOI and TR-SOI substrates). At lower temperature, the increase of substrate harmonic distortion is mainly attributed to the increase of carriers mobility.

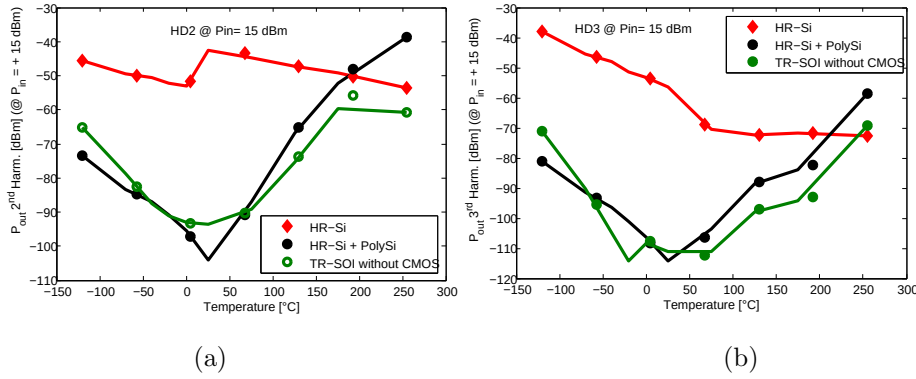


Fig. 5.32: Variation of (a) 2nd and (b) 3rd Harmonic distortions of a 2,146 μm -long CPW line on HR-Si, HR-Si + 400 nm-thick PolySi, HR-SOI and TR-SOI without CMOS process substrates with temperature.

5.4 RF PERFORMANCE OF HR-SOI AND TR-SOI WAFERS AFTER CMOS PROCESS

CMOS-SOI technology is already a leading technology in a wide range of applications, with substantial advantages compare with bulk CMOS, allowing optimization for high temperature and extremely low voltage/ low power applications. In the same time, SOI does not require major changes to the well-known and well-mastered complementary metal oxide semiconductor (CMOS) process flow. The CMOS process contains more than 8 thermal treatment steps made at temperature range from 600 °C to 950 °C. The compatibility of SOI technology with high-resistivity silicon substrates permits to realize high performance Tx/Rx switches to increase the quality factor of inductors or tunable MEMS capacitors and reduce substrate RF losses and coupling effects. However, as previously investigated in the previous Chapter, the parasitic surface conduction effect at the substrate surface due to highly conductive accumulation/inversion layer at the SiO₂-Si interface drastically degrades high resistivity properties of the HR-SOI wafer. To further improve the high frequency performance of HR-SOI substrates, commercially available trap-rich HR-SOI technology was developed [6] and proven as a promote solution to overcome the PSC effect which is inherent oxidized HR-Si wafers. It has been demonstrated from previous Chapter that

CMOS process thermal budget does not affect DC or RF performance of SOI CMOS transistors designed and processed on TR-SOI wafers [27].

Through this section, passive devices were fabricated using a standard SOI CMOS process [7] and the passivation efficiency of TR-SOI substrates will be investigated with respect to extreme temperature operation.

5.4.1 RF losses, substrate non-linearity and crosstalk at ambient temperature

A 2000 μm -long CPW line structure is used to investigate RF substrate losses and non-linearity behaviour and a two rectangular crosstalk structure with a constant spacing of 50 μm is considered. Fig. 5.33 (a) and (b) displays CPW lineic losses and extracted effective resistivity on both HR-SOI and TR-SOI wafers after CMOS process at ambient temperature. It can be seen that the introduced trap-rich layer decreases RF losses by more than 50 % and the high resistivity properties of HR-SOI handle wafer are recovered. Substrate linearity is improved on TR-SOI wafers as shown in Fig. 5.34 where the 2nd harmonic distortion level is reduced by more than 25 dB compare with the initial HR-SOI wafer. As presented in the previous Chapter from effective resistivity and non-linearity measurements, CMOS process does not affect HR properties and linearity of TR-SOI wafers in contrary to HR-SOI where its RF performance are degraded as outlined in Section 4.1.

The increased effective resistivity on TR-SOI simultaneously reduces substrate RF losses and coupling effects. This is observed from Fig. 5.35 where a significant crosstalk reduction is achieved (more than 15 dB at 100 MHz). A pure capacitive coupling behaviour is depicted through the entire measured frequency range, which was modelled in Chapter 2 (Section 2.3.2) by a simple equivalent capacitive model.

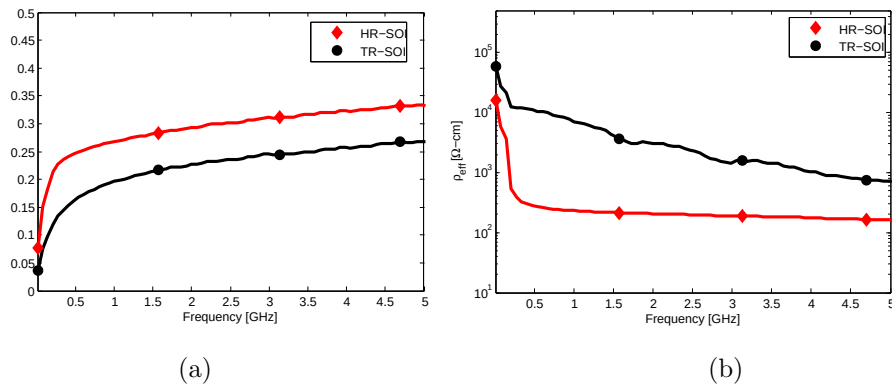


Fig. 5.33: Measured (a) CPW lines lineic losses and (b) effective resistivity on HR-SOI and TR-SOI after CMOS process substrates at ambient temperature.

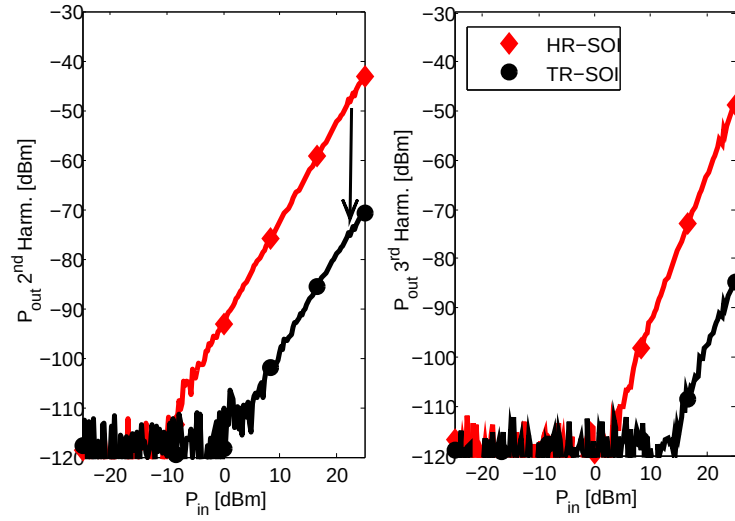


Fig. 5.34: Harmonic distortion for a input signal at 900 MHz of a 2,146 μm -long CPW line on HR-SOI and TR-SOI after CMOS process substrates at ambient temperature.

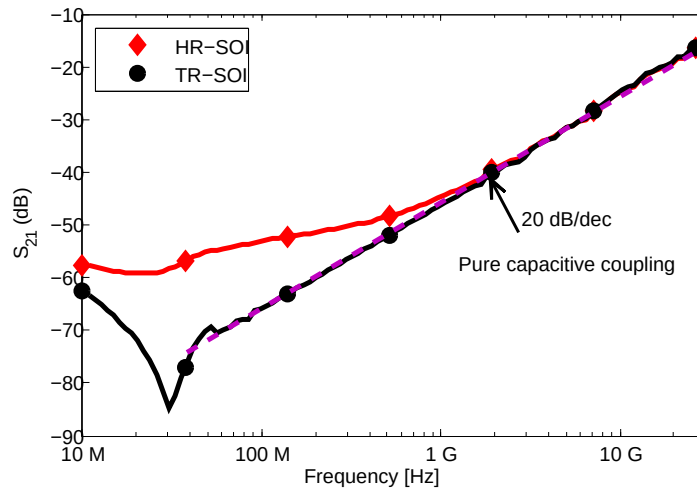


Fig. 5.35: Measured Substrate crosstalk on HR-SOI and TR-SOI after CMOS process substrates at ambient temperature.

5.4.2 RF characterization with temperature

CMOS SOI circuits and devices was demonstrated to have capability of successful operation at temperature beyond 250 °C [25]. This opens new fields of applications for co-integration of low voltage/low power, RF and high temperature circuits and devices on the same chip.

It is known from previous CPW and crosstalk measurements that the trap-rich passivation solution is a promising technology to further improve the handle substrate high resistivity properties for high performance RF applications. Measured TR-SOI processed using a standard clean room process that involves only metalization step has demonstrated its efficiency at extreme temperature operation, up to 175 °C. Additional measurements as function of temperature conditions will be investigated on HR-SOI and TR-SOI wafers processed using a 1 μm -standard CMOS process at UCL clean room. Multiple annealing steps were used during this process to define the gate oxide and active zones for the SOI MOSFET transistors.

Temperature performance of the designed CPW and crosstalk passive structures was measured by probing the wafers placed on cryogenic nitrogen cooled chuck or a heated chuck as explained in Section 5.2. The lower temperature limit used of the first experimental setup was -120°C , whereas the upper temperature limit of second setup was 255°C .

Fig. 5.36 (a) and (b) display CPW lineic losses and extracted effective resistivity on HR-SOI and TR-SOI wafers with respect to temperature variation. It is clear that TR-SOI has a lower substrate losses and higher effective resistivity over a large temperature range. The CMOS process thermal budget does not impact the efficiency of the trap-rich passivation technique up to 135°C . As temperature increases beyond this limit intrinsic carrier concentration increases and trapping capability decreases, which is outlined by the increase of lineic losses, and decrease of the effective resistivity.

The variation of lineic losses on HR-SOI at low and high temperature as function of frequency in Fig. 5.37 (a) and (b), respectively, indicate that substrate losses increase for temperature as high as 175°C , whereas lower temperature does not have a significant effect. With a clear evidence that TR-SOI wafer exhibits lower lineic losses (50 % lower than HR-SOI), it is observed that losses increase again beyond 175°C . At cryogenic temperatures the fluctuation of lineic in Fig. 5.38. losses could be attributed to the change substrate potential and also to the charge potential at the grain boundaries due to the increase of carriers mobility.

As illustrated in Fig. 5.39 (a) and (b) the extracted effective resistivity on HR-SOI wafer at low and high temperatures as function of frequency explains the variation of substrate losses with temperature. In fact, a slight reduction is seen at lower temperatures where ρ_{eff} decreases at temperature beyond 175°C and reach $20\ \Omega\cdot\text{cm}$ at 255°C .

The extracted effective resistivity on TR-SOI substrate at low temperature is lowered by less than 10 %, whereas it decreases by more than 90 % as the

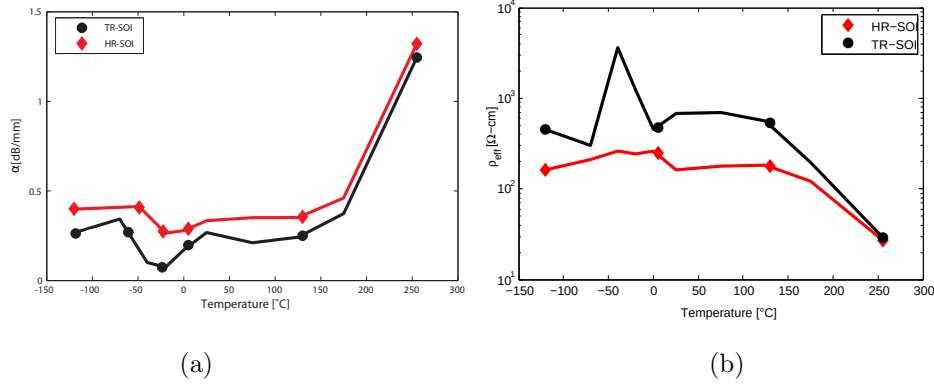


Fig. 5.36: Variation of (a) CPW lines lineic losses and (b) effective resistivity at 5 GHz of a 2,146 μm -long CPW line on HR-SOI and TR-SOI after CMOS process substrates with temperature.

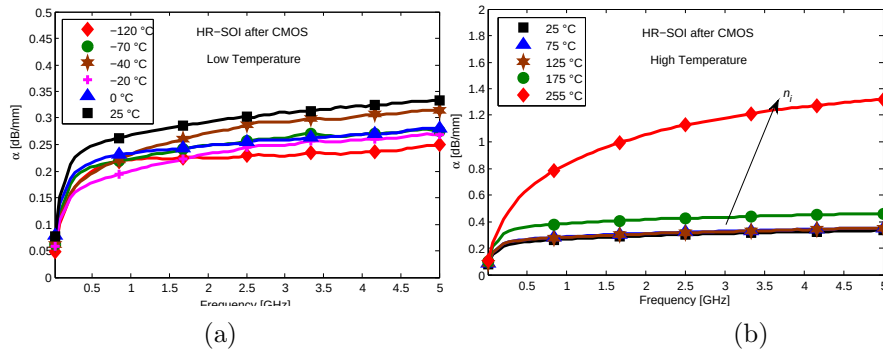


Fig. 5.37: Measured lineic losses of a 2,146 μm -long CPW line on HR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

temperature increases to 175 °C. Both the trapping capability of the trap-rich passivation layer and the decrease of its nominal resistivity as well as the nominal resistivity of the Si handle substrate are the main causes. In fact, due to the increase of carriers concentration the initial HR wafer behaves as an intrinsic silicon substrate with a nominal resistivity lower than 20 $\Omega\cdot\text{cm}$ at 255 °C.

The non-linearity behaviour shown in Fig. 5.41 also highlights the substrate resistivity degradation at extreme temperature operation. Both 2nd and 3rd harmonic distortions increase when temperature decreases below -55 °C or increases beyond 135 °C. This non-linearity behaviour is mainly associated to the carriers distribution inside the substrate, which was described by a non-linear capacitance and conductance equivalent elements [8].

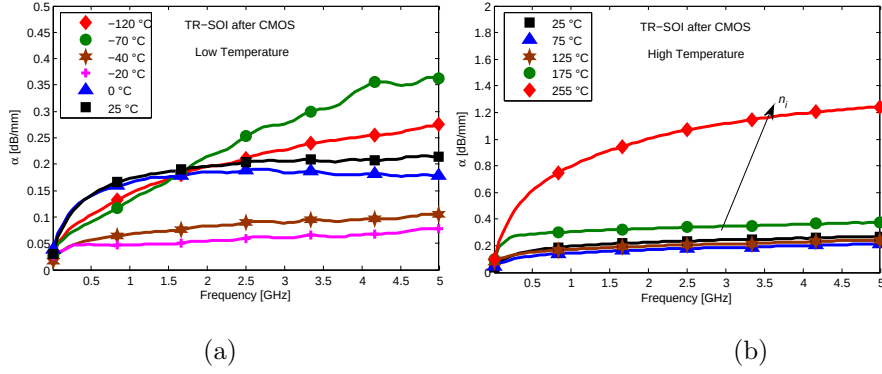


Fig. 5.38: Measured lineic losses of a 2,146 μm -long CPW line on TR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

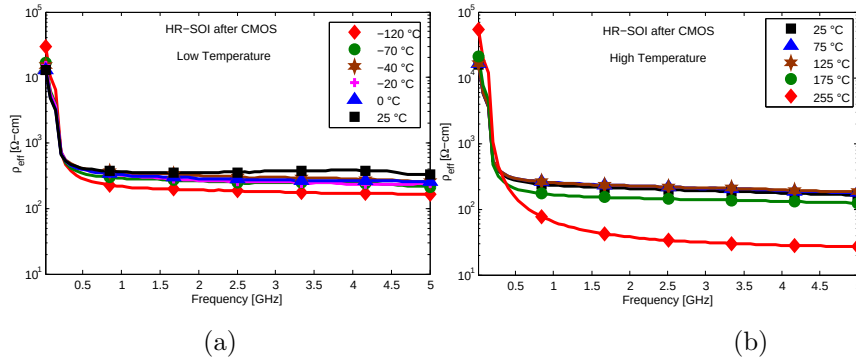


Fig. 5.39: Measured effective resistivity of a 2,146 μm -long CPW line on HR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

The extracted 2^{nd} harmonic distortion of a 2,146 μm -long CPW line on HR-SOI wafer at low and high temperature conditions in Fig. 5.42 shows a very slight variation. Although, the measured effective resistivity increases beyond 175 °C, it does not affect the non-linearity behaviour of HR-SOI wafer which is already very high as the output power of the 2^{nd} harmonic distortion is -40 dBm at an input power of 25 dBm. However, on TR-SOI wafer the non-linearity increases either at higher or lower temperatures as displayed in Fig. 5.43 (a) and (b), respectively. Such an increase of TR-SOI non-linearity can be attributed to the increase of free carriers concentration within the substrate at high temperature so that the efficiency of the interface traps is lowered. In addition, the carriers initially frozen at the grain boundaries will be activated and may change the charge distribution in the substrate, thus reducing the effectiveness

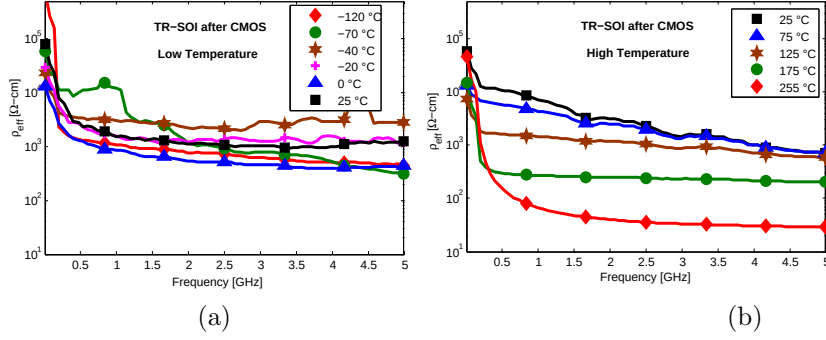


Fig. 5.40: Measured effective resistivity of a 2,146 μm -long CPW line on TR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

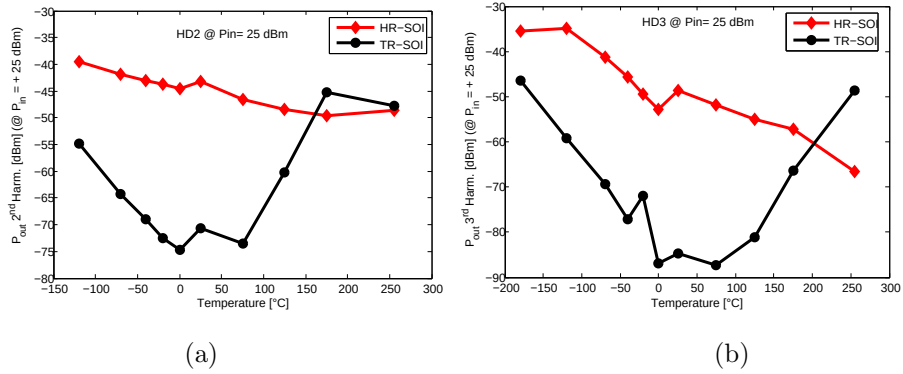


Fig. 5.41: Variation of (a) 2nd and (b) 3rd Harmonic distortions of a 2,146 μm -long CPW line on HR-SOI and TR-SOI after CMOS process substrates with temperature.

of the trap-rich passivation layer.

The coupling through the common substrate is also influenced by the effect of heating the wafer. Even a slight increase is depicted at low temperature on HR-SOI substrate as in Fig. 5.44 (a), the crosstalk on TR-SOI remains unchanged as shown in Fig. 5.45 (a). However, Fig. 5.44 (b) and Fig. 5.45 (b) outline that the crosstalk level increases on both HR-SOI and TR-SOI wafers beyond 175 °C, respectively.

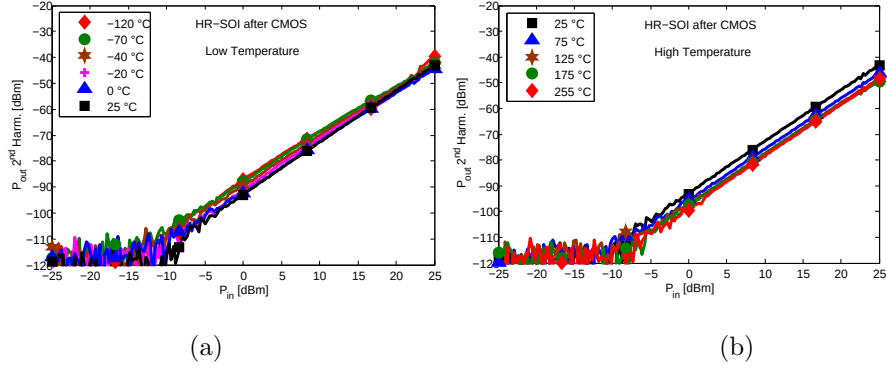


Fig. 5.42: Measured 2^{nd} harmonic distortion of a 2,146 μm -long CPW line on HR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

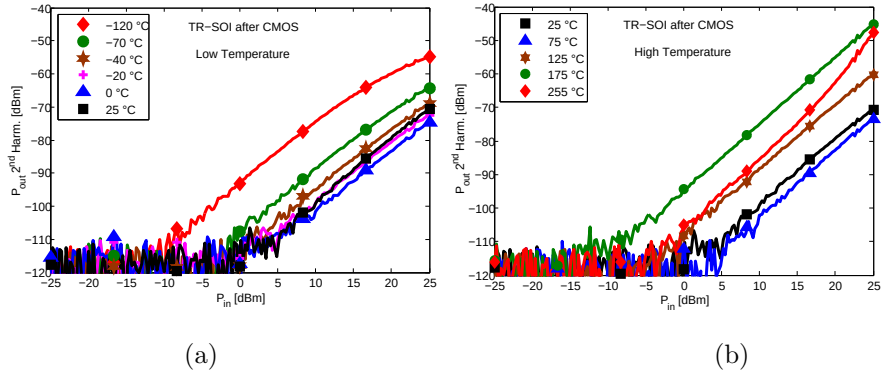


Fig. 5.43: Measured 2^{nd} harmonic distortion of a 2,146 μm -long CPW line on TR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

5.4.3 Conclusion

Investigation of temperature effect on oxidized HR-Si, trap-rich HR-Si, HR-SOI and TR-SOI wafers has demonstrated the efficiency to TR-SOI technology to reduce substrate losses, coupling and non-linearity over a large temperature range. The efficiency of interface traps within the trap-rich passivation layer is reduced beyond 175 °C, which suggests another alternative with a high density of traps over the whole substrate volume. The following section introduces a locally grown porous silicon layer technique that enhances the high resistivity of the handle Si-based substrate and aims to compare the effect of high

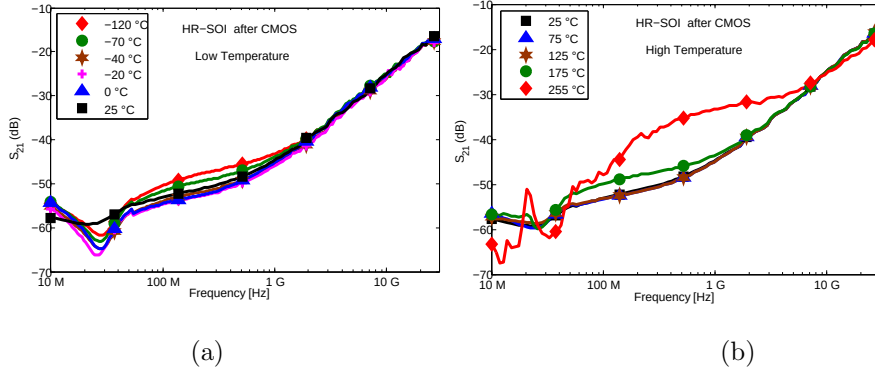


Fig. 5.44: Measured substrate crosstalk on HR-SOI substrate after CMOS process (a) at low temperature and (b) at high temperature.

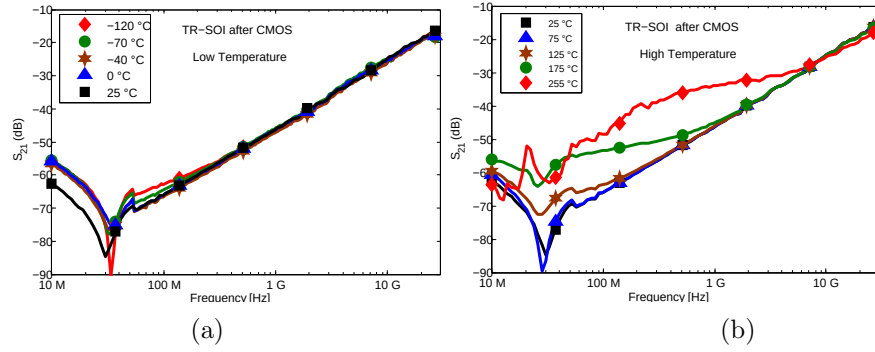


Fig. 5.45: Measured substrate crosstalk on HR-Si + 400nm-thick PolySi substrate (a) at low temperature and (b) at high temperature.

temperature on trap-rich HR-Si and porous Si RF performance.

5.5 RF PERFORMANCE OF LOCALLY GROWN POROUS SI COMPARED WITH TRAP-RICH HR-SI TECHNOLOGY

For bulk CMOS technology a promising solution for on-chip passive integration is to locally create a thick porous silicon (PSi) layer, with intrinsic high-resistivity properties [28, 29]. PSi is today the only viable solution for achieving high resistivity properties on standard-Si (std-Si) wafers while being compatible with the high thermal budget of Si CMOS process [30]. Locally grown porous Si layer (PSi) on Si substrate [31] permits to integrate isolated RF devices on a local area

of the wafer, while other CMOS electronics are fabricated over the rest of the wafer [32]. An additional advantage of PSi is its lower permittivity, four times smaller than Si [33]. Lower permittivity values help reducing the crosstalk at high frequencies (> 3 GHz) between devices fabricated on the same chip [34]. It also allows the fabrication of high-impedance transmission lines with low attenuation levels as the strip width dimension can be relaxed. In fact, integrated CPW lines on porous Si substrate can present characteristic impedances as high as 145Ω [32, 34]. The choice between TR-SOI or locally grown PSi technology depends on whether the used CMOS technology is bulk or SOI. They are not competitive technologies as they cannot be used together within the same CMOS technology. The use of TR-SOI seems being more easily done, as existing SOI CMOS circuits can directly migrate into TR-SOI technology without any additional fabrication steps. On the contrary, the PSi solution would need additional steps and dedicated masks. Nevertheless, PSi could be better positioned for the fabrication of RF circuits on Si, including high-quality passive elements, as cheap standard-Si wafers can be used instead of TR-SOI.

In this section, advanced RF performance of porous Si and trap-rich HR-Si substrates are investigated under small- and large-signal high frequency operation and compared with their corresponding initial standard Si and HR-Si substrates, respectively. The non-linear behaviour and the effect of temperature on the RF properties of both PSi and TR-Si technologies are addressed.

Four types of substrate are compared: standard p-type silicon ($1-10 \Omega\cdot\text{cm}$), high-resistivity silicon ($> 4 \text{ k}\Omega\cdot\text{cm}$), trap-rich HR-Si, and porous Si substrates. All of them include a top 500 nm-thick oxide layer to electrically isolate the RF devices from the Si substrate. PSi substrate (Fig. 5.46) consists of a locally formed 200 μm -thick porous silicon layer on p-type Si with resistivity in the range of $0.001-0.005 \Omega\cdot\text{cm}$, covered with 500 nm-thick SiO_2 capping layer. The fabrication process of the thick porous Si layer has been described in details in [30]. It includes electrochemical etching of the Si substrate in a 2 HF (50 %): 3 EtOH (99.9 %) solution with a constant current density of $J = 20 \text{ mA}/\text{cm}^2$. Trap-rich HR-Si substrate consists of a n-type HR-Si wafer with a nominal resistivity higher than $10 \text{ k}\Omega\cdot\text{cm}$, and a layer of 500 nm-thick trap-rich poly-Si layer deposited by low pressure chemical vapor deposition (LPCVD) at 625°C . The top dielectric passivation layer is a 500 nm-thick TEOS SiO_2 .

The same set of CPW lines is integrated on the four investigated substrates. The dimensions of the CPW line in Fig. 5.46 are: signal line width, $W = 26 \mu\text{m}$, signal line-to-ground plane distance, $S = 12 \mu\text{m}$, and ground width, $W_g = 208 \mu\text{m}$. On each substrate, a set of specific de-embedding structures is also included for accurate device parameter extraction.

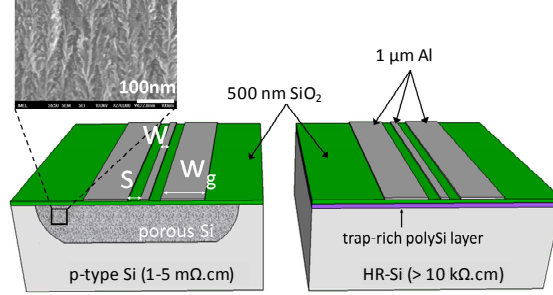


Fig. 5.46: Schematic of a CPW transmission line fabricated on a 200 μm -thick porous-Si layer (left) and on Trap-Rich Si substrate (right).

5.5.1 RF characterization of Si-based substrates at ambient temperature

In order to obtain an initial RF performance comparison between the investigated substrates, the CPW propagation and electrical substrate properties are measured at 25 °C.

5.5.1.1 Small and large-signal RF measurements of CPW

The RF losses as well as the effective resistivity ρ_{eff} of the wafers are extracted from the measurements with the method explained in [9]. The CPW lines characteristic impedance Z_c was extracted using Dehan's method [35]. We note from Fig. 5.47 (a) that the extracted Z_c value for std-Si, HR-Si and TR-Si wafers is around 50 Ω while it is 95 Ω on PSi substrate. The larger Z_c value in the case of CPW lines on PSi substrate is expected due to its lower relative permittivity ($\epsilon_{r,PSi} = 3.5$) compared with the Si value ($\epsilon_{r,Si} = 11.9$). The effective relative permittivity ($\epsilon_{r,eff}$) as a function of frequency is presented in Fig. 5.47 (b). The difference in the values of $\epsilon_{r,eff}$ between porous Si and HR-Si is representative of the difference in the substrate relative permittivity (ϵ_r) as described by [36]:

$$\epsilon_{r,eff} = \frac{\epsilon_r + 1}{2} \quad (5.4)$$

Equation 5.4 is valid for CPW line when the substrate can be considered infinitely thick, which is true in our case since the following condition is maintained: $h > 2(W + 2S)$, with h equal to the total substrate thickness [36]. A comparison of the attenuation coefficient (α) of the CPW lines made on the four substrates is shown in Fig. 5.48 (a). It clearly shows the excellent RF lossless properties of TR-Si and PSi substrates compared with their corresponding initial substrates, i.e. HR-Si and std-Si, respectively. The losses at room temperature for TR-Si and PSi substrates are around 0.35 dB/mm and 0.25 dB/mm at 30 GHz, respectively. The lower attenuation of PSi compared with TR-Si is not entirely related to its higher resistivity properties but also to the difference in the characteristic impedance as expressed in Eq. 5.5. The following equation describes the attenuation constant

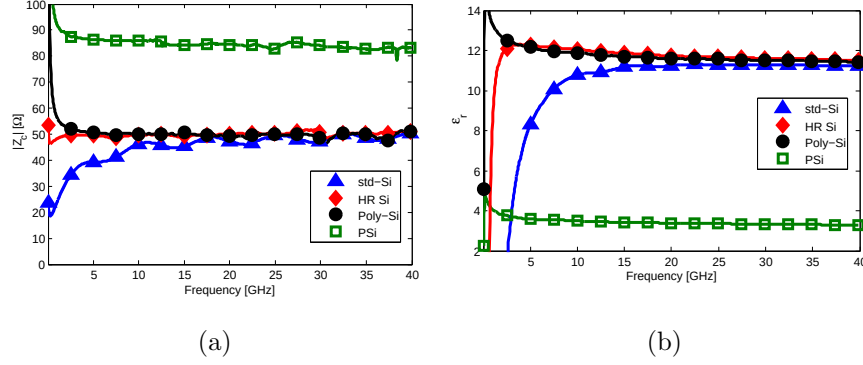


Fig. 5.47: Extracted (a) characteristic impedances and (b) effective relative permittivity on the investigated Si-based solutions at ambient temperature.

as function of the metal resistance (R), the substrate conductance (G) and the characteristic impedance (Z_c) at high frequencies [37].

$$\alpha = \frac{R}{2Z_c} + \frac{G}{2} Z_c \simeq \frac{R}{2Z_c} \quad (5.5)$$

The high-resistivity property of TR-Si and PSi substrates is confirmed by the

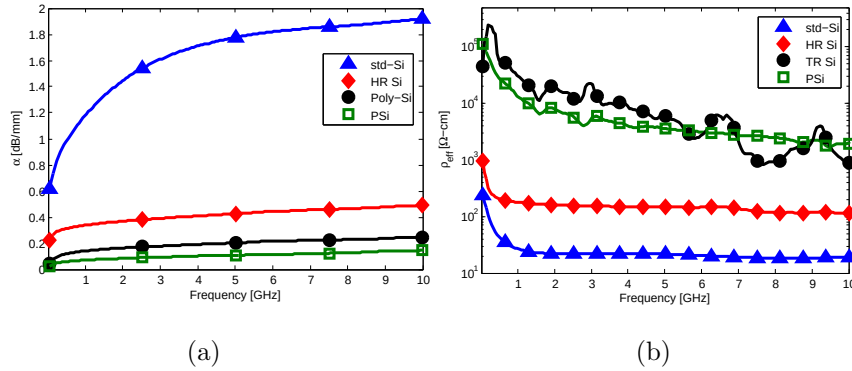


Fig. 5.48: Measured (a) lineic losses and (b) effective resistivity on the investigated Si-based substrates at ambient temperature.

extracted effective resistivity value shown in Fig. 5.47 (b). Despite its high nominal resistivity, the effective resistivity sensed by the CPW line on HR-Si wafer is only 200 $\Omega\cdot\text{cm}$, which explains the high harmonic level (Fig. 5.49) measured on both std-Si and HR-Si wafers [38]. Fortunately, the TR-Si and locally grown PSi reduce substrate generated harmonics, thereby they have true high resistivity properties and a ρ_{eff} higher than 4 k $\Omega\cdot\text{cm}$. Both PSi and TR-Si substrates

show harmonic distortion levels lower than the measurement noise floor (NF = -110 dBm) at the power levels used in this work. The numerous traps created by silicon dangling bonds in poly-Si are able to absorb the free carriers attracted at the SiO_2/Si interface and greatly reduce substrate losses and non-linearity. Porous silicon has a very high surface area. Therefore, it contains a high density of Si dangling bonds and impurities such as hydrogen and fluorine that are residuals from the electrolyte used during PSi formation. The electrical resistivity of the PSi layer is very high due to its nano structure. The resistivity of porous silicon changes with the porosity of the sample as it depends on the quantum confinement, mobility and drift of the carriers, changes in the band structure, temperature and on the medium inside the pores [39].

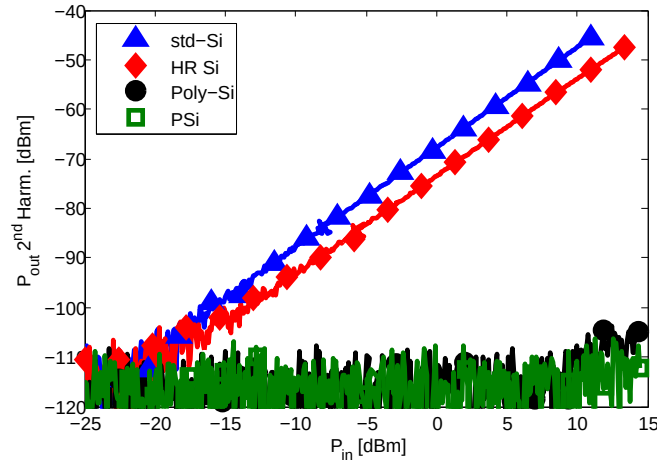


Fig. 5.49: Harmonic distortion for a input signal at 900 MHz of a 2,146 μm -long CPW line on the investigated Si-based substrates at ambient temperature.

5.5.1.2 Substrate crosstalk on Si based substrates

The efficiency of the TR-Si and PSi Si-based solutions is assessed by measuring the crosstalk level (S_{21}). The experimental test structure consists of two identical rectangular metallic pads ($50 \times 150 \mu\text{m}$) spaced by $50 \mu\text{m}$ and embedded in a coplanar structure for RF probe measurement as shown in the inset of Fig. 5.50. A pure capacitive coupling is depicted in Fig. 5.50 for Trap-rich HR-Si and PSi, with a characteristic 20 dB/dec slope over the whole frequency range [13]. PSi exhibits 10 dB lower crosstalk level than TR-Si due to its lower permittivity (see Fig. 5.47 (b)). These results clearly show the efficiency of TR-Si and PSi solutions in minimizing the noise coupling. A reduction by more than 15 dB and 30 dB is observed at 100 MHz for TR-Si and PSi, respectively, compared with

their initial counterpart HR-Si and std-Si substrates. Thanks to the combination of high effective resistivity and low effective permittivity, PSi exceeds in the crosstalk reduction.

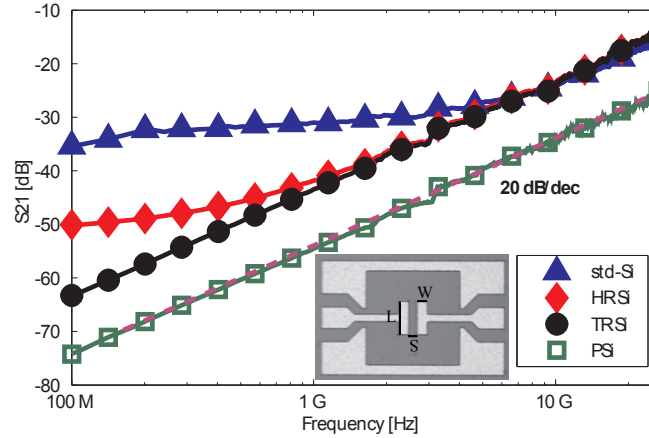


Fig. 5.50: Substrate crosstalk on the investigated substrates at ambient temperature.

5.5.2 RF characterization of Si-based substrates at high temperature

In order to study the behaviour of Si-based substrates versus temperature, RF measurements are performed at different temperatures, ranging from 25 °C upto 175 °C. Two calibrations steps are applied to extract the transmission lines parameters. First, to set the measurement reference at the CPW probe tips, a SOLT (Short-open-load-thru) calibration technique is done using a standard calibration structures on an alumina substrate. Then, a TRL (Thru-reflect-line) calibration is used to subtract the metallic CPW probe pad parasitics, and thus determine the characteristics of the designed CPW lines. The latter step is repeated for each temperature value. It is well known that the permittivity of Si does not change when the temperature increases. As far as the structural properties of TR-Si and PSi are stable with temperature their permittivity (and Z_c) is stable. As it is shown respectively, in Fig. 5.51 (a) and (b), the extracted Z_c and $\epsilon_{r,eff}$ parameters remain constant over the whole temperature range, confirming the structural stability of both TR-Si and PSi substrates.

Regarding the extracted attenuation at 5 GHz as a function of temperature, presented in Fig. 5.52 (a), we can conclude that for both TR-Si and PSi substrates the improvement in term of losses compared with their respective counterpart HR-Si and std-Si substrates is maintained over the whole temperature range. A gradual attenuation decrease on std-Si with temperature increase

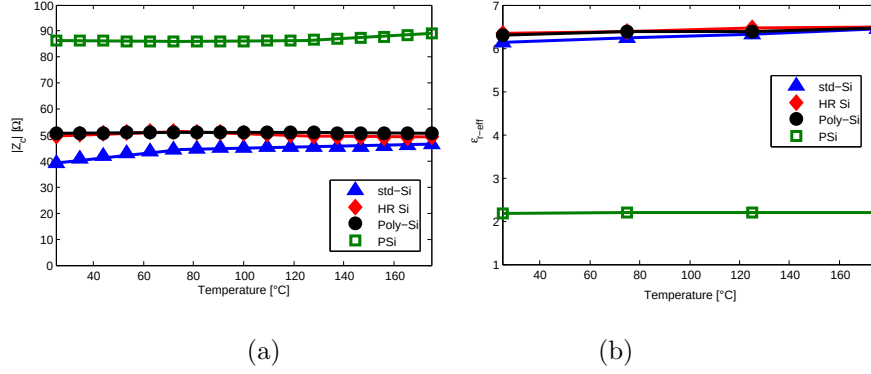


Fig. 5.51: Variation of the (a) characteristic impedance and (b) effective relative permittivity as function of temperature at 5 GHz on the investigated substrates.

can be appreciated. Such lower attenuation, equivalent to a higher substrate resistivity, is due to the mobility reduction of free carriers with increasing temperature. On the other hand, and for all three high-resistivity substrates (HR-Si, TR-Si and PSi) attenuation increases with increasing temperature. This phenomenon is mainly due to the degradation of substrate resistivity with temperature, confirmed by the extracted effective resistivity reduction that is shown in Fig. 5.52 (b), and in smaller extend to the increase of metallic losses with temperature. The conductive substrate losses of TR-Si [40] become the dominant loss mechanism at 175 °C due to the increase of intrinsic carriers and also the depletion width underneath the metal is reduced due to the increment of intrinsic carrier concentration. Such decrease of bulk resistivity increases the substrate losses as previously investigated for HR-Si substrate in [41] where the reduction of free carrier concentration inside the substrate to a value close to n_i highlighted its independent on substrate level doping above 175 °C.

As it was proven in [8] that the total harmonic distortion is governed by the 2nd harmonic component and strongly depends on the effective substrate resistivity. Thus a reduction of the resistivity due to temperature results in an equivalent increase of the substrate non-linearities. It is indeed the case for the investigated TR-Si and PSi substrates as depicted in Fig. 5.53. The harmonic distortion level of TR-Si and PSi increases and in the case of TR-Si it becomes close to those of HR-Si and std-Si wafers at a temperature of 175 °C.

5.6 CONCLUSIONS

The loss characteristics of TR-SOI wafers are compared regarding the trapping capability of trap-rich passivation layer. It was demonstrated that the trap-rich HR-SOI RF performances are maintained for a large temperature range from

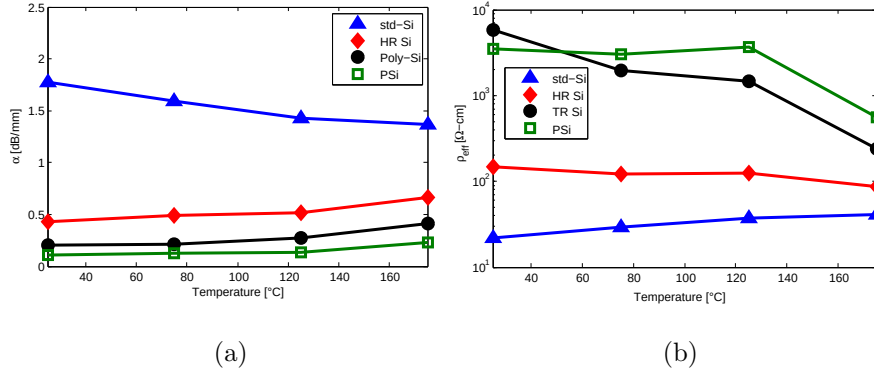


Fig. 5.52: Variation of (a) lineic losses and (b) effective resistivity at 5 GHz of a 2,146 μm -long CPW line as function of temperature on the investigated substrates.

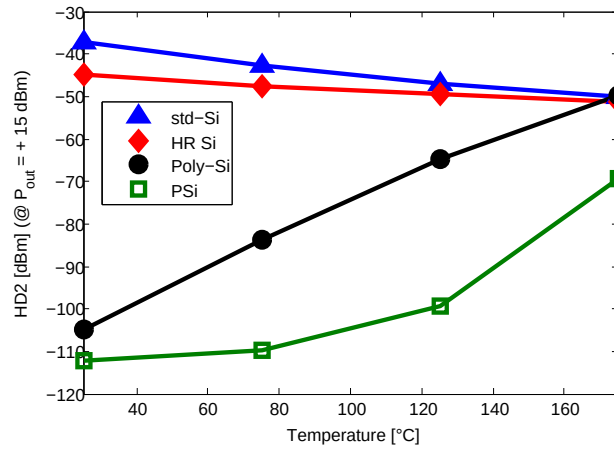


Fig. 5.53: Harmonic distortion of a 2,146 μm -long CPW line on the investigated substrates with temperature.

–55 °C up to 175 °C. As the temperature increases both HR-SOI and TR-SOI loose their high resistivity characteristics which mainly related to the increase of intrinsic carriers density. Moreover, the interface traps efficiency is lowered for higher temperatures, and such impact is more pronounced for TR-SOI wafers which receive different annealing steps during the SOI process.

RF performance of TR-SOI wafers was investigated before and after CMOS process, and it was demonstrated that the thermal budget of the CMOS process does not affect TR-SOI high resistivity properties in terms of reducing substrate

losses, non-linearity and crosstalk at extreme temperature operation when compared with HR-SOI initial wafer.

The last part of this chapter introduces a high resistivity Si-based substrate, low cost and CMOS compatible, which consists on locally formed thick porous Si layer on a low resistivity Si wafer. RF performance of porous Si and trap-rich HR-Si substrates was investigated by means of experimental small and large-signal measurements at high temperature. The characterization of PSi and trap-rich HR-Si substrates confirms the excellent properties of both materials in terms of substrate losses and linearity when compared with standard Si and high resistivity Si substrates. Nevertheless, our measurements showed that the porous Si substrate exhibits reduced substrate losses compared with the trap-rich HR-Si and lower harmonic distortion values. In addition, the tailored lower permittivity of PSi makes it more attractive for crosstalk reduction by more than 10 dB. Despite of the reduction of their effective resistivity both Si-based solutions remain acceptable for RF applications at higher temperatures up to 175 °C, above which they start suffering from significant RF losses and become comparable to their corresponding initial substrates.

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CHAPTER 6

CONCLUSIONS AND PERSPECTIVES

6.1 CONCLUSION

6.1.1 TR-SOI a quasi-lossless RF substrate

The main objectives of this thesis was to complete previous research on engineered RF substrate to assess the suitability of HR-SOI and trap-rich HR-SOI technologies for co-integration of digital/analog, optical and RF passive/active devices on the same chip.

6.1.1.1 HR-Si and trap-rich HR-Si substrate modelling

Through Chapter 2 electrical substrate crosstalk was investigated on HR-Si and trap-rich HR-Si wafers over a wide frequency band has been analysed. A lumped element equivalent circuit model from 100 kHz up to several GHz, based on the physical understanding of substrate crosstalk, has been proposed and compared with measurements and numerical simulations. It includes the impact of parasitic surface effect (PSC) where the oxidized HR-Si handle wafer loses it's high resistivity properties mainly due to fixed oxide charges which attract free carriers at the substrate surface creating a high conductive layer. The introduction of a trap-rich layer at the oxide-Si substrate interface such as

PolySi has been successfully simulated and allow to recover the nominal high resistivity of the HR-Si handle wafer. Moreover, by means of simulations and crosstalk measurements it has been proved that trap-rich HR-Si substrate is an efficient solution to drastically reduce electrical coupling through the substrate at frequencies below 10 GHz. Thanks to this trap-rich PolySi layer, a purely capacitive lumped equivalent circuit that properly describes the quasi-lossless HR-Si substrate was developed. This simple capacitive model can be used by RF designers to build RF, analog and digital devices lying on a PolySi trap-rich HR-Si substrate. By leveraging the excellent properties of the HR-Si (or HR-SOI) for low loss RF, mixed mode and SoC applications, the TR-HR-Si (HR-SOI) technology becomes highly competitive with traditionally well known microwave substrates such as GaAs and SOS or SOQ. Its full compatibility with SOI CMOS fabrication process provide a major advantage to integrate high quality passive elements in multi-standard multi-band front end modules.

6.1.1.2 *Photo-induced CPW RF switch and optical crosstalk on HR-Si and trap-rich HR-Si*

Recent advances in optically controlled devices on Si-based substrate has currently made Silicon-on-insulator optoelectronic devices an increasingly attractive area of interest with it's truly CMOS processing compatibility. However, it has been demonstrated that photogenerated carriers in HR-Si with low excess carriers lifetime ($\tau = 10^{-4}s$) spread over a large laterally area which causes high optical crosstalk photo-generation rate which influences drastically the behaviour and performance of neighbour interconnections and devices. As investigated in Chapter 3 the trap-rich passivation technique has proved its efficiency to reduce lateral photogeneration. Thanks to it high traps density and recombination centers, the excess carriers life time can be altered and photogenerated carriers are immediately recombined when generated.

The efficiency of the trap-rich polysilicon passivation technique to reduce lateral carriers photo-generation has been demonstrated using physical simulations and experimental measurements. In fact, it has been found that the optical crosstalk is drastically reduced thanks to the high recombination rate in the PolySi layer. A well-controlled process was developed to locally etch the polysilicon window, which define the active area of the optically controlled CPW RF switch. The efficiency of the new designed CPW RF switch on locally etched polysilicon layer was compared to the literature as presented in Table 3.1. Depending on the application, the dimensions of the trap-rich free area; i.e. where a highly photo-conductive region is wanted, must be optimized in order to assure the good performance of the optically controlled RF device under low optical power and simultaneously minimize the optical crosstalk between the different components when integrated in a System-on-Chip (SoC) application.

6.1.1.3 Static and RF performance of passive and active devices on HR-SOI and TR-SOI commercial wafers

In chapter 4, passive and active devices were fabricated using an academic 1 μm SOI CMOS process on top of commercial 200 mm HR-SOI and TR-SOI both provided by Soitec. The non-linear behaviour, RF losses and substrate crosstalk are experimentally investigated. The correlation between the substrate effective resistivity and the generated harmonic distortion along a CPW line demonstrated the efficiency of a TR-SOI substrate as a viable solution for RF front-end modules integration. Fig. 6.1 highlight the RF performance improvement of TR-SOI technology compare with its HR-SOI counterpart and versus the ideal target. Passive elements such as inductors, capacitors and interconnection transmission lines are widely used in the front-end blocks and cover a large area on the chip. Enhancing RF performance of such passive on-chip components leads to a significant improvement for whole front-end modules. Measurement results on the trap-rich passivated HR-SOI substrate indicate a significant improvement in terms of substrate RF losses, crosstalk and non-linearity reduction as well as larger inductor quality factor Q compare with HR-SOI counterpart.

The excellent matching between the experimental static and RF characteristics of measured FD SOI MOSFETs on top of both HR-SOI and TR-SOI clearly demonstrates that it does not alter the DC or RF behaviour of SOI MOS transistors. The efficiency of TR-SOI to reduce substrate crosstalk and digital switching noise is demonstrated. It provides a linear behaviour and an adequate level of isolation that could be considered as an excellent solution for integration of highly performance passive elements, analog/RF and digital circuits in RF FEM for SoC applications. All these results correlate with the proposed pure capacitive model that simplify and describes the quasi-lossless TR-SOI wafer.

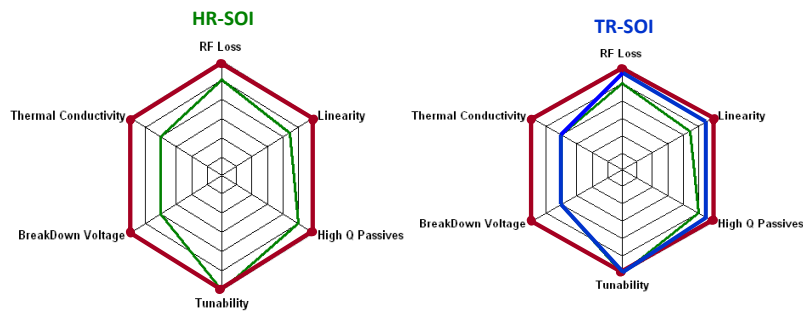


Fig. 6.1: HR-SOI and TR-SOI substrate process performance versus ideal target.

6.1.1.4 Impact of temperature on TR-SOI RF performance

Engineered substrate enable multiple technologies to be integrated on a single chip. High voltage RF MEMS sensors and units, high temperature applications, power management units and digital microprocessors and memories need to be built around a single system-on chip when keeping low loss and low coupling effect between the different blocks. In this context we investigate the efficiency of trap-rich HR-SOI substrates at a large temperature range from -120°C up to 255°C by means of small- and large-signal measurements.

The loss characteristics, non-linearity and crosstalk on TR-SOI wafers regarding the effect of temperature on its trapping capability were compared to HR-SOI wafers. It was demonstrated that the effective resistivity was degraded on trap-rich HR-SOI reaching almost $1\text{ k}\Omega\cdot\text{cm}$ at 125°C and becomes much lower than that for high temperatures. As the temperature increases both HR-SOI and TR-SOI loose their high resistivity characteristics which is mainly related to the increase of intrinsic carriers density. Therefore, a solutions to reduce the impact of intrinsic carriers thermally activated in the volume of the Si substrate is highly required.

The characterization of porous (PSi) and trap-rich HR-Si substrates confirms the excellent properties of both materials in terms of substrate losses and linearity when compared with standard Si and high resistivity Si substrates. Nevertheless, our measurements showed that the porous Si substrate exhibits reduced substrate losses compared with the trap-rich HR-Si and lower harmonic distortion values. In addition, the tailored lower permittivity of PSi makes it more attractive for crosstalk reduction. Despite of the reduction of their effective resistivity both Si-based solutions remain acceptable for RF applications at higher temperatures up to 175°C , above which they start suffering from significant RF losses and become comparable to their corresponding initial substrates.

6.2 PERSPECTIVES AND FUTURE WORK

With the continuing development of next-generation wireless communication systems, there has been a great interest to multi-mode multi-band building blocks. HR-SOI CMOS technology has several advantages with the availability of high-performance RF power switches and more than 65 % of fabricated handset switches are SOI based.

The TR-SOI technology (commercially named as eSI substrate) has proven its high RF performance compare to traditionally well known SOS, SOQ RF substrates adding more compatibility with CMOS integration. Further research should be conducted in the fabrication of RF circuits and blocks which will be integrated in mixed mode circuits on TR-SOI. Moreover, with the scaling down of transistor gate length and the emergence of UTB, UTBB, FD SOI MOSFET's and FinFETs "More Moore" devices, it would be very interesting to evaluate the compatibility of the TR-SOI technology with such scaled technology nodes. Further research covering the robustness of TR-SOI technology at harsh

environment conditions (irradiation, temperature effect on active devices, ...) will help evaluating the economical and efficiency performance of such TR-SOI technology for fully integrated SoC.

In this dissertation our research main topics has covered substrate coupling effect through passive crosstalk structure and injection noise in the proximity of single FD SOI MOSFET. While successful improvement in terms of reduction of substrate crosstalk using trap-rich HR-SOI technology was achieved, it would be very interesting to evaluate substrate coupling effect using a complex RF circuits such as Low Noise amplifier (LNA), Power amplifier (PA) and voltage controlled oscillator (VCO) and investigate how different block could alter the RF performance of its neighbour circuit. The evaluation of different front end blocks will offers the path towards to integrate all the modules on enhanced integrity HR-SOI (eSI HR-SOI) substrate. While investigating the efficiency of the proposed technology for integration of FEM on HR-SOI, RF circuits on GaAs or SOS substrates will migrate to a compatible SOI CMOS process.

Another interesting topic would be the modelling the coupling mechanisms through the common silicon substrate on TR-SOI technology and how to integrate such simplified model in those of active devices and circuits. In fact, the equivalent circuit model should be analysed and added to the design software in order to emulate the real case of active and passive devices fabricated on eSI HR-SOI technology.

APPENDIX A

WAFERS LIST DESCRIPTION FOR EACH CHAPTER

Chapter	Wafers	oxide thickness : t_{SiO_2} (nm)	trap-rich		Si		ρ ($\Omega \cdot cm$)
			Type	Thickness (nm)	Type	Thickness (μm)	
2	Std-Si	145 nm (thermal)			P	525	20
	HR-Si	145 nm (thermal)			P	725	5 k
	HR-Si + PolySi	145 nm (thermal)	LPCVD PolySi	≈ 300	P	725	5 k
	HR-Si + PolySi_1	3000 nm (PECVD)	LPCVD PolySi	≈ 76	P	725	5 k
	HR-Si + PolySi_2	3000 nm (PECVD)	LPCVD PolySi	≈ 172	P	725	5 k
	HR-Si + PolySi_3	3000 nm (PECVD)	LPCVD PolySi	≈ 435	P	725	5 k
3	HR-Si	50 nm (thermal)			N	725	> 4 k
	HR-Si + PolySi	50 nm (thermal)	LPCVD PolySi	≈ 400	N	725	> 4 k
4	HR-SOI	400 (thermal)			N	> 700	> 3 k
	TR-SOI	400 (thermal)	Not Available	2000	N	> 700	> 3 k
	HR-4k	150 (thermal)			P	725	> 4 k
	HR-10k	150 (thermal)			N	725	> 10 k
	TR-4k	150 (thermal)	LPCVD α -Si	360	P	725	> 4 k
	TR-10k	150 (thermal)	LPCVD PolySi	330	N	725	> 10 k

Table A.1.: Substrates description used for each chapter (2, 3 and 4).

Chapter	Wafers	oxide thickness : t_{SiO_2} (nm)	Trap-rich		PSi Thickness (μm)	Si		
			Type	Thickness (nm)		Type	Thickness (μm)	ρ ($\Omega.cm$)
5	HR-Si	50 nm (thermal)				N	725	> 4 k
	HR-Si + PolySi	50 nm (thermal)	LPCVD PolySi	≈ 400		N	725	> 4 k
	Quartz		> 725 μm					
	HR-SOI without CMOS	400 (thermal)				N	> 700	> 3 k
	TR-SOI without CMOS	400 (thermal)	Not Available	2000		N	> 700	> 3 k
	HR-SOI after CMOS	400 (thermal)				N	> 700	> 3 k
	TR-SOI after CMOS	400 (thermal)	Not Available			N	> 700	> 3 k
	Std-Si	500 (thermal)				P	525	0.005
	HR-Si	500 (thermal)				N	515	> 4 k
	HR-Si + PolySi	500 (thermal)	LPCVD PolySi	≈ 500		N	515	> 4 k
	Porous Si (PSi)	500 (thermal)			200	P	525	0.005

Table A.2.: Substrates description used through chapter 5.

APPENDIX B

DESIGN AND FABRICATION OF RF-MEMS DEVICES ON HIGH RESISTIVITY SILICON SUBSTRATE

RADIO Frequency Radio Frequency microelectricalmechanical systems (RF MEMS) is an emerging technology as a viable alternative to solid-state control devices for microwave circuits. Its low power consumption, large tuning range, excellent RF performance and integration capability are the key characteristics enabling system implementation with potential improvement in size, cost and increased functionality. The main RF MEMS devices include switches, high-Q inductors, capacitors, antennas, resonators and filters, etc. [1]. The fabrication process of these devices is usually CMOS compatible which allows the co-integration of MEMS devices and CMOS devices and circuits [2].

By leveraging existing state of the art of CMOS Integrated Circuits (IC's) fabrication technologies based on silicon, MEMS technology exhibits many advantages that provide higher performance required for RF and millimetre wave application, in addition to a low fabrication cost and high level of integration [2]. While the concept of integrating tunable RF MEMS devices with CMOS monolithic microwave integrated circuits on silicon substrate is appealing, their performance is limited by the high RF losses and crosstalk of the low resistivity ($10 \Omega\cdot\text{cm}$) substrate, even using advanced Silicon-on-Insulator (SOI) technology.

Nowadays, the use of high-resistivity silicon (HR-Si) has converted Si into a suitable technology for high frequency applications. Indeed, HR-Si can be used as a handle substrate for SOI substrates, also known as high-resistivity SOI (HR

SOI), offering hybrid integration capability, improved RF performances, and SOI-CMOS compatibility [3]. Furthermore, using HR SOI, the advantages of low-complex process design RF MEMS devices added to reduced losses, improved substrate isolation, and SOI-CMOS technology compatibility has already been proved [4]. These advantages make HR-Si substrate a very attractive handle substrate for System-on-Chip applications. However, oxidized HR-Si suffers from parasitic surface conduction (PSC) effect at the Si/SiO_2 interface. The low conductivity of the HR-Si effectively suppresses RF bulk losses but not the losses associated with an accumulation or inversion at the Si/SiO_2 interface, hence reducing the final effective resistivity of the wafer [5]. The impact of PSC is more pronounced for coplanar devices, e. g. coplanar waveguide (CPW), in which the electric field is more concentrated at the wafer surface than in microstrip structures [6]. In addition, surface charge concentration depends on the applied voltage leading to bias-dependent losses. In CMOS circuits this bias voltage is approximately 1-3 V and is higher than 10 V for MEMS devices, thereby the substrate losses could be much higher than expected [7]. This PSC affects the RF characteristics of the MEMS devices, and thus degrades its performance. Fortunately, it has been also proved that this highly conductive surface layer can be effectively suppressed by introducing a high trap-rich layer between the oxide and the HR-Si substrate [8]. Several techniques have been reported to introduce such trap-rich layer to passivate HR-Si substrates, such as the deposition of polycrystalline silicon [8] or amorphous silicon [9] between the bulk Si and the oxide.

In this annexe a simple fabrication process with two photolithographic steps is used in the Winfab clean-room at UCL [10] to implement RF-MEMS on top of an oxidized HR-Si substrate as presented in [11]. Fig. B.1 demonstrates the principle of the designed low complexity RF MEMS structure compared with that presented by Siegel et al in [12]. The performance of two RF MEMS devices: a reconfigurable patch antenna and a tunable coplanar low-pass filter, lying on HR-Si substrate are investigated by means of 3D electromagnetic simulations and experimental measurements. The impact of the substrate losses on RF-MEMS tunable filters is discussed.

B.1 RF-MEMS PERFORMANCE ON HR-SI SUBSTRATE

B.1.1 Fabrication Process

The low-complexity fabrication process of RF-MEMS consists of two mask-layers process fully compatible with standard CMOS processing [11]. It requires only three film depositions and two photolithographic steps as presented by the fabrication process flow in Fig. B.2. First, a 1 μm silicon oxide layer is deposited on top of a commercial p-type HR-Si substrate ($\rho > 10 \text{ k}\Omega\cdot\text{cm}$) by plasma enhanced chemical vapor eposition (PECVD). Next, a low-pressure chemical vapour deposition (LPCVD) is used to deposit a 200 nm silicon nitride at 800 °C. This layer is used to define the switchable part of the MEMS structure. Then, an alu-

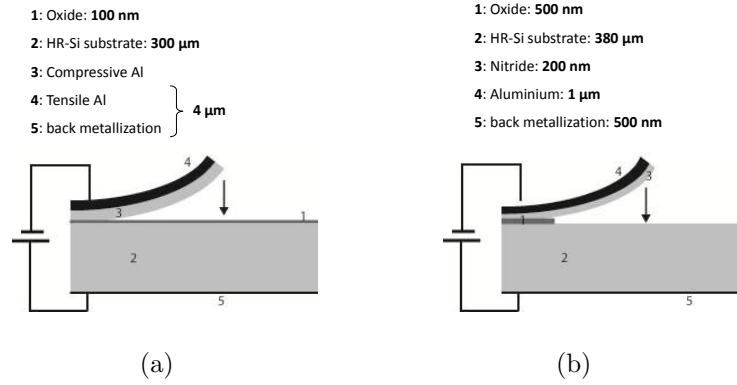


Fig. B.1: Principle of the low complexity RF- MEMS (a) Reference [12] and (b) This work.

minium layer of 2 μm -thick is evaporated in an E-gun vacuum system at 150 °C and patterned in chlorine-based plasma. A 500 nm-thick aluminium layer is then evaporated at the backside of the Si wafer. Finally, the MEMS structures release is performed via the wet etching of the PECVD silicon oxide sacrificial layer in a mixture of concentrated fluoridric acid (HF 73 %) and isopropanol.

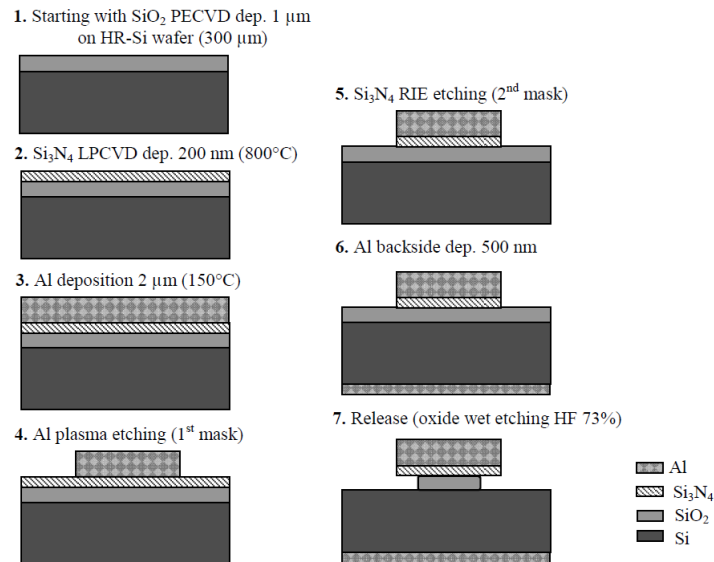


Fig. B.2: Process flow for the fabrication of 3-D RF MEMS.

B.1.2 Reconfigurable Patch Antenna

Reconfigurable antennas similar to those reported in the work done by Siegel et al. [12] have been designed, fabricated and measured. Fig. B.3 shows microscope photography of a patch antenna with coplanar-to-microstrip transition required for the CPW probing and measurement of the patch antenna [13]. The rectangular patch antenna is designed to operate at 35 GHz in its down state, i.e. when the movable parts of the antenna are in the plane of the wafer. The patch is $1700\text{ }\mu\text{m}$ -wide and $1124\text{ }\mu\text{m}$ -long and it is directly fed at its edge using microstrip line and matched to $50\text{ }\Omega$ by choosing the right insert feed depth of $420\text{ }\mu\text{m}$. After etching away the sacrificial layer the switchable part of the MEMS structure bends up due to the out-of-plane gradient of stress within the aluminium-silicon nitride bilayer as depicted in Fig. B.3. The out-of-plane MEMS structure can then be moved up and down via the application of a DC bias applied between the movable MEMS parts and the Si wafer to modulate the electric length of the patch and hence change its radiating frequency.

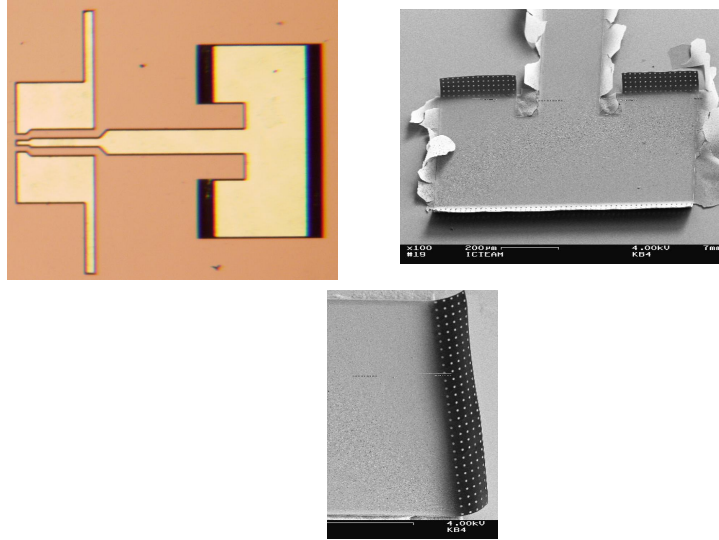


Fig. B.3: Top view photography of the fabricated RF MEMS patch antenna.

Simulations of the MEMS antenna have been performed using a 3D full-wave electromagnetic simulator software (IE3D). As it can be seen in Figs. 3 and 4, both simulations and measurements are in well accordance with results presented in [14]. This agreement confirms the similarities, quality performance, and repeatability of such a simple MEMS fabrication process. In Fig. 3, for a $100\text{ }\mu\text{m}$ -long released region the resonance frequency is shifted from 35 GHz in the

down-state 37.5 GHz in the up-state (extreme point of the cantilever is located at $20\text{ }\mu\text{m}$ above the substrate surface). The achieved frequency shift increases with the length of the bending part of the antenna, thus Fig. 3 shows a shift of more than 2 GHz between the down- and up-state for a $160\text{ }\mu\text{m}$ -long released region.

From measurement curves presented in Fig. 4 it can be seen that the resonance frequency shifts from 34.2 GHz in the down-state to 36 and 37.1 GHz in the up-state for, respectively, $100\text{ }\mu\text{m}$ and $160\text{ }\mu\text{m}$ released region length with a return loss better than -20 dB. The 3 dB difference at low frequency between the measured and simulated results can be mainly explained by the parasitic coplanar-to-microstrip propagation mode at the transition region [13].

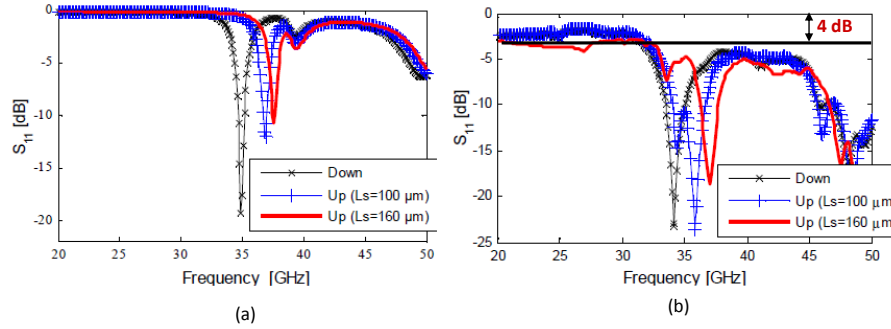


Fig. B.4: Simulated (a) and measured (b) [14] in down- and up-states with $100\text{ }\mu\text{m}$ and $160\text{ }\mu\text{m}$ switchable height on each side of the patch antenna.

B.1.3 Tunable Low Pass Filter

For RF MEMS design and fabrication it is much more convenient to use CPW than microstrip (MS) as the implementation requires only uniplanar fabrication technology where the shunt switches are directly connected to the ground plane using anchors [1]. Furthermore, in CPW microwave losses are lower than MS structure because of the electric field distribution close to the edges of the CPW. In this context, low-pass filters are designed and fabricated using a stepped impedance implementation based on CPW lines [15]. The high and low impedance sections of the filter correspond to $92\text{ }\Omega$ and $25\text{ }\Omega$, respectively, while the feed line is designed to be $50\text{ }\Omega$ as shown in Fig. B.5 (a). The filter section lengths are initially approximated by means of the equivalent circuit model of short transmission line sections, to achieve a cut-off frequency of 40 GHz. By switching up a bending region of the low impedance, the filter stepped impedances change and thus the cut-off frequency is also varied. Fig. B.5 (a)

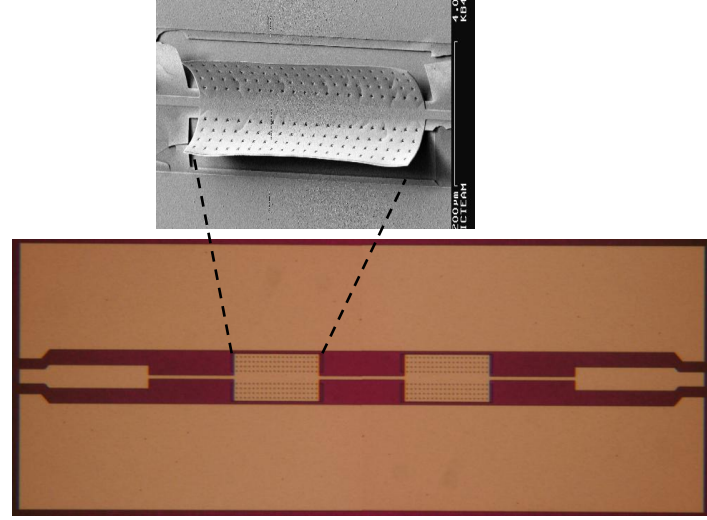
and (b) show a top view of the fabricated CPW low-pass filter when the bending regions switched up and the simulated structure with the corresponding dimensions for each CPW line section.

From the simulation results on a HR-Si substrate ($\rho=10 \text{ k}\Omega\cdot\text{cm}$) presented in Fig. B.6, the cut-off frequency is shifted from 40 GHz in the down-state to 57 GHz in the up-state (40 μm height for the upper point of the movable part), providing a maximum possible 17 GHz tunable range. RF-MEMS filters have been fabricated using the same simple process than previously described for the tunable antennas.

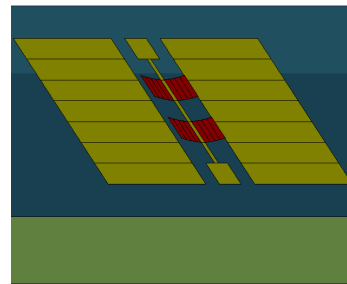
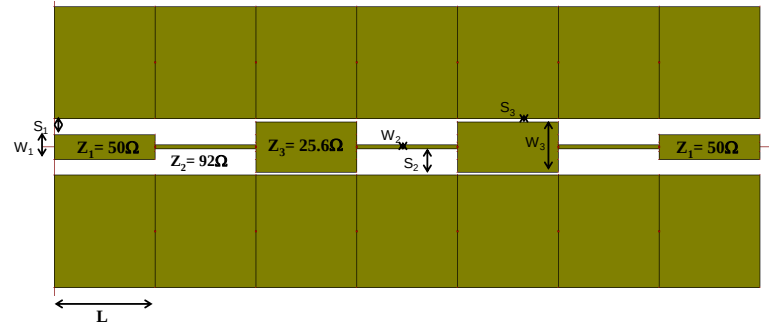
As depicted in Fig. B.7, the measured 3-dB cut-off frequency of the tunable low-pass filter shifts by 10 GHz from down- to up-state. It can also be observed that an attenuation of 4-dB exists over the whole filter bandwidth in the down-state. This pretty high insertion loss was not predicted by the simulations. As it is explained hereafter, that attenuation is mainly related to the substrate losses due to the PSC effect. This attenuation is reduced in the up-state after release of the oxide under the switchable part and hence reducing surface charge effect at that region. Since the substrate RF losses are a key factor for RF filters, we extract the effective resistivity (ρ_{eff}) of a CPW line lying on the same HR-Si substrate using the method described in [5]. The final ρ_{eff} seen by the coplanar structure is $\rho = 50 \text{ }\Omega\cdot\text{cm}$ instead of $10 \text{ k}\Omega\cdot\text{cm}$, its nominal value. This low ρ_{eff} value is due to the PSC effect at the Si/SiO_2 interface [6], [8]. In fact, the PECVD oxide presents a high density of fixed oxide charges which attract free carriers in the silicon substrate and create a high surface conduction layer. Therefore, the final effective resistivity of the wafer is reduced and hence the RF performance of the CPW line.

We simulate again the investigated low-pass filter structure using a $50 \text{ }\Omega\cdot\text{cm}$ silicon substrate. The simulated frequency response of the filter is shown in Fig. B.8. Simulations show in this case a better agreement with the measured data presented in Fig. B.7. The large attenuation in the filter bandwidth can then be explained by the degradation of the substrate resistivity.

Measurements of the filter frequency response on top of HR-Si substrate passivated with a polysilicon layer underneath the oxide is shown in Fig. B.9. It can be seen that the high density of traps provided by the trap-rich passivation layer stabilize the substrate and the attenuation caused by the parasitic surface effect at the Si/SiO_2 interface was literally eliminated.



(a)



$Z_3 = 25.6\Omega$	$Z_2 = 92\Omega$	$Z_1 = 50\Omega$
$W_3 = 192\mu\text{m}$	$W_2 = 16\mu\text{m}$	$W_1 = 94.6\mu\text{m}$
$S_3 = 11\mu\text{m}$	$S_2 = 100\mu\text{m}$	$S_1 = 60\mu\text{m}$
$L = 386\mu\text{m}$	$L = 386\mu\text{m}$	$L = 386\mu\text{m}$
$W_g = 428\mu\text{m}$	$W_g = 428\mu\text{m}$	$W_g = 428\mu\text{m}$
$\epsilon_{\text{eff}} = 5.72$	$\epsilon_{\text{eff}} = 6.11$	$\epsilon_{\text{eff}} = 6.1$
$\lambda_g = 3.132\text{mm}$	$\lambda_g = 3.025\text{mm}$	$\lambda_g = 3.034\text{mm}$

(b)

Fig. B.5: top view of the (a) fabricated CPW low-pass filter when the bending regions switched up and (b) simulated structure with the corresponding dimensions for each CPW line section.

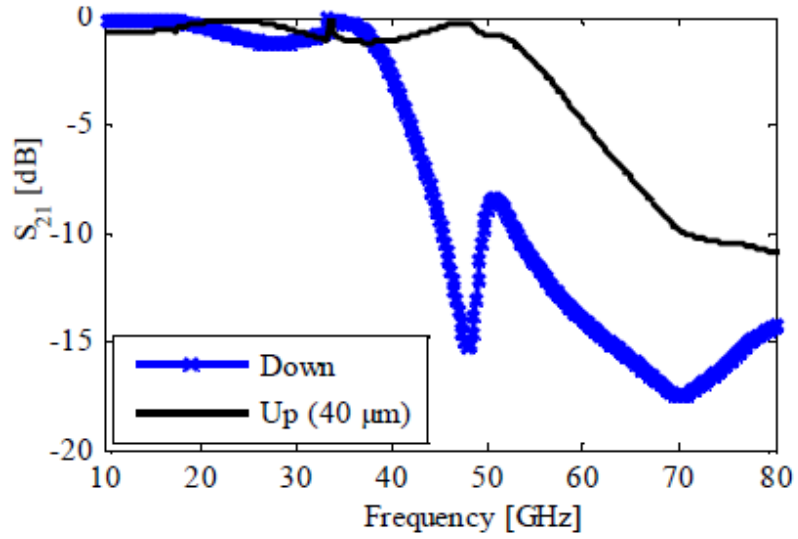


Fig. B.6: Simulated S_{21} characteristic for the low-pass filter on HR-Si substrate.

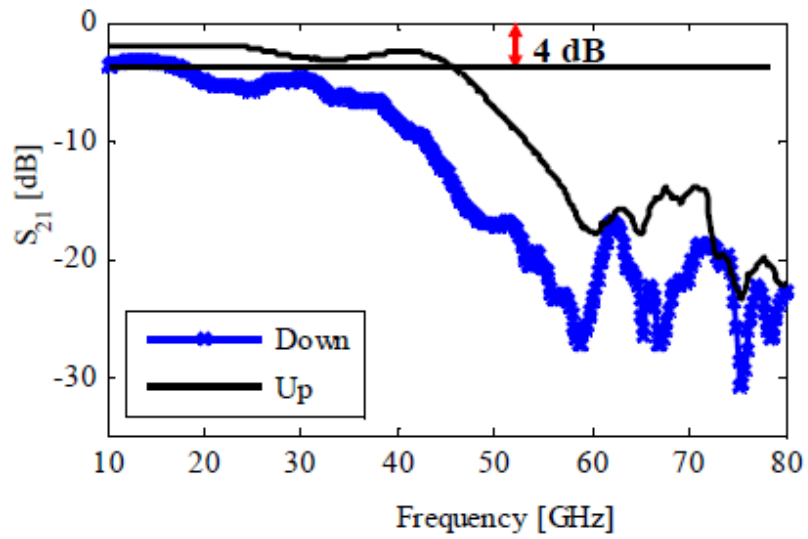


Fig. B.7: Measured S_{21} characteristic for the low-pass filter on HR-Si substrate.

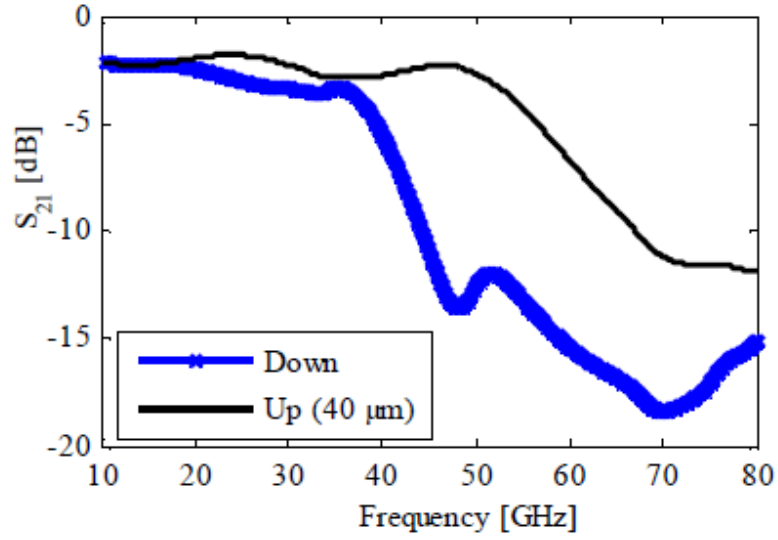


Fig. B.8: Simulated S_{21} characteristic for the low-pass filter on Si substrate with $\rho = 50 \Omega \cdot \text{cm}$.

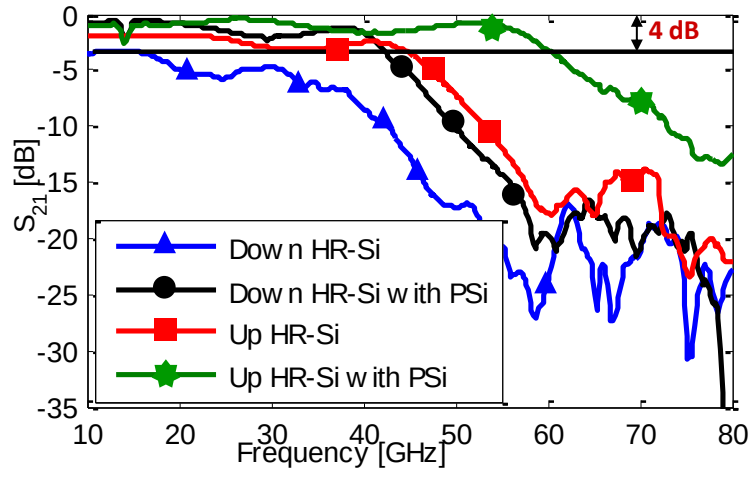


Fig. B.9: Measured S_{21} characteristics for the low-pass filter on HR-Si and HR-Si + PolySi substrates.

B.2 CONCLUSION

RF MEMS reconfigurable patch antenna and tunable low-pass filter were fabricated on top of a high resistivity silicon substrate using a low complexity fabrication process. The substrate losses and the parasitic surface effect which degrade the effective resistivity of the silicon substrate have a strong influence on the RF performance of the CPW filter. However, these variations can be drastically reduced by passivating the substrate surface with trap-rich polysilicon layer [6]. Designed CPW filters including a trap-rich layer at the SiO_2/Si interface have demonstrated a much higher stability and the shift of the cut-off frequency when the bending regions switched up is increased.

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