# Performances of Strained Nanowire Devices: Ballistic Versus Scattering-Limited Currents

**Article** *in* IEEE Transactions on Electron Devices · May 2013

DOI: 10.1109/TED.2013.2248734



**4 authors**, including:

Viet Hung Nguyen
Sorbonne Université
**114** PUBLICATIONS **1,582** CITATIONS
SEE PROFILE

Yann-Michel Niquet
Atomic Energy and Alternative Energies Commission
**263** PUBLICATIONS **6,628** CITATIONS
SEE PROFILE

# Performances of strained nanowire devices: ballistic versus scattering-limited currents

Viet-Hung Nguyen, François Triozon, Frédéric D. R. Bonnet and Yann-Michel Niquet

***Abstract*—We discuss the performances of $\langle 001 \rangle$ and $\langle 110 \rangle$ oriented gate-all-around silicon nanowire (Si NW) transistors within a Non-Equilibrium Green's Functions framework, taking surface roughness and phonon scatterings into account. We show, in agreement with previous studies, that uniaxial tensile (resp. compressive) strains can significantly improve the mobility of electrons (resp. holes) in the channel. This does not, however, necessarily result in a comparable enhancement of the device performances: Indeed, the current in short channels is limited by both the scattering and the number of sub-bands available for carrier transport in quantum confined systems (intrinsic "ballistic" resistance). The dependence of the mobility and ballistic resistance on strains can be different, which calls for a careful design of the devices. We show, in this respect, that $\langle 110 \rangle$ Si NWs provide the best opportunities for strain engineering in ultimate short channel transistors.**

***Index Terms*—Nanowire; Transistor; Mobility; Strain; Green functions**

## I. Introduction

THE challenges posed by the extreme scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) have strengthened the need for innovative device architectures with better electrostatic control and minimal short channel effects [1]. In principle, gate-all-around silicon nanowire (Si NW) transistors can achieve the best gate efficiencies, and are therefore promising candidates for sub-10 nm technology nodes [2]–[4]. However, simulations have shown that the carrier mobility usually goes down with decreasing nanowire diameter [5]–[8], which questions the benefits of these architectures. The electrical properties of semiconductor devices can, nonetheless, be improved using strain engineering techniques [9], [10]. The latter are already widespread in planar technologies, and shall be even more efficient in Si NWs, which can withstand large strains. Significant performance enhancements have been predicted in sub-10 nm Si NWs [11]–[14], and have been already observed experimentally [15].

The impact of strain however needs to be assessed in realistic short-channel devices and at high drain-source bias. The Non-Equilibrium Green's Functions (NEGF) method [16] is best suited for that purpose, because it treats quantum confinement, scattering, out-of-equilibrium and short channel effects in a unified framework. Three-dimensional (3D) NEGF simulations have already unveiled a lot of information about transport in quantum confined Si NWs (with surface roughness and/or phonons for example [17]–[23]). The carrier mobility in Si NWs has, in particular, been extracted from gate length scaling analyses, for different scattering mechanisms [21], [24].

These calculations have highlighted the importance of the "ballistic" corrections in short channel devices [25], [26]. Indeed, the current in a Si NW can be limited by the number of sub-bands $N_m$ available for carrier transport. The resistance of a ballistic channel actually tends to $1/(G_0 N_m)$ at low temperature, where $G_0 = 2e^2/h$ is the quantum of conductance. The current in ballistic Si NW devices can be computed with NEGF methods [27], or with simpler top-of-the-barrier models [28], [29]. A few studies have discussed the impact of strain on ballistic Si NW transistors [30], [31]. However, NEGF calculations capturing the interplay between strains, ballistic resistance and scattering are still missing.

In this article, we present NEGF simulations of uniaxially strained $n$- and $p$-type Si nanowire field effect transistors (NWFETs), with phonon and surface roughness scattering. This study features several novelties. It combines the strengths of the 3D NEGF approach (self-consistent treatment of scattering) with multi-bands $\mathbf{k} \cdot \mathbf{p}$ descriptions of the effects of strains on electrons and holes in Si NWs with a diameter of 8 nm, close to the size of experimental devices [3], [4]. More importantly, accurate mobilities and ballistic resistances are obtained from additional NEGF simulations on junctionless Si NWs with different lengths. This allows a quantitative analysis of the balance between ballistic and scattering-limited currents as a function of channel orientation and strains. This study extends the mobility calculations discussed in [14] and provides quantitative guidelines for strain engineering in short channel devices.

## II. Methodology

The transport properties of the Si NWs are computed in a NEGF framework [16] based on a two bands $\mathbf{k} \cdot \mathbf{p}$ model for the electrons [32] and on a three bands $\mathbf{k} \cdot \mathbf{p}$ model for the holes (no spin-orbit coupling) [33]. The two bands $\mathbf{k} \cdot \mathbf{p}$ model, which couples opposite $\Delta$ valleys, indeed reproduces the effects of non-parabolicity and shear strains on the conduction bands very well, at variance with the simple effective mass approximation [34]. Moreover, ballistic and mobility calculations (along the lines of Ref. [8]) show that spin-orbit coupling has little effect ($< 5\%$) on the current in the nanowires.

Manuscript received April 19, 2005; revised January 11, 2007. This work was supported by the French National Research Agency (ANR) project Quasanova (contract ANR-10-NANO-011-02). The calculation were run on the TGCC/Curie machine using allocations from GENCI and PRACE (project 2010PA0885).

V.-H. Nguyen, F. Bonnet and Y.-M. Niquet (e-mail: yann-michel.niquet@cea.fr) are with L_Sim, SP2M, UMR-E CEA/UJF-Grenoble 1, INAC, Grenoble, France.

F. Triozon is with CEA, LETI, MINATEC Campus, Grenoble, France.

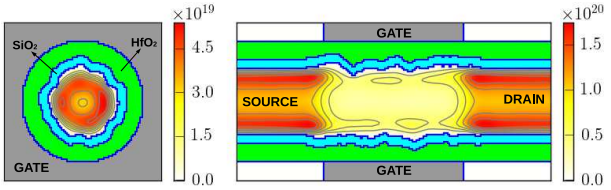


Fig. 1. The simulated devices are cylindrical gate-all-around Si NWFETs with diameter $d = 8$ nm and gate length $L_g = 16$ nm. The carrier density in a $n$-doped, unstrained [110] oriented device is plotted at $V_{\rm gs} - V_{\rm th} = 0.5$ V and $V_{\rm ds} = 25$ mV.

The devices are cylindrical gate-all-around Si NWFETs with diameter $d = 8$ nm, gate length $L_g = 16$ nm, and $\langle 001 \rangle$ or $\langle 110 \rangle$ orientation. The gate stack is made of a 1 nm thick $SiO_2$ and of a 2 nm thick $HfO_2$ shell (not included in the $\mathbf{k} \cdot \mathbf{p}$ models). The simulation domain includes 16 nm long source/drain access regions with $n$ or $p$-type doping (background dopant concentration $N = 10^{20}$ cm$^{-3}$). The channel is undoped. The $\mathbf{k} \cdot \mathbf{p}$ hamiltonians are discretized on a finite differences mesh with a 2 Å step. In uniaxially stretched Si NWs, the perpendicular strains $\varepsilon_\perp$ are computed [35] as a function of the applied longitudinal strain $\varepsilon_\parallel$ following Ref. [14].

The NEGF equations are solved self-consistently in a fully coupled mode space approach [36] (192 modes for electrons and 320 modes for holes). NEGF can account for both elastic (surface roughness) and inelastic (phonons) scattering in a seamless way. We use a standard exponential autocorrelation function model for surface roughness (SR) [37], with rms radius fluctuations $\Delta = 0.25$ nm and correlation length $L_c = 1.4$ nm. As for phonons, we use the local approximation [38] for the "lesser" self-energies $\Sigma^<$,

$$\Sigma_i^<(E) = \sum_n K_n \Xi_n G_i^<(E) \Xi_n \,. \qquad (1)$$

Here $i$ stands for a given mesh point, $K_n$ is the coupling constant for phonon mode $n$, $\Xi_n$ is a $2 \times 2$ (electrons) or $3 \times 3$ (holes) matrix mixing $\mathbf{k} \cdot \mathbf{p}$ bands, and $G_i^<(E)$ is the lesser Green function at energy $E$. For electrons, we borrowed the intra-valley acoustic deformation potential, the 3 $f$-type and the 3 $g$-type inter-valleys processes from Ref. [39]. For holes, we designed [40] a model based on the acoustic deformation potentials $a_v$, $b_v$ and $d_v$ of the valence band, and on Ref. [41] for optical phonon scattering. Both models reproduce the temperature dependence of the bulk mobilities.

## III. Results and Discussion

The current in $n$- and $p$-type Si NWFETs is plotted as a function of the gate overdrive $V_{\rm gs} - V_{\rm th}$ in Fig. 2, at low source-drain bias $V_{\rm ds} = 25$ mV in the linear regime. The threshold voltages $V_{\rm th}$ and the transconductances $g_m$ have been extracted from the ON-state data [$I = \pm g_m (V_{\rm gs} - V_{\rm th} - V_{\rm ds}/2)$], and the subthreshold slopes $S$ from the OFF-state data [$\log_{10} I(V_{\rm gs}) = \pm V_{\rm gs}/S + C$]. The $I(V_{\rm ds})$ characteristics of the same devices are plotted in Fig. 3, for three different gate overdrives.

There are two striking features on these figures. First, the ON-state performances of unstrained Si NWFETs can

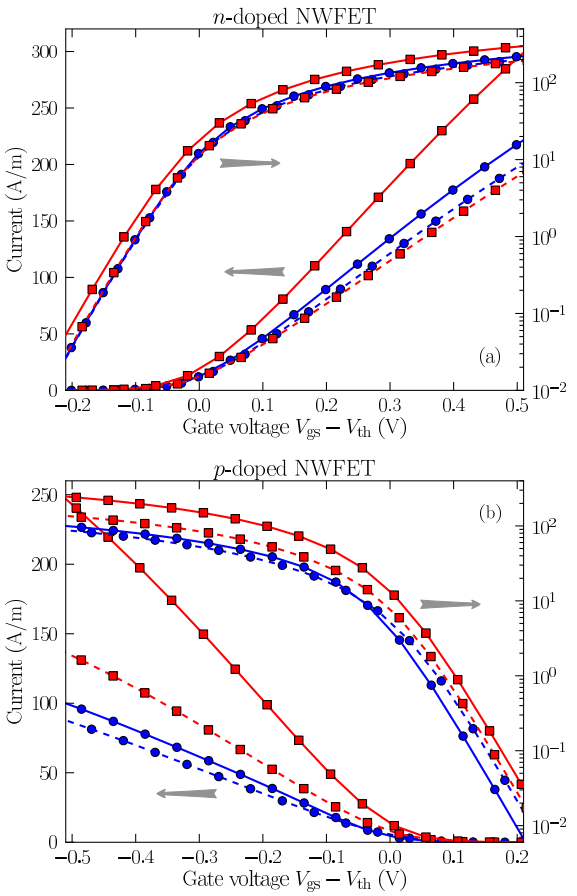


Fig. 2. Room-temperature $I(V_{\rm gs})$ characteristics of free standing (dashed lines) and uniaxially strained (solid lines) $n$- and $p$-type Si NWFETs, at low source-drain bias $V_{\rm ds} = 25$ mV. Blue lines with dots (●) are $\langle 001 \rangle$ oriented devices, while red lines with squares (■) are $\langle 110 \rangle$ oriented devices. The longitudinal strain is $\varepsilon_\parallel = 1.5\%$ for $n$-type NWFETs, and $\varepsilon_\parallel = -1.5\%$ for $p$-type NWFETs. The current is normalized with respect to the circumference $\pi d = 25.1$ nm of the nanowires.

be very dependent on the nanowire orientation. While the transconductance is about the same in $\langle 001 \rangle$ and $\langle 110 \rangle$ $n$-NWFETs, it is 60% larger in $\langle 110 \rangle$ than in $\langle 001 \rangle$ $p$-NWFETs. The currents in the saturation regime are, likewise, between 30 and 40% larger in $\langle 110 \rangle$ $p$-NWFETs (depending on the gate overdrive).

Second, the responses of these Si NWFETs to strains are very different. Whatever the orientation, uniaxial tensile strains increase the performances of $n$-NWFETs, while compressive strains tend to increase the performances of $p$-NWFETs. The improvement is however marginal in $\langle 001 \rangle$ oriented devices, while it can reach almost $2\times$ in $\langle 110 \rangle$ oriented NWFETs [15]. The subthreshold slope ranges between 70 and 75 mV/decade for all (strained and unstrained) devices.

These data suggest that the devices have different transport properties (e.g., carrier mobilities) and/or different electrostatics (gate capacitances). However, at gate overdrive $V_{\rm gs} - V_{\rm th} = 0.5$ V and low bias $V_{\rm ds} = 25$ mV for example, the carrier density per unit length, $n_{\rm 1d}$, is the same ($\pm 4\%$) in the channel of all $n$-NWFETs, and of all *but* strained $\langle 001 \rangle$ $p$-NWFETs (where it is $\sim 10\%$ lower). Transport properties are, therefore, essentially ruling the behavior of these devices.

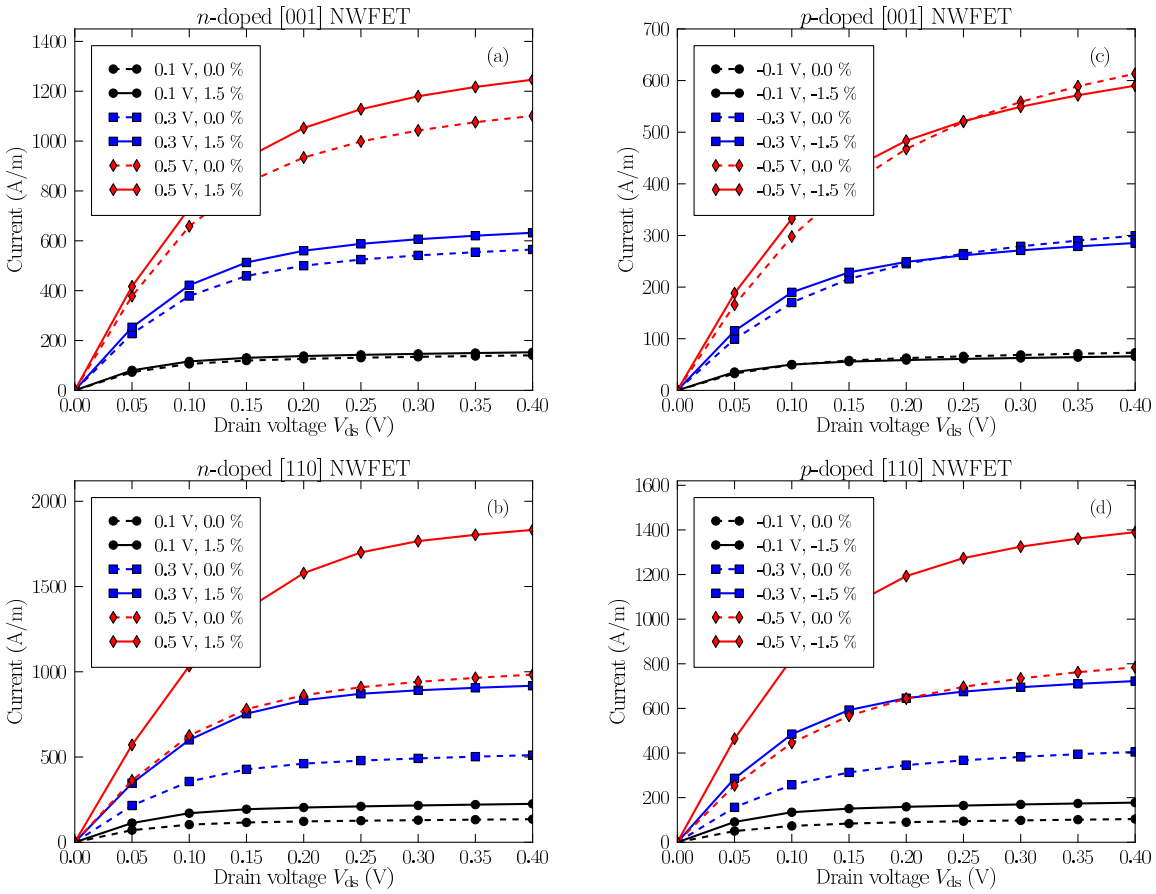


Fig. 3. Room-temperature $I(V_{\rm ds})$ characteristics of the same devices as in Fig. 2. The legend gives the gate overdrive $V_{\rm gs}-V_{\rm th}$ and the longitudinal strain $\varepsilon_{\parallel}$ for each line.

In the following, we mostly focus our discussion on the low bias (linear) regime. It nicely illustrates the physics at hand and explains at least qualitatively the trends at high bias (Fig. 3), as suggested by the simplest models for field-effect transistors [42].

As we shall confirm later, the current in the devices is mostly limited by the resistance $R_{\rm ch}$ of the channel. The resistance of the heavily doped access regions is indeed much lower than $R_{\rm ch}$ [43], thanks to the very large carrier density and the absence of SR scattering there (see Fig. 1). Our simulations are therefore essentially probing the response of the channel to strains. At low $V_{\rm ds}$, $R_{\rm ch}$ can be written:

$$R_{\rm ch}(L_g) = R_0 + \frac{L_g}{n_{\rm 1d}\mu e}\,. \qquad (2)$$

The second term ($\propto L_g$) is the usual "diffusive" resistance that can be characterized by the carrier mobility $\mu$. The first term ($R_0$) is known as the "ballistic" resistance [25], [26]. It is primarily bound to the number of sub-bands $N_{\rm m}$ available for carrier transport in the channel. At zero temperature, the resistance of a purely ballistic device is indeed $R_0 = 1/(G_0 N_{\rm m}) = 12.9{\rm k}\Omega/N_{\rm m}$. At finite temperature $T$, assuming Maxwell-Boltzmann statistics and a single transport mass $m^*$ for all sub-bands [44]:

$$\frac{1}{R_0} = -\frac{2e^2}{h}\int d\varepsilon \left(\frac{\partial f}{\partial \varepsilon}\right) t(\varepsilon) = \frac{n_{\rm 1d}e^2}{\sqrt{2\pi m^* kT}} \qquad (3)$$

where $f(\varepsilon) = \exp[(\varepsilon_f - \varepsilon)/kT]$ is the distribution function, and $t(\varepsilon)$ the transmission function, which is equal to the number of sub-bands at energy $\varepsilon$. Although the above assumptions may not hold in general, this equation nicely evidences the main parameters and trends of the problem.

In long channels, the current is ultimately limited by the diffusive term ($L_g/(n_{\rm 1d}\mu e) \gg R_0$). $R_0$ however puts a fundamental, lower limit to the contact and spreading resistance of the devices, and shall therefore be dominant in short enough channels.

We have computed the carrier mobility and ballistic resistance of the nanowires within our NEGF framework. For that purpose, we considered fully gated, junctionless Si NWs (no doped access regions) with lengths $L$ ranging from 8 to 32 nm. We applied a small, constant longitudinal electric field $V_{\rm ds} = (0.0625\ {\rm mV/nm})L$ and swept the gate voltage $V_{\rm gs}$. We monitored the average carrier density $n_{\rm 1d}$ in the nanowires and their resistance $R(L, n_{\rm 1d}) = V_{\rm ds}/I$. We finally extracted $\mu(n_{\rm 1d})$ and $R_0(n_{\rm 1d})$ from a linear regression with Eq. (2). This is illustrated in Fig. 4 for different surface roughness profiles. In general, the resistance is pretty linear with $L$ and

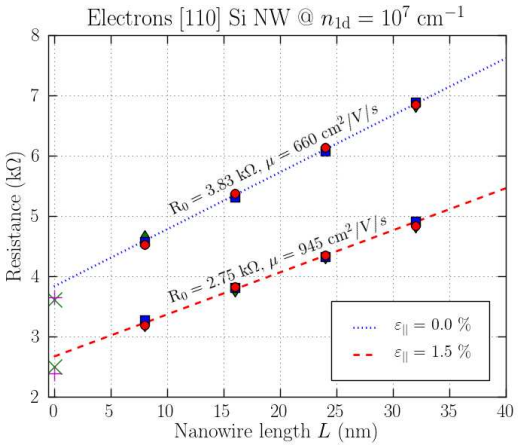


Fig. 4. Resistance $R$ as a function of length $L$ in free standing and uniaxially strained $\langle 110 \rangle$ Si NWs with diameter $d = 8$ nm. The electron density is $n_{1d} = 10^7$ cm$^{-1}$. The data for 3 different surface roughness profiles are plotted for each length. The lines are fits by Eq. (2). The resistance $R_0$ computed in a purely ballistic device ["$\times$" symbols at $L = 0$] and with Eq. (3) ["+" symbols at $L = 0$] are also given.

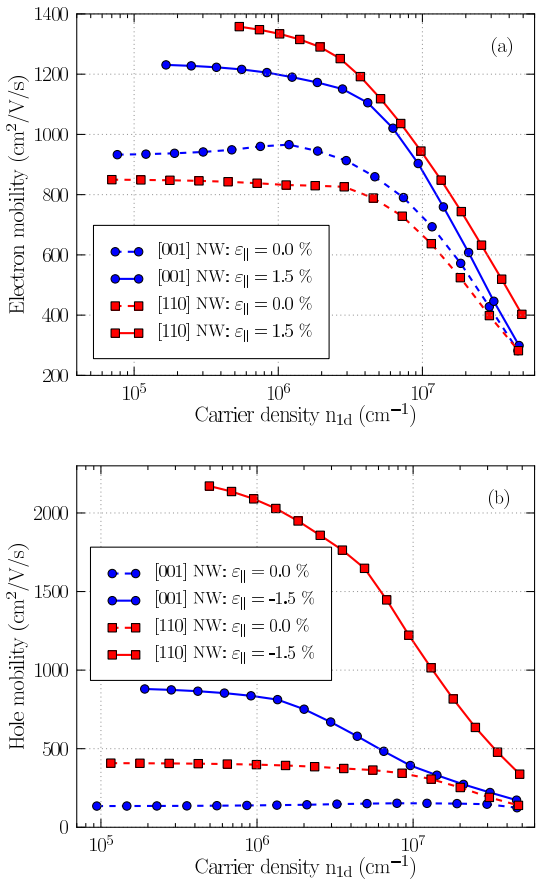


Fig. 5. Room-temperature, phonon+surface roughness limited electron and hole mobilities as a function of carrier density in free standing and uniaxially strained Si NWs with diameter $d = 8$ nm.

does not show much variability (except possibly in the shortest NWs). The NWs are, indeed, typically much longer than the correlation length of the SR disorder, and electron-phonon interactions help mitigate localization. We have also reported on Fig. 4 the resistance $R_0$ computed in a purely ballistic NW (neither phonons nor SR scattering), and with the simple Eq. (3). Actually, the ballistic resistance $R_0$ extracted from Eq. (2) is always slightly larger than the resistance of the purely ballistic NW, as is tends to be limited by the thinnest sections in rough devices [45].

The mobility is plotted as a function of the carrier density in Fig. 5. At low carrier density, where the current is mostly limited by electron-phonon interactions, the data are consistent with the results of Refs. [8] and [14]. The electron mobility is almost the same in $\langle 001 \rangle$ and $\langle 110 \rangle$ Si NWs. It is enhanced by uniaxial tensile strains, that empty the heavy $\Delta$ valleys off $\Gamma$ into the light $\Delta$ valleys at $\Gamma$, as illustrated in Fig. 6 (up to $50\%$ increase at $\varepsilon_\parallel = 1.5\%$). The hole mobility is $3\times$ larger in $\langle 110 \rangle$ than in $\langle 001 \rangle$ Si NWs, and is strongly improved by unaxial compressive strains, that promote light hole bands (up to $5-6\times$ increase at $\varepsilon_\parallel = -1.5\%$). The picture is however different at large carrier density, where surface roughness scattering comes into play. First, the differences between unstrained $\langle 001 \rangle$ and $\langle 110 \rangle$ get thinner, especially for holes. Second, strains hardly improve the carrier mobility in $\langle 001 \rangle$ Si NWs, while they remain an efficient booster in $\langle 110 \rangle$ Si NWs. These trends are reminiscent of the shape of the band structure at high energy; In this respect $\langle 110 \rangle$ Si NWs exhibit worthwhile properties (in particular, high carrier velocities) in a larger energy window than $\langle 001 \rangle$ Si NWs, especially in strained devices.

The devices of Fig. 2 typically operate in the $\lesssim 2 \times 10^7$ carriers per cm range. It is clear from Fig. 5 that the mobility $\mu$ does not quantitatively explain the orientational and strain dependence of the current. In particular, the increase of current in strained $\langle 001 \rangle$ NWs is much lower than expected from the mobility data. We therefore now turn our attention to the first term of Eq. (2), $R_0$.

The ballistic resistance $R_0$ extracted from the linear regression and the total resistance $R_{\rm ch}$ of the 16 nm long channel are plotted in Fig. 7. $R_0$ is actually as large as $0.75R_{\rm ch}$ in unstrained $\langle 110 \rangle$ $n$-NWFETs, and about $0.6R_{\rm ch}$ in unstrained $\langle 110 \rangle$ $p$-NWFET. It is, therefore, a major part of the resistance of the channel. The relation $I \sim V_{\rm ds}/R_{\rm ch}$ is satisfied within $15\%$ by the devices of Fig. 2. This confirms that the resistance of the highly doped source/drain access regions, and the resistance due to mode mismatch at the entrance of the channel, are both negligible here – a basic assumption also made in top-of-the-barrier models for example [28], [29].

Understanding the dependence of the ballistic resistance on strains is, therefore, of primary importance. Let us focus on $n$-NWFETs first. In $\langle 001 \rangle$ Si NWs, the $\Delta$ valleys split into light, fourfold degenerate $\Delta_1 \equiv \Delta_{x,y}$ valleys at $\Gamma$ ($m^* = 0.19$) and heavier, twofold degenerate $\Delta_2 \equiv \Delta_z$ valleys off $\Gamma$ ($m^* = 0.92$, see Fig. 6). Likewise, in $\langle 110 \rangle$ Si NWs, the $\Delta$ valleys split into light, twofold degenerate $\Delta_1 \equiv \Delta_z$ valleys at $\Gamma$ ($m^* = 0.18$) and heavier, fourfold degenerate $\Delta_2 \equiv \Delta_{x,y}$ valleys off $\Gamma$ ($m^* = 0.55$) [14]. $R_0$ is therefore the ballistic resistance $R_{0,\Delta_1}$ of the $\Delta_1$ valleys in parallel with the ballistic resistance $R_{0,\Delta_2}$ of the $\Delta_2$ valleys; namely

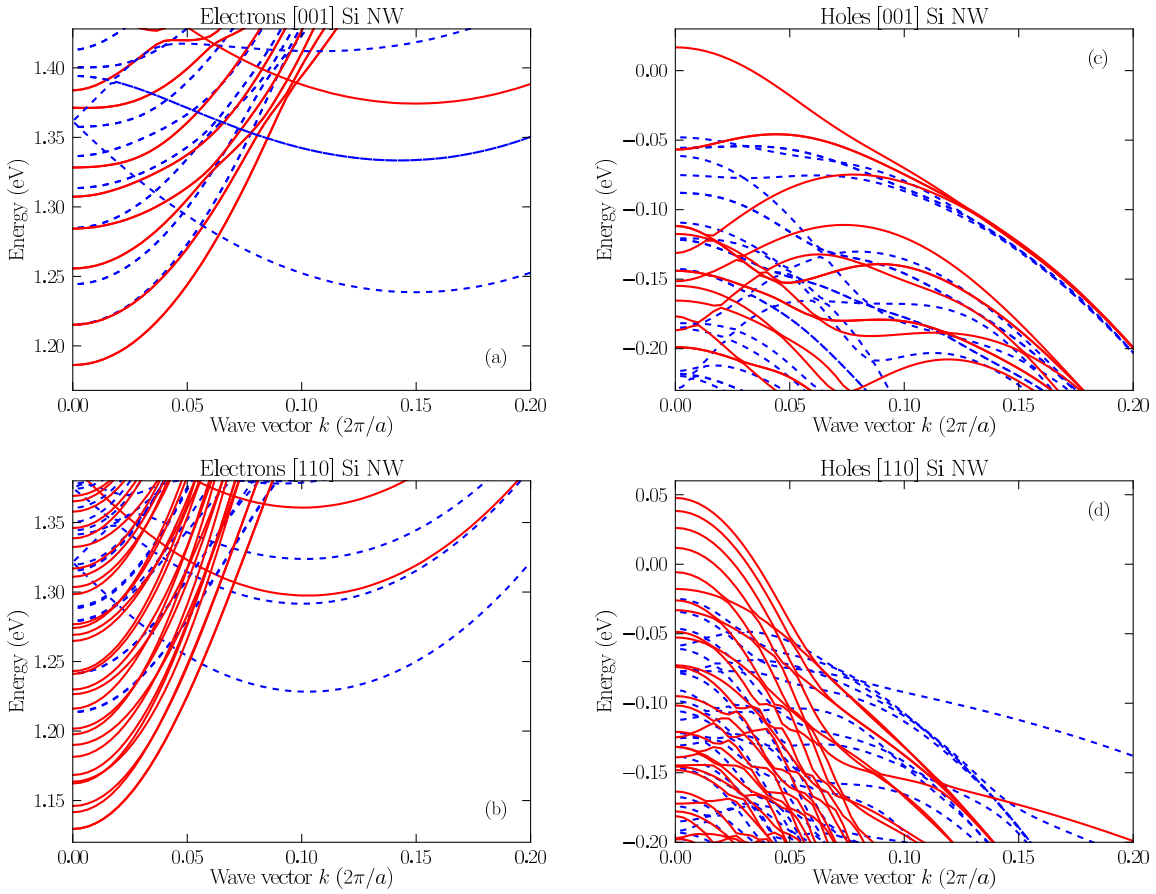


Fig. 6. Conduction and valence band structures of free standing (dotted blue lines) and uniaxially strained (solid red lines) Si NWs with diameter $d = 8$ nm ($\varepsilon_{\parallel} = 1.5\%$ for electrons and $\varepsilon_{\parallel} = -1.5\%$ for holes). $a = 5.431$ Å is the lattice parameter of Si.

$R_0^{-1} = R_{0,\Delta_1}^{-1}(n_1) + R_{0,\Delta_2}^{-1}(n_2)$, where $n_1$ and $n_2$ are the partial densities in $\Delta_1$ and $\Delta_2$ valleys (see "+" symbols on Fig. 4 for an illustration). Since $R_0 \propto m^{*1/2}$, the $\Delta_2$ valleys show a much larger ballistic resistance than the $\Delta_1$ valleys (for a given density). Under unaxial tensile strains, the $\Delta_2$ valleys rise in energy and empty into the $\Delta_1$ valleys, which increases $R_{0,\Delta_2}$, but decreases $R_{0,\Delta_1}$ (hence $R_0$). The gain is, however, much greater in $\langle 110 \rangle$ NWFETs because *i*) the population of the unfavorable $\Delta_2$ valleys is larger in unstrained $\langle 110 \rangle$ than in unstrained $\langle 001 \rangle$ devices (fourfold vs twofold $\Delta_2$ degeneracy), and *ii*) the mass of the $\Delta_1$ valleys of $\langle 110 \rangle$ NWs decreases from $m^* = 0.18$ at $\varepsilon_{\parallel} = 0$ down to $m^* = 0.13$ at $\varepsilon_{\parallel} = 1.5\%$ due to shear strains [14], [34]. Therefore, the $\langle 110 \rangle$ $n$-NWFETs show a $35\%$ decrease in ballistic resistance $R_0$ at $\varepsilon_{\parallel} = 1.5\%$, while the $\langle 001 \rangle$ $n$-NWFETs only show a modest $12\%$ improvement.

As for holes, uniaxial compressive strains push heavy holes down and bring light holes at the top of the valence band in $\langle 110 \rangle$ $p$-NWFETs (see Fig. 6). This increases the population of light with respect to heavy holes, and significantly reduces the ballistic resistance $R_0$ (by up to $38\%$ at $\varepsilon_{\parallel} = -1.5\%$). The situation is more complex and contrasted in $\langle 001 \rangle$ Si NWs. As discussed in Ref. [14], the holes are very heavy in unstrained nanowires; Although strains improve the picture, many high-lying valence bands remain little dispersive, which degrades the ballistic resistance at large carrier densities, and limits the enhancement of the performances of strained $\langle 001 \rangle$ $p$-NWFETs. Also, as pointed out earlier, the carrier density is about $10\%$ lower in strained $\langle 001 \rangle$ $p$-NWFETs than in other $p$-type devices at large gate overdrives. Although our estimate for the threshold voltage can be questioned, the $\langle 001 \rangle$ $p$-NWFETs are the only devices showing large discrepancies between current and charge based criterions for $V_{\rm th}$, reminiscent of the stronger non-linearities visible, e.g., on Fig. 7.

## IV. Conclusion

Our results demonstrate that the ballistic resistance is an important part of the total resistance of short channels and must be optimized along with the mobility. In general, unaxial tensile strains, which increase electron mobility, also decrease ballistic resistance in $n$-NWFETs, while uniaxial compressive strains, which increase hole mobility, also decrease ballistic resistance in $p$-NWFETs. The quantitative trends are, however, different in $\langle 001 \rangle$ and $\langle 110 \rangle$ Si NWs. The ballistic resistance is not improved as much as the mobility in strained $\langle 001 \rangle$ Si NWs, so that the performances of short channels are little enhanced. On the contrary, uniaxial strains consistently improve ballistic resistance and mobility in $\langle 110 \rangle$ Si NWs, providing much more opportunities for efficient strain engineering in these nanowires.

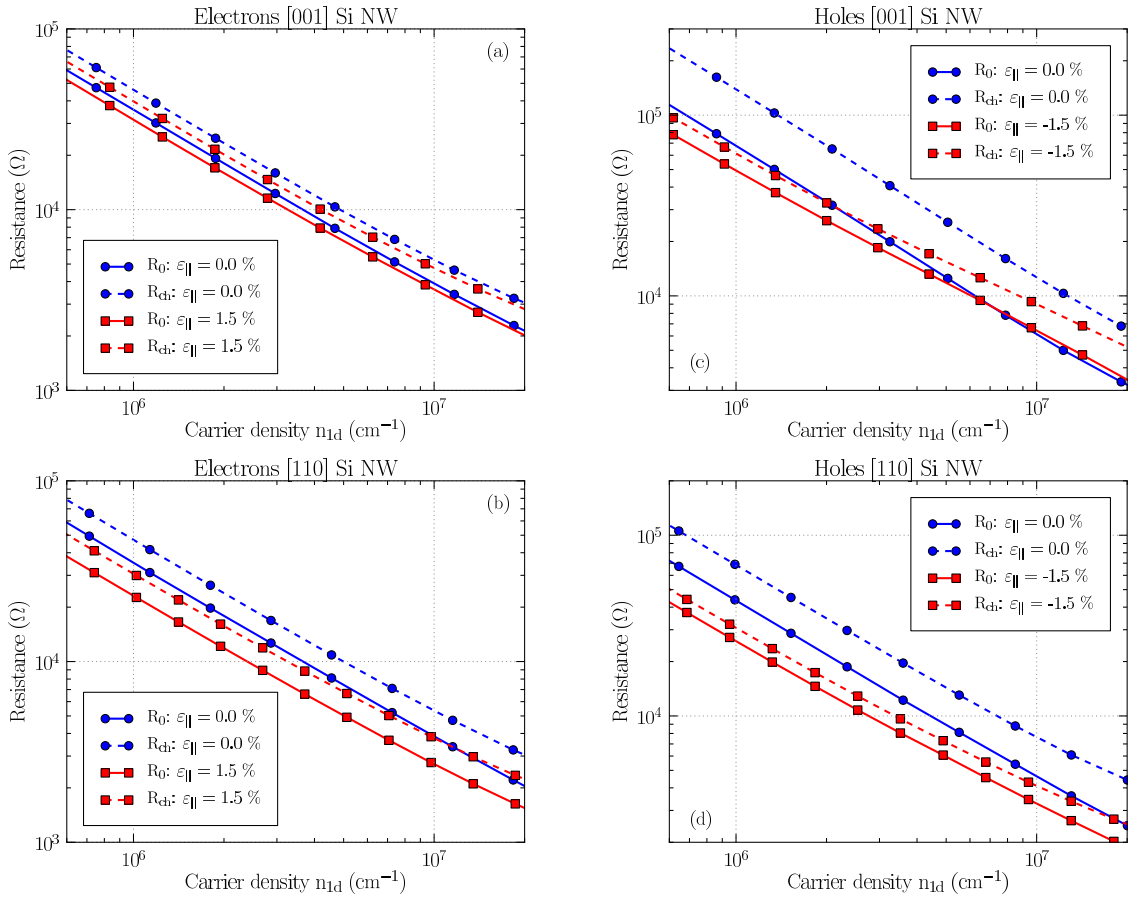


Fig. 7. Ballistic resistance $R_0$ as a function of carrier density in free standing and uniaxially strained Si NWs with diameter $d = 8$ nm. The total (ballistic+diffusive) resistance $R_{\rm ch}$ of a 16 nm long channel is also plotted for comparison.

## REFERENCES


[1] "Itrs roadmap." [Online]. Available: http://www.itrs.net/

[2] N. Singh, A. Agarwal, L. Bera, T. Liow, R. Yang, S. Rustagi, C. Tung, R. Kumar, G. Lo, N. Balasubramanian, and D.-L. Kwong, "High-performance fully depleted silicon nanowire (diameter $\leq$ 5 nm) gate-all-around cmos devices," *Electron Device Letters, IEEE*, vol. 27, no. 5, pp. 383–386, 2006.

[3] M. Cassé, K. Tachi, S. Thiele, and T. Ernst, "Spectroscopic charge pumping in si nanowire transistors with a high-kappa/metal gate," *Applied Physics Letters*, vol. 96, no. 12, p. 123506, 2010.

[4] S. Barraud, R. Coquand, M. Casse, M. Koyama, J.-M. Hartmann, V. Maffini-Alvaro, C. Comboroure, C. Vizioz, F. Aussenac, O. Faynot, and T. Poiroux, "Performance of omega-shaped-gate silicon nanowire mosfet with diameter down to 8 nm," *Electron Device Letters, IEEE*, vol. 33, no. 11, pp. 1526–1528, 2012.

[5] R. Kotlyar, B. Obradovic, P. Matagne, M. Stettler, and M. D. Giles, "Assessment of room-temperature phonon-limited mobility in gated silicon nanowires," *Applied Physics Letters*, vol. 84, no. 25, pp. 5270–5272, 2004.

[6] E. B. Ramayya, D. Vasileska, S. M. Goodnick, and I. Knezevic, "Electron mobility in silicon nanowires," *Nanotechnology, IEEE Transactions on*, vol. 6, no. 1, pp. 113–117, 2007.

[7] N. Neophytou and H. Kosina, "Atomistic simulations of low-field mobility in si nanowires: Influence of confinement and orientation," *Physical Review B*, vol. 84, p. 085313, 2011.

[8] Y.-M. Niquet, C. Delerue, D. Rideau, and B. Videau, "Fully atomistic simulations of phonon-limited mobility of electrons and holes in ⟨001⟩- , ⟨110⟩-, and ⟨111⟩-oriented si nanowires," *Electron Devices, IEEE Transactions on*, vol. 59, no. 5, pp. 1480–1487, 2012.

[9] S. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-si: extending the cmos roadmap," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 1010–1020, 2006.

[10] M. O. Baykan, S. E. Thompson, and T. Nishida, "Strain effects on three-dimensional, two-dimensional, and one-dimensional silicon logic devices: Predicting the future of strained silicon," *Journal of Applied Physics*, vol. 108, no. 9, p. 093716, 2010.

[11] K.-H. Hong, J. Kim, S.-H. Lee, and J. K. Shin, "Strain-driven electronic band structure modulation of si nanowires," *Nano Letters*, vol. 8, no. 5, pp. 1335–1340, 2008.

[12] D. Shiri, Y. Kong, A. Buin, and M. P. Anantram, "Strain induced change of bandgap and effective mass in silicon nanowires," *Applied Physics Letters*, vol. 93, no. 7, p. 073114, 2008.

[13] T. Maegawa, T. Yamauchi, T. Hara, H. Tsuchiya, and M. Ogawa, "Strain effects on electronic bandstructures in nanoscaled silicon: From bulk to nanowire," *Electron Devices, IEEE Transactions on*, vol. 56, no. 4, pp. 553–559, 2009.

[14] Y.-M. Niquet, C. Delerue, and C. Krzeminski, "Effects of strain on the carrier mobility in silicon nanowires," *Nano Letters*, vol. 12, no. 7, pp. 3545–3550, 2012.

[15] P. Hashemi, L. Gomez, and J. Hoyt, "Gate-all-around n-mosfets with uniaxial tensile strain-induced performance enhancement scalable to sub-10-nm nanowire diameter," *Electron Device Letters, IEEE*, vol. 30, no. 4, pp. 401–403, 2009.

[16] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of nanoscale devices," *Proceedings of the IEEE*, vol. 96, pp. 1511–1550, 2008.

[17] M. Luisier, A. Schenk, and W. Fichtner, "Atomistic treatment of interface roughness in si nanowire transistors with different channel orientations," *Applied Physics Letters*, vol. 90, no. 10, p. 102103, 2007.

[18] A. Martinez, M. Bescond, J. Barker, A. Svizhenko, M. Anantram, C. Millar, and A. Asenov, "A self-consistent full 3-d real-space negf simulator for studying nonperturbative effects in nano-mosfets," *Electron Devices, IEEE Transactions on*, vol. 54, no. 9, pp. 2213–2222, 2007.

[19] N. Pons, N. Cavassilas, F. Michelini, L. Raymond, and M. Bescond, "Original shaped nanowire metal-oxide-semiconductor field-effect tran-

sistor with enhanced current characteristics based on three-dimensional modeling," *Journal of Applied Physics*, vol. 106, no. 5, p. 053711, 2009.
[20] S. Poli, M. Pala, T. Poiroux, S. Deleonibus, and G. Baccarani, "Size dependence of surface-roughness-limited mobility in silicon-nanowire fets," *Electron Devices, IEEE Transactions on*, vol. 55, no. 11, pp. 2968–2976, 2008.
[21] S. Poli and M. Pala, "Channel-length dependence of low-field mobility in silicon-nanowire fets," *Electron Device Letters, IEEE*, vol. 30, no. 11, pp. 1212–1214, 2009.
[22] K. Rogdakis, S. Poli, E. Bano, K. Zekentes, and M. G. Pala, "Phonon- and surface-roughness-limited mobility of gate-all-around 3c-sic and sinanowire fets," *Nanotechnology*, vol. 20, no. 29, p. 295202, 2009.
[23] A. Cresti, M. Pala, S. Poli, M. Mouis, and G. Ghibaudo, "A comparative study of surface-roughness-induced variability in silicon nanowire and double-gate fets," *Electron Devices, IEEE Transactions on*, vol. 58, no. 8, pp. 2274–2281, 2011.
[24] M. Aldegunde, A. Martinez, and A. Asenov, "Non-equilibrium green's function analysis of cross section and channel length dependence of phonon scattering and its impact on the performance of si nanowire field effect transistors," *Journal of Applied Physics*, vol. 110, no. 9, p. 094518, 2011.
[25] S. Datta, F. Assad, and M. Lundstrom, "The silicon mosfet from a transmission viewpoint," *Superlattices and Microstructures*, vol. 23, no. 34, pp. 771–780, 1998.
[26] M. Shur, "Low ballistic mobility in submicron hemts," *Electron Device Letters, IEEE*, vol. 23, no. 9, pp. 511–513, 2002.
[27] M. Shin, S. Lee, and G. Klimeck, "Computational study on the performance of si nanowire pmosfets based on the $k \cdot p$ method," *Electron Devices, IEEE Transactions on*, vol. 57, no. 9, pp. 2274–2283, 2010.
[28] N. Neophytou, A. Paul, M. Lundstrom, and G. Klimeck, "Bandstructure effects in silicon nanowire electron transport," *Electron Devices, IEEE Transactions on*, vol. 55, no. 6, pp. 1286 –1297, 2008.
[29] A. Paul, S. Mehrotra, M. Luisier, and G. Klimeck, "Performance prediction of ultrascaled sige/si core/shell electron and hole nanowire mosfets," *Electron Device Letters, IEEE*, vol. 31, no. 4, pp. 278–280, 2010.
[30] H. Minari, T. Kitayama, M. Yamamoto, and N. Mori, "Strain effects on hole current in silicon nanowire fets," in *Simulation of Semiconductor Processes and Devices (SISPAD), 2010 International Conference on*, 2010, pp. 207–210.
[31] L. Zhang, H. Lou, J. He, and M. Chan, "Uniaxial strain effects on electron ballistic transport in gate-all-around silicon nanowire mosfets," *Electron Devices, IEEE Transactions on*, vol. 58, no. 11, pp. 3829–3836, 2011.
[32] J. C. Hensel, H. Hasegawa, and M. Nakayama, "Cyclotron resonance in uniaxially stressed silicon. ii. nature of the covalent bond," *Physical Review*, vol. 138, pp. A225–A238, 1965.
[33] G. Bastard, *Wave mechanics applied to semiconductor heterostructures*, ser. Monographies de physique. Les Éditions de Physique, 1988.
[34] V. Sverdlov, G. Karlowatz, S. Dhar, H. Kosina, and S. Selberherr, "Two-band k.p model for the conduction band in silicon: Impact of strain and confinement on band structure and mobility," *Solid-State Electronics*, vol. 52, no. 10, pp. 1563–1568, 2008.
[35] In [001] SiNWs, $\varepsilon_\perp = -c_{12}\varepsilon_\parallel/(c_{11}+c_{12})$. In [110] SiNWs, $\varepsilon_{\perp,x} = -4c_{12}c_{44}\varepsilon_\parallel/K$ along the [001] direction, and $\varepsilon_{\perp,y} = -[(c_{11}-c_{12})(c_{11}+2c_{12})-2c_{11}c_{44}]\varepsilon_\parallel/K$ along the $[1\bar{1}0]$ direction, where $K=(c_{11}-c_{12})(c_{11}+2c_{12})+2c_{11}c_{44}$, and $c_{11}=166$ GPa, $c_{12}=64$ GPa and $c_{44}=79.6$ GPa are the elastic constants of bulk silicon.
[36] J. Wang, E. Polizzi, and M. Lundstrom, "A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation," *Journal of Applied Physics*, vol. 96, no. 4, pp. 2192–2203, 2004.
[37] S. M. Goodnick, D. K. Ferry, C. W. Wilmsen, Z. Liliental, D. Fathy, and O. L. Krivanek, "Surface roughness at the si(100)-sio$_2$ interface," *Physical Review B*, vol. 32, pp. 8171–8186, 1985.
[38] S. Jin, Y. J. Park, and H. S. Min, "A three-dimensional simulation of quantum transport in silicon nanowire transistor in the presence of electron-phonon interactions," *Journal of Applied Physics*, vol. 99, no. 12, p. 123719, 2006.
[39] C. Jacoboni and L. Reggiani, "The monte carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Reviews of Modern Physics*, vol. 55, pp. 645–705, 1983.
[40] V. H. Nguyen, F. Triozon and Y. M. Niquet, to be submitted.
[41] F. Szmulowicz, "Calculation of optical- and acoustic-phonon limited conductivity and hall mobilities for $p$-type silicon and germanium," *Physical Review B*, vol. 28, pp. 5943–5963, 1983.
[42] T. Ytterdal, C. Y. Hua, and T. A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*. Chichester: Wiley, 2003.
[43] The purpose of the access regions included in the simulations is to provide an almost ideal source and drain of carriers, and to allow for the potential to reach steady conditions at the boundaries. It is not intended to mimick a real, resistive access to the nanowire.
[44] Assuming sub-bands with edges $E_i$, the transmission reads $t(\varepsilon) = \sum_i \Theta(\varepsilon - E_i)$ while the density of states reads $\rho(\varepsilon) = (2\sqrt{2m^*}/h)\sum_i(\varepsilon - E_i)^{-1/2}$. Factorization of the density $n_{1\mathrm{d}} = \int d\varepsilon f(\varepsilon)\rho(\varepsilon)$ in Eq. (3) then yields the final result.
[45] The mismatch between the resistance of a purely ballistic nanowire and the $R_0$ term in a rough nanowire can alternatively be cast into a length dependent effective mobilty, as discussed in Ref. [21].

**Viet-Hung Nguyen** received the M.S. degree in physics from the Institute of Physics and Hanoi National University of Education, Hanoi, Vietnam in 2007, and the Ph.D. degree in physics from University of Paris-Sud, Orsay, France in 2010. He has been a researcher with the Institute of Physics in Hanoi (on leave) from 2010, and a postdoctoral fellow with the L_Sim laboratory of INAC, CEA, Grenoble since 2012. He has been involved in the simulation of electron and spin polarized transport in graphene-based devices in his Ph.D thesis and is now working on the theory and modelling of the transport properties of nanowire devices.

**François Triozon** received a M.S. degree in condensed matter physics from Ecole Normale Supérieure de Lyon in 1996, and a Ph.D. degree in physics from the University of Grenoble in 2002. Since June 2005, he is a permanent researcher at LETI, CEA Grenoble, France. He is working on the simulation of electronic transport in semiconducting nanowires, carbon nanotubes, and graphene, using quantum approaches.

**Frederic D. R. Bonnet** received his Ph.D. in theoretical and Astrophysics in 2002 and his Ph.D. in Electrical and Electronics Engineering in 2009 from the University of Adelaide, Adelaide, Australia. In 2011 he joined the ongoing efforts at the Institute for the Nanoscience and Cryogenics (INAC) as a Postdoctoral research engineer at CEA. He is working in high performance computing, in particular on GPU based coding, as well as various aspects of grid computing within nanoscience.

**Yann-Michel Niquet** received an engineering degree in electronics from the ISEN school in Lille, a master degree in Physics from the university of Paris XI in 1998, and a PhD degree in physics from the university of Lille in 2001. Since december 2003, he is a permanent researcher at the Institute for Nanosciences and Cryogenics (INAC) of the CEA Grenoble, France. He is working on the electronic, optical and transport properties of semiconductor nanostructures, in particular semiconductor nanowires.