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Wideband characterization of SOI materials and devices

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Abstract

In the present paper, the interest of wideband characterization for the development of integrated technologies is highlighted. The extraction of electrical equivalent circuits for passive and active devices in silicon-on-insulator (SOI) technology is described. The electrical characteristics of the SOI substrate versus DC bias and high frequency signal is presented as well as the wideband behavior of several advanced MOSFETs, such as 120 nm partially depleted (PD) SOI MOSFETs, 120 nm dynamic threshold (DT) voltage MOS, 50 nm FinFETs as well as long-channel planar double gate MOSFETs. Based on these wideband equivalent circuits, RF designers can define optimized circuits and precious information can be delivered to engineers for the improvement of the fabrication process as well.
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1. Introduction

The extraction of an electrical equivalent circuit is of first importance for, of course, the circuit designers but also for the engineers working on the optimization of fabrication processes. Indeed, thanks to the direct wideband extraction techniques presented in this paper we can analyze deeply and quantify the impact of each part (intrinsic and extrinsic) of a specific device under test on its global electrical behavior. For instance, the systematic extraction of the parasitic access resistances at the source, drain and gate electrodes of a transistor can be used to control the efficiency of the silicidation process of these contacts, the extraction of the overlap capacitance to monitor the diffusion of impurities below the gate oxide, and so on.

Usually, when passive devices such as transmission lines, integrated inductors, interdigitated capacitors, etc. are analyzed over a wide frequency band, the impact of DC bias is rarely considered. Moreover, at the early stage of advanced transistors development only the static behavior of novel devices is actually considered. Indeed, the I_{on}/I_{off} ratio, the subthreshold slope (S), the threshold voltage roll-off and the drain induced barrier lowering (DIBL) are the primary figures of merit that are extracted after each process run and which provide insights on the process quality. The static analysis of the built transistors is then extended to the measurements of the gate transconductance (G_m) in saturation as well as the output conductance (G_d) or early voltage (V_{EA}). A typical feature of a node development scheme is that the dynamic behavior of advanced devices is most of the time considered only at the end of the fabrication process developments. Moreover, this dynamic analysis is usually limited to the frequency band of available vectorial network analyzer (VNA) leading to an unexplored frequency band located from a few Hz up to 1 GHz.

However, a full frequency band analysis is precious for separating physical phenomena taking place in advanced MOS devices and which are characterized by clearly distinct time constants. Indeed, thermal and floating body effects typically appear from DC up to a few kHz in partially depleted (PD) SOI devices. In the MHz range the efficiency of the body contact in body-contacted (BC) PD SOI MOSFETs starts to degrade and untied carriers (i.e., minority carriers in the substrate or majority carriers in a floating body) can no longer follow the AC excitation. Finally, in the GHz range the relaxation time related to

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majority carriers is no more negligible and most of the parasitic capacitances and resistances specific to the 3-D physical structure mainly affect the dynamic behavior of active devices as well as the crosstalk between circuits lying on the same substrate.

Electrical characterization from DC up to 110 GHz of integrated transmission lines as well as advanced SOI MOS devices will be presented in this paper. Several direct characterization techniques have been developed for extracting small and large signal electrical models. Beside these measurement and extraction techniques, the use of finite element simulation tools are useful to explore and understand the device internal physics. For instance, the 3-D module of Atlas from Silvaco was used for simulating the fringing capacitances of gate-all-around MOS as well as FinFETs [1].

In Section 2, the wideband behavior of high-resistivity SOI substrate, the performance of coplanar waveguide (CPW) lines as well as the crosstalk problematic are presented. In Sections 3–5, the body contact behavior of PD SOI MOSFETs is deeply analyzed versus DC bias and frequency. The small signal equivalent circuits of multiple gate devices such as FinFETs and planar double gate are presented in Sections 6 and 7, respectively. Based on these extracted equivalent electrical circuits, technological problems to be solved for multiple gate MOSFETs are highlighted.

2. Analysis of SOI substrates

2.1. MOS capacitor

An active or passive device integrated into a SOI technology is basically lying on a oxide layer (named BOX for buried oxide) on top of a silicon substrate. This bilayered structure (BOX-silicon substrate) being underneath each integrated device and circuit, its electrical analysis is of first importance. In order to analyze the electrical behavior of the SOI substrate over a wide frequency band, we proposed to extract the equivalent capacitance and conductance of a simple capacitive structure, similar to a MOS capacitor, using the buried and field oxides as the insulator layer. The behavior of the MOS structure, or more generally called MIS (Metal–insulator–semiconductor) structure, has been reported in numerous papers several years ago. Most authors studied the behavior of this multilayered structure assuming that the majority carriers in the semiconductor substrate respond to bias variations without delay. They consider the relaxation time of majority carriers is negligible [2–4]. Others were interested in fundamental transmission properties of planar lines on semiconductor substrate [5–8]. For a microstrip line, RLCG equivalent circuits were developed for each propagation modes. For the quasi-transverse electro-magnetic (quasi-TEM) dielectric mode [5] they implicitly consider the relaxation time of majority carriers in the substrate through the definition of propagation parameters. Here, the fundamental mechanisms of carriers in a MOS structure as function of applied voltages and frequency are described. This study is necessary to develop SOI substrate models valid over a wide frequency band. The interpretation of the equivalent conductance and capacitance (macroscopic parameters) of the MOS structure will allow to understand the behavior of the minority and majority carriers in the structure (microscopic phenomena). The equivalent capacitance calculated by MEDICI for an idealized MOS capacitor versus various frequencies and bias conditions is presented in Fig. 1 for a high-resistivity p-type substrate (5000 Ω cm). The results are obtained from an AC analysis superposing a small sine signal (v_{ac}) at various frequencies to the DC bias condition. The variation of the MOS capacitance for low and medium frequencies (from 1 Hz to 10 kHz) obtained with MEDICI agrees with what is widely explained in the literature [2–4]. We find the different well known regimes of operation in function of bias conditions and frequency: accumulation for negative bias conditions, inversion or deep depletion for the positive bias conditions. But this theory is valid only if we assume that the majority carriers (the holes in this case) respond to the excitation v_{ac}, i.e., their inertia is negligible. The 2-D MEDICI simulations clearly show that there exists a frequency point above which neither minority nor majority carriers can follow the excitation such that the MOS equivalent capacitance drastically vanishes to a mere value $\varepsilon_0\varepsilon_{Si}S/t_{Si}$ (Fig. 1, for frequencies above 1 GHz), where ε_{Si}, t_{Si}, and S are the relative silicon permittivity, the silicon substrate thickness and the area of the MOS capacitor, respectively. These simulated results have been validated by measurements of a MOS capacitor on a wide frequency band in [9].

We see that it is very important to take into account the relaxation time of majority carriers in the silicon substrate. Above the relaxation frequency of interfacial polarization, the inertia of majority carriers is not negligible and is

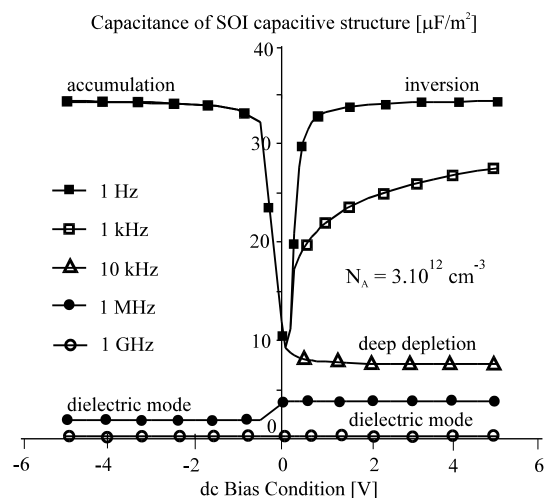

Fig. 1. Simulated small signal characteristics of MOS capacitor versus applied DC voltage for different frequencies and the total oxide thickness $t_{ox} = 1$ μm, Si substrate thickness $t_{Si} = 500$ μm and $\rho_{Si} = 5000$ Ω cm.

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defined by $\tau = \varepsilon_{Si} \cdot \rho_{Si}$. Contrary to purely resistive previous crosstalk models [10,11], the relaxation time of majority carriers in the silicon substrate is not neglected and is modeled by the simple RC networks as presented in [12].

2.2. Transmission lines

Microstrip lines (MS) and coplanar waveguides (CPW) are widely used in monolithic microwave integrated circuits (MMIC's) as interconnects and matching networks. Designing low-loss transmission lines is therefore a key factor in order to obtain high performance MMIC's. Since silicon is by nature a non-magnetic material, a detailed analysis of the losses in silicon-based MMIC should consider only two distinct contributions: substrate (α_{sub}) and conductor (α_{cond}) losses. When α_{sub} and α_{cond} are both low, it is usually admitted that the overall losses of a planar structure can be estimated from the sum of both sources: $\alpha_{tot} = \alpha_{sub} + \alpha_{cond}$ [13]. Yet our attention in this work will be restricted to substrate losses only, which are intimately related to the electrical characteristics of the silicon wafer. In this context high-resistivity (HR) silicon substrates ($\rho_{Si} > 3$ kΩ cm) have been demonstrated to be adequate for microwave applications [14].

Indeed, simulation results displayed in Fig. 2 outline how this parameter affects substrate and total losses for a typical CPW line. These data were obtained with analytical formulas presented in [15], and assuming a metal conductivity of 3.10^7 S/m. It is seen that substrate losses are small ($\alpha_{sub} \approx 0.1$ dB/cm) when the effective resistivity of the substrate (ρ_{eff}) is close to 3 kΩ cm and become clearly meaningless compared to conductor losses (α_{cond}) when ρ_{eff} reaches 10 kΩ cm.

However in [16], Reyes et al. showed that CPW losses increase if an insulating SiO_2 layer is grown between the

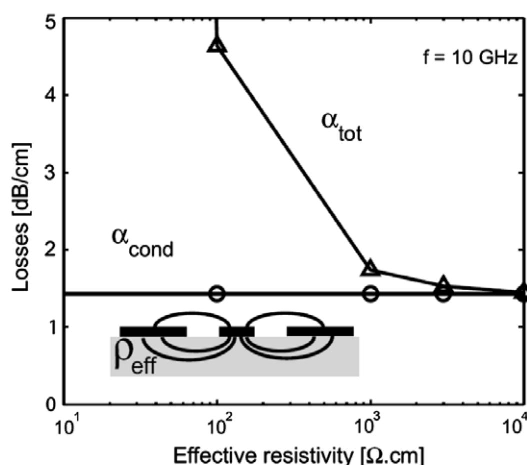

Fig. 2. Simulated total (α_{tot}) and conductor (α_{cond}) losses according to [15] for a 50 Ω-coplanar waveguides (CPW), with central conductor width of 40 μm and spacing between conductors of 24 μm, versus the effective resistivity of the silicon substrate at 10 GHz.

silicon and the metal lines. They attribute this effect to the presence of free carriers at the silicon/oxide interface. In those studies no RF measurements of CPW were performed for other bias values than 0 V. In current applications however DC bias is usually added to the RF signal propagation along the CPW or MS lines. This DC bias supply is approximately 1–3 V for CMOS circuits and typically higher than 10 V for integrated switches and MEMS devices [17]. The dependence of the losses with respect to the applied bias in the case of CPW lines has been experimentally studied by Zhao et al. in [18]. The authors showed that losses increase when an accumulation or an inversion layer exists at the insulator/silicon interface.

Similarly, high-resistivity SOI wafers suffer from parasitic conduction at the substrate surface due to the presence of an inverted layer underneath the buried oxide (BOX) [16,19]. In [20], we investigated the effect of parasitic surface conduction in the case of different technologies, all relying on oxidized p-type HR bulk/SOI substrates. The passive structures investigated in this work were fabricated using two industrial technologies (techno A and B) as well as three experimental, one metal layer home-made processes (techno C, D and E). In all cases, the metallic structures were patterned on either oxidized p-type HR Unibond SOI (techno A, B, C) or oxidized p-type HR bulk-Si (techno D and E) substrates. For techno E, the substrate was passivated with polysilicon before the oxidation step. Additional technological details are provided in Table 1. Fifty Ohm-characteristic impedance CPW lines with similar geometry (central conductor width of 40 μm, ground plane spacing of 80 μm, ground plane width >110 μm) were present on all investigated wafers. For all lines the RF measurements were conducted by also applying a DC bias (V_a) on the central conductor.

Those total RF losses (α_{tot}) of the CPW lines were extracted from the measured *S*-parameters with a TLR method. They are reported at 10 GHz in Fig. 3. Fig. 3a shows that losses may be significantly affected by (V_a) when the oxide thickness is well below 1 μm (techno C). Indeed, in that case highly positive or negative biases have a significant impact on the free carrier concentration underneath the oxide, thereby strongly affecting substrate losses. This effect is clearly attenuated for thicker oxides (techno A, B and D). The V_a value for which losses are minimum ($V_{a,min}$) corresponds to a state of deep depletion underneath the oxide. This point depends on the flatband voltage of the structure and is therefore dependent on the oxide thickness (t_{ox}) as well as the oxide charge density (Q_{ox}). As the figure shows, the value of $V_{a,min}$ may thus significantly change from one technology to the other, while for a given technology, it should also be dependent on the level of the lowest metal layer used to process the structures. The figure also indicates that substrate passivation with polysilicon (techno E) significantly reduces RF losses while getting rid of the V_a influence. This is because traps present inside the polysilicon layer can absorb the free carrier layer and pin the surface potential to a value independent on V_a.

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Table 1
Additional information on the different technologies investigated in [20]

Techno	Starting wafer	Node (μm)	Metal layer	t_{ox} (μm)	Si passivation	Oxide type
A	HR SOI	1	M3/xx M3	3/NA/3	No	BOX + oxidized SOI + interlayer dielectrics
B	HR SOI	0.13	M5–M6/M1–M2/xx	4.1/1.17/NA	No	BOX + oxidized SOI + interlayer dielectrics
C	HR SOI	1	M1	0.3/NA/NA	No	BOX + oxidized SOI
D	HR bulk	1	M1	1/NA/NA	No	PECVD
E	HR bulk	1	M1	1/NA/1	polysilicon	PECVD

The data in columns 4 and 5, respectively, indicate the metal levels that were used and the total equivalent oxide thickness for CPW: lines and crosstalk structures.

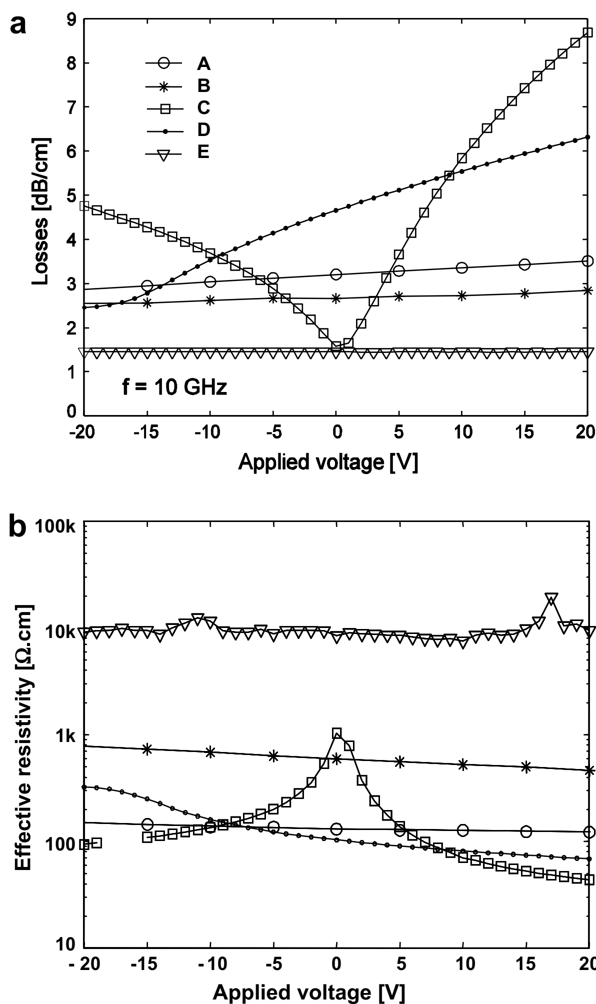

Fig. 3. (a) CPW losses and (b) effective substrate resistivity extracted from CPW measured on the different technologies as a function of DC bias and at 10 GHz.

For all wafers, the effective resistivity (ρ_{eff}) of the distinct wafers shown in Fig. 3b was extracted according to a method depicted in [21]. This figure of merit represents the resistivity value that a uniform (without oxide nor space charge effect) substrate should have in order to sustain identical losses. Not surprisingly, the highest ρ_{eff} value is observed for the passivated substrate, while at 0 V, the lowest value is obtained for the low quality (Q_{ox}-rich) plasma enhanced chemical vapor deposition (PECVD) oxide. It should also be noticed that due to the inverted layer underneath the BOX in techno A and B, the extracted values of ρ_{eff} do not exceed 130 and 580 Ω cm, respectively. These values are both more than one order of magnitude lower than the nominal substrate resistivity and demonstrate the enormous impact of Q_{ox} on ρ_{eff}.

In [22], we have presented a new technique to passivate the substrate surface of HR silicon wafers and avoid effective resistivity degradation in oxide-covered HR wafers. The proposed method consists in the low pressure chemical vapor deposition (LPCVD) of amorphous silicon followed by Si-crystallization at 900 °C with a RTA. This method was compared with previously published techniques (LPCVD polysilicon in [23] or passivation with amorphous silicon in [24]) and was demonstrated to perform better in terms of substrate loss reduction: effective resistivity values higher than 10 kΩ cm were reported, compared to 3 and 6 kΩ cm in the case of amorphous Si and LPCVD polysilicon passivation, respectively. The new passivation method was also shown to present better rms surface roughness ($\sigma = 0.37$ nm) and to remain effective after long thermal anneals. A successful bonding of this layer with an oxidized substrate was achieved, showing that this new passivation technique could be introduced at reduced cost inside a smartcut or BESOI process in order to fabricate SOI wafers with enhanced resistivity, i.e., higher than 10 kΩ cm.

2.3. Crosstalk

The coupling through the substrate is an important limiting factor in mixed-mode high frequency integrated circuits, including switched capacitors filters, A/D and D/A converters. The analog part of the chip must indeed work in a noisy environment and, unlike the digital part, is very sensitive to voltage variations of the power supplies as well as of the substrate ground. On the other hand, digital circuits, due to their strong and sudden signal switching, inject a significant amount of noise in the substrate. This noise is transmitted to the analog part lying on the same chip, causing a reduction of its performance. The increase of the operating frequency, required by the new telecom circuits, raises the noise injection to a level that could compromise the performance of the circuit. Therefore, the study of the coupling characteristics of the substrate as well as the crosstalk reduction techniques are becoming more

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and more important. In [12], the interest of very high-resistivity SOI substrates, as recommended for very high frequency or microwave applications, for reducing the crosstalk have been analyzed in details. To study the behavior of the substrate from a crosstalk point of view, we used a simplified representation of the mixed-mode circuit. Considering a complete circuit does not allow for deep physical understanding of the mechanisms that rule the phenomena, and therefore for finding ways to reduce crosstalk. For that purpose coupled metallic pads lying on the BOX are considered for emitting and sensing the noise coupling through the silicon substrate (inset of Fig. 4).

As mentioned in previous paragraph, oxidized HR silicon (such as HR SOI material) is known to suffer from parasitic surface conduction (PSC) below the oxide, which reduces the effective resistivity (ρ_{eff}) of the wafers by more than one order of magnitude. As demonstrated in [12], the substrate resistivity has a direct impact on the crosstalk level. Fig. 4 displays the crosstalk level ($|S_{21}|$) measured for various DC bias (symmetrically applied on the two signal pads) values. The figure reports significantly higher ($\sim$13 dB at 0 V) crosstalk level below 1 GHz and a strong bias dependence for the standard HR SOI (un-passivated) wafer, due to conductive effects in the substrate and PSC [20]. The substrate-passivated wafer on the other hand displays no bias dependence and exhibits 20 dB/dec curves, suggesting a purely capacitive coupling in that frequency range and thus, a lossless substrate behavior.

In [25], we investigated the impact of the presence of a polysilicon layer below the buried oxide (BOX) on the performance of an *industrial* SOI CMOS technology. The RF behavior of passive devices is analyzed using both CPWs and crosstalk structures, demonstrating that the substrate passivated with polysilicon behaves as virtually lossless. The effect of the underlying polysilicon on the performance of *active* devices (MOSFETs) is also studied. We reported no effect of the underlying polysilicon on the DC and RF behavior of the MOSFETs. This suggests that substrate passivation using polysilicon is a promising tool to completely eradicate substrate losses in HR SOI wafers while maintaining the performance of functional SOI logic as well as high speed SOI circuits at its highest level.

3. Gate-induced floating body effects in ultrathin oxide PD SOI MOSFET

Tunneling through gate oxides about 2 nm-thick is one of the major challenges faced by today's bulk-Si and SOI CMOS technologies. Gate tunneling does not only increase device leakage and power dissipation, but also leads to charging and discharging of PD SOI MOSFET body region causing floating body and device history-dependent effects [26,27]. For n-type PD SOI MOSFETs, gate tunneling injects holes into the floating body thus increasing its voltage. This affects the device DC-characteristics and induces the so-called gate-induced floating body effects (GIFBE) recently disclosed in [28,29]. The impact of GIFBE on device DC transconductance was carefully examined in [28,29], in which it was shown that gate tunneling induces a sharp second peak in the transconductance (G_{m}) – gate voltage curve of the studied devices. It was also demonstrated that the amplitude as well as the location of this peak are dependent on the measurement conditions and the device history. Recently, we proposed a method based on wideband small signal frequency measurements to characterize the dynamics of GIFBE [30]. This study was performed on n-channel 120 nm PD SOI MOSFETs with a silicon film and a buried oxide thickness of 150 and 400 nm, respectively, and a gate oxide of approximately 2 nm-thick. The DC measurements were performed with an HP4145 at a drain bias of 50 mV and using a delay time of 2 s between successive DC points. The results of the DC measurements clearly display GIFBE (Fig. 5), since a second peak appears in the G_{m} versus V_{g} curve. This peak is associated with a DC body voltage increase caused by the injection of holes, which are generated by electron

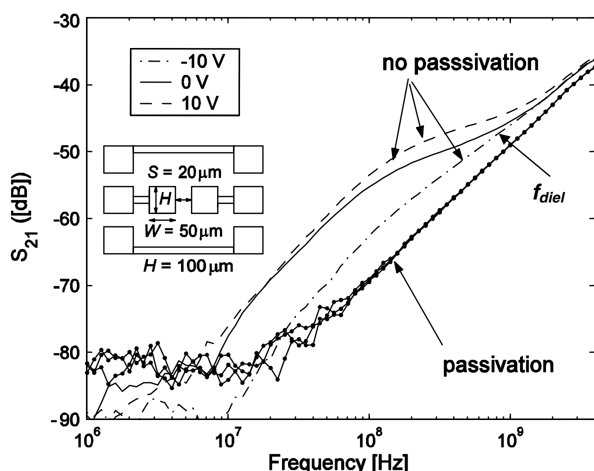

Fig. 4. Measured crosstalk on the passivated and un-passivated HR SOI wafers.

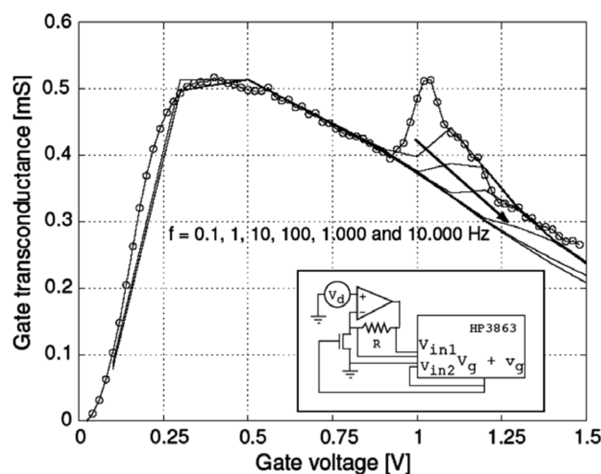

Fig. 5. Total gate transconductance versus gate voltage for a floating body PD SOI MOSFET with $L = 2$ μm, $W = 60$ μm and $V_{\text{d}} = 50$ mV.

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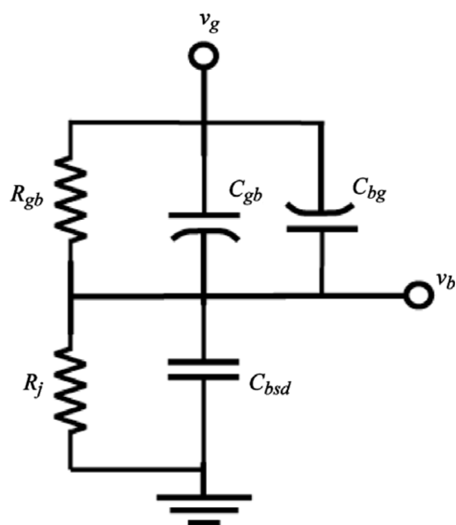

Fig. 6. Equivalent circuit of internal body node dynamic behavior due to AC gate excitation through ultrathin gate oxide for a floating body PD SOI MOSFET.

valence band tunneling through the gate oxide [28,29]. The experimental set up used for the AC measurements is depicted in the inset of Fig. 5. The small amplitude (20 mV) AC signal at the gate electrode was superimposed on the DC bias using an HP3563 System Analyzer. The AC variations of the drain current were recorded by measuring the potential drop across a resistance and an operational amplifier was also used to fix the DC drain bias at 50 mV. The AC measurements were performed between 0.1 Hz and 10 kHz for various DC bias conditions. The AC values are displayed in Fig. 5 for different frequencies.

These AC variations of G_m are expected to have negative impacts on low frequency analog circuits requiring high gain and high accuracy. For example, in the case of operational amplifiers, they may cause gain reduction at very low frequencies and produce circuit instabilities due to reduced settling time constants. As shown in details in [30] GIFBE are characterized by a very low frequency pole that is associated with the high impedance seen by the floating body toward external nodes. These effects can be relatively well reproduced with the BSIMSOI model and with a simple equivalent AC circuit that includes the internal body node as well as gate tunneling (Fig. 6).

4. High frequency degradation of body-contacted PD SOI MOSFET output conductance

Partially depleted SOI technology suffers from non-linearities in MOSFETs output conductance introduced by the so-called ‘‘kink effect’’. Under DC or low frequency conditions, this inconvenient has now been successfully overcome by several alternative solutions, such as fully depleted (FD), body tied (BT) or dynamic threshold (DT) MOS devices (Fig. 7a) [31]. However, with the aggressive downscaling of channel length and SOI film thickness the efficiency of the body contact is reduced due to an

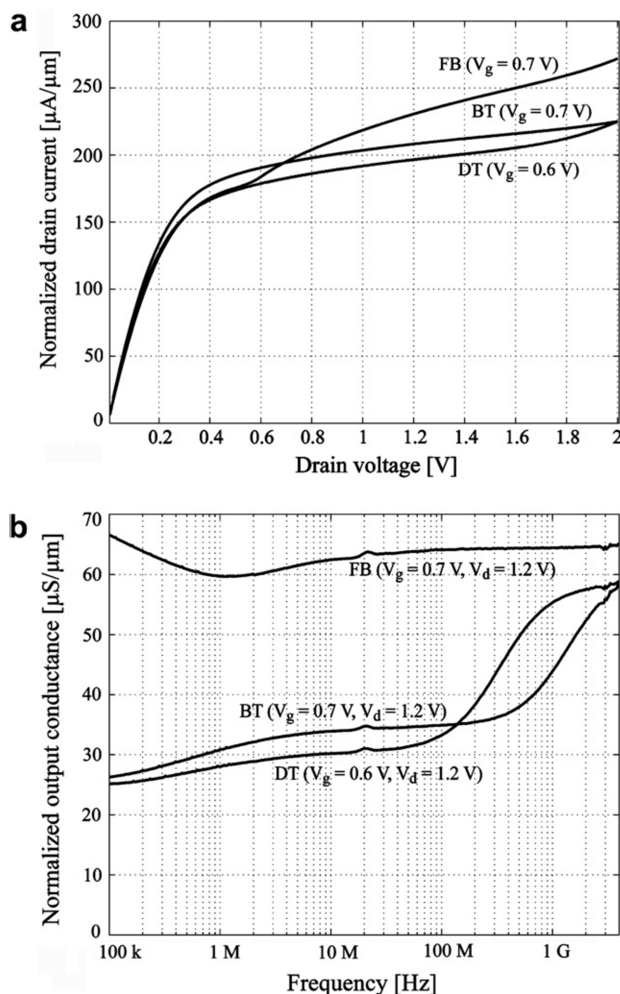

Fig. 7. (a) Measured I_d normalized by the total drawn gate width versus drain voltage and (b) measured normalized output conductance measured as a function of the frequency for the measured FB, BT, DT PD SOI MOSFETs with $L = 0.18$ µm.

increase of body resistance. In [32,33], we analyzed the efficiency of the body contact from an output conductance point of view by comparing the G_d values measured on floating body (FB), BT, DT and FD devices of the 0.18 and 0.24 µm SOI technology node. The measurements were performed in DC and in the 100 kHz–4 GHz frequency range. At low frequencies, Fig. 7b highlights the significant improvement obtained on G_d by connecting the body to the source or the gate, since both DT and BT structures exhibit a value of G_d more than two times lower than on FB devices. However, it seems that this positive effect is lost at higher frequencies, since both DT and BT devices suffer from a 150% G_d degradation between DC and high frequency (4 GHz) levels. To explain and discuss these observations we proposed in [32,33] a small signal modeling of the PD devices seen from the drain terminal. The model includes the body region and its accesses to external nodes. It also accounts for AC impact ionization effects and AC charging of body potential. The model clearly points out the non-zero value of the body resistance (R_{be}) as the origin

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of the G_d degradation. Reducing R_{be} by technological means would then provide an efficient way to reject this parasitic G_d increase to higher frequencies. In the next section an original method based on three-port RF measurements [34] to accurately extract the body resistance in body-accessed PD SOI MOSFETs is briefly described.

5. Extraction of the body contact resistance

Accurate characterization of R_{be} is crucial to assess the efficiency of the body contact in a given technology. It can also be used to assess the validity of compact models such as BSIMSOI. The proposed method is based on the measurement of S-parameters over a wide frequency band under three-port VNA configuration: the two classical ports for the gate and the drain and the third port is connected to the body of the device.

The measured devices originate from a 0.13 μm SOI technology from ST-Microelectronics, Crolles, France. Different geometries (varying number of fingers (N_f) or finger width (W_f)) and body connections (either to the gate (DT) or to a third RF access) were considered. In all cases the body was accessed at both sides of the active area in order to reduce R_{be}. The S-parameters were measured with a multiport Rhode & Schwartz VNA up to 8 GHz and were de-embedded with a three-port open subtraction method.

The modeling of the RF PD SOI devices was based on the small signal equivalent circuit presented in Fig. 8. It can be seen that both intrinsic (subscript i) and extrinsic (subscript e) elements were considered between each pair of electrodes, including the body (B). By extrinsic, we mean all parasitics that could not be removed during the de-embedding step. The modeling of the body node was therefore achieved by considering all extrinsic capacitances (C_{bge}, C_{bse} and C_{bde}), its access resistance (R_{be}), its intrinsic body-gate (C_{bgi}) as well as body-source (C_{bsi}) and body-drain (C_{bdi}) junction capacitances, and its intrinsic body-source junction resistance (R_{jbsi}). The body-drain junction resistance was neglected due to reverse biasing of this junction when devices are biased in saturation. The extraction of R_{be} was performed by analyzing the output admittance seen from the body node terminal (Y_{33}). Indeed, as shown in Fig. 9 the value of $\mathrm{Im}(Y_{33})/(2\pi f)$ clearly exhibits a pole-zero pair dependence, which is typical of the simple R–C network included in Fig. 9. In this circuit, the high frequency (C_{HF}) value of $\mathrm{Im}(Y_{33})/(2\pi f)$ is simply the sum of all extrinsic capacitances seen from the body terminal (i.e., $C_{HF} = C_{be} = C_{bse} + C_{bde} + C_{bge}$) while its low frequency value (C_{LF}) is the sum of all intrinsic and extrinsic capacitances seen from the body terminal (i.e., $C_{LF} = C_{bsi} + C_{bdi} + C_{bgi} + C_{be}$). In these conditions, it is immediate to see that the pole expression is given by

$$f_p = \frac{1}{R_{be}(C_{LF} - C_{HF})} = \frac{1}{R_{be}(C_{bsi} + C_{bgi} + C_{bdi})} \quad (1)$$

and is therefore strongly dependent on the value of R_{be}.

By fitting the R–C network on the measurements this value could then be extracted. Fig. 10 shows the value of R_{be} obtained for devices with varying N_f (with constant $N_f \cdot W_f$ product) and W_f (with constant N_f) values. It is seen that (1) R_{be} closely decreases as $(1/N_f)^2$ (similarly to R_{ge} [35]) while (2) a linear dependence with W_f is observed. These two trends agree with predictions made by the

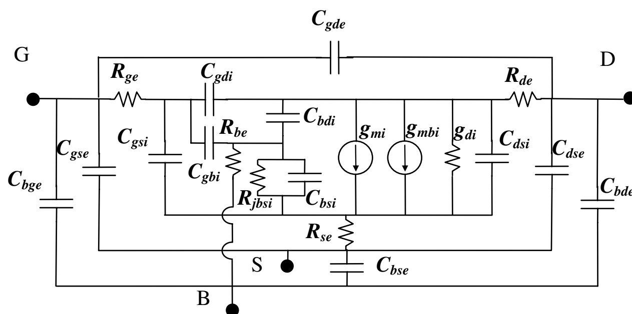

Fig. 8. Complete small signal equivalent circuit of the three-port devices, including the external body node.

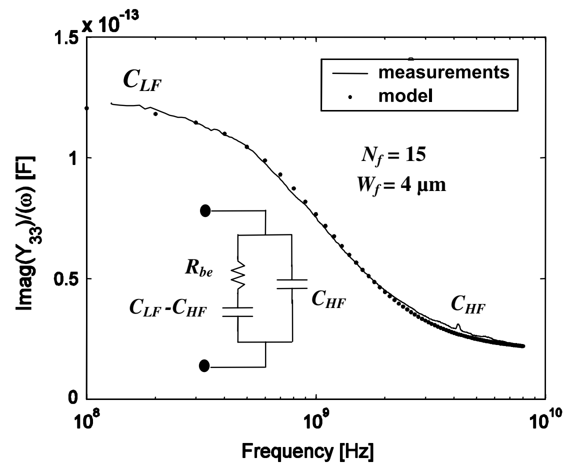

Fig. 9. Measured and simulated $\mathrm{Im}(Y_{33})/\omega$ data as a function of frequency for $V_g = V_b = 0.6$ V and $V_d = 1.2$ V, inset: R–C model used.

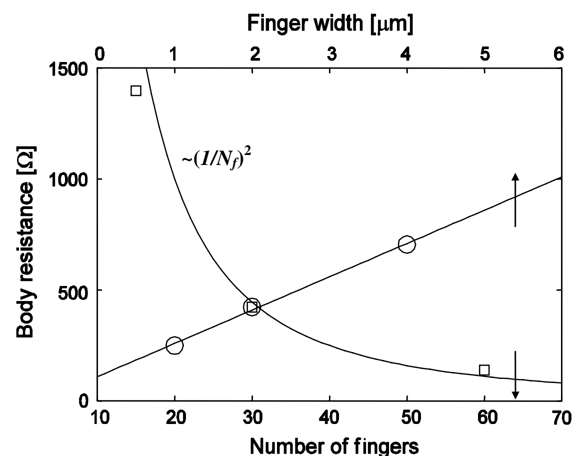

Fig. 10. Extracted values of R_{be} with respect to W_f and N_f.

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scalable BSIMSOI model [36], further supporting the validity of the extraction method.

The extrapolated value of R_{be} obtained for $W_f = 0$ (~150 Ω) therefore provides a good estimation of the parasitic resistance associated with the body interconnects (R_{bout}) outside the active region. The figure shows that its contribution is not negligible with regards to the overall value of R_{be}. Indeed, normalized values of R_{be} and R_{bout} were found to be close to 21 kΩ/μm/finger and 2.25 kΩ/finger, respectively, assuming only one contact per finger. The body node characterization was further achieved by extracting (C_{bge}, C_{bgi}) and (C_{bde}, C_{bdi}) from the high frequency and low frequency parts of Im(Y_{31}) and Im(Y_{32}), respectively. The body-source capacitances were then obtained from C_{LF} and C_{HF} and the back gate transconductance (g_{mbi}) was given by Re(Y_{23}). The value of R_{jbsi} could theoretically be extracted from $\mathrm{Re}(Y_{33}) = (R_{be} + R_{jbsi})^{-1}$ at low frequencies but was too high (>100 kΩ) to be accurately measured. It was therefore assumed to be infinitely high in the model. The rest of the device parameters were obtained with the cold-FET method [35], while R_{se}, R_{de} and R_{ge} were obtained with a method depicted in [37]. Fig. 11a and b show that an accurate modeling of both real and imaginary parts of the Y-parameters are obtained up to ~4 GHz for a 4 μm-wide device with $N_f = 15$, $V_g = 0.6$ V, $V_d = 1.2$ V, $V_b = 0.6$ V. The model was then further tested by connecting the body to the gate terminal, forming a two-port network and compared with measurement results obtained on a DTMOSFET with the same geometry. It is seen in Fig. 11a and b

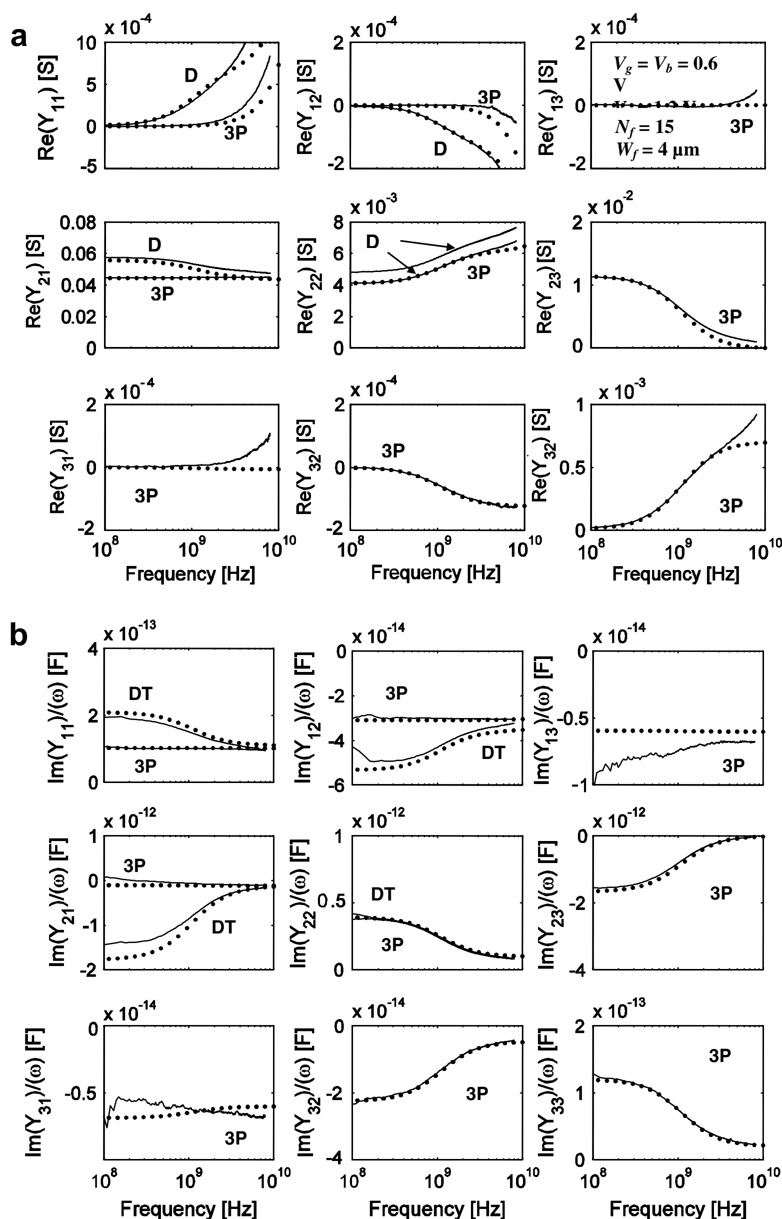

Fig. 11. Measured (straight lines) and simulated (dots): (a) Re(Y_{ij}) and (b) Im(Y_{ij})/ω for the three-port device (3P) as well as for the DT MOSFET (DT) with body connected to gate.

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that a good agreement is obtained between measured and simulated data, despite a small output conductance difference observed for the DTMOSFET, which could be due to a subtle bias shift.

6. Extraction of parasitic capacitances and resistances of FinFET

The dynamic performance of FinFETs was investigated on 50 nm-long RF n-doped devices with two gate fingers of 5, 15, 25 and 30 μm-width. The fin width and the fin spacing were set to 55 and 100 nm, respectively. It is expected that these devices operate in fully depleted regime for such fin width, which was further confirmed by DC measurements. The *S*-parameters of the RF devices were measured in saturation ($V_d = 1.2$ V) at the maximum transconductance value ($V_g = V_g(G_{m_max})$) up to 110 GHz and the pad parasitics were removed from the raw data with an open subtraction method. In Fig. 12, the measured and modeled current gains are presented. The curve noted Simulation 1 was obtained with a classical equivalent circuit for FET (including a simple RC network to model the transistor input impedance) and Simulation 2 for the model shown in Fig. 13 in which a distributed parasitic network ($R_{ge1}, C_{gs1}, C_{gd1}$ and $R_{ge2}, C_{gs2}, C_{gd2}$) at the transistor input is considered. It can be seen in Fig. 12 that this improved model (circles) can closely reproduce the frequency behavior of the FinFET gain curves over the whole frequency band. The physical origin of this distributed RC at the input of the FinFET is related to the non-optimized gate silicidation (high gate resistance) and higher gate capacitance due to polysilicon residues along the silicon fins [38]. These lines of residual polysilicon are due to an incomplete polysilicon etch in the BOX recess when the polysilicon gate is patterned by resist trimming. These technological problems were solved and cutoff frequencies higher than 100 GHz have been recently measured for 60 nm FinFETs [39].

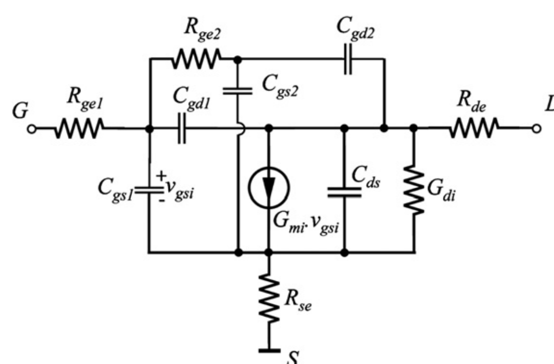

Fig. 13. Small signal equivalent circuits used for modeling the RF FinFET devices.

This example illustrates well the interest of wideband characterization performed at the early stage of a novel device development. Indeed, these technological problems would not have been identified based on DC measurements.

7. Backgate resistance extraction of planar double gate SOI MOSFET

In the clean room facilities of UCL we have built and measured long-channel (20 down to 1 μm) planar double gate (DG) SOI MOSFETs. The fabrication process of these DG devices is based on the transfer of a high quality thin silicon film above a pre-etched cavity in an oxide layer [40]. As shown in Fig. 14 the G_m DC value of the DG device is indeed twice higher than that of the SG device. As expected by the high sheet resistance of the unsilicided top polysilicon gate, a severe drop of G_m occurs above a few GHz. However, we also observe another kink in the G_m curve of the DG transistor at around a few kHz. After

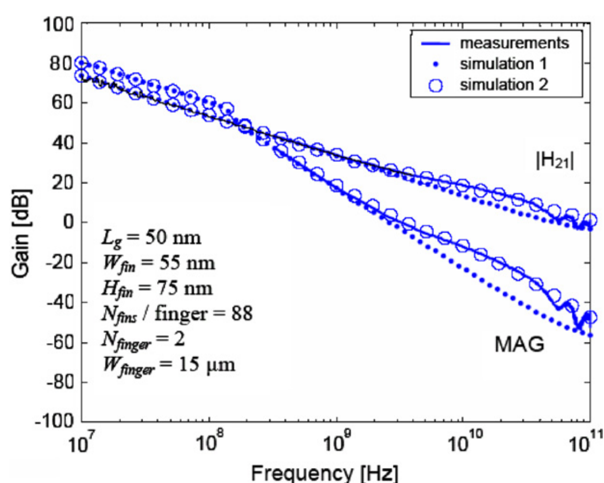

Fig. 12. Measured and simulated $|H_{21}|$ and MAG for a RF FinFET. The models considered were a classical equivalent circuit for FET (Simulation 1, dots) and that of Fig. 13 (Simulation 2, circles).

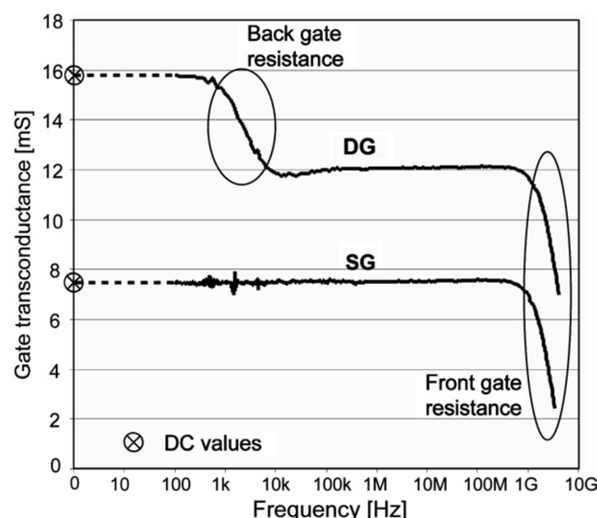

Fig. 14. Gate transconductance G_m of the measured single (SG) and double gate (DG) devices versus frequency.

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the extraction of a complete equivalent circuit over this wide frequency band, it was demonstrated that this G_m drop is related to the higher resistance of the back gate. This dissymmetry between the front and back gate polysilicon resistivity can be explained by the poor doping atoms diffusion into the polysilicon filling the cavity. In situ doping of the polysilicon is then required to avoid this high backgate parasitic resistance.

8. Conclusion

From these examples, it is quite obvious that a wideband electrical characterization has to be considered at the early stage of technology development. The direct extraction of physical parameters such as parasitic capacitances, resistances, relaxation of carriers, body contact, etc., which cannot be extracted under static bias conditions, is of first importance in the improvement cycle of any advanced technology. The results presented here also indicate that as transistors dimensions are continuously shrinking, it is also crucial to develop new measurement and characterization techniques in order to maintain a high accuracy on the extracted parameters of advanced devices.

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