On the Excitability of Ultra-Low-Power CMOS Analog Spiking Neurons

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***Abstract*—The excitability property of spiking neurons describes their capability to output an action potential as a real-time response to an input synaptic excitation current and is central to the event-based neuromorphic computing paradigm. The spiking mechanism is analysed in a representative ultra-low-power analog neuron from the circuit literature. Relying on conventional SPICE simulations compatible with industrial transistor compact models, we establish a excitation criterion, quantified either in terms of critical supplied charge or membrane potential threshold. Only the latter is found intrinsic to the neuron, i.e. independent of the input stimulus. Rigorous analysis of the nonlinear neuron dynamics provides insight but still needs to be explored further, as well as the effect of the intrinsic noise.**

I. Introduction

Within the neuromorphic paradigm, spiking neurons are the fundamental building blocks of spiking neural networks. Neuronal cells are massively replicated and interconnected through synapses to perform computation in real time [1]. A large variety of neuron architectures can be found [2], either in CMOS technology (either analog [1]–[4] or digital [5]), or based on emerging devices such as volatile memristors [6], [7]. There is an obvious tradeoff between the complexity of the architecture (i.e. required number of devices) that translates into higher power consumption, and the biophysical plausibility of the mathematical model of the neuron (which can be quantified by the number of behaviours of biological neurons that can be mimicked [8]). With this regard, the Morris-Lecar model [9], that translates well to subthreshold MOS transistor physics, can be appreciated as a tradeoff between the basic integrate-and-fire [2] and the conductance-based Hodgkin-Huxley [10].

An ultra-low-power CMOS design proposed by [11] is shown in Figure 1(a). Although relatively simple, the architecture has strong similarities (in terms of elementary blocks and operation) with adaptive exponential (leaky) integrate-and-fire neuron circuits [1] as integrated in state-of-the-art neuromorphic processors [12], and will therefore be used as case study. While previous work [13] performed some preliminary analyses of the neuron reliability in presence of process variations, an insightful and quantitative spiking criterion remained to be established. This connects to the notion of *excitability* of neurons [14] that is central to the event-based analog neuromorphic computing paradigm [15]. Papers [16], [17] investigated excitability based on theoretical neuron models only, in a control perspective.

The present work aims instead to rely on conventional SPICE simulations that are not specific to a particular neuron architecture and moreover compatible with advanced industrial transistor compact models. The rest of this paper is structured as follows. The operation of the neuron of Figure 1(a) is extensively described in Section II. Excitability property and spiking criterion are addressed in Section III. Section IV draws the conclusions and opens perspectives for future work.

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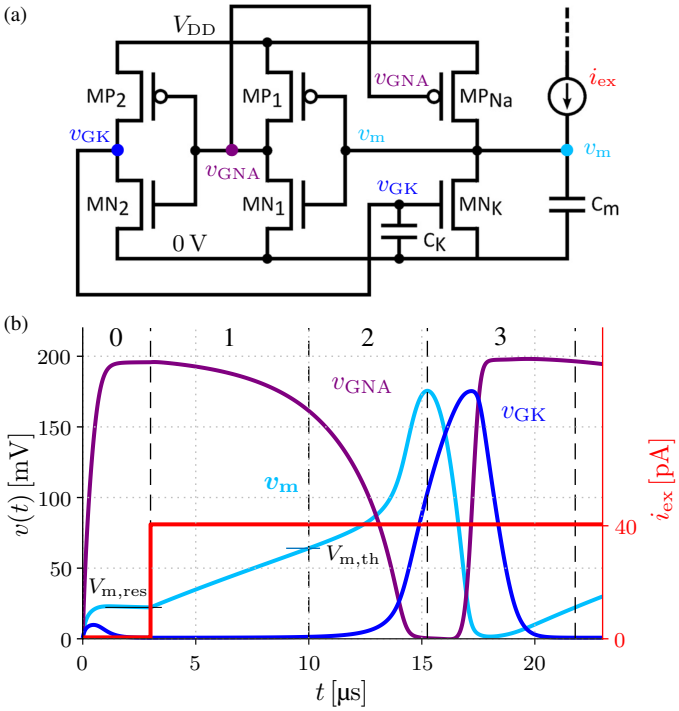

Figure 1. (a) Diagram of a CMOS analog spiking neuron [11].
(b) Waveforms at the different nodes of the circuit labelled in (a) under constant excitation current pulse of amplitude $I_{ex} = 40\,\text{pA}$. Resting membrane potential is $V_{m,res} \approx 22\,\text{mV}$ and threshold potential $V_{m,res} \approx 64\,\text{mV}$.
Case study: 65 nm CMOS technology design of [11], whose parameters are given in Table I and operating at ultra low $V_{DD} = 200\,\text{mV}$ and $T = 300\,\text{K}$.

Table I
Transistor width W and capacitances of the neuron of Figure 1(a). All the transistor lengths are $L = 65\,\text{nm}$ [11].

MP_1	MP_2	MP_{NA}	MN_1	MN_2	MN_K	C_K	C_m
300 nm	360 nm	400 nm	600 nm	120 nm	1.2 µm	8 fF	4 fF

II. Spiking Neuron Operation

The operation of the neuron of Figure 1(a), leading to one action potential, that is one spike on the output v_{GK}, is illustrated in Figure 1(b) following successive phases:

0 We assume cold initial conditions:
$$(v_{\mathrm{m}}(0), v_{\mathrm{GNA}}(0), v_{\mathrm{GK}}(0)) = (0\,\mathrm{V}, 0\,\mathrm{V}, 0\,\mathrm{V}),$$
i.e. no initial residual charge in the circuit of Figure 1(a). During *power-up*, the supply voltage is turned from 0 to V_{DD} and the circuit state naturally evolves towards a stable steady state (equilibrium) [18]. The stabilisation time, of a few µs for the design of Table I, is mostly determined by the inverter dynamics. The membrane potential v_{m} stabilises at its *resting potential* $V_{\mathrm{m,res}}$.

1 Once the input synaptic excitation current i_{ex} is injected and integrated over the membrane capacitance, v_{m} increases quasi linearly, while the evolution of v_{GNA} is dictated by inverter MN_1-MP_1.

2 After v_{m} crosses a certain *threshold* $V_{\mathrm{m,th}}$ (which will be quantitatively defined and extracted further), the decrease in v_{GNA} becomes faster. This makes the pMOS transistor $\mathrm{MP}_{\mathrm{NA}}$ more and more conducting (yet in subthreshold regime for the studied ultra-low V_{DD} design), which results in an exponential increase in v_{m}. This, in turn, further reinforces the decrease in v_{GNA}: the neuron has entered in *strong feedback mode*, similar to SRAM state-transition dynamics [19], [20]. This positive feedback makes all the node voltages vary almost exponentially as can be observed in Figure 1(b). Notably, the quickly decreasing v_{GNA} activates more and more the inverter MN_2-MP_2, which starts to generate an output spike on v_{GK}.

3 The transistor MP_{K} becomes activated by the high v_{GK} and inhibits the membrane potential, that is it lowers v_{m} almost to the ground. If, and only if, the excitation current is sustained, v_{m} starts to rise again and the spiking cycle can resume from phase 1; otherwise the neuron returns to its stable equilibrium (v_{m} at $V_{\mathrm{m,res}}$).

III. Dynamics and Excitability of the Neuron

Strictly speaking, the neuron of Figure 1(a) is a third-order system, whose state trajectory must be described by the triplet $(v_{\mathrm{m}}(t), v_{\mathrm{GNA}}(t), v_{\mathrm{GK}}(t))$ and plotted in a three-dimensional (3D) state space. As pointed out in [16], the description of such nonlinear system dynamics in terms of trajectories is daunting. Therefore, complex neurons are more conveniently characterised in terms of *excitability*, that is an intrinsic input-output property that does not necessarily require the knowledge of the full internal state model [16], [17], [21].

A. Excitation Threshold and Critical Charge

In Figure 2(a), we have assessed the excitability of the neuron of Figure 1(a) through SPICE noiseless transient simulations. Starting from cold initial conditions as described in Section II, we have injected synaptic current pulses (like the one shown in Figure 1(b)) sweeping amplitudes I_{ex} and durations ΔT_{p}. For each case, we observe the output potential v_{GK}: the neuron has been successfully excited if one output spike is recorded

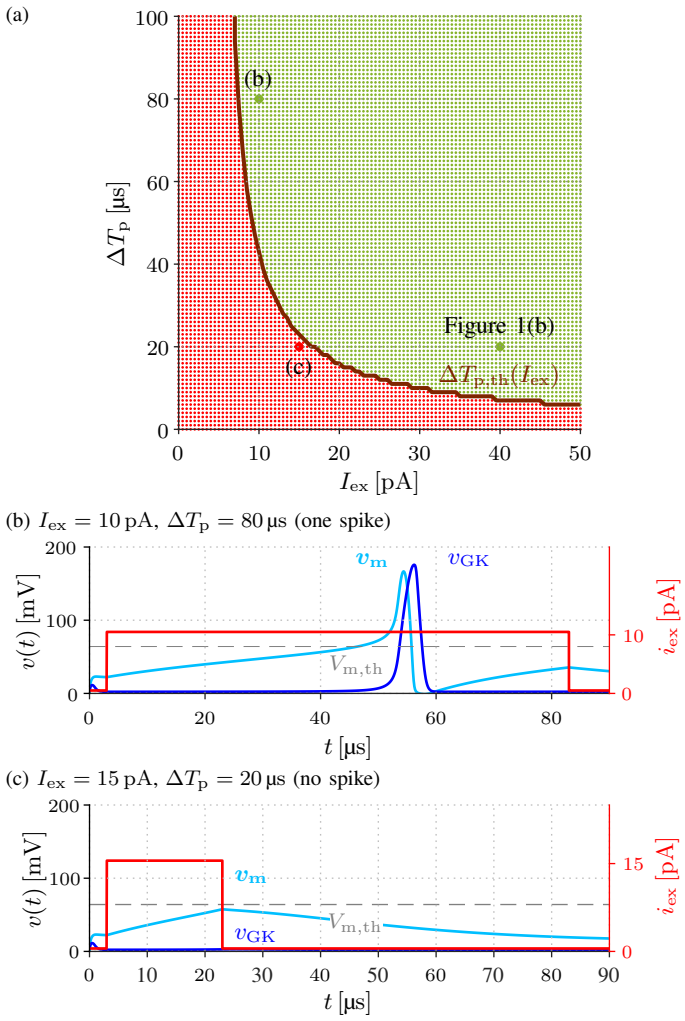

Figure 2. (a) Threshold property of the excitable neuron of Figure 1(a) (plot suggested by [16], [17]), extracted from deterministic SPICE transient simulations with a sweep on excitation current pulse parameters $(I_{\mathrm{ex}}, \Delta T_{\mathrm{p}})$, resp. amplitude and duration. The green region corresponds to input pulses i_{ex} that lead to an action potential, i.e. a spike on output v_{GK}. Low-energy pulses located in the red region fail to active the spiking mechanism of the circuit.

(b) (c) Membrane and action potential waveforms of two illustrative cases marked by dots in (a), in addition to the case shown in Figure 1(b). For the pulse (b), the membrane potential crosses the threshold $V_{\mathrm{m,th}}$ and the neuron fires a spike. The pulse (c) does not supply a sufficient amount of energy.

(green region in Figure 2(a)). Examples are Figure 1(b) and Figure 2(b): a small-amplitude pulse triggers a spike if it is sustained for a sufficient duration. Similar criterion was established for a state transition to occur in SRAM bitcells subject to deterministic pulse disturbances [19] or random telegraph noise [22]. Figure 2(c) shows one instance of pulse that is too low and short to trigger the spiking mechanism, thereby located in the red region of Figure 2(a). In all, observation suggests to determine a threshold criterion that would take into account both the amplitude *and* the duration of the injected pulse.

For a given amplitude I_{ex} of the excitation current pulse, the threshold boundary (in brown line in Figure 2(a)) provides the minimum duration of the pulse, denoted $\Delta T_{\mathrm{p,th}}(I_{\mathrm{ex}})$, needed to generate a spike on v_{GK}. Conversely, a given ΔT_{p} imposes a minimum I_{ex}. It can be noticed that the integral of $i_{\mathrm{ex}}(t)$,

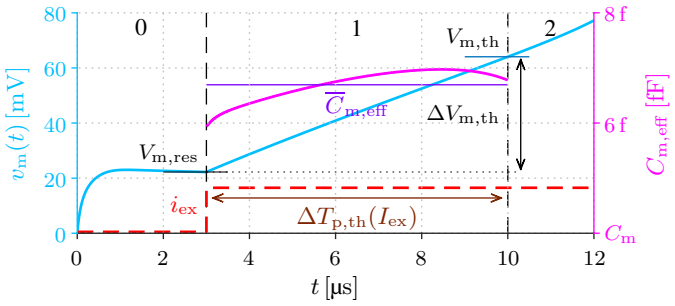

Figure 3. Definition of the threshold potential $V_{\mathrm{m,th}}$ as the value reached by v_{m} when excited by a current pulse of duration $\Delta T_{\mathrm{p,th}}(I_{\mathrm{ex}})$ provided by Figure 2(a) for some given amplitude I_{ex}. While $I_{\mathrm{ex}} = 40\,\mathrm{pA}$ was arbitrarily chosen for illustration (as in Figure 1(b)), the threshold $V_{\mathrm{m,th}}$ is an intrinsic property of the neuron and does not depend on I_{ex}. The extraction of the nonlinear effective total membrane capacitance $C_{\mathrm{m,eff}}$ according to the definition (3) is also shown; $\overline{C}_{\mathrm{m,eff}}$ denotes the averaged effective capacitance over the phase 1 during which v_{m} rises from $V_{\mathrm{m,res}}$ to $V_{\mathrm{m,th}}$.

i.e. the product of I_{ex} and ΔT_{p} yields a *critical charge*, i.e. the minimum amount of charge that must be supplied to excite the neuron [16]:

$$\Delta Q_{\mathrm{th}}(I_{\mathrm{ex}}) = \int_{t_0}^{t_0+\Delta T_{\mathrm{p,th}}} i_{\mathrm{ex}}(t)\ \mathrm{d}t = I_{\mathrm{ex}} \cdot \Delta T_{\mathrm{p,th}}. \quad (1)$$

This allows to extend the analysis to other types of synaptic current than a rectangular pulse, like a spike train as will be exemplified in Section III-C.

However, our numerical investigation reveals that the critical charge varies with I_{ex} and hence is not a unique quantity, which the notation $\Delta Q_{\mathrm{th}}(I_{\mathrm{ex}})$ in (1) reflects. The excitation boundary in Figure 2(a) is indeed not an isoenergetic curve [17]. Since the critical charge can depend on the input stimulus, it is not an intrinsic property of the neuron. This non-trivial dependency comes from the nonlinear dynamics of the neuron and the complexity of its responses to different stimuli. The difficulty of proposing a simple and general definition of the threshold of excitable systems was recently pointed out by [17].

B. Membrane Potential Threshold as Spiking Criterion

The previous section has highlighted the difficulty of identifying a unique excitability threshold in terms of charge or energy only based on the input-output response of the system (black-box approach). This issue gets solved if internal states of the system are observable and their dynamical evolution can be modelled, as is the case here with the detailed knowledge of the circuit architecture (Figure 1(a)) and the possibility to probe any signal in SPICE.

For all the bordelines cases of Figure 2(a), we have observed that the *spiking criterion* is that the membrane potential exceeds a certain threshold $V_{\mathrm{m,th}}$ that is indicated in Figures 1(b), 2(b) and 2(c). This is nothing but the expected natural behaviour of any integrate-and-fire neuron [1], [2]. Thus, an output spike is fired when the synaptic excitation current supplies a sufficient amount of energy to make v_{m} rise from $V_{\mathrm{m,res}}$ to $V_{\mathrm{m,th}}$ (the phase 1 described in Section II). The potential difference will be denoted $\Delta V_{\mathrm{m,th}} = V_{\mathrm{m,th}} - V_{\mathrm{m,res}}$. All the important quantities are summarised in Figure 3. It would be insightful to relate it to the critical charge (1) in order to unify the criteria.

1) Effective Total Membrane Capacitance: The application of Kirchhoff's current law at node v_{m} (see Figure 1(a)) yields

$$i_{\mathrm{ex}}(t) = C_{\mathrm{m}}\frac{\mathrm{d}v_{\mathrm{m}}(t)}{\mathrm{d}t} - i_{\mathrm{D,Na}}(t) + i_{\mathrm{D,K}}(t) + i_{\mathrm{in,Inv1}}(t). \quad (2)$$

$i_{\mathrm{in,Inv1}}(t)$ is a pure dynamic current in the input gates capacitances of inverter MN_1-MP_1. However, the drain currents of the transistors $\mathrm{MP}_{\mathrm{Na}}$ and MN_{K}, $i_{\mathrm{D,Na}}(t)$ and $i_{\mathrm{D,K}}(t)$, have both quasi-static and dynamic components. The quasi-static components are the leakage currents of the transistors, which are small in phase 1 when v_{GNA} remains close to V_{DD} and V_{GK} is still almost at 0 V (see Figure 1(b)) but never rigorously zero.

We aim to extract an *effective* total membrane capacitance (possibly nonlinear) such that

$$i_{\mathrm{ex}}(t) \equiv C_{\mathrm{m,eff}}(t)\,\frac{\mathrm{d}v_{\mathrm{m}}(t)}{\mathrm{d}t}. \quad (3)$$

The $C_{\mathrm{m,eff}}$ defined by (3) is said effective because it encompasses the implemented C_{m} (seen in Figure 1(a)), the contribution of all intrinsic MOS and parasitic interconnect capacitances connected to the node v_{m}, as well as the effect of leakage currents discussed above. Subsequently, we extract the nonlinear $C_{\mathrm{m,eff}}(t)$ from SPICE transient simulation of the circuit (Figure 3) excited by a constant current pulse $i_{\mathrm{ex}}(t) = I_{\mathrm{ex}}$. The $C_{\mathrm{m,eff}}(t) = I_{\mathrm{ex}}/(\mathrm{d}v_{\mathrm{m}}(t)/\,\mathrm{d}t)$, obtained from (3) in phase 1, is plotted in magenta in Figure 3. The non-constancy of $C_{\mathrm{m,eff}}(t)$ reflects the weak nonlinearity of $v_{\mathrm{m}}(t)$. It should be noticed that reducing the $C_{\mathrm{m,eff}}$ to C_{m} (as given in Table I) only would be a coarse approximation.

Finally, the combination of (1) and (3) consistently relates the critical supplied charge to the membrane potential threshold:

$$\Delta Q_{\mathrm{th}} = \overline{C}_{\mathrm{m,eff}} \cdot \Delta V_{\mathrm{m,th}}, \quad (4)$$

where the averaged effective total membrane capacitance (thin violet line in Figure 3) has been introduced:

$$\overline{C}_{\mathrm{m,eff}}(I_{\mathrm{ex}}) \equiv \frac{1}{\Delta V_{\mathrm{m,th}}}\int_{V_{\mathrm{m,res}}}^{V_{\mathrm{m,th}}} C_{\mathrm{m,eff}}(v_{\mathrm{m}})\ \mathrm{d}v_{\mathrm{m}}. \quad (5)$$

2) Neuron Dynamics in Two-Dimensional State Subspace: We conclude this section by explaining the found empirical value of the membrane potential threshold $V_{\mathrm{m,th}}$ with an analysis of the neuron dynamics. Figure 4 shows the two-dimensional (2D) state subspace of the neuron, where only the state variables $(v_{\mathrm{m}}, v_{\mathrm{GNA}})$ are considered. This 2D subspace can be regarded as a projection of the full 3D state space, meaning that the dynamics are approximated. The state trajectory $(v_{\mathrm{m}}(t), v_{\mathrm{GNA}}(t))$ corresponding to the simulation of Figure 1(b) is depicted, along with the different phases annotated. One can see the *limit cycle*, i.e. the closed and periodic orbit followed when the neuron operates in always-spiking or oscillating configuration (when a sufficient large constant I_{ex} or a continuous spike train is applied as synaptic current in Figure 1(a) as will be shown in Section III-C).

The quasi-static voltage transfer characteristics (VTCs) $V_{\mathrm{GNA}} = f_1(V_{\mathrm{m}})$ and $V_{\mathrm{m}} = f_{\mathrm{NA}}(V_{\mathrm{GNA}})$, obtained by sweeping a DC voltage source introduced on purpose and applied at a node (resp. v_{m} and v_{GNA}) of Figure 1(a) are also shown (in brown) in Figure 4. Akin to the butterfly plot for CMOS SRAM

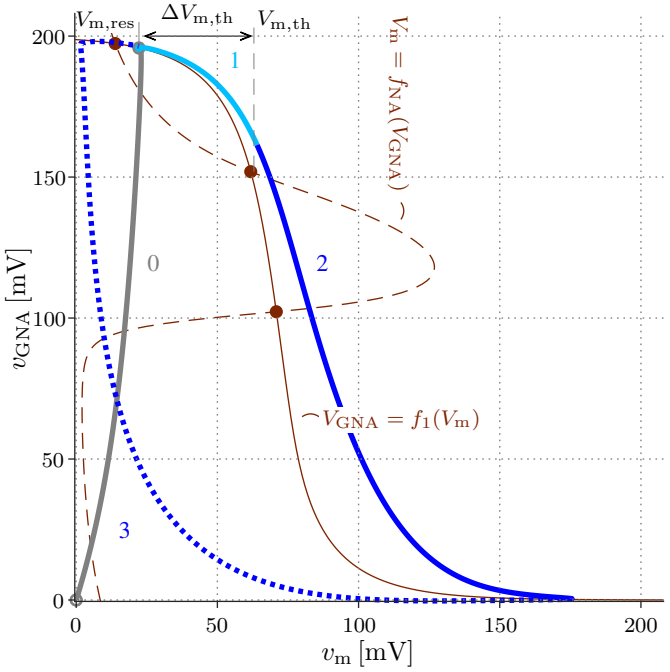

Figure 4. Trajectory in the 2D state subspace $(v_{\mathrm{m}}, v_{\mathrm{GNA}})$, corresponding to the simulated waveforms and operation phases of Figure 1(b). Membrane potential $V_{\mathrm{m,res}}$ and the threshold potential $V_{\mathrm{m,res}}$ are indicated. The quasi-static voltage transfer characteristics $V_{\mathrm{GNA}} = f_1(V_{\mathrm{m}})$ (inverter $\mathrm{MN_1}$-$\mathrm{MP_1}$) and $V_{\mathrm{m}} = f_{\mathrm{NA}}(V_{\mathrm{GNA}})$ (transistor $\mathrm{MP_{Na}}$ with a feedback effect of the whole circuit) are shown in brown lines, resp. full and dashed.

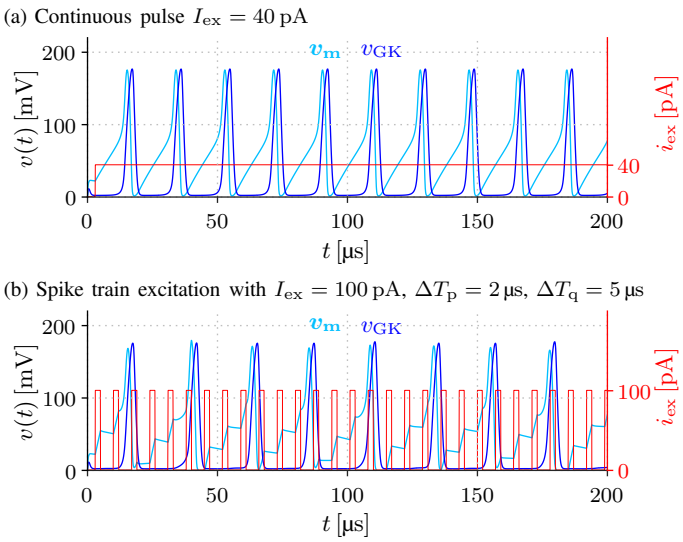

Figure 5. Action potential train (output spike train) sustained by (a) a constant synaptic excitation current pulse; (b) a synaptic current spike train.
Illustrated case: same neuron design as Figure 1 and Table I.

bitcells [20], the intersections of these curves determine the steady states (stable *or* unstable) of the circuit. The top-left brown point is found to underestimate $V_{\mathrm{m,res}}$ (from which the trajectory evolves in the beginning of phase 1, in sky blue): the error could result from the current sunk by the DC voltage source (which alters the original circuit behaviour) and the projection from 3D to 2D. The middle intersection of the VTCs is an *unstable* steady state whose x-location closely confirms the $V_{\mathrm{m,th}}$ found earlier from SPICE transient simulations. While deeper and more quantitative analyses of the neuron dynamics [23] are left for future work, we can hypothesise that this threshold point lies on a *separatrix* [20]. Triggering a spike requires to excite the neuron so that its state $(v_{\mathrm{m}}(t), v_{\mathrm{GNA}}(t))$ crosses the separatrix to escape from the attraction of the resting state, which quantitatively explains the role of $V_{\mathrm{m,th}}$.

C. Always-Spiking Configuration

So far, we have focused on the mechanism for generating a single action potential under a constant synaptic excitation current. The critical supplied charge or the membrane potential threshold were established as spiking criterion.

As can be seen in Figure 5(a), sustaining the synaptic current pulse yields an *action potential train*, i.e. an output spike train on v_{GK}. The output spike frequency obviously increases with I_{ex}, however nonlinearly as shown in previous works [11], [13].

Figure 5(b) depicts the waveforms when the neuron is excited by an *input synaptic current spike train*, which emulates a more biologically plausible stimulus [24] moreover relevant for event-based neuromorphic computing systems [15]. Each individual spike is *integrated* on the membrane capacitance, thereby supplying a certain amount of charge and gradually increases v_{m}. During the *refractory period* [2], that is the quiescient period ΔT_{q} between two input spikes, v_{m} can be observed to decrease: this is the manifestation of the *leaky* property of the neuron of Figure 1(a) physically implemented by the transistor $\mathrm{MN_K}$. Only when a sufficient number of input spikes have been injected, so that the critical charge has been reached and v_{m} has exceeded $V_{\mathrm{m,th}}$, an action potential is *fired* by the circuit. If the input spike train is periodically sustained, one again obtains an action potential train, that is a periodic output spike train whose frequency is directly affected by the magnitude and timing parameters of the input spike train.

IV. Conclusions and Perspectives

Spiking neurons are nonlinear circuits that are the fundamental building blocks of spiking neural networks. Ultra-low-voltage CMOS designs can be found in the literature. We have focused this work on the study of the excitability property of the neuron, illustrated on an architecture implementing a simplified Morris-Lecar neuronal model. Relying on conventional SPICE transient simulations allowing for a fully data-driven approach, we have explored and established the spiking criterion. While the critical charge does depend on the excitation current amplitude and hence cannot be considered as an intrinsic property of the neuron, the criterion that the membrane potential must exceed a certain threshold (intrinsic to a given neuron design) was shown to be universal. The knowledge of the effective nonlinear membrane capacitance allows to relate charge and potential thresholds according to (4). When a biologically-realistic input synaptic current spike train is supplied, the studied neuron exhibits a typical leaky integrate-and-fire behaviour whose output is an action potential spike train. Drawing on our experience in SRAM dynamics modelling, the study of the interplay between analog neuron excitability and noise will be part of future work, notably assessing the propagation of spike jitter.

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REFERENCES

[1] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, "Neuromorphic electronic circuits for building autonomous cognitive systems," *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1388, 2014.

[2] G. Indiveri, B. Linares-Barranco, T. J. Hamilton, A. v. Schaik, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Dudek, P. Häfliger, S. Renaud *et al.*, "Neuromorphic silicon neuron circuits," *Frontiers in neuroscience*, vol. 5, p. 73, 2011.

[3] D. Querlioz and V. Trauchessec, "Stochastic resonance in an analog current-mode neuromorphic circuit," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2013, pp. 1596–1599.

[4] F. Danneville, I. Sourikopoulos, S. Hedayat, C. Loyez, V. Hoël, and A. Cappy, "Ultra Low Power Analog Design and Technology for Artificial Neurons," in *2017 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*. IEEE, 2017, pp. 1–8.

[5] C. Frenkel, M. Lefebvre, J.-D. Legat, and D. Bol, "A 0.086-mm2 12.7-pJ/SOP 64k-Synapse 256-Neuron Online-Learning Digital Spiking Neuromorphic Processor in 28-nm CMOS," *IEEE Transactions on Biomedical Vircuits and Systems*, vol. 13, no. 1, pp. 145–158, 2018.

[6] R. Carboni and D. Ielmini, "Stochastic memory devices for security and computing," *Advanced Electronic Materials*, vol. 5, no. 9, p. 1900198, 2019.

[7] A. Ascoli, A. S. Demirkol, I. Messaris, V. Ntinas, D. Prousalis, S. Slesazeck, T. Mikolajick, F. Corinto, M. Bonnin, M. Gilli *et al.*, "Edge of chaos theory unveils the first and simplest ever reported hodgkin–huxley neuristor," *Advanced Electronic Materials*, vol. 11, no. 8, p. 2400789, 2025.

[8] E. Izhikevich, "Which Model to Use for Cortical Spiking Neurons?" *IEEE Transactions on Neural Networks*, vol. 15, no. 5, pp. 1063–1070, sep 2004, DOI: https://doi.org/10.1109/TNN.2004.832719.

[9] C. Morris and H. Lecar, "Voltage oscillations in the barnacle giant muscle fiber," *Biophysical journal*, vol. 35, no. 1, pp. 193–213, 1981.

[10] A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *The Journal of physiology*, vol. 117, no. 4, p. 500, 1952.

[11] I. Sourikopoulos, S. Hedayat, C. Loyez, F. Danneville, V. Hoel, E. Mercier, and A. Cappy, "A 4-fj/spike artificial neuron in 65 nm cmos technology," *Frontiers in neuroscience*, vol. 11, p. 123, 2017.

[12] H. Greatorex, O. Richter, M. Mastella, M. Cotteret, P. Klein, M. Fabre, A. Rubino, W. Soares Girão, J. Chen, M. Ziegler *et al.*, "A neuromorphic processor with on-chip learning for beyond-cmos device integration," *Nature communications*, vol. 16, no. 1, p. 6424, 2025.

[13] G. Brandsteert, L. Van Brandt, and D. Flandre, "Reliability Analyses of Ultra-Low Voltage Analog Spiking Neurons," in *2025 32nd International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*. IEEE, 2025, pp. 156–160.

[14] E. M. Izhikevich, "Neural excitability, spiking and bursting," *International journal of bifurcation and chaos*, vol. 10, no. 06, pp. 1171–1266, 2000.

[15] S.-C. Liu, T. Delbruck, G. Indiveri, A. Whatley, and R. Douglas, *Event-based neuromorphic systems*. John Wiley & Sons, 2014.

[16] R. Sepulchre, G. Drion, and A. Franci, "Excitable behaviors," in *Emerging Applications of Control and Systems Theory: A Festschrift in Honor of Mathukumalli Vidyasagar*. Springer, 2018, pp. 269–280.

[17] R. Sepulchre and G. Tong, "On the threshold of excitable systems: An energy-based perspective," *arXiv preprint arXiv:2504.02171*, 2025.

[18] E. I. Vatajelu, G. Di Natale, and P. Prinetto, "Towards a highly reliable sram-based pufs," in *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2016, pp. 273–276.

[19] B. Zhang, A. Arapostathis, S. Nassif, and M. Orshansky, "Analytical Modeling of SRAM Dynamic Stability," in *Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design*, 2006, pp. 315–322.

[20] L. Van Brandt, M. Bonnin, M. B. da Silva, P. Bolcato, G. I. Wirth, D. Flandre, and J.-C. Delvenne, "Modeling and Predicting Noise-Induced Failure Rates in Ultra-Low-Voltage SRAM Bitcells Affected by Process Variations," *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2025.

[21] R. Sepulchre, "Spiking control systems," *Proceedings of the IEEE*, vol. 110, no. 5, pp. 577–589, 2022.

[22] L. Van Brandt, F. Silveira, J.-C. Delvenne, and D. Flandre, "On Noise-Induced Transient Bit Flips in Subthreshold SRAM," *Solid-State Electronics*, vol. 208, p. 108715, 2023.

[23] E. M. Izhikevich, *Dynamical Systems in Neuroscience*. MIT press, 2007.

[24] C. Koch, *Biophysics of computation: information processing in single neurons*. Oxford university press, 2004.