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Symmetrical Ambipolar Transport in SnO Thin-Film Transistors Enabled by Dopant-Induced Preferential Crystal Orientation toward Complementary Logic

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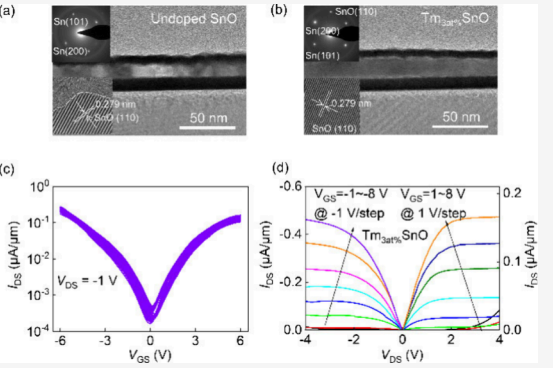
ABSTRACT: Herein, we present a thulium (Tm) doping strategy combined with hafnium oxide passivation annealing to enhance the preferable orientation crystallinity in SnO films toward balanced hole and electron transport. The optimized ambipolar Tm-doped SnO thin-film transistors (TFTs) exhibit hole and electron mobilities of 30.1 $cm^2/V{\cdot}s$ and 11.8 $cm^2/V{\cdot}s$ with a turn-on voltage about 0 V, respectively. Furthermore, we fabricate complementary thin-film logic circuits using these ambipolar SnO TFTs, including inverters and NAND and NOR gates. A record gain of 474.5 (V/V) is obtained for our ambipolar SnO inverter at a supply voltage of 6 V, which is the highest value reported among all ambipolar material systems due to the matched p- and n-type behaviors of the ambipolar SnO TFTs. By expanding the understanding of ambipolar inverter behavior, this work highlights the significant potential of ambipolar SnO TFTs for future high-performance complementary thin-film circuits.



KEYWORDS: *complementary logics, preferred orientation, Tm doping, ambipolar SnO*

Ambipolar thin-film transistors (TFTs), integrating p- and n-type electrical performance into monolithic chip integration, are particularly advantageous for functional applications like complementary thin-film logic circuits, as they reduce the number of device components while facilitating miniaturization and streamlining the manufacturing process.[1,2] Tin monoxide (SnO) is one of the few metal oxide semiconductors demonstrating intrinsic ambipolar behavior, enabling both electron and hole conduction as the channel of ambipolar TFTs, thanks to the combined influence of Sn 5p orbitals contributing to the conduction band minimum (CBM) and the strong hybridization between spherically distributed 5s orbitals and the O 2p orbital contributing to the valence band maximum (VBM).[3−9] Simultaneously, SnO combines the low thermal budget of oxide semiconductors with excellent back-end-of-line process compatibility, positioning it as a compelling candidate for complementary thin-film logic circuits in monolithic integration.[10] However, due to the thermodynamic metastability of SnO, nonequilibrium valence states, such as Sn^{4+} and metallic Sn, act as detrimental defect states that significantly degrade the microstructural and electrical properties of SnO thin films.[11] Consequently, most SnO TFTs exhibit predominantly p-type transport behavior, with severely unbalanced carrier conduction.

As noted in the previous research, atomic layer deposition (ALD) encapsulation combined with postpassivation annealing has been used for enabling n-type conduction and ambipolar TFT behavior of SnO.[3,6,12] Nevertheless, realizing balanced electron and hole mobilities necessary to achieve low-power-consumption and high-gain inverters remains a persistent challenge. In our previous work, ambipolar SnO TFTs were fabricated using Al_2O_3/HfO_2 as the passivation layer.[13] Incorporating copper (Cu) as interstitial particle yielded a high electron mobility of 43.8 $cm^2/V{\cdot}s$, while the hole mobility is orders of magnitude lower.[14] Critically, achieving high crystallinity in SnO films is paramount to optimal TFT performance. Enhanced crystallinity reduces grain-boundary scattering and suppresses defect states (e.g., Sn vacancies (V_{Sn}) and oxygen vacancies (V_O)), directly improving carrier mobility and subthreshold swing (SS).[1] Previous studies on p-type SnO TFTs have demonstrated that enhancing the

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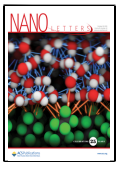

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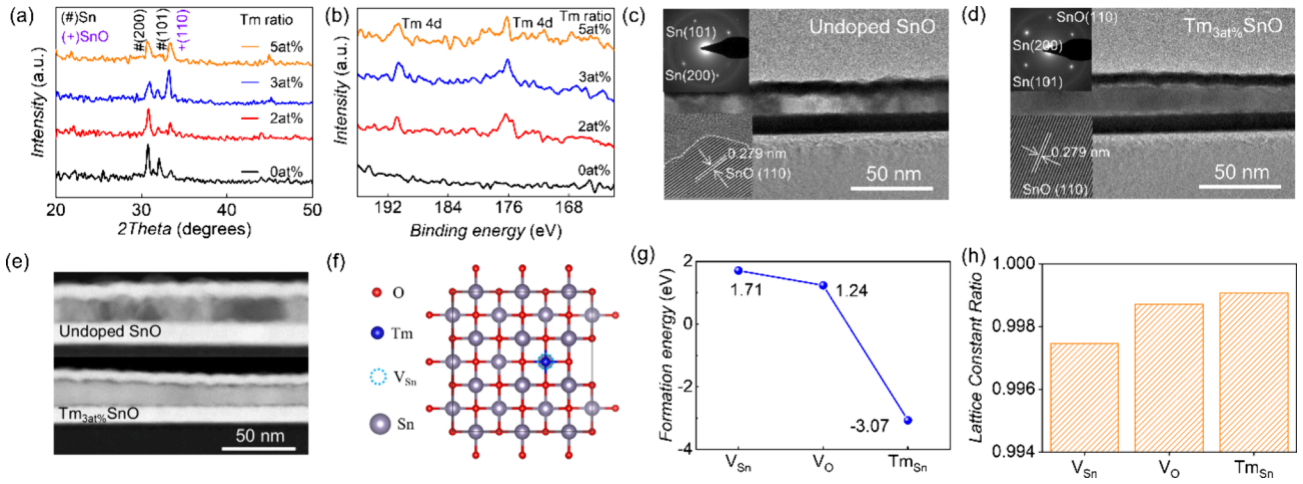

Figure 1. Microstructure analysis and DFT computations. (a) GIXRD spectra of SnO thin films with different Tm contents. (b) XPS spectra of Tm 4d. Bright field TEM images of SnO thin film (c) without Tm and (d) with 3 atom % Tm; the inset images are the SAED pattern (top left) and HR-TEM image (bottom left). (e) HAADF images of SnO thin film without (top) and with 3 atom % (bottom) Tm. (f) DFT lattice structure where Tm replaces the V_{Sn} in SnO. (g) DFT-calculated formation energy and (h) lattice constant ratio of V_{Sn}, V_O, and Tm_{Sn} under Sn-rich conditions.

crystallinity of SnO films, through ALD growth, in situ aluminum oxide capping layer, and substrate interface modification, improves device performance.[3,6,12,15,16] Innovatively, the thulium (Tm) doping strategy is represented to enhance the (110) plane crystal in the p-type SnO channel. By enabling the formation of Tm-interstitial oxygen (Tm-O_i) complexes, this approach not only overcomes the long-standing ionization barrier of O_i to boost hole concentration substantially but also uses the induced O_i to reduce excessive high-order Sn^{4+} and drive preferential crystallization along the SnO (110) plane—an orientation with optimized Sn 5s/O 2p orbital overlap that minimizes grain boundary scattering.[17] However, the strategies remain unexplored for ambipolar SnO devices.

In this work, a novel effect combining HfO_2 encapsulation with Tm doping is proposed to enhance the preferential orientation of SnO films and yield high-performance ambipolar SnO TFTs with symmetrical electrical properties. The mechanism of Tm doping in ambipolar SnO TFTs with HfO_2 passivation annealing is further investigated. Tm^{3+} ions acting as substitutional dopants can passivate V_{Sn}, thereby promoting preferential growth of grains in SnO films and reducing charge-trapping defects such as grain boundaries. Corresponding SnO TFTs with 3 atom % Tm-doped concentration exhibit a high hole field-effect mobility ($\mu_{h,FE}$) of 30.1 $cm^2/V{\cdot}s$, which is 10 times higher than that of undoped devices, while a symmetrical electron mobility ($\mu_{e,FE}$) of 11.8 $cm^2/V{\cdot}s$ is obtained with a high on/off ratio above 10^3. Notably, the complementary logic circuits including inverter and NAND and NOR gates are successfully fabricated by utilizing the ambipolar Tm-doped SnO TFTs, in which the inverter demonstrates an impressive voltage gain of 474.5.

In order to achieve ambipolar transport, the SnO thin films (~20 nm thickness) with different Tm compositions are deposited from different TmSn targets using magnetron sputtering onto atomic-layer-deposited HfO_2 (20 nm thickness) dielectric; then another HfO_2 layer (10 nm thickness) is prepared as encapsulation, followed annealing at 230 °C for 1 h. A series of film analyses was performed to clarify the effects of Tm doping on the SnO films annealed after ALD HfO_2 encapsulation. Based on grazing-incidence X-ray diffraction (GIXRD), the undoped SnO film shows an evident polycrystalline characteristic and simultaneous presence of metal Sn and SnO. After Tm is incorporated, while the phase of metal Sn is obviously reduced, the phase of SnO is increased (Figure 1a). Tm-doped SnO (Tm:SnO) films present prominent diffraction peaks at the SnO (110) plane, which becomes the predominant one and suggests a preferential crystal orientation.[18] As shown in Figure 1b, XPS is employed to analyze the composition of SnO films, in which peak values of Tm 4d spectra are obtained with binding energies of 176.3 and 190.8 eV. The Sn 3d spectra of SnO and Tm:SnO films are displayed in Figure S1, with each spectrum deconvoluted into two separate subpeaks that correspond to the chemical states of Sn^0 (metal Sn) and Sn^{2+}, respectively. Figure S2 provides a summary of the atomic percentages of the two Sn phases in the SnO thin film. It is worth highlighting that the metal Sn content in the SnO film is significantly reduced with the increase of Tm-doped concentration to 3 atom %. Thus, doping with Tm contributes to preserving a sufficient amount of the SnO phase while inhibiting the formation of excess Sn phases. This is significant because the VBM state is affected by the overlap of the Sn−Sn orbitals.

We then sought to understand the microstructural changes after Tm doping by using high-resolution transmission electron microscopy (HR-TEM) and selective area electron diffraction (SAED). The analysis confirmed that both SnO and Tm:SnO films have indeed crystallized in the SnO polymorph, featuring an atomic spacing of 0.279 nm in the HR-TEM image that corresponds to the (110) plane of SnO. Notably, the cross-sectional HR-TEM images in Figure 1c and Figure 1d reveal an obvious change between the crystal size, exhibiting long-range order of Tm-doped SnO. A more intuitive comparison of crystalline states could be observed in Figure S3, in which the crystallization direction changes from being disordered in undoped films (Figure S3a) to being long-range ordered in doped films (Figure S3b). Figure 1e demonstrates the high-angle annular dark-field (HAADF) image of SnO films without and with Tm, also confirming that the Tm-doped SnO films are highly crystalline.

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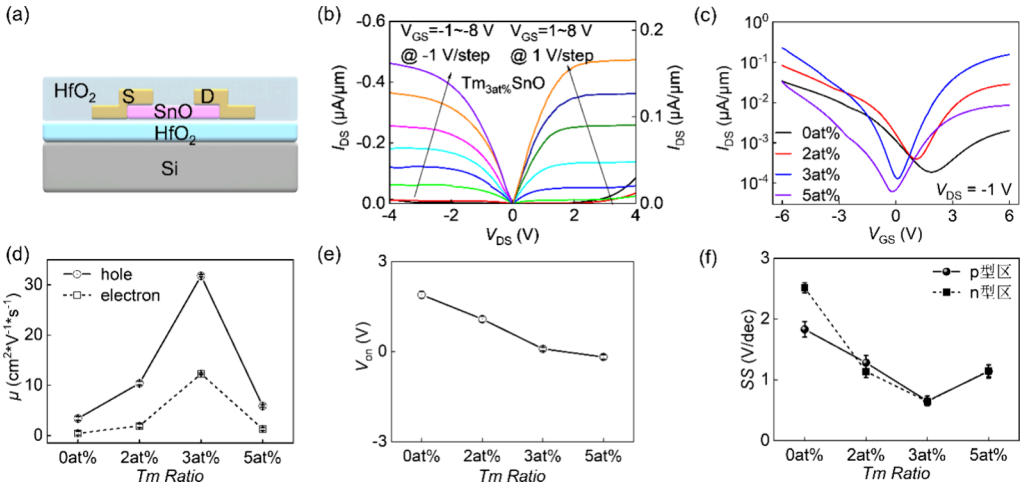

Figure 2. TFT electrical properties. (a) Structural schematic of the SnO TFT realized in this work. (b) I_{DS}−V_{DS} of the $Tm_{3at\%}SnO$ TFT. (c) I_{DS}−V_{GS} of the SnO TFTs with diverse Tm content. (d) μ_{FE}, (e) V_{on}, and (f) SS of TFTs based on channels fabricated with different Tm ratios.

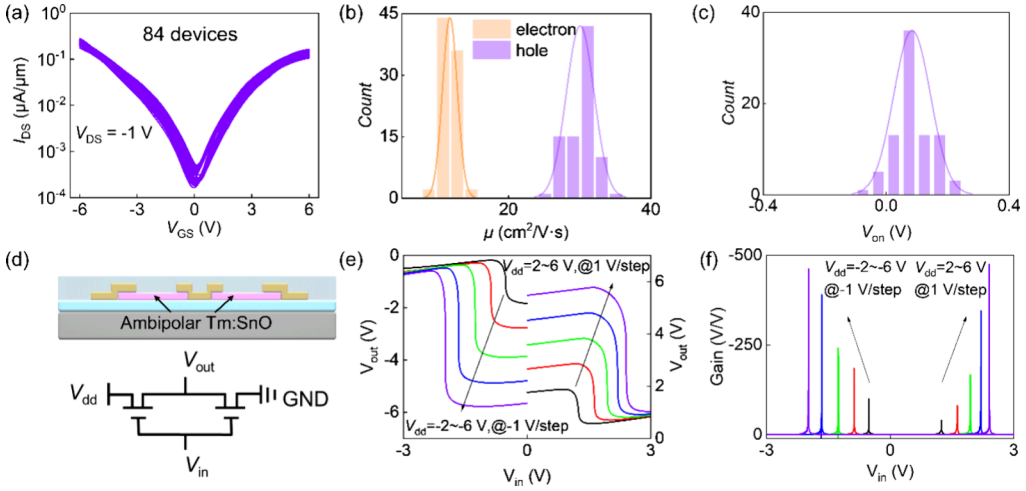

Figure 3. Electrical statistics and complementary inverter. (a) I_{DS}−V_{GS} curves of 84 individual $Tm_{3at\%}SnO$ TFTs fabricated from 10 different batches. (b) μ_{FE} and (c) V_{on} statistics. (d) Schematic and equivalent circuit of complementary inverter configured with ambipolar Tm:SnO TFTs. (e) VTC curves of the inverter under different V_{dd}. (f) Voltage gain of the inverter.

According to our calculations, Tm^{3+} ions fill V_{Sn} and suppress V_O formation. The formula reveals the defect formation energy H_f^{defet}:[19,20]

$$H_f^{defet} = E_{total}^{defet} - E_{total}^{pristine} - \sum_i \Delta n_i (E_i + \mu_i) \quad (1)$$

in which E_{total}^{defet} and $E_{total}^{pristine}$ stand for the total energy of the defective bulk and the pristine bulk, respectively. Δn_i refers to the change in the amount of element i. When atoms of i are added (removed), Δn_i takes a positive (negative) value. E_i donates the ground-state elemental-phase energy, and μ_i is the chemical potential of element i. Under Sn-rich conditions, μ_{Sn} = 0 eV and $\mu_O = \mu_{SnO} - \mu_{Sn}$. We define μ_{Tm} as 0 eV for the Tm impurities.

Figures 1f and S4 sketch the atomic structure of Tm_{Sn}, in which Tm^{3+} ions fill V_{Sn} and suppress V_O formation. The process not only induces vacancy repair but also results in oxygen stabilization. Tm^{3+} (ionic radius ≈ 0.0869 nm) substitutes Sn^{2+} sites (radius ≈ 0.093 nm). Its higher valence Tm^{3+} reduces the V_{Sn} concentration through compensation, minimizing lattice distortion. Additionally, the positive charge of Tm^{3+} suppresses oxygen escape through Coulombic interaction with O^{2-} ions, decreasing V_O. As shown in Figure 1g, the calculated formation energy of Tm_{Sn} is −3.07 eV, which is lower than that of the V_{Sn} complex (+1.71 eV) and in contrast to the single V_O (+1.24 eV). This suggests that the Tm_{Sn} is more favorable than the V_{Sn} and V_O complex during competitive formation of Tm-containing impurities. Figure 1h shows the lattice constant ratio of V_{Sn}, V_O, and Tm_{Sn}, exhibiting reduced lattice distortion with Tm doping.

Figure 2a exhibits the structural schematic of a bottom-gate top-contact TFT, with Cr/Au acting as the source and drain electrode. The preparation details are given in the Methods. The output curves (I_{DS}−V_{DS}) of $Tm_{3at\%}SnO$ TFT show current linearity at low V_{DS}, indicating Ohmic contact between the SnO channel and Cr/Au electrodes (Figure 2b). Typical transfer curves (I_{DS}−V_{GS}) of SnO TFTs with different doping ratios are shown in Figure 2c with low gate leakage current (Figure S5, Supporting Information). It is noteworthy that the device achieved a significant ambipolar transistor characteristic with the desired enhancement operation mode (i.e., turn-on voltage, V_{on} ≈ 0 V for 3% and 5% doping). In addition, a minor hysteresis is observed for the $Tm_{3at\%}SnO$ TFT (Figure S6, Supporting Information), indicating low interface trap states at

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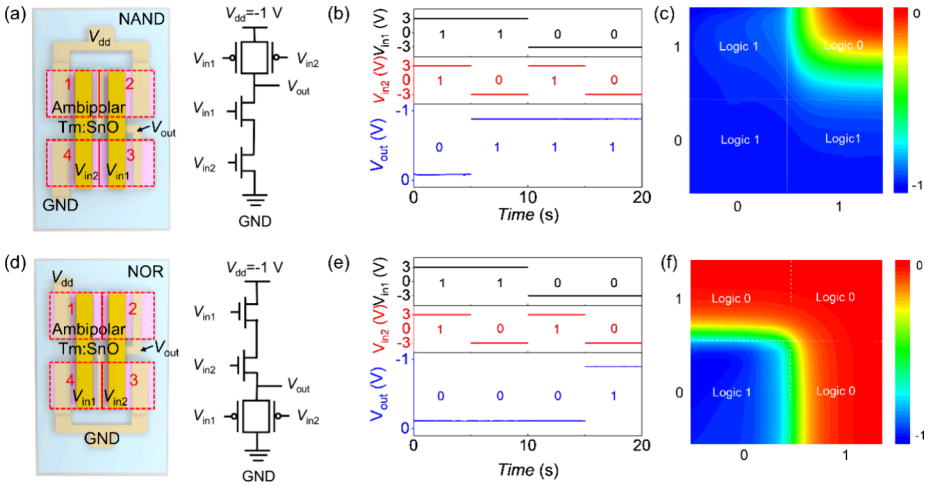

Figure 4. Complementary NAND and NOR logics. (a) Schematic and equivalent circuits for complementary NAND. (b) Output voltage of the logic NAND gate at typical input states with a power supply of $V_{dd} = -1$ V. (c) Operation of NAND gates with different V_{in1} and V_{in2} values. (d) Schematic and equivalent circuits for complementary NOR. (e) Output voltage of the logic NOR gate at typical input states with a power supply of $V_{dd} = -1$ V. (f) Operation of NOR gates with different V_{in1} and V_{in2} values.

the channel/dielectric interface, which is crucial for stable transistor operation in applications like CMOS logic.

The $I_{DS}-V_{GS}$ curves allow quantitative extraction of field-effect mobility (μ_{FE}) and SS to evaluate the performance of TFTs. Here, the μ_{FE} is given by[21,22]

$$\mu_{FE} = \frac{LG_m}{WV_{DS}C_{ox}} \tag{2}$$

$$SS = \frac{dV_{GS}}{d \log I_{DS}} \tag{3}$$

where L (200 μm) and W (100 μm) are channel length and width, respectively; G_m is the maximum transconductance, calculated by dI_{DS}/dV_{GS}; and C_{ox} is the oxide capacitance per unit area, i.e., 4.43 μF/cm^2 for a 20 nm thick HfO_2 dielectric layer. The improved $\mu_{e,FE}$ at Tm doping of SnO TFTs can be attributed to the enhanced long-range ordering of the microstructures. Among these, the postannealing at 230 °C for 1 h yielded a well-balanced ambipolar $Tm_{3at\%}SnO$ TFT performance, including a high $\mu_{h,FE}$ of 30.1 cm^2/V·s and $\mu_{e,FE}$ of 11.8 cm^2/V·s (Figure 2d), $V_{on} \approx 0$ V (Figure 2e), and reduced SS (Figure 2f). Increasing the Tm content in the SnO films from 0 atom % to 3 atom % significantly enhances both electron and hole mobilities and reduces the SS in the TFTs. This enhancement is primarily attributed to Tm incorporation occupying the Sn sites and passivating V_{Sn}. Furthermore, the high oxygen binding energy of Tm suppresses V_O formation. Consequently, defect autocomparison and carrier scattering in the SnO TFTs are effectively reduced. Conversely, when the Tm content reaches 5 atom %, device performance degrades significantly. This degradation is attributed to lattice distortion within the SnO film induced by the incorporation of an excessive number of Tm atoms.

The TFTs are also highly reproducible (Figure 3a), and an average $\mu_{h,FE}$ of 30.1 ± 1.9 and $\mu_{e,FE}$ of 11.8 ± 1.0 cm^2/V·s are obtained from 84 devices in 10 different batches (Figure 3b) with an average V_{on} of 0.1 ± 0.1 V (Figure 3c). The TFTs exhibit excellent electrical performance compared to other reported SnO TFTs (Table S1 in the Supporting Information). Finally, to demonstrate the compatibility of ambipolar Tm:SnO with complementary digital circuit designs, we integrate inverter and NAND and NOR gates. Figure 3d presents the schematic and electrical circuit of an ambipolar Tm:SnO-based inverter constructed by linking two Tm:SnO TFTs. The two Tm:SnO TFTs share a common bottom Si gate electrode. The input voltage (V_{in}) is applied between this shared gate electrode and the ground terminal. The supply voltage (V_{dd}) connects to the source electrode of one Tm:SnO TFT, which thus acts as the pull-up Tm:SnO TFT. Meanwhile, the ground terminal connects to the source electrode of the other Tm:SnO TFT, forming the pull-down Tm:SnO TFT. The output voltage (V_{out}) is measured at the junction where the drain terminals of the two Tm:SnO TFTs are connected. The voltage-transfer characteristics (VTC) of the inverter (Figure 3e) are distinctly observed in the first (i.e., positive V_{dd} and positive V_{in}, where V_{dd} ranges from 2 to 6 V and V_{in} ranges from 0 to 3 V) and third quadrants (i.e., negative V_{dd} and negative V_{in}, where V_{dd} ranges from −2 V to −6 V and V_{in} ranges from −3 to 0 V). This observation indicates that each Tm:SnO-TFT switches by transitioning between p-channel and n-channel modes, which is a unique characteristic of inverters constructed with ambipolar transistors.[23] The inverter exhibits full-swing characteristics with rapid voltage transitions (Figures 3d–f). A high voltage gain of 474.5 V is achieved at $V_{dd} = 6$ V, which stands as the highest value reported among all ambipolar material systems (see Table S2 in the Supporting Information). Inverter gain is determined not by mobility balance alone but by the coordinated optimization of threshold voltage, SS, leakage current, and defect properties. The Tm-doped ambipolar SnO TFT's capacity to perform exceptionally across all these metrics—while eliminating the integration mismatches inherent to heterogeneous CMOS systems—establishes it as a transformative solution for high-performance, stable, and manufacturable all-oxide logic circuits.

Next, complementary NAND and NOR logics are implemented using ambipolar Tm:SnO TFTs. Specifically, Tm:Sn thin films are deposited on a Si/SiO_2 substrate. Subsequently, the contact electrodes are deposited, followed by encapsulation with a HfO_2 dielectric and a subsequent annealing process. Finally, the gate electrodes are deposited. The schematic and circuit diagram for NAND are shown in Figure 4a. This circuit consists of four identical ambipolar

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Tm:SnO TFTs, grouped into two pairs (defined as 1 and 4 and 2 and 3), where each pair shares a common top gate electrode. Ambipolar Tm:SnO TFTs 1 and 2 are connected in parallel, with their source terminals tied to the supply voltage ($V_{dd} = -1$ V). In contrast, ambipolar Tm:SnO TFTs 3 and 4 are connected in series, with the source terminal of TFT 4 connected to the ground. The output is measured at a common junction.

To demonstrate NAND logic operation, two input voltages (V_{in1} and V_{in2}), serving as logic inputs, are applied to two separate top gate electrodes (Figure 4b). When one or both inputs are at logic "0", the output node voltage rises close to V_{dd}, resulting in a logic "1" output. On the other hand, when both inputs are at logic "1", the output node potential is down to ground, generating a logic "0" output for the circuit. The outputs corresponding to all possible combinations of logic inputs are measured and verified against the truth tables (Figure S7a, Supporting Information) and graphical depiction (Figure 4c), and they match the anticipated response of a two-input NAND gate.

A NOR gate is also constructed using four identical ambipolar Tm:SnO TFTs, with the schematic and circuit diagram illustrated in Figure 4d. In the NOR gate circuit, the TFTs 1 and 2 are connected in series, while the TFTs 3 and 4 are wired in parallel. When one or both inputs are at logic "1", the output node is pulled down to ground, resulting in a logic "0" output. Conversely, only when both inputs are at logic "0" does the output node get pulled up close to V_{dd}, yielding a logic "1" output. The input−output combinations shown in Figure 4e,f and Figure S7b align with the expected behavior of a two-input NOR gate. These results confirm that Tm:SnO-based ambipolar TFTs are viable candidates for developing single-component logic devices.

Interestingly, NAND and NOR gates could be converted into each other by switching the bias voltages ("V_{dd}" and "Ground (GND)") thanks to identical transistors featuring intrinsic semiconducting channels.[24] Ambipolar Tm:SnO TFT circuits exhibit voltage-controlled polymorphism,[25] enabling a range of applications, including circuit self-checking and embedding extra or hidden functions in circuits for tagging and identity verification.[26,27] The inherent ambipolarity of these Tm:SnO TFTs also allows for much simpler circuit designs compared to conventional CMOS-based implementations of polymorphic circuits.[28]

We report high-performance ambipolar SnO TFTs by incorporating a Tm to construct long-range-ordered channel films. Tm doping can enhance the crystal texture and form preferential orientation in the SnO thin film. DFT reveals that Tm^{3+} ions fill V_{Sn} and suppress V_O formation, minimizing lattice distortion. This Tm doping strategy results in a high $\mu_{h,FE}$ of 30.1 $cm^2/V{\cdot}s$ and $\mu_{e,FE}$ of 11.8 $cm^2/V{\cdot}s$ with 3 atom % doping concentration, which is 10 times higher than that of the undoped devices, along with a high on/off ratio above 10^3. Moreover, by utilizing Tm-doped ambipolar SnO TFTs, complementary logic circuits, including inverters and NAND and NOR gates, are successfully fabricated. Notably, the inverter circuit demonstrates an impressive voltage gain of 474.5.

METHODS

Simulation Method. The calculations were carried out using the Vienna Ab-initio Simulation Package,[29] which is based on density functional theory.[30] To characterize the exchange−correlation potential energy, the Perdew−Burke−Ernzerhof functional within the generalized gradient approximation was utilized.[31] The projector augmented wave method was applied to handle core−valence interactions.[32] A cutoff energy of 500 eV was used. The calculations were performed on a 3 × 3 × 2 supercell, with the Brillouin zone sampled using a 4 × 4 × 5 Monkhorst−Pack k-point mesh. Convergence thresholds for energy and force were set to 10^{-5} eV and 0.01 eV $Å^{-1}$, respectively.

Device Fabrication. All devices were fabricated on silicon substrates. The HfO_2 dielectric layer was grown at 100 °C via an ALD system (TALD-150R), using dimethylamine hafnium and H_2O as precursor materials. A 99.99% pure Tm:Sn alloy target (supplied by HZAM) was RF-sputtered with a JSD300 magnetron sputtering system. Deposition occurred at 30 W under room temperature with pressure maintained at 0.88 Pa. During this process, the oxygen partial pressure was held at 2.31% ($P_O = O_2/(O_2 + Ar)$%). Cr/Au electrodes, acting as both contact and interconnect electrodes, were deposited by using a vacuum thermal evaporation system. Annealing was performed in air with OTF-1200X equipment at 230 °C for 1 h after ALD HfO_2 capping.

Electrical Measurement and Characterization. Testing of TFTs, inverters, NAND gates, and NOR gates was conducted at room temperature in ambient air with an Agilent B1500A semiconductor parameter analyzer, supported by the LakeShore TTPX. The films were subjected to XPS analysis using an EscaLab 250Xi instrument. GIXRD patterns of the films—measured at an incident angle of 0.5°—were collected via an X'Pert PROMPD diffractometer. A TEM was used to capture the cross-sectional image [Themis Z (3.2), Thermo Scientific].

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.5c04300.

Sn 3d XPS spectrum for the Tm:SnO films; percent chemical binding state of Sn element; TEM images of SnO thin film; lattice structure where Tm replaces the V_{Sn} in SnO; leakage current of TFTs with different Tm contents; hysteresis characteristic of ambipolar $Tm_{3at\%}$:SnO TFT; truth table; summary of device performance for the reported SnO TFTs; record reported inverter gain based ambipolar materials (PDF)

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Author Contributions

L.L. and P.H.H. conceived and designed the experiments. L.M.T. and H.Z.L. performed the DFT computations. R.H.H. fabricated and characterized the devices. X.X.X., X.Y., Q.L.T., and Y.S. assisted with the experiments related to device fabrication. M.Y.C., Y.R.W., B.X.Z., and L.T. contributed to the device characterization. G.L.L., J.P.R., D.F., W.Z., X.Q.L., and X.M.Z. provided valuable suggestions for improving the quality of this work and revised the manuscript. All authors reviewed, commented on, and approved the final manuscript.

Notes

The authors declare no competing financial interest.

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