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Impact of passivation layer on the subthreshold behavior of p-type CuO accumulation-mode thin-film transistors

Qi Chen *, Xi Zeng, Denis Flandre

Institute of Information and Communication Technologies, Electronics and Applied Mathematics, UCLouvain, Louvain-la-Neuve 1348, Belgium

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ABSTRACT

In this work, models of p-type CuO metal-oxide- semiconductor (MOS) capacitor and thin-film transistors (TFTs) are established using numerical simulation tools and compared with experimental data, to investigate the impact of a passivation layer on the TFT subthreshold behavior. Simulated transfer curves and hole concentrations of back-gated CuO TFT with 10 μm channel length confirm the experimental observation of buried-channel and accumulation-mode conduction mechanisms. The subthreshold behavior is analyzed with HfO2 passivation on the top CuO surface varying the densities of fixed oxide charge and interface states, as well as the thickness of the CuO film. The simulation results demonstrate a significant potential improvement of the subthreshold slope and on/off current ratio, mainly thanks to the optimization of the fixed oxide charge densities.

1. Introduction

Thin-film transistors (TFTs) based on metal oxide semiconductors have attracted wide attention as candidates for advanced displays and sensors, for their low processing temperature, excellent uniformity, and adequate carrier mobilities [1]. N-type metal oxide TFTs, such as amorphous indium-gallium-zinc-oxide (IGZO) and zinc oxide (ZnO) TFTs, were extensively reported with excellent performance [2,3]. On the contrary, p-type metal oxide TFTs are less studied. While necessary to realize complementary metal oxide semiconductor (CMOS) circuits, they still feature poor performance compared to their n-type counterparts [4,5].

CuO has been proposed as a promising channel layer for p-type metal oxide TFTs for its tunable bandgap from 1.2 to 1.9 eV and high Hall mobility [6,7]. Recently, we reported CuO TFTs with high-k HfO2 as a back-gate dielectric and no top passivation [8]. Our devices exhibited state-of-the-art performance, with still limited inverse subthreshold slope (SS), carrier mobility, and on/off current ratio. An Al2O3 passivation layer on top of a Cu2O film was proposed to improve the subthreshold characteristics [9]. Kim et al. also reported similar effects of passivation layer on device switching characteristics for p-type SnO TFTs [10]. Unlike Al2O3, HfO2 generally features positive fixed charges and was also reported as a passivation layer material [11].

In this work, simulation methodology is used to investigate the impact of a HfO2 passivation layer on the subthreshold behavior of back-gate CuO TFT. Numerical models of MOS capacitor and TFTs are constructed based on our previous experimental results. The impact of fixed oxide charge density (*Qf*) and interface trap densities (*Dit*) at the top HfO2 passivation layer interface is studied. HfO2-passivated TFTs with a thinner CuO film are finally studied to further optimize the device subthreshold performance.

2. Results and discussion

2.1. Reference structure without passivation

The material parameters of CuO and HfO2 films extracted from our experiments [8] are used in Silvaco Atlas simulations (Table 1) [12]. Notably, HfO_2 has both interface and bulk oxide fixed charges. However, in Silvaco Atlas, oxide fixed charge can only be specified as a sheet charge at the interface [12]. We thus combine the interface and bulk fixed charges, according to [13], using an effective oxide fixed sheet charge density Q_f that has an equivalent electrical effect on the device flat-band voltage and conduction mechanisms. The starting values of Q_f and interface donor defect density D_{it} used in the simulations have been obtained from the experiments of [8]. Furthermore, the energy level dependence of CuO/HfO_2 interface defects is introduced as a Gaussian distribution with a peak at 0.45 eV measured from valence band edge, i.e. to be electrically active when scanning the gate voltage from depletion to accumulation regions of our devices.

* Corresponding author.
E-mail address: qi.chen@uclouvain.be (Q. Chen).

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The simulated *C-V* curve of Au-HfO2-CuO-Au capacitor fairly compares with the experiment, as illustrated in Fig. 1(a) at a frequency of 500 kHz. The approximations of the flat-band voltage and of the maximum depletion region in experimental and simulated *C-V* curves validate the starting material parameters of Table 1 that will be used in the TFT simulations, in which a variation of the top interface parameters is further considered to study the underlying physical mechanisms. The observed deviations between experimental and simulated *C-V* curves could be related to bulk charges and defects within the CuO film. This is however lowly discussed in literature till now and is beyond the scope of this paper. Therefore, we do not take them directly into consideration in the CuO TFT simulations but indirectly through the used values of the doping and the mobility as extracted from the experimental data. As shown in Fig. 1(b), such approximation does not appear to impact the simulated *I-V* curves compared to the experimental ones, as much as it does for the *C-V* curves (Fig. 1(a)).

The structure of the unpassivated back-gated CuO TFT with a channel length of 10 um is depicted in the inset of Fig. 1(b). The thicknesses of Au contacts in the CuO TFT are 100 nm. A layer of air is introduced above the top CuO interface between source and drain. Fig. 1 (b) shows a good fit between simulated and measured transfer curves. Two threshold voltages are extracted from the second derivative of the drain current (*ID*) – gate voltage (*VGS*) curve: the first threshold voltage, *V*th1, is observed at around 0.6 V when a buried channel forms in the CuO film, and the second threshold voltage, *V*th2, is identified at the flat band voltage (- 1.7 V), according to the accumulation-mode TFT theory [14,15].

Fig. 2(a) depicts the simulated hole concentration distribution in the CuO film for gate voltages stepped from 1 to − 0.5 V to study the behavior around threshold. For $VGS > Vth1$, the CuO film is fully depleted and the current is cut-off. For $Vth2 < VGS < Vth1$, a partial depletion occurs at the mid-depth in the CuO layer, resulting in a buried conduction channel that enlarges for decreased gate voltages, leaving a thin depletion layer at the top. SS can then be interpreted by a simplified capacitance model of the accumulation-mode CuO TFT (Fig. 2(b)), leading to the following approximated theoretical equation [16]

$$SS = \ln 10 \frac{kT}{q}\left(1 + \frac{C_{bc}}{C_{gc}}\right) \quad (1)$$

where kT/q is the thermal voltage, *Cgc* and *Cbc* are the gate to channel and buried channel to source capacitances, respectively. In Fig. 2(a), in subthreshold regime, the buried channel is closer to the top interface than to the bottom, which results in a small *C*gc and a large *C*bc, and hence increases the SS according to equation (1).

2.2. Top passivated structure

To investigate the top passivation impact on the simulated subthreshold performance, a 100-nm- thick HfO2 layer is introduced at the front CuO interface between source and drain contacts (inset of Fig. 3 (a)). Fig. 3(a) and (b) show the respective transfer curves simulated for different densities of interface traps D_{it} and fixed oxide charges Q_f at the front CuO/HfO_2 interface., for ranges of values determined according to the measurements (see Table 1) i.e. considering a front CuO/HfO_2 interface nature similar to the back. Unexpectedly, the SS (extracted as $((dV_{GS}/d\log(I_D))|_{max})^{-1}$) degrades from 0.74 to 1.9 V/dec when decreasing the front donor D_{it} from 4×10^{13} to 4×10^{10} $eV^{-1}cm^{-2}$ (while acceptor D_{it} have no impact). Increasing *Q*f from 1×10^{12} to 3×10^{12} cm^{-2}, SS and on/off ratio improve significantly to 0.061 V/dec and 2.28 $\times 10^7$, respectively. SS then degrades to 0.123 V/dec for higher *Q*f.

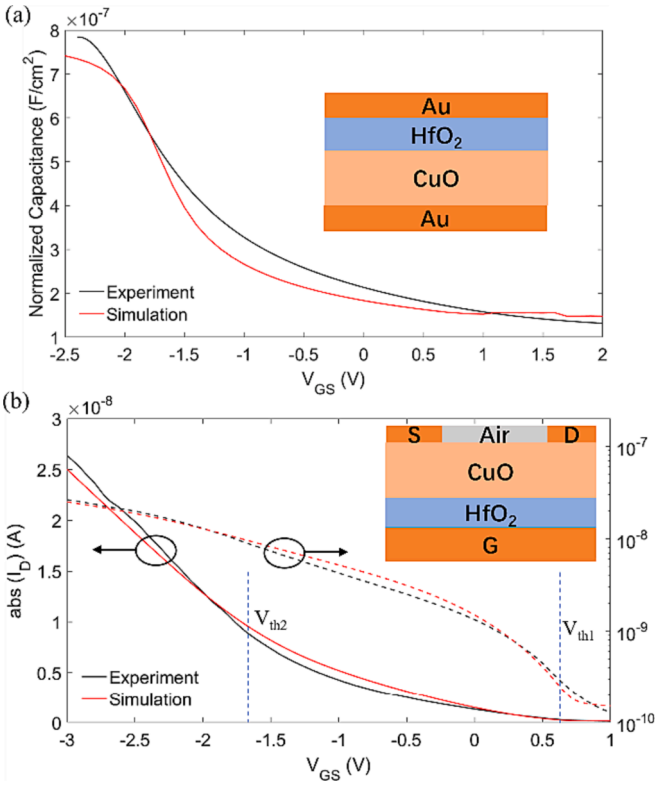

Fig. 1. Simulated (red) and measured (black) (a) MOS capacitor capacitance–voltage curves at 500 kHz and (b) TFT transfer curves at *V*DS = -1V, the device structures are depicted in insets (schematics are not at scale). S, D and G denote source, drain, and gate Au contacts, respectively. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

To understand these effects, Fig. 3(c) and (d) show the respective hole and electron concentrations at comparable gate biases in the subthreshold region, along channel depth at half channel length. Increased front *Q*f and donor *D*it enlarge the top depletion width and push the subthreshold buried channel closer to the back gate, leading to a higher *C*gc and a smaller *C*bc, which significantly improves SS as well as the on/off current ratio. However, a top inversion layer appears for *Q*f larger than 3×10^{12} cm^{-2} (Fig. 3(d)), pinning the top surface potential, thus increasing *C*bc and degrading SS.

2.3. Optimized structure

To further study the subthreshold behavior of HfO2 passivated CuO TFT, a thinner CuO film (90 nm) was also studied. Transfer curves with different front *Q*f and constant reference *D*it (=3.57×10^{13} $eV^{-1}cm^{-2}$) are shown in Fig. 4(a). SS, on/off ratio, and threshold voltage *V*th1 with different front *Q*f and CuO film thicknesses are compared in Table 2. SS significantly improves when CuO film thickness decreases from 120 to 90 nm at $Qf = 1 \times 10^{12}$ and 2×10^{12} cm^{-2}, because of a larger *C*gc in

Table 1
CuO material parameters extracted from our experiments [8] and used in the simulations of Fig. 1.

Material	CuO					HfO2	
Parameter	Band Gap (eV)	Mobility ($cm^2V^{-1}s^{-1}$)	Thickness (nm)	Doping Density (cm^{-3})	Interface Donor Defect Density *D*it (eV^{-1} cm^{-2})	Fixed Oxide Charges (cm^{-2})	Thickness (nm)
Value	1.6	6.2×10^{-4}	TFT: 120 Capacitor:115	5×10^{17}	Back (HfO2): 6×10^{10} Front (air): 3.57×10^{13}	Back: 8.78×10^{12} Front: -	25

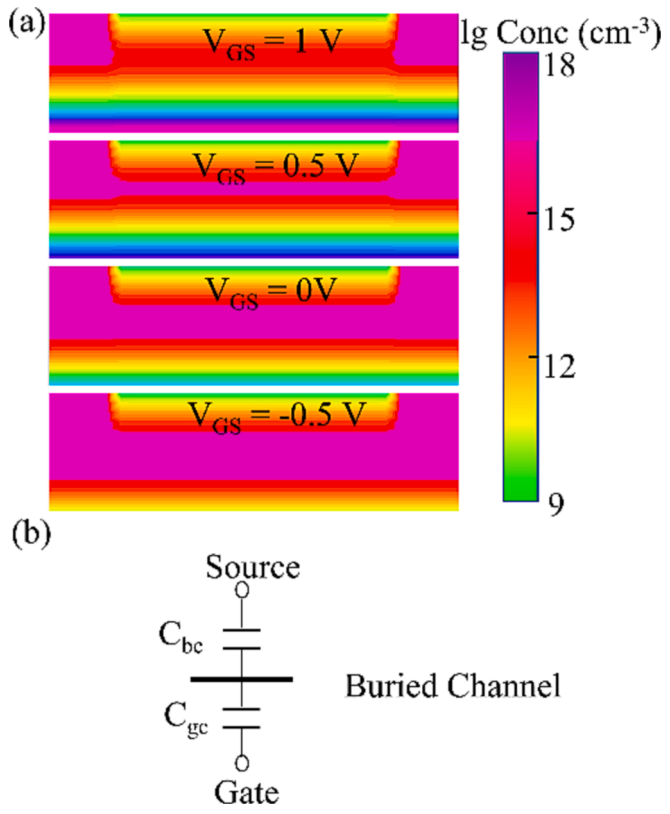

Fig. 2. (a) Simulated hole concentrations in the TFT CuO film for gate voltages stepped from 1 to −0.5 V. VDS = 0 V. (b) A simplified capacitance model of the accumulation-mode CuO TFT in subthreshold operation.

thinner CuO film. SS approaches theoretical limit at $Qf = 3 \times 10^{12}$ cm^{-2} and then degrades at $Qf = 4 \times 10^{12}$ cm^{-2} regardless of the CuO film thickness due to the aforementioned front inversion layer. *V*th1 shifts towards more negative values with 90 nm CuO film compared to 120 nm, as expected from enhanced full depletion in subthreshold, that also reduces the off current, especially for $Qf = 1 \times 10^{12}$ and 2×10^{12} cm^{-2}. A negative *V*th1 is more adequate for CMOS circuit applications. In addition, *I*on measured at the same |*V*GS-*V*th1| slightly increases with decreased CuO thickness and thus larger on/off ratio are obtained at $Qf = 3 \times 10^{12}$ and 4×10^{12} cm^{-2}.

The transfer curves under different front *D*it with 90 nm CuO film and constant front *Q*f (=2×10^{12} cm^{2}) are shown in Fig. 4(b). SS slightly improves from 0.1 to 0.061 V/dec with *D*it increasing from 1×10^{11} to 1×10^{13} eV^{-1}cm^{-2}, which is opposite to the observation for larger *D*it values made in the case of 120 nm CuO film (Fig. 3(a)). Fig. 4(c) shows the potential evolution in the film is detailed as a function of *V*GS in subthreshold region. In the thin CuO film, increasing the front *D*it does not significantly push the buried channel towards the back gate but rather pins the potential at the front interface. This reduced control of the gate bias on the film potential leads to an increase of SS according to extended models of accumulation-mode transistors [17].

3. Conclusion

Our simulations, calibrated on experimental devices, demonstrate that in accumulation-mode p- type TFTs with 120 nm-thick CuO films, increased positive *Q*f (up to 3×10^{12} cm^{-2}) and donor *D*it (up to 4×10^{13} eV^{-1}cm^{-2}) at top CuO/passivation interface enlarges the front depletion and pushes the buried channel towards the bottom of the CuO film, thus improving the back gate control and the subthreshold behavior. The effect of *Q*f on the subthreshold behavior is much more significant than that of *D*it. However too large *Q*f (4×10^{12} cm^{-2}) can form a front inversion layer, degrading SS due to the pinned potential at the top interface. HfO2-passivated TFTs with thinner (90 nm) CuO film show excellent subthreshold performance in our simulations with moderate densities of positive *Q*f (2×10^{12} cm^{-2}) and donor *D*it (1×10^{11} eV^{-1}cm^{-2}) at the passivated interface. Such ranges of *Q*f and *D*it can be more readily controlled in experimental fabrication. The resulting optimized p-type TFT structure shows values of threshold voltage, subthreshold slope, and on/off current ratio very adequate for CMOS-like circuit implementations.

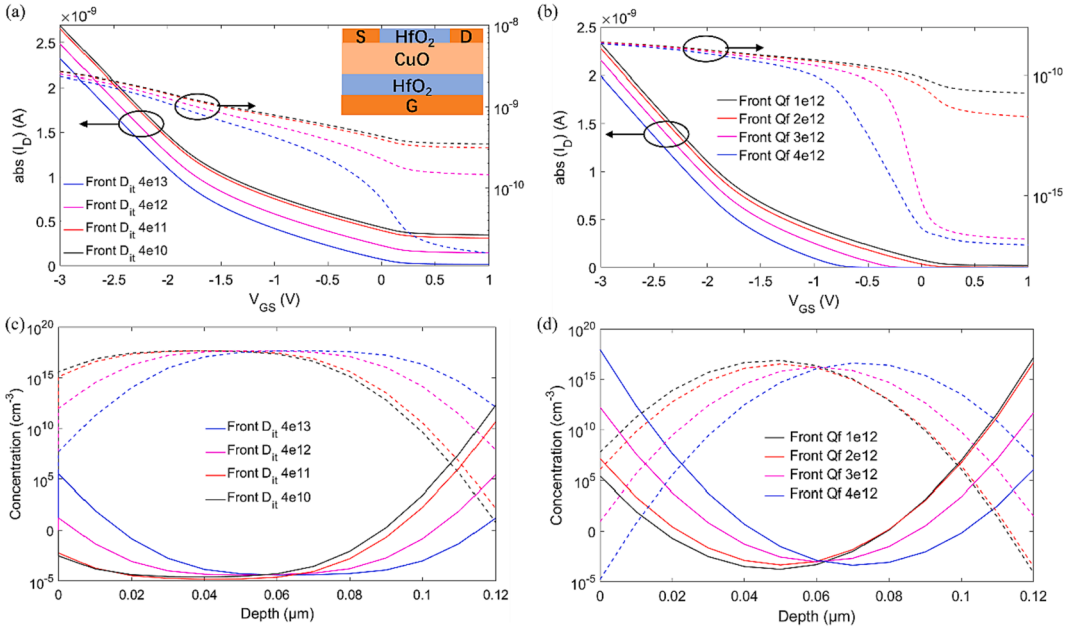

Fig. 3. CuO TFT structure with a top 100 nm HfO2 passivation layer (inset). Impact of (a,c) top CuO/HfO2 interface donor defect densities *D*it at constant |*I*D| (=5×10^{-10} A) and front *Q*f (=10^{12} cm^{-2}) and (b,d) top CuO/HfO2 interface fixed oxide charge densities *Q*f under constant |*I*D| (=2×10^{-10} A) and *D*it (=3.57×10^{13} eV^{-1}cm^{-2}) on (a,b) transfer curves (*V*DS = -0.1 V) as well as (c,d) hole (dashed lines) and electron (solid lines) concentrations from front (0 nm) to bottom (120 nm) of CuO film, at half channel length. Other parameters are set as in Table 1.

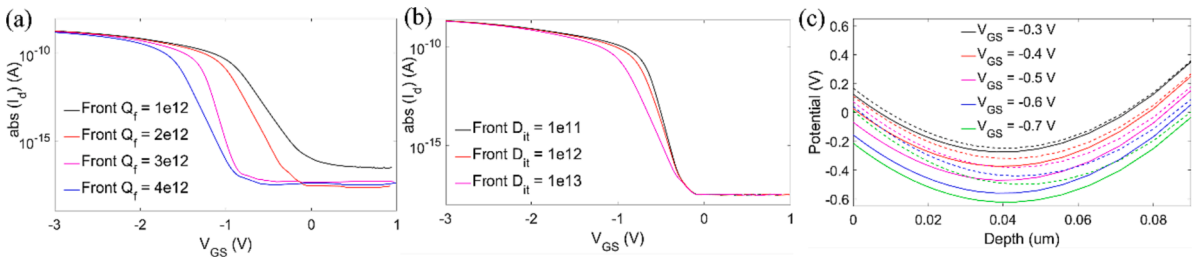

Fig. 4. Simulations of top-passivated back-gated 90 nm-thick CuO TFT: (a,b) Transfer curves with (a) different front *Q*f and constant *D*it (=3.57 × 10^{13} $eV^{-1}cm^{-2}$), (b) different front *D*it and constant front *Q*f (=2 × 10^{12} cm^{-2}); (c) Potential in the CuO film (refered to source voltage) as a function of depth, at half channel length, for different VGS values at *D*it = 1 × 10^{11} (solid lines) or 1 × 10^{13} $eV^{-1}cm^{-2}$ (dashed lines) with constant front *Q*f = 2 × 10^{12} cm^{-2}. *V*DS = -0.1 V.

Table 2
SS, threshold voltage *V*th1 and Ion/Ioff ratio in top passivated CuO TFT with different front *Q*f, for 90 and 120 nm CuO thicknesses. Front *D*it = 3.57 × 10^{13} $eV^{-1}cm^{-2}$, *V*DS = -0.1 V. Other parameters as in. *I*on are extracted at *V*GS-*V*th1 = -1 V and *I*off corresponds to the minimum current value.

Front *Q*f (cm^{-2})	SS (mV/dec)		*V*th1 (V)		*I*on/*I*off	
	TCuO = 90 nm	TCuO = 120 nm	TCuO = 90 nm	TCuO = 120 nm	TCuO = 90 nm	TCuO = 120 nm
1 × 10^{12}	140	560	−0.89	0.16	1.89 × 10^{7}	1.8 × 10^{1}
2 × 10^{12}	110	260	−1.02	0.13	8.45 × 10^{7}	1.47 × 10^{2}
3 × 10^{12}	61	61	−1.28	−0.29	1.09 × 10^{8}	2.28 × 10^{7}
4 × 10^{12}	97	123	−1.58	−0.75	1.35 × 10^{8}	5.67 × 10^{7}

This simulation work of the impact of passivation layer on sub-threshold behavior of accumulation-mode TFTs provides guidelines to improve the performance of other p-type TFTs and could be applied to other metal oxide semiconductors such Cu2O and SnO.

CRediT authorship contribution statement

Qi Chen: Data curation, Formal analysis, Funding acquisition, Investigation, Methodology, Validation, Visualization, Writing – original draft, Writing – review & editing. **Xi Zeng:** Data curation, Formal analysis. **Denis Flandre:** Conceptualization, Formal analysis, Funding acquisition, Supervision, Writing – original draft, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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