45nm PD SOI FET gate resistance optimization for mmw applications

D. Lederer, S. Jain, S. Saroop, A. Kumar, G. Freeman
GLOBALFOUNDRIES, Hopewell Junction, NY USA

***Abstract*—This paper investigates the impact of phosphorous polysilicon gate pre-doping and silicide thickness on the gate resistance of NFETs. The analysis is performed on a 45nm partially depleted (PD) Silicon-on-Insulator (SOI) technology with a Ni silicided poly SiON gate stack. It is shown that both process features contribute differently to R_g improvements, making their respective benefits dependent on device finger width (W_f). The data also show that combining both approaches can simultaneously improve R_g and, consequently, device maximum oscillation frequency (F_{max}) on both small and large W_f devices.**

Keywords—Gate resistance, silicide, interface resistivity, phosphorous, millimeter-wave, partially-depleted silicon-on-insulator, maximum oscillation frequency.

I. Introduction

Thanks to continuous downscaling and FET architecture improvements (including G, S and D silicidation, stress liner introduction, spacer optimization, sub-100nm gate downscaling) CMOS technologies are now well suited for millimeter wave integrated circuits. Gate length (L_g) scaling increases gate transconductance (g_m) and other FET figures of merit (FOM) such as device cutoff frequency (F_t) and maximum oscillation frequency (F_{max}) but unfortunately also increases device gate resistance (R_g). As R_g is a key device FOM impacting phase noise and receiver noise figure it is crucial to find technological approaches that can compensate for this R_g impairment. This paper investigates for the first time ways to improve the gate resistance of a 45nm PD SOI technology with a Ni silicided poly/SiON gate stack by optimizing pre-doping gate implant and silicide layer thickness.

II. Experimental Approach

A. Technology

GLOBALFOUNDRIES's 45RFSOI technology is an evolution of SOI12S0 [1], a high performance partially depleted SOI CMOS technology developed for IBM POWER7® featuring embedded DRAM. The gate stack in 45RFSOI consists of silicon oxynitride dielectric, polySi and a top Ni silicide layer for gate resistance reduction.

B. Gate resistance extraction

To evaluate the impact of process experiments on R_g the de-embedded S-parameters of a suite of RF devices with various W_f are measured. R_g is then extracted from the measured Z-parameters using:

$$Re[Z_{11}] - Re[Z_{12}] = R_g + R_{ch} = \frac{R_{g,finger}}{N_f} + R_{ch} \qquad (1)$$

with R_{ch} [Ohm] being the channel contribution, $R_{g,finger}$ [Ohm] the resistance of a single finger and N_f the number of fingers. R_{ch} is removed from (1) using the method described in [2]. This method assumes that R_{ch} is a linear function of $(V_{gs}-V_t)^{-1}$ and, as a consequence, that R_g can be extracted from the extrapolated Y-intercept of the $Re[Z_{11}] - Re[Z_{12}]$ vs $(V_{gs}-V_t)^{-1}$ curve when the device is biased in strong inversion.

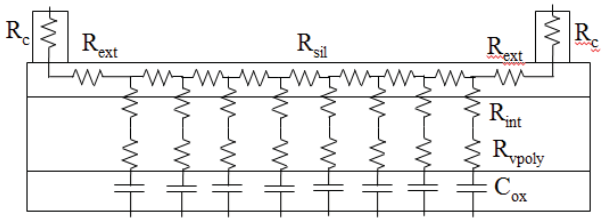

Fig. 1. Cross section of a gate finger showing the contributions to $R_{g,finger}$.

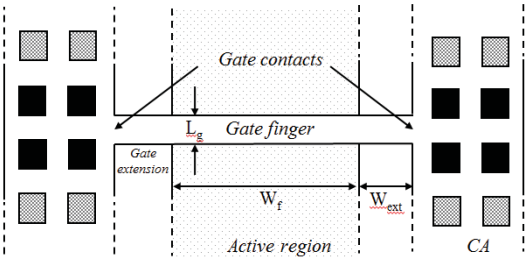

Fig. 2. Top view of a gate finger showing relevant geometrical parameters.

C. Gate resistance model

Similarly as in [3]-[6] $R_{g,finger}$ is modeled as the sum of several serial contributions (defined in Fig. 1), grouped into horizontal (R_{hor}) and vertical (R_{ver}) components:

$$R_{g,finger} = R_{hor} + R_{ver}$$

$$= \left[\frac{R_c}{N_c} + \frac{R_{sil}W_{ext}}{L_g N_c} + \frac{R_{sil}W_f}{3L_g N_c^2}\right] + \left[\frac{R_v}{L_g W_f}\right] \qquad (2)$$

In (2), R_{sil} [Ohm/sq] and R_v [Ohm.um^2] respectively denote the sheet silicide resistivity and the vertical resistivity, with $R_v = R_{int} + R_{vpoly}$ where R_{int} is the silicide/polysilicon interface resistivity and R_{vpol} the vertical resistivity of the non-

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silicided polysilicon. W_{ext} and N_c are geometrical parameters respectively describing, the polysilicon extension on the STI oxide [um], and the number of gate contacts (Nc =1, 2) per finger (Fig. 2).

The first-to-fourth terms in (2) respectively account for (i) the resistance of the metal-to-polysilicon contacts on each side of the finger (in this work we assume that 4 contacts are actively connected to each finger edge), (ii) the resistance of the gate extension over the non-active part of the DUT, (iii) the horizontal resistance of the gate silicided layer (the factor 3 is used to account for the distributed nature of this resistance [7]) and (iv) the vertical resistance related to the silicide-polysilicon interface and unsilicided region of the polysilicon..

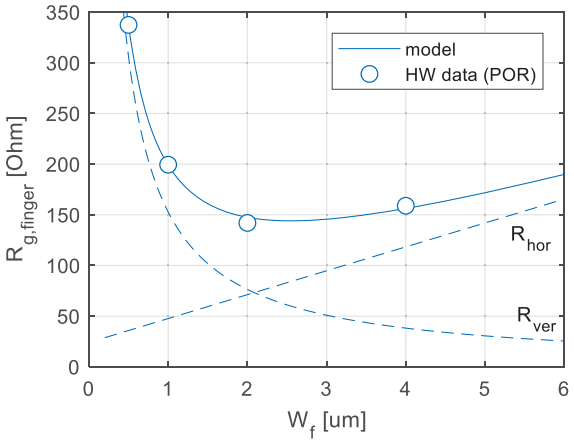

Fig. 3. Correlation between measured and modeled data and highlight of the horizontal (R_{hor}) as well as vertical (R_{ver}) contributions to the gate resistance.

D. Experimental data

Nominal L_g devices of various geometries are first measured on a control (or Process of Reference – POR) wafer and their gate resistance is plotted vs W_f in Fig. 3. A nonlinear least square fit is then applied on the measured data to extract R_{sil} and R_v. A good match is observed between model and measurements. The figure also highlights the different contributions of R_{hor} and R_{ver} to R_g, showing that R_v amounts to at least 75% of R_g for small width (<1um) devices. The extracted R_{sil} and R_v values are listed in Table I, and agree with previously published sub-100nm RF CMOS data [4], [5].

To improve R_v a first set of experiments is conducted in which the gate phosphorous (P) pre-doping dose is increased by 2x, 3x and 4x the POR value. This P implant is needed to minimize depletion effects in the gate polysilicon when the channel is biased in strong inversion. No other process parameter than the P implant dose is changed in this experiment.

The extracted R_{sil} and R_v data are plotted in Fig. 4 as a function of the implanted dose. A significant reduction of R_v is observed (ie, more than 30%) for a 2x POR dose value. Higher dose levels reduce benefits as R_v increases for 3x and 4x POR dose values compared to the 2x POR value. As indicated by TEM pictures of the samples (not shown) this R_v increase can be explained by a reduction of the silicided volume that occurs when the P implant dose is increased by 3x and 4x, which is then accompanied by lower silicide-polysilicon area and a subsequent increase in vertical resistance.

The impact of gate pre-doping on R_{sil} is different as R_{sil} is monotonically degraded with increased P dose, and shows a sharp increase (40~50%) between 2x and 3x the POR level. This trend is confirmed by DC measurements obtained on silicided poly resistors (dashed curve in Fig. 4) and can also be explained by the reduction of the silicided volume when the P implant dose is increased.

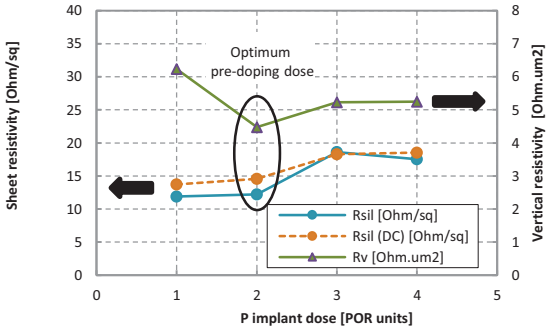

Fig. 4. Extracted R_{sil} and R_v gate components as a function of implant dose.

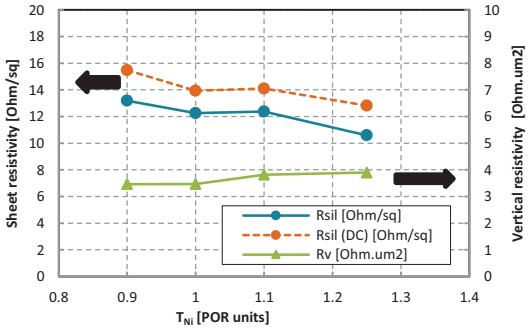

Fig. 5. Extracted R_{sil} and R_v gate components as a function of T_{Ni}.

III. Discussion

The drastic reduction of R_v with a 2x increase in pre-doping dose level is similar to what was observed in [6] on HKMG devices and can be explained by higher dopant segregation at the silicide/polySi interface, resulting in lower Schottky barrier height and reduced silicide/polySi interface resistivity. Reduced R_{vpoly} is also expected with increased pre-doping dose.

Since both R_{sil} and R_v contribute linearly to the gate resistance a minimum-R_g 'sweet' spot is highlighted in Fig. 4 for a 2x pre-doping dose level. As shown in Fig. 6 (squares), increasing the pre-doping level by a factor of 2 leads to a R_g reduction of more than 25% for W_f<2um. However, for higher W_f values, the penalty endured on R_{sil} from the pre-doping leads to reduced R_g benefit. Additional experiments were therefore conducted to test the sensitivity of R_g to the thickness of the deposited nickel layer (T_{Ni}) to reduce R_{sil}, and hence R_{hor}.. Extracted R_{sil} and R_v data are plotted vs T_{Ni} in Fig. 5 and show the clear benefit obtained on R_{sil} when increasing T_{Ni}, which is

also highlighted in the third row of Table I. The impact of T_{Ni} on R_v is minor, as could be expected. Fig. 6 (triangles) also highlights the fact that, since T_{Ni} mostly impacts R_{hor}, the benefit on R_g reduction is most noticeable on large (ie, W_f>2um) devices.

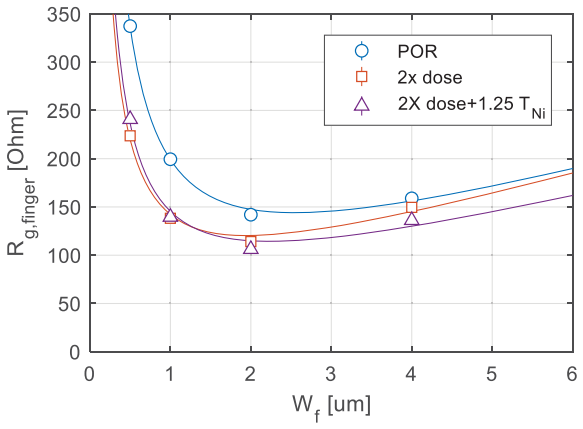

Fig. 6. Experimental and modeled data on the POR, 2x dose and 2x dose+1.25 T_{Ni} process split.

Lastly, the impact of both pre-doping and silicide layer thickening is investigated on device cut-off frequency, a device RF FOM known to be sensitive to R_g. The relative F_{max} improvements are plotted vs W_f in Fig. 7, and are seen to nicely correlate with the $R_{g,finger}$ trends shown in Fig. 6: pre-doping benefit is more observable on small W_f devices while thickening the silicide layer mostly impacts large W_f devices. This indicates that the combination of gate pre-doping optimization and T_{Ni} increase is an effective way to improve F_{max} both for small and large W_f devices.

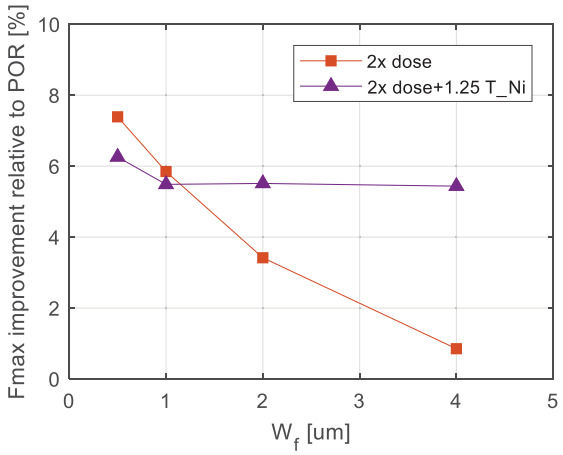

Fig. 7. Fmax improvement measured as a function of W_f on the POR, 2x dose and 2x dose+1.25T_{Ni} experiments.

TABLE I. EXTRACTED SILICIDE AND VERTICAL RESISTIVITY VALUES

Process split	*R_v [Ohm.um^2]*	*R_{sil} [Ohm/sq]*
POR	6.23	11.90
2x dose	4.25	11.68
2x dose + 1.25T_{Ni}	4.15	9.92

IV. CONCLUSION

The investigation performed in this paper indicates that the vertical component of the gate resistance (which is mainly attributed to the silicide-polysilicon interface resistance) amounts to at least 75% of R_g for small W_f (ie, W_f<1um) in NFET PD SOI 40nm-L_g devices with a gate Ni silicided polySiON gate stack. Increasing the gate pre-doping level by a factor of 2 compared to digital FET values can reduce this contribution by more than 30%. However it does have a slightly negative impact on the horizontal component of R_g, which can be compensated for by increasing the silicide thickness through thicker Ni layer deposition. Combined gate pre-doping and silicide thickness optimization increase are thus shown as effective ways to improve the gate resistance of digital CMOS technologies and improve their RF and millimeter wave performance across a large spectrum of W_f values.

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REFERENCES

[1] S. S. Iyer *et al.,* "45-nm silicon-on-insulator CMOS technology integrating embedded DRAM for high-performance server and ASIC applications", IBM J. Red. & Dev., May/June 2011, vol. 55(3), paper 5.

[2] A. Bracale "A new approach for SOI devices small signal parameters extraction" in Analog and Integrated Circuits and Signal Processing The Netherlands Dordrecht:Kluwer pp. 157-169 Nov. 2000.

[3] B. Dormieu, P. Scheer, C. Charbuillet, H. Jaouen and F. Danneville, "Revisited RF Compact Model of Gate Resistance Suitable for High-K/Metal Gate Technology," in IEEE Transactions on Electron Devices, vol. 60, no. 1, pp. 13-19, Jan. 2013.

[4] A. Tanabe, K. Hijioka and Y. Hayashi, "A Novel Monitoring Method of RF Characteristics Variations for Sub-0.1µm MOSFETs with Precise Gate-resistance Model," IEEE Custom Integrated Circuits Conference 2006, San Jose, CA, 2006, pp. 725-728.

[5] R. A. Wachnik et al., "Gate stack resistance and limits to CMOS logic performance," Proceedings of the IEEE 2013 Custom Integrated Circuits Conference, San Jose, CA, 2013, pp. 1-4.

[6] C. Schwan et al., "CMOS RF performance gain by gate resistance optimization," 2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), San Francisco, CA, 2016, pp. 114-117

[7] B. Razavi, R.-H. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 41, no. 11, pp. 750–754, Nov. 1994.