High-Temperature Characterization of Novel Silicon-Based Substrate Solutions for RF-IC Applications

Q. Courte, M. Rack, M. Nabet, P. Cardinael and J.-P. Raskin

ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium

{quentin.courte, martin.rack, massinissa.nabet, pieter.cardinael, jean-pierre.raskin}@uclouvain.be

Abstract — This paper focuses on the comparison of various advanced substrates such as trap-rich (TR), porous silicon (PSi), gold-doped (Au-Si) and smart-implants PN-junction (DP) in terms of RF performances. Both small- and large-signal measurements were performed, including the study of the influence of temperature and bias voltage. The purpose of this paper is to provide an overview of the characteristics of these multiple substrates to facilitate design choices for RF-IC applications.

Keywords — Silicon-on-Insulator (SOI) technology; effective resistivity; trap-rich (TR) substrate; Parasitic Surface Conduction (PSC); RF characterization; RF substrate; harmonic distortion (HD); gold-doped silicon substrate (Au-Si); high temperature.

I. Introduction

The demand for RF Front End Modules (FEM) is driven by market needs for increasing data rates in wireless communication applications [1]. Silicon technology, and especially SOI, is seen to be the most serious competitor to build these future analog FEMs, thanks to its low cost and easy integration with silicon digital circuits. This put a tremendous amount of constraints on the silicon technology to provide good Radio Frequency (RF) performances, which are deeply influenced by the substrate [2]. Indeed, substrate accounts for RF losses, coupling and nonlinearities, that are a consequence of its conductive nature. The Standard (Std) low resistivity (10 $\Omega.\,\mathrm{cm}$) substrate used for digital applications is not suited for RF applications. Switching noise from the digital part, can be injected through the bulk and perturbate the analog parts of the circuit on the same chip. RF signals penetrate into the bulk, increasing losses and crosstalk [3]. Several advanced substrates have been developed throughout the years, to allow SOI technology to tackle the aforementioned problems. One solution is to use lowly doped silicon. It presents the advantage of having a high nominal resistivity ρ_{nom}, above 1 $\mathrm{k\Omega.\,cm}$ forming the so-called High Resistivity (HR) substrate. However, due to Parasitic Surface Conduction (PSC), a sheet of high carrier density inherent to the fabrication process and formed because of the presence of fixed charges at the insulator/semiconductor interface (usually positive in Si/SiO_2 structures), the effective resistivity of the substrate is reduced by several orders of magnitude [4]. This PSC makes the use of a HR substrate ineffective for improving the performance of overlying ICs [5]. An innovative SOI substrate called Trap Rich (TR) has been developed to suppress PSC by introducing a thin layer (300 nm to 2 µm) of Polysilicon at the $Si-SiO_2$ interface. This layer can trap carriers from the PSC sheet and restores the nominal resistivity of the substrate and drastically reduces Harmonic Distortion (HD) of the passives [6],[7]. Today, TR is present in all smartphone FEMs [8]. Another solution is the gold-doped silicon (Au-Si) substrate which consists in doping a Std silicon wafer with gold atoms that will create traps in the silicon bandgap. Carriers that are trapped in the bandgap cannot participate to conduction [9],[10]. In the case of porous silicon (PSi), a part of the silicon bulk is removed by electrochemical dissolution, creating air spaces preventing conduction, but also traps at the pore walls like in TR [11]. Finally, smart-implants PN-junction (DP) is a more recent proposal where the alternance of P and N doped regions near the BOX creates PN-junctions with depletion regions at the interface between the N and P regions [12]. In these depletion regions, the PSC is interrupted and the local resistivity is very high since very few carriers are present.

This paper presents these substrates and compares their RF performances with one-another up to high temperature (25°C to 175°C) to facilitate the choice of the appropriate substrate given design and application constraints. To this end, the substrates are analyzed through measurements both in small-signal up to 10 GHz and large-signal at a fundamental frequency of 900 MHz. The influence of DC bias is also studied.

II. Substrates Description

Coplanar waveguides (CPW) were fabricated for RF characterization on the seven types of silicon-based substrates. All substrates are described in Fig. 1.

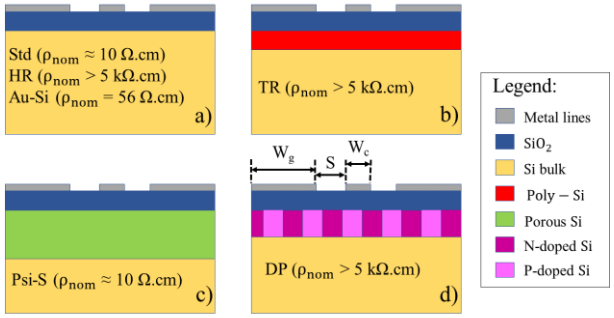

Fig. 1. Cross-section of the studied substrates. The thickness of the BOX and handle Si substrate are, respectively, for: Std – 500 nm, 381 µm; HR – 500 nm, 725 µm; TR – 500 nm, 725 µm; PSi – 500 nm, 381 µm; Au-Si – 200 nm, 725 µm; DP – 200 nm, 381 µm. Dimensions of the lines (in µm) are: Std, HR, TR, PSi – W_c=38, S=18, W_g=208; Au-Si – W_c=26, S=12, W_g=208; DP – W_c=26, S=12, W_g=160. All lines have a length of L = 2 mm.

● Fig. 1a: Standard p-type silicon (ρ_{nom} =1–10 Ω. cm), High-Resistivity (HR) silicon (ρ_{nom} > 5 kΩ. cm), gold-doped silicon (ρ_{nom} ≈ 56 Ω. cm).

● Fig. 1b: Trap-rich (TR) enhanced high resistivity silicon (ρ_{nom}> 5 kΩ. cm);

● Fig. 1c: Porous Si substrates, PSi-S (ρ_{nom}=10 Ω. cm);

● Fig. 1d: DP, PN-junctions Si substrate (ρ_{nom} > 5 kΩ. cm). P and N doped pattern are 1 and 3 µm wide, respectively.

More details can be found on substrate fabrication in [11] for Std, HR, TR and PSi substrates, in [13] for Au-Si substrate and [14] for DP substrate.

III. Substrates Measurements

A. Measurement setup

On-wafer measurements of CPW lines were performed using an Agilent 2-port PNA-X vector network analyzer and a pair of GSG | Z | probes from Cascade Microtech. From the measured S-parameters we extract the effective resistivity (ρ_{eff}) and RF line losses (α) using the method described in [15], up to 10 GHz and from room temperature up to 175°C. SOLT calibration was performed as well as the de-embedding scheme proposed by Gillon *et al*. [16]. Large-signal measurements were performed, using an Agilent 4-port PNA-X vector network analyzer to assess the nonlinear behaviour of the substrates. A single tone with a fundamental frequency f_0 of 900 MHz was injected into the first port of the CPW line [13]. The input power was varied from -25 to 25 dBm. The distorted signal was measured at the second port of the CPW line. The second harmonic component H2 (at frequency 2 f_0 = 1.8 GHz) indicates how non-linear the substrate response is to a large-amplitude RF signal.

B. Small-signal characterization

In this section, PSi, Au-Si and DP substrates will be compared with commercially available Std, HR and TR.

Fig. 2 shows the effective resistivity ρ_{eff} and the lineic losses α for the studied substrates. Std silicon substrate exhibits a ρ_{eff} of 10 Ω. cm at 10 GHz. For HR, ρ_{eff} is around 30-40 Ω. cm and TR has the highest ρ_{eff} than the latters with 3-4 kΩ. cm. TR samples with ρ_{eff} in the range of several tens of kΩ. cm are also available [17]. The same logic can be observed for lineic RF losses α, for which Std shows the highest losses of 3 dB/mm at 10 GHz, followed by HR between 1 and 2 dB/mm and finally TR with 0.3 dB/mm losses which originate mainly from the metallic line resistivity. Effective resistivity and losses are directly linked to the free carrier concentration in the substrate beneath the BOX. Std substrate shows an effective resistivity comparable to its nominal resistivity, which is not the case for HR because of the PSC effect. However, once the PSC effect is counter-acted by the polysilicon layer, the TR substrate recovers an effective resistivity close to its nominal resistivity of 5 kΩ. cm. PSi shows effective resistivity comparable to TR or even slightly higher, with a mean ρ_{eff} of 7.7 kΩ. cm over the 1-10 GHz frequency range, and lineic losses of 0.2 dB/mm at 10 GHz. While the effectiveness of the TR to increase the effective resistivity and reduce line losses comes from its ability to trap free carriers, PSi successfully vanishes the PSC by two means. First, it reduces the total amount of conductive bulk silicon as a consequence of the porosification process and replaces it by nanometer-sized air cavities.

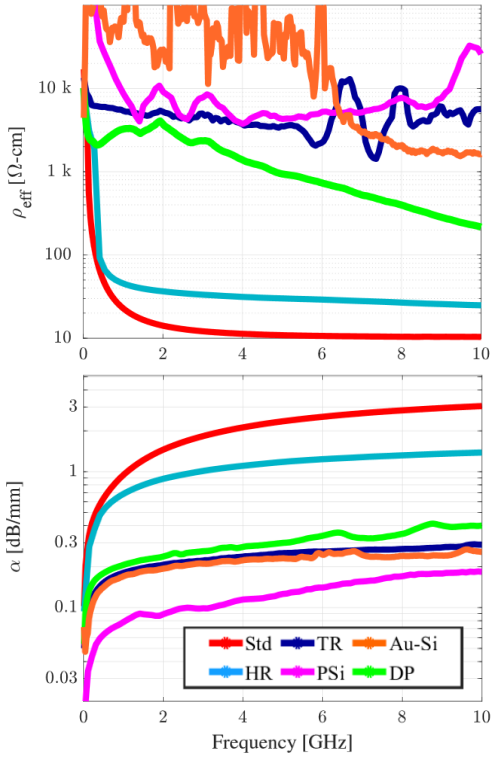

Fig. 2. Electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW-lines at 25°C as a function of frequency. Top: effective substrate resistivity. Bottom: CPW line losses per unit length.

Secondly, by creating trapping states at pores surface just like TR creates interface traps at grains boundaries or along electrically active defects inside the polysilicon grains. Both combined effects are at the origin of the better RF performances of PSi compared with TR. Au-Si shows ρ_{eff} > 10 kΩ. cm up to 6 GHz, which is the highest value for the samples presented and insertion losses are comparable to TR. The fact that α is high proportionally to the substrate's effective resistivity is due to the metallic losses that are dominant when ρ_{eff} is high (~> 10 kΩ. cm). DP substrate also shows improvements compared to HR, with ρ_{eff} above 2 kΩ. cm up to 3 GHz. It then decreases to 200 Ω. cm at 10 GHz. The reason is that it is composed of highly conductive (doped) regions separated by depleted regions having a capacitive behaviour, with thus an increased junction-junction admittance with frequency. DP shows lineic losses of 0.4 dB/mm at 10 GHz.

Note that ρ_{eff} extracted from Fig. 2 suffers from important variations when the resistivity is very high. Au-Si shows ρ_{eff} values between 10 k and 100 kΩ. cm, TR between 2 and 10 kΩ. cm and PSi between 4 and more than 10 kΩ. cm. Those fluctuations come from the fact that these substrates are quasi-lossless, and the lineic conductance parameters extracted from the CPW line measurements are then very low, and prone to calibration and probing errors and to noise. It is then a challenge to extract clean ρ_{eff} data above 10 kΩ. cm [18].

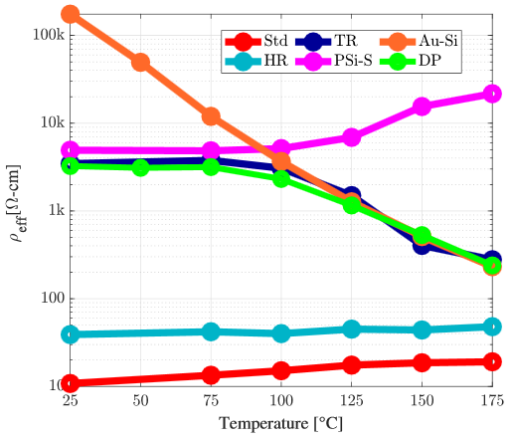

Fig. 3. Effective resistivity as a function of the temperature for Std, HR, TR, PSi and Au-Si. ρ_{eff} is averaged from end of slow-wave mode (different for each substrate) up to 10 GHz. ρ_{eff} for DP is extracted at 1 GHz.

Consequently, ρ_{eff} with temperature in Fig. 3 is obtained by averaging it from the end of the slow-wave mode up to 10 GHz. This is not the case for DP which was extracted at 1 GHz, where it still shows a good effective resistivity. Thus, the extracted ρ_{eff} will change greatly with the frequency of extraction, even though the trend of decreasing ρ_{eff} with temperature will be maintained, which is not the case for the other substrates because of their steady behaviour with frequency. Increased temperature in highly resistive semiconductor substrates, such as TR, Au-Si and PSi, usually has the effect of degrading their performances, by increasing the number of thermally generated intrinsic free carriers in such carrier-free semiconductors. This in turn decreases the effective resistivity which has the unwanted effects of raising substrate losses as well as noise coupling levels. This phenomenon is observed in the TR, Au-Si and DP substrates, see Fig. 3. For Au-Si, ρ_{eff} is decreasing by 1 order of magnitude every 50°C. For TR and DP, it decreases above 100-125°C with a reduction of one order of magnitude up to 175°C. On the other hand, the effective resistivity of the Std and HR substrates slightly increases with temperature. In such substrates with very high concentration of free carriers, the addition of thermally generated carriers is negligible at these temperatures. The reason for the increasing tendency of the Std curve in Fig. 3 is due to a reduction in carrier mobility as temperature increases, because the vibrating crystal lattice impedes more strongly the displacement of the free carriers within the bulk, due to their scattering with phonons. The twofold increase in effective resistivity from 25°C to 175°C is in good agreement with the twofold decrease in carrier mobility given by Arora's models and measurements in [19], as well as by Silvaco ATLAS mobility models [20]. PSi's effective resistivity increases above 125°C.

C. Large-signal characterization

The goal of these measurements is to compare the linearity of the different substrates, as a function of temperature and bias conditions. Nonlinearities are created by the changing properties of the line under the influence of the signal it is carrying. These properties are the admittance and capacitance that change with the concentration of free carriers modulated by the changing voltage of the travelling signal. When temperature increases, the number of thermally generated carriers will increase, but also the sensitivity of the substrate to signal voltage variations. Consequently, it can be expected that the trends (in temperature) observed for effective resistivity will be reproduced for linearity.

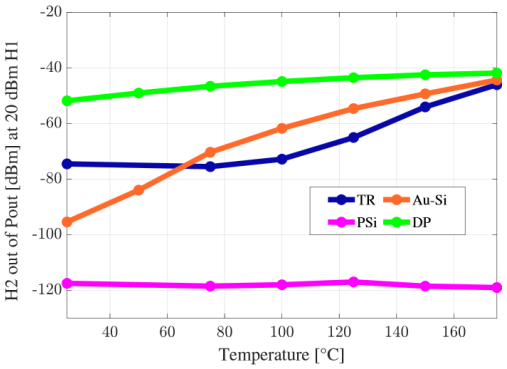

Fig. 4. Harmonic H2 at 20 dBm of fundamental H1 as a function of temperature (H1 and H2 are extracted, respectively, at 0.9 and 1.8 GHz).

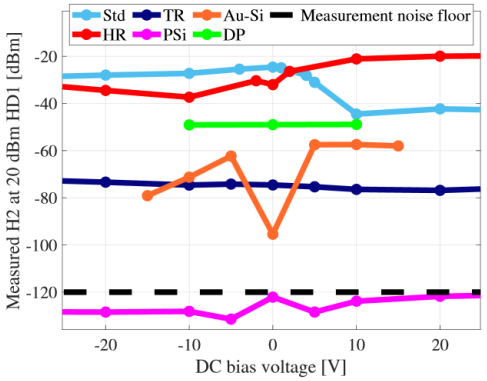

Fig. 5. Harmonic H2 at 20 dBm of fundamental H1 as a function of DC bias.

To confirm this, H2 is plotted as a function of temperature in Fig. 4 at 20 dBm of output power H1. DP substrate is the most nonlinear, with H2 of -50 dBm at 25°C, which increases slowly up to -43 dBm at 175°C. TR is flat both for ρ_{eff} and H2 (with H2 ≈ -75 dBm) up to 100°C with an increase in nonlinearity where a decrease of effective resistivity was observed. Au-Si is the one exhibiting the highest variations in ρ_{eff} which is also the case for H2 with more than 40 dBm of variation over the whole temperature range. This behaviour is explained in [13] based on the physics of the interface and Au-trap centers. Finally, PSi has significantly lower H2 (close to the noise level of -120 dBm) than TR while having comparable ρ_{eff}.

Fig. 5 plots the H2 levels of the substrates for varying DC bias at a H1 output level of 20 dBm. Std and HR show both high H2 and variations of H2 with bias of around 20 dBm on the whole bias range. For DP, H2 stays constant at -50 dBm from -10 to +10 V. TR has a lower H2, at around -70 dBm, that also stays constant with DC bias (3 dBm of H2 variation across the whole DC bias range). Au-Si is extremely bias sensitive, with H2 lower than TR at 0 V bias (-95 dBm), which degrades by around 40 dBm by applying 5 V bias and consequently is less

linear than TR at 5-15 V [13]. PSi substrate is the most linear, with the lowest H2 and therefore with the lowest signal voltage sensitivity.

IV. Discussion

This article compared performances of various innovative substrates, TR, DP, Au-Si and PSi, both in small- and large-signal over a wide temperature range. TR shows good performances (ρ_{eff} and α) also against temperature and bias. It must be noticed that some commercially available TR can reach values of ρ_{eff} greater than 50 kΩ.cm and H2 levels close to -100 dBm. Au-Si shows good performances with a high effective resistivity (>10 kΩ.cm) and high linearity (H2 < -70 dBm), it has also the advantage to be manufactured from a standard substrate 56 kΩ.cm. However, Au-Si does not keep its good properties against temperature and bias, and is not suitable for active devices. When gold penetrates in MOSFET channel it reduces carrier mobility, therefore, gold is not welcome in silicon foundries due to its high diffusivity and the high risk of contamination [13]. DP is a medium substrate in terms of performances but has an easy fabrication as it only uses standard doping implantation process steps. It is a recent prototype so its performances can be greatly increased through additional research, for instance by reducing the PN-junction pattern size [14]. PSi exhibits effective resistivity comparable to TR and has the lowest insertion losses and best linearity than the others. Furthermore, it keeps its good performances up to 175°C, which makes it ideal for high frequency, high temperature applications. However, robustness and repeatability issues in the fabrication process make it difficult to transfer to the industry.

Table 1. Summary of substrate performances.

Substrate	ρ_{eff}	Linearity	T° variations	Bias variations	Fabrication
TR	++	+	+	++	+
Au-Si	++	+	- -	- -	- -
DP	+	-	+	++	++
PSi	++	++	++	+	- -

V. Conclusion

This paper studied small- and large-signal performances of Au-Si, DP and PSi substrates as compared to commercially available Std, HR and TR as a reference. Measurements were performed up to 10 GHz to extract effective resistivity and lineic losses. The impact of temperature on effective resistivity was also highlighted. Finally, the linearity of the substrates was compared both in temperature up to 175 °C and as a function of DC bias from -25 up to 25 V. Advantages and drawbacks of the substrates are summarized in Table 1. Even though the Au-Si and PSi substrates have the benefit to be manufactured from a standard substrate and show RF performances comparable to TR, their application in the foundries for large scale manufacturing still challenging in terms of process. The DP is a solution to overcome the PSC. One of its big advantages is the compatibility with the modern CMOS process, but further research will be needed to develop it to its full potential.

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References

[1] M. Rack and J.-P. Raskin, "SOI technologies for RF and millimeter wave applications", *Electrochemical Society Transactions*, vol. 92, no. 4, pp. 79-94, 2019.

[2] K. Ben Ali *et al.*, "RF Performance of SOI CMOS Technology on Commercial 200-mm Enhanced Signal Integrity High Resistivity SOI Substrate", *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 722-728, Mar. 2014, 10.1109/TED.2014.2302685.

[3] Y. Wu *et al.*, "SiO_2 interface layer effects on microwave loss of high-resistivity CPW line", *IEEE Microw. Guided Wave Lett.*, vol. 9, no. 1, pp. 10–12, Jan. 1999, 10.1109/75.752108.

[4] D. Lederer and J.-P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity", *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 805-807, Nov. 2005.

[5] K. Ma, S. Mou and K. S. Yeo, "A study of CMOS SOI for RF, Microwave and millimeter wave applications", in *International SoC Design Conference (ISOCC)*, 2015.

[6] C. Roda Neve and J.-P. Raskin, "RF harmonic distortion of CPW lines on HR-Si and Trap-Rich HR-Si substrates", *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 924-932, April 2012.

[7] K. Ben Ali *et al.*, "RF SOI CMOS Technology on Commercial Trap-Rich High Resistivity SOI Wafer", in *IEEE International SOI Conference (SOI)*, 2012.

[8] D. C. Kerr *et al.*, "The effect of a SiO_2 interface on RF harmonic distortion in CPW lines on silicon or passivated silicon", in *Proc. 8th Topical Meeting Silicon Monolithic Integr. Circuits RF Syst.*, Orlando, FL, USA, Jan. 2008, pp. 151–154.

[9] N. Z. I. Hashim, "Au-compensated high resistivity silicon for low loss microwave devices-suppression of parasitic surface conduction effect", PhD Thesis, University of Southampton, 2015.

[10] W. Bullis, "Properties of gold in silicon", *Solid-State Electronics*, vol. 9, no. 2, pp. 143-168, 1966.

[11] M. Rack *et al.*, "Small- and large-signal performance up to 175°C of low-cost porous silicon substrate for RF applications", *IEEE Trans. Electron Devices,* vol. 65, no. 5, pp. 1887-1895, May 2018.

[12] J.-P. Raskin and M. Rack, "Integrated circuit device and method of manufacturing thereof", European Patent Office EP3564995A1, Sep. 6, 2019.

[13] M. Nabet *et al.*, "Behavior of gold-doped silicon substrate under small- and large-RF signal", *Solid State Electronics*, vol. 168, 107718, June 2020.

[14] M. Rack, L. Nyssens and J.-P. Raskin, "Low-loss Si-substrates enhanced using buried PN junctions for RF applications", *IEEE Electron Device Letters*, vol. 40, no. 5, pp. 690-693, May 2019.

[15] D. Lederer and J.-P. Raskin, "Effective resistivity of fully-processed SOI substrates", *Solid-State Electronics*, vol. 49, no. 3, pp. 491–496, Mar. 2005.

[16] R. Gillon *et al.*, "Determining the reference impedance of on-wafer TLR calibrations on lossy substrates", in *Proc. 26th Eur. Microw. Conf.*, Prague, Czech Republic, Sept. 1996, pp. 170-173.

[17] F. Allibert *et al.*, "Engineering SOI substrates for RF to mm-wave front-ends", *Microwave Journal*, pp. 72-82, Oct. 2020.

[18] L. Nyssens, M. Rack and J.-P. Raskin, "Effective resistivity extraction of low-loss silicon substrates at millimeter-wave frequencies", *International Journal of Microwave and Wireless Technologies*, vol. 12, pp. 615-628, September 2020.

[19] SILVACO, ATLAS User Manual, 2007.

[20] N. D. Arora *et al.*, "Electron and hole mobilities in silicon as a function of concentration and temperature", *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 292-295, Feb. 1982.