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Characteristics of noise degradation and recovery in gamma-irradiated SOI nMOSFET with in-situ thermal annealing

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ABSTRACT

This paper demonstrates a procedure for complete in-situ recovery of on-membrane CMOS devices from total ionizing dose (TID) defects induced by gamma radiation. Several annealing steps were applied using an integrated micro-heater with a maximum temperature of 365 °C. The electrical characteristics of the on-membrane nMOSFET are recorded prior and during irradiation (up to 348 krad (Si)), as well as after each step of the in-situ thermal annealing. High-resolution current sampling measurements reveal the presence of oxide defects after irradiation, with a clear dominant single-trap signature in the random telegraph noise (RTN) traces. Drain current over time measurements are used for the trap identification and further for the defects' parameters extraction. The power spectral density (PSD) curves confirm a clear dominance of the RTN behavior in the low-frequency noise. A radiation-induced oxide trap is detected at 5.4 nm from the Si-SiO_2 interface, with an energy of 0.086 eV from the Fermi level in the bandgap. After annealing, the RTN behavior vanishes with a further important reduction of flicker noise. Low-frequency noise measurements of the transistor confirmed the neutralization of oxide defects after annealing. The electro-thermal annealing of the nMOSFET allows a total recovery of its original characteristics after being severely degraded by radiation-induced defects.

1. Introduction

Silicon-on-insulator (SOI) technology has been widely shown to be suitable for electronics applications used in radioactive environments. SOI-based devices benefit from an intrinsic immunity to transient ionizing radiation effects thanks to the buried oxide (BOX) layer, which separates a relatively thin Si active layer from the thick Si substrate, thus minimizing the charges induced by ionizing particles [1]. However, these latter remain more sensitive to the Total Ionizing Dose (TID) effects, as the thick BOX forms an additional layer for radiation-induced positive charges that directly impact the electrical characteristics of the MOSFETs [2]. Various techniques are used for the mitigation of single event effects (SEEs), such as radiation-hardened design, redundancy, shielding, etc. [3]. However, TID effects remain more challenging to mitigate due to the cumulative creation of fixed positive charges in the SiO_2 insulating layers as well as the Si-SiO_2 interfaces' states [4]. This issue is problematic for the robustness and reliability of CMOS circuits in radiative environments. Low-frequency noise measurements have long been considered a fundamental tool to gather important information about the properties of the oxide defects under constant bias conditions [5]. This technique is used in our work to analyze the radiation-induced oxide defects and confirm the neutralization of the traps after the thermal annealing approach.

Recently, an increasing interest has been shed on in-situ electro-thermal annealing methods for the recovery of oxide defects begotten by TID [6–7]. These techniques are based on the thermal emission of holes from oxide-traps into the valence band [8]. Recent works on low-power and in-situ thermal annealing systems have demonstrated efficient recovery of active devices from radiation-induced defects. The recovery of on-membrane MOSFETs and CMOS devices was demonstrated after irradiation with fast proton and gamma doses of $10^{14}p^{+}/cm^{2}$ and 360 krad, respectively [9]. This work is an extension of our conference paper, outlining preliminary results on the noise PSD behavior of nMOSFET before and after annealing [10]. The current paper goes beyond our previous investigations by discussing in-depth (i) the degradation of the nMOSFET at different gamma doses, (ii) the characteristics of the radiation-induced defects and the origin of the in-situ recovery by electro-thermal annealing. The on-membrane MOSFETs are studied through electrical and RTN (Random Telegraph Noise) measurements. The paper is organized as follows: Section II describes

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the devices under test and measurement setup. In section III, the electrical MOSFET characteristics are investigated, demonstrating the shift of the transistors' features after a total dose of 348 krad(Si), and then after using different annealing temperatures. Section IV presents the Low Frequency Noise (LFN) measurements of the n-type MOSFET in fresh condition (*i.e.* after DRIE etching), after irradiation, and finally after the thermal annealing. Last measurements clearly demonstrate the creation of a radiation-induced oxide trap and confirm the neutralization of the defect by thermal annealing. The defect's properties (e.g. emission and capture time constants, current jumps, etc.) are extracted to generate the Lorentzian model and compare it with the noise PSD. This method demonstrates the clear dominance of strong RTN behavior due to gamma irradiation.

2. Experimental details

2.1. Studied devices

All devices under test (DUTs) are fabricated using a 1 μm partially depleted (PD) CMOS SOI technology. They consist of a body-tied 6 μm-wide 1 μm-long n-MOSFET, implemented in a circular membrane with a 600 μm diameter. The transistor is located in the close vicinity of a tungsten-based micro-heater, used for the in-situ thermal annealing by Joule heating (Fig. 1). Two positive-intrinsic-negative (PIN) diodes are implemented underneath the micro-heater and next to the transistor side for temperature monitoring. An isolation process is used to reduce the leakage current through the silicon substrate and therefore the crosstalk between different transistors, which can eventually affect the logic state (ON-OFF) of each device. All the devices are embedded on-membrane after etching the silicon substrate backside with a deep reactive ion etching (DRIE) process. Such a design is widely used in gas sensors to minimize heat dissipation through the substrate at the high activation temperatures required for gas-sensitive layers [11]. The device initially demonstrated showed a reliable characteristic at room temperature as well as at elevated temperatures up to 280 °C [12]. The calibration of thermo-diodes and the temperature monitoring technique are described in a previous work [12].

2.2. Experimental procedure

Drain current (I_{ds}) versus gate voltage (V_{gs}) of the n-type MOSFET were measured in both linear and saturation regimes, with $V_{ds} = 50$ mV and $V_{ds} = 3$ V, respectively. The voltage transfer characteristics of the on-membrane CMOS inverter were investigated under a supply voltage of $V_{dd} = 3$ V. These electrical measurements were performed at different conditions: in fresh condition, under gamma radiation (after each dose of 3.6 krad up to 348 krad), and after each annealing step. The purpose of these measurements is to study the degradation of the transistor's electrical performance under gamma radiation and the effect of the annealing temperature on the radiation-induced defects. Low Frequency Noise (LFN) measurements were also performed in each condition. The RTN and flicker noise measurements were performed at constant drain voltage with $V_{ds} = 3$ V. These measurements are performed at different drain currents ranging from 1nA up to 10 μA. All temporal measurements were recorded for 5 s with a time step Δt of 1 μs. This time resolution was considered sufficient to extract the emission and capture time constants of the observed defects. The PSD measurements were performed from 1 Hz to 1 MHz.

The chip was housed in a Dual In-line (DIL) ceramic package and connected to a pre-designed printed circuit board for bias application and monitoring during irradiation. Next, the DUT was installed in a room with a ^{60}Co gamma panoramic irradiator (located in the Cyclotron Research Center at UCLouvain, Belgium). Two sources of ^{60}Co were used, providing a maximum dose rate of 1.2 krad/h each. An HP4145 semiconductor analyzer and a laptop with a pre-defined IC-CAP script were installed in a shielded room and connected to the device through coaxial cables. A permanent positive bias V_{gs} of 3 V was applied to the transistor's gate during irradiation. The other contacts were connected to the ground. This configuration is considered the worst case and is generally used to separate electron-hole pairs, attract holes towards the Si/SiO_2 interface, and thus increase the sensitivity to radiation. A total dose of 348 krad(Si) was reached. An advanced analyzer from Keysight (ALFNA–E4727A) was used for noise measurements.

3. Results analysis

3.1. I-V measurements

Fig. 2 presents the Id-Vg characteristics of the MOSFET in linear regime with $V_{ds} = 50$ mV, measured before and after different doses of gamma radiation up to a total dose of 348 krad(Si) corresponding to 286 h of irradiation. One can notice a non-exponential behavior in the subthreshold regime. This could be explained by the post-processing defects created by the backside DRIE etching [13]. The leakage current of these process-induced defects is modeled by a parasitic transistor in the subthreshold region [14]. At lower radiation doses, a remarkable degradation of the subthreshold slope appears due to the cumulative creation of positive traps in the gate oxide, with a negligible degradation of the

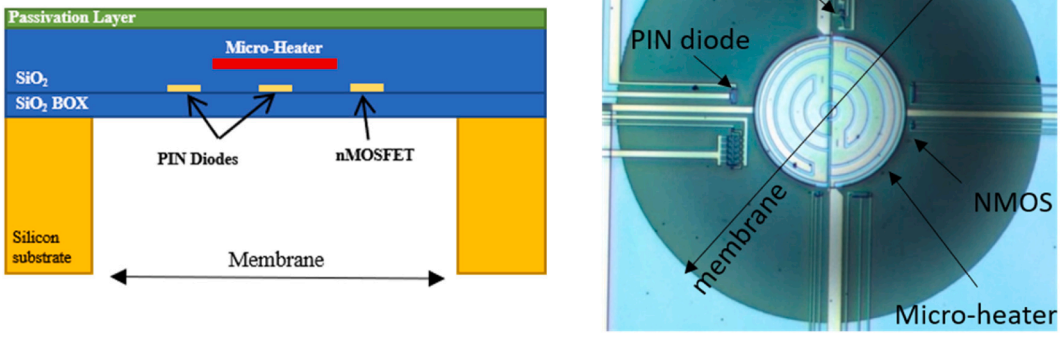

Fig. 1. Device under test: (a) cross-section schematic, (b) microscopic front view showing the membrane and other embedded elements.

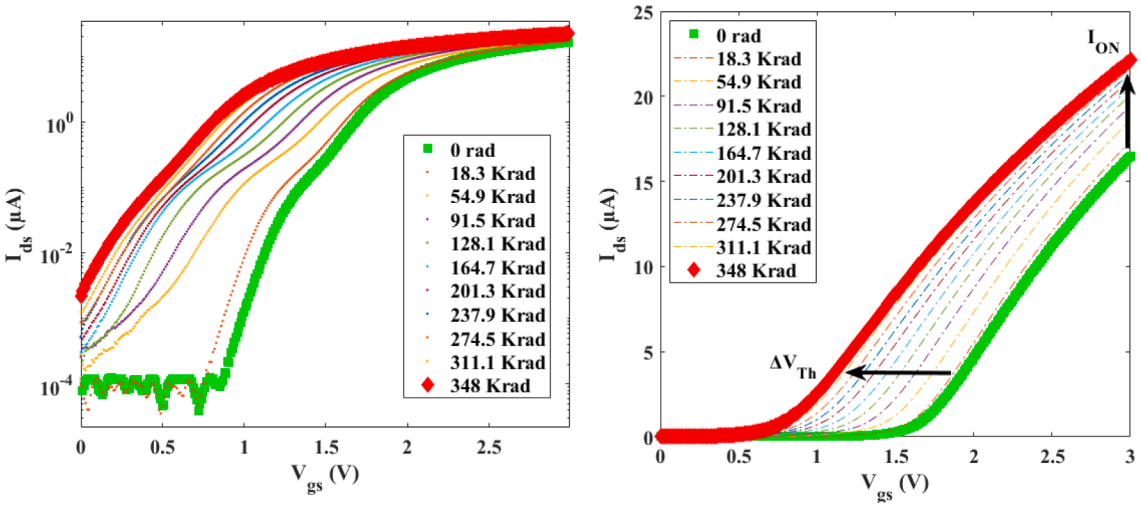

Fig. 2. I_{ds} versus V_{gs} measurements in the linear regime (V_{ds} = 50 mV) extracted at different doses of gamma irradiation (Presented in (a) logarithmic and (b) linear scales).

subthreshold slope. This is explained by the high influence of the oxide trapped defects over the interface traps due to gamma radiation.

The I-V measurements reveal an important shift in the threshold voltage. V_{th} was extracted from the I_{ds} versus V_{gs} measurement in the linear regime using the extrapolation methods. A strong shift of the threshold voltage ($\Delta V_{Th.}$ = 850 mV) is noticed after irradiation (Fig. 3. a). These degradations are mainly due to the creation of positive charge traps in the gate oxide layer. The threshold voltage is directly dependent on radiation-induced charges Q_{total} as expressed in the following model by [15]:

$$V_{Th} = \Phi_{MS} + 2\,\Phi_f + \frac{\sqrt{2\,q\,\varepsilon_{si}\,N_a\,2\,\Phi_f}}{C_{ox}} - \frac{Q_{total}}{C_{ox}} \tag{1}$$

where q is the electron charge, ε_{si} is the dielectric permittivity of silicon, N_a is the substrate doping, C_{ox} is the gate oxide capacitance per unit area, Φ_{MS} the metal–semiconductor work function difference, Φ_f is the Fermi level potential, and Q_{total} is the total gate oxide charge density per unit area at threshold. The negative shift of the threshold voltage can be expressed by:

$$\Delta V_{Th} = -\frac{Q_{total}}{C_{ox}} \tag{2}$$

In addition to the V_{th} shift, one can clearly observe g_m degradation (Fig. 4.a). The maximum g_m value at V_{ds} = 50 mV decreased by 13% after the applied total dose. This is related to the mobility degradation caused by the additional scattering due to the charged defects created by irradiation. The thermal annealing is applied after the exposure to gamma radiation using the on-membrane micro-heater. Fig. 3.a presents the V_{Th} variations after being exposed to gamma radiation, and Fig. 3.b after each step of 30 s, at different annealing temperatures. Starting from the temperature of 265 °C, the threshold voltage slightly increases after each step, reaching a limit of V_{th} = 1.33 V after 16 annealing steps. Higher annealing temperatures are necessary for the complete recovery. The pre-radiation threshold voltage is recovered after a maximum

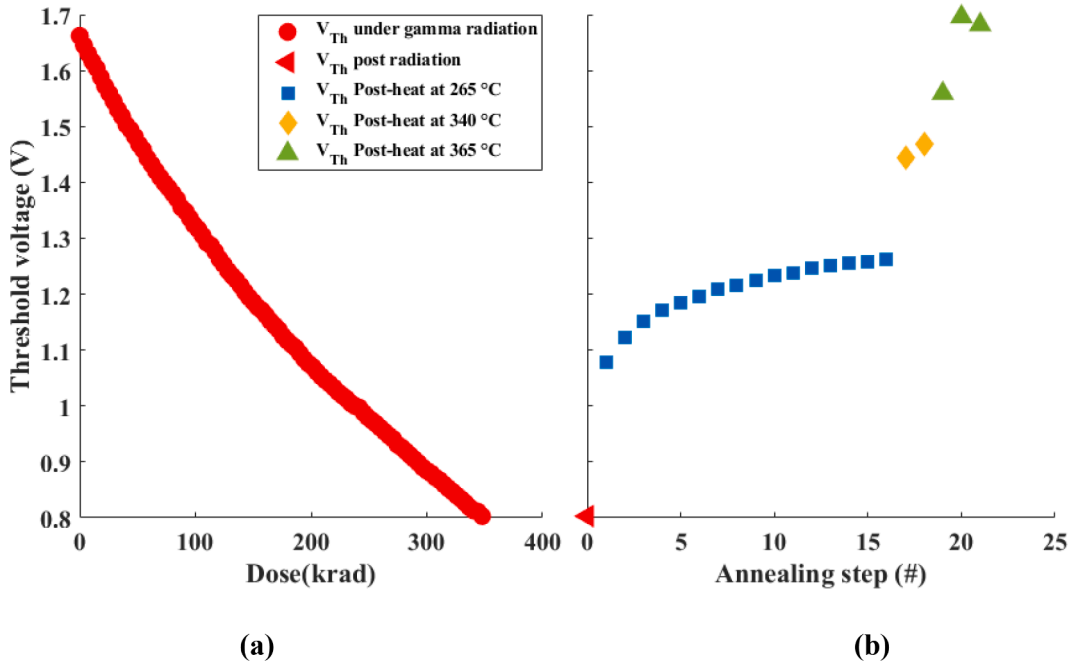

Fig. 3. Threshold voltage of the nMOSFET extracted in linear regime (a) under gamma irradiation with a step of 3.6 krad, (b) after each step of thermal annealing.

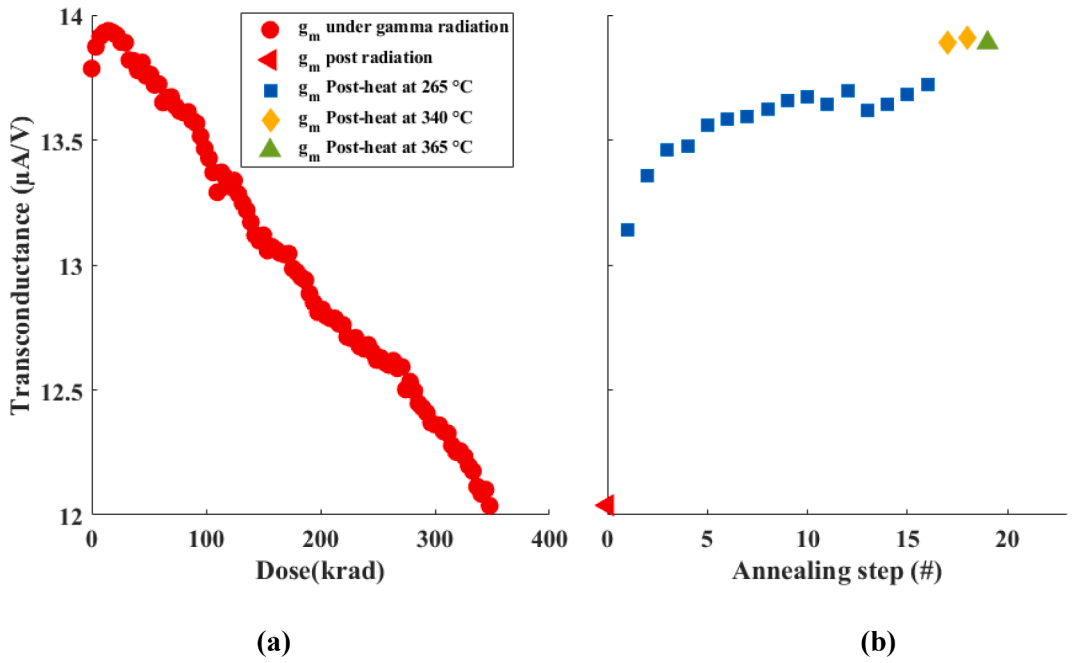

Fig. 4. Maximum transconductance of the nMOSFET extracted in linear regime (a) under gamma irradiation with a step of 3.6 krad, (b) after each step of thermal annealing.

thermal annealing at 365 °C. The evolution of the maximum transconductance (g_m) with thermal annealing is presented in Fig. 4.b, which shows an almost complete recovery at a temperature of 265 °C.

3.2. Low frequency noise measurements

Noise measurements are carried out on the fresh die, after gamma irradiation with the maximum dose, and finally after the thermal annealing. The noise behavior is analyzed in saturation (V_{ds} = 3 V) and at different fixed drain currents of 1nA, 10nA, 100nA, 1 µA, and 10 µA, which allows a comparison of fresh, irradiated, and annealed devices in close conditions of inversion (*i.e.* surface potential or band bending that impacts the interface states).

Fig. 5apresents the noise PSD measured in fresh condition, after radiation and after annealing at a fixed drain current of I_{ds} = 10 µA. After irradiation, a clear Lorentzian-like plateau above 3 Hz and a $1/f^2$ decrease above about 100 Hz are observed. This indicates the dominance of single-trap RTN behavior, as created by the ionizing radiation [13]. The total noise power was integrated at the different drain current levels for a quantitative comparison in each of the three conditions. The minimum roll-off frequency due to the output capacitances is noted at I_{ds} = 1nA with $f_{Roll\text{-}off}$ = 606 Hz. Beyond this frequency, the noise PSD could be influenced by a strong $1/f^2$ effect at the specified current level. For a fair comparison between the current levels, the integration is

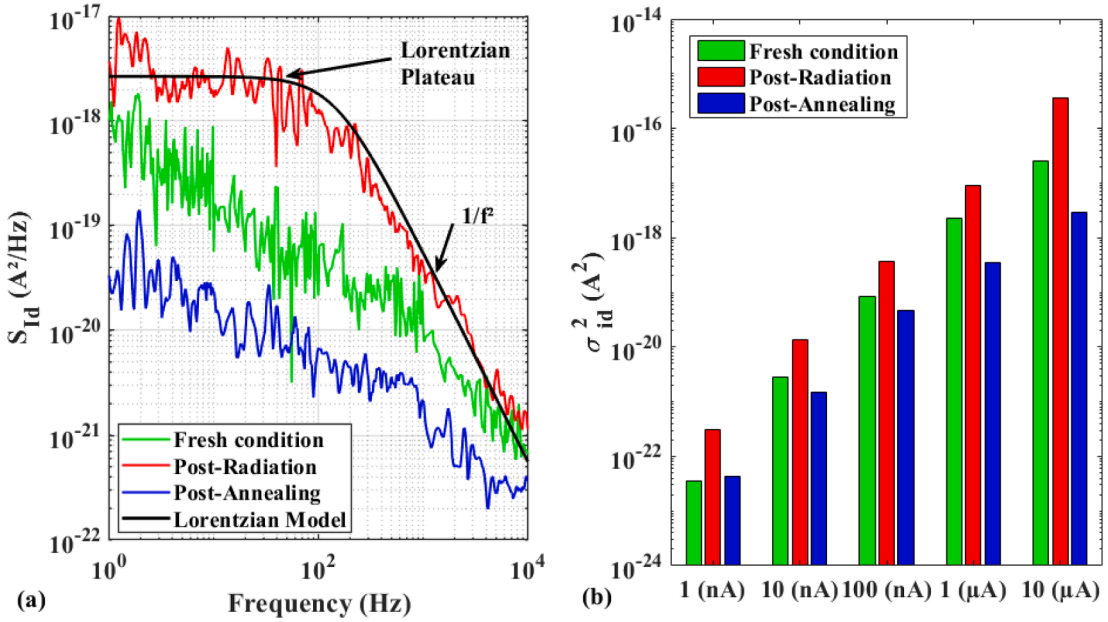

Fig. 5. (a) Power spectral density of noise measurements after radiation measured at a gate voltage overdrive VGO = Vgs -Vth = 220 mV, measured in Fresh condition, after radiation and after annealing. (b)Total power noise at different drain currents (from weak to strong inversion integrated from 1 Hz to 606 Hz).

applied to the frequency range between f_{min} and f_{max} using (Eq. (3)).

$$\sigma_{id}^2 = \int_{f_{min}}^{f_{max}} S_{id}(f)df \quad (3)$$

with f_{min} = 1 Hz and $f_{max} = f_{Roll\text{-}Off}$. The noise power integration is presented using the bar graph method in Fig. 5.b. These experimental measurements show a direct dependence of the total power noise on the applied gate bias. This could be related to the domination of the carrier number fluctuation over the carrier mobility fluctuation as explained in [16]. By increasing the gate bias and hence vertical electrical field, the carrier density increases in the vicinity of the Si/SiO_2 interface. That endorses the dynamic trapping and de-trapping of carriers between the channel and the oxide traps located near the interface [16–18]. After gamma irradiation, an important increase of the total power noise occurred in both weak and strong inversion regions compared to the fresh condition of the die. After thermal annealing, the noise power is remarkably decreased, reaching the lowest noise level.

Current-time measurements (also known as RTN traces) are a complementary noise analysis approach that allows not only for the clear visualization of trap(s) presence, but also for the extraction of parameters that can then be fed into a Lorentzian model. Fig. 6 presents a portion of the RTN traces of fresh, irradiated, and completely annealed (according to I-V, g_m-V curves) MOSFET at a fixed drain current of 10 μA, with V_{ds} = 3 V. No clear RTN behavior is observed in the fresh state except for a few rare current surges, which could be related to DRIE process-induced defects in the BOX layer [19]. After gamma irradiation, a clear RTN behavior dominated by a single trap manifests with current jumps of about ΔIds = 100nA. This is directly due to the creation of positive radiation-induced trapped charges in the oxide layer. The RTN behavior is explained by the electron capture (*i.e.* high current level) and emission (*i.e.* low current level) between the channel and the oxide trap. As can be seen in Fig. 6, after thermal annealing, the RTN behavior totally disappears due to the neutralization of the radiation-induced and DRIE defects in the oxide layers.

The preceding discussion, which is based on a subset of I(t) traces, is supported by the histogram and time lag plot allowing us to visualize and analyze complete sets of records. The histogram of these recorded samples is presented in Fig. 7 for the three cases. After DRIE etching (*i.e.* fresh state), the histogram shows a slightly asymmetric distribution, where low current occurrences are present due to the rare current jumps caused by the process-induced defects. Contrarily, two Gaussian peaks are clearly visible in the histogram after irradiation which indicates the presence of a radiation-induced oxide trap (where each Gaussian corresponds to one charge state of the trap). Furthermore, we notice a quite

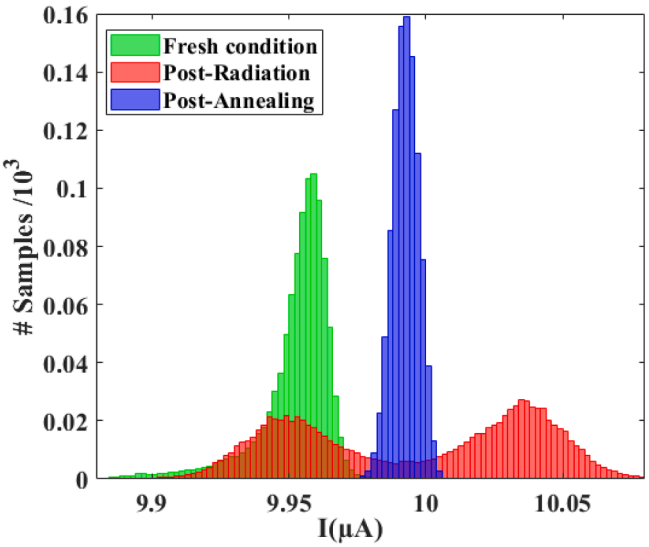

Fig. 7. Histogram presentation of the recorded time trace measurements of drain current measured at fixed I_{ds} = 10 μA and V_{ds} = 3 V.

similar height of the two peaks, which is explained by similar capture and emission time constants (*i.e.* $\tau_c \cong \tau_e$). This indicates that the energetic level of the defect is close to the Fermi level of the channel, with a probability of occupancy close to 0.5 [5]. After thermal annealing, a single Gaussian peak occurred instead of the two Gaussian peaks previously seen after irradiation, thus confirming successful annealing of the radiation-induced oxide trap.

The histogram method provides a good understanding of the RTN signal behavior and a first investigation of the trap's existence [20]. This method provides a precise extraction of the current jump value presented by the distance between the two peaks. Another means of analysis is a lag plot presentation, as shown in Fig. 8.a and (b) for "after gamma irradiation" and "after annealing" cases, respectively. The lag plot representation consists of a color-weighted scatter-plot based on the measured I(t) samples (the same that is used in the histogram presentation). The x- and y-coordinates of each point correspond to two successive drain current steps for instant t and t + 1, respectively. This technique remains more reliable for extracting the parameters in the case of multiple traps, thanks to the larger separation of the peaks in a two-dimensional coordinate system [21]. The color-weighted plot yields the frequency of drain current occurrences, with the yellow and blue

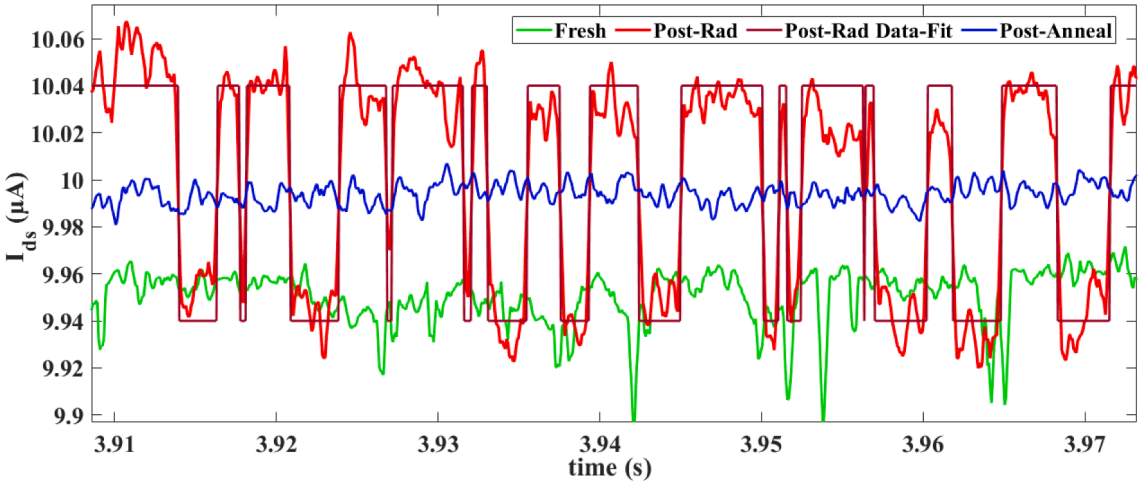

Fig. 6. Fragment of time trace measurements $I_{ds}(t)$ (Pre-post radiation and post annealing at fixed current I_{ds} = 10 μA with V_{ds} = 3 V) measured with a time step Δt ~ 1 μs for 5.3 s.

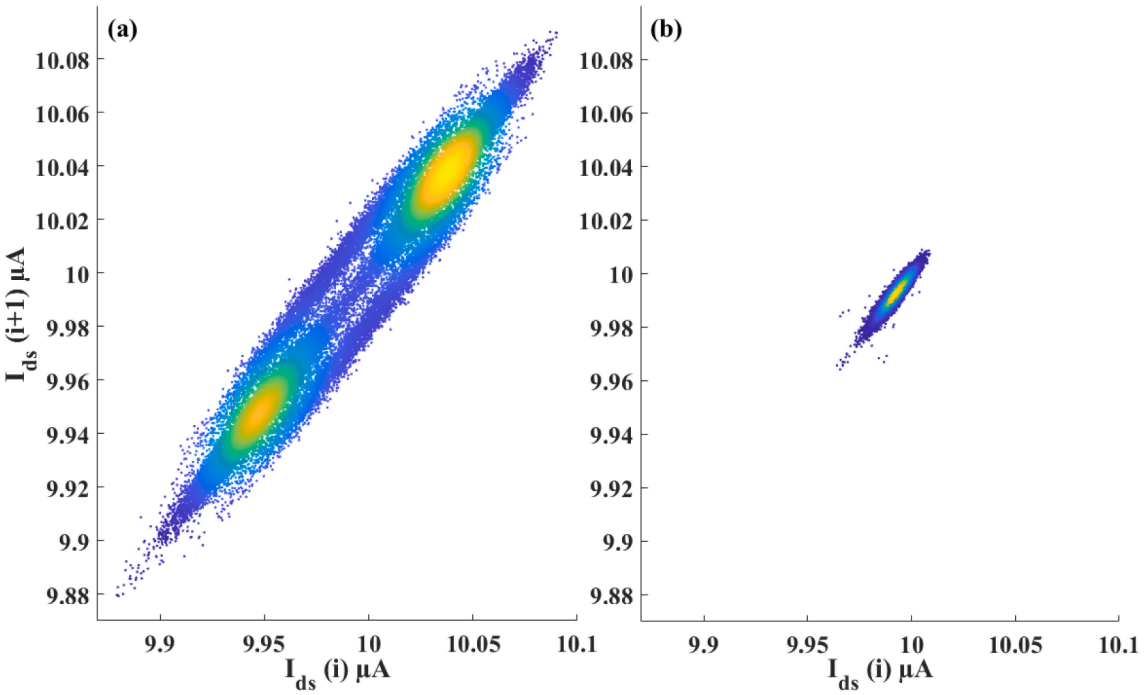

Fig. 8. Lag plot presentation of $I_{ds}(t)$: (a) after irradiation, and (b) post-annealing, measured at fixed $I_{ds} = 10$ µA and $V_{ds} = 3$ V.

colors depicting the highest and lowest frequencies, respectively. Fig. 8. a clearly demonstrates that RTN measurements detect one trap with two current states after gamma irradiation. A cloud of transition states is present around the two main states. After annealing, this behavior totally disappears and the drain current converges towards the expected value of 10 µA.

Noise analysis can be further quantified using the Lorentzian model (Eq. (4)) and by extracting the capture and emission time constants (τ_c and τ_e) from the time trace Id(t) measurements. In order to determine the transition between the capture and emission states, a threshold current value is fixed at ΔI/2 to assign two regions of drain current to the charge states. The emission time τ_e is the average time to emit a trapped carrier, while the capture time τ_c is the average time to capture the carrier (*i.e.* high current level). The distributions of the capture and emission time constants are presented in Fig. 9 (a) and (b), respectively. The exponential distribution around their mean values is represented by the strong lines when using the following model:

$$f\tau(\tau_{c,e}) = \frac{1}{\overline{\tau}_{c,e}} \exp\left(-\frac{\tau_{c,e}}{\overline{\tau}_{c,e}}\right) \tag{4}$$

with $\overline{\tau}_c = 2.01ms$ and $\overline{\tau}_e = 2.42ms$ the mean values of the extracted experimental capture and emission time constants, respectively.

The Lorentzian model is used with the extracted time constants from the time trace measurements at Ids = 10 µA and presented in Fig. 5.a with a solid black line. A fair match between the Lorentzian model and the noise PSD is obtained. This confirms the dominance of the RTN behavior over the flicker noise after gamma irradiation.

$$S_{id,RTN}(f) = \Delta I_d{}^2 \frac{4\tau^2}{\tau_e + \tau_c} \frac{1}{1 + (2\pi f\tau)^2} \tag{5}$$

with ΔI_d is the current level difference between the emission and capture states, and τ is the equivalent time constant.

3.3. Extraction of the trap's position and energy

In order to investigate the properties of the radiation-induced defect, such as e.g. the spatial position of the trap within the gate oxide and its energy E_T, we extend the analysis to another gate bias condition with Ids = 1µA and Vds = 3 V. The noise PSD in fresh conditions is compared to the measurements after gamma irradiation and after the full-recovery

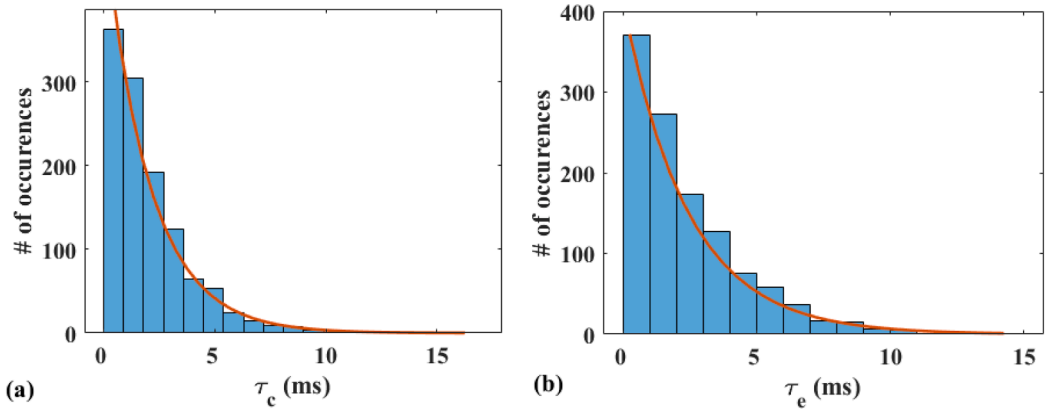

Fig. 9. Time constant distributions of: (a) τ_c and (b) τ_e, extracted from time trace measurements at $I_{ds} = 10$ µA.

annealing as presented in Fig. 10.a. After annealing, the RTN behavior vanishes with a significant decrease in the flicker noise related to the neutralization of the defects caused by both the irradiation and the prior DRIE post-processing. The noise PSD in fresh condition and after annealing shows a substantial $1/f^{\gamma}$ flicker-noise behavior with $\gamma \sim 0.9$ and $\gamma \sim 0.8$, respectively. The non-uniform distribution of the oxide traps near the Si-SiO_2 interface was suggested [22] to cause a slight deviation of the γ factor from the theoretical unity value, yielding typical values in a range between 0.8 and 1.2 [23–24]. According to [25], a trap distribution skew towards the SiO_2 interface yields higher frequency traps, thus causing $\gamma < 1$. However, when a trap distribution skews away from the interface, a greater number of low-frequency traps takes place and leads to $\gamma > 1$ [25]." Fig. 10.b presents the histogram of the RTN measurements, at the same bias conditions. Similar behavior of the time trace measurements is noted in the fresh state and after annealing when compared to histogram presentations at Ids = 10μA (Fig. 7). However, a different behavior is noticed after gamma irradiation, where two clear current states are present but with a higher occupation frequency of one state than the other. This behavior is due to an important difference between the capture and emission times of the trap.

The capture/emission time constants of the RTN measurements are extracted with the same methodology used previously. These RTN traces show different asymmetric behavior where $\overline{\tau}_c = 8.5ms$ and $\overline{\tau}_e = 0.6ms$. Fig. 11 (a) and (b) present the dependence of $\overline{\tau}_c$, $\overline{\tau}_e$ and their $\overline{\tau}_c/\overline{\tau}_e$ ratio on V_{gs}, respectively, for the two analyzed current levels.

The decrease in $\overline{\tau}_c/\overline{\tau}_e$ ratio with V_{gs} indicates that the capture and emission levels of the RTN traces are due to the carrier exchanges between the channel and the oxide trap [26]. The spatial localization of the defect is extracted using the following model [26–27]:

$$X_T = -Tox\,\frac{kT}{q}\,\frac{d(\ln(\tau_c/\tau_e))}{dV_{gs}} \tag{6}$$

with X_T the trap depth in the silicon dioxide layer with respect to the Si-SiO_2 interface, and k is the Boltzmann constant. The radiation-induced trap is estimated to be located at 5.4 nm from the Si-SiO_2 interface. The cross point between τ_e-V_{gs} and τ_c - V_{gs} curves corresponds to the conditions where the trap energy aligns with the Fermi level. This condition is defined here by V_{g0} and τ_0 values. The trap energy at zero electric field condition E_{T0} is 0.086 eV, calculated with respect to the Fermi level using the following equation [26]:

$$E_{T0} - E_F = q\left(V_{g0} + V_0\right)\frac{X_T}{T_{ox}} \tag{7}$$

with $V_0 = -V_{FB} - \Phi_S$, where V_{FB} is flat-band voltage and Φ_S the surface potential. In the strong inversion, the surface potential is estimated by the following equation as usual:

$$\Phi_s = 2\Phi_F = 2k_B T\ln(\frac{N_A}{n_i}) \tag{8}$$

The flat-band voltage is estimated to be 0.92 V using equation (1):

$$V_{FB} = V_{Th} - \Phi_s - \frac{\sqrt{2\epsilon_{si}qN_a}}{C_{ox}}\sqrt{\Phi_s} \tag{9}$$

4. Conclusion

This work studies the benefits of in-situ thermal annealing to recover nMOSFET I-V characteristics after strong gamma irradiation. Significant degradations of the threshold voltage and transconductance are observed. These are cause by the creation of positive charges in the BOX and gate-oxide layers. Following gamma irradiation, the electrical characteristics are investigated after different in-situ annealing temperatures. A total recovery of the initial characteristics has been achieved in the nMOS transistor with a maximum heating temperature of 365 °C. Low-frequency noise measurements are performed in fresh conditions, after gamma irradiation, and after thermal annealing. A clear RTN signal is measured after gamma irradiation, confirming the creation of oxide defects at the gate-oxide layer. A Lorentzian model is used to further analyze the RTN behavior. The trap parameters are extracted from the time trace measurements at two different gate biases. The decrease in the $\overline{\tau}_c/\overline{\tau}_e$ ratio confirms that the observed RTN behavior after irradiation is due to carrier exchange between the trap and the channel. The radiation-induced trap is estimated to be localized at 5.4 nm from the Si-SiO2 interface, with an energy of 0.086 (eV) from the Fermi level in the band-gap. After in-situ thermal annealing, the pre-radiation characteristics of the MOS device are recovered. The RTN behavior and the Lorentzian-like plateau disappeared, with a further remarkable decrease in the flicker noise.

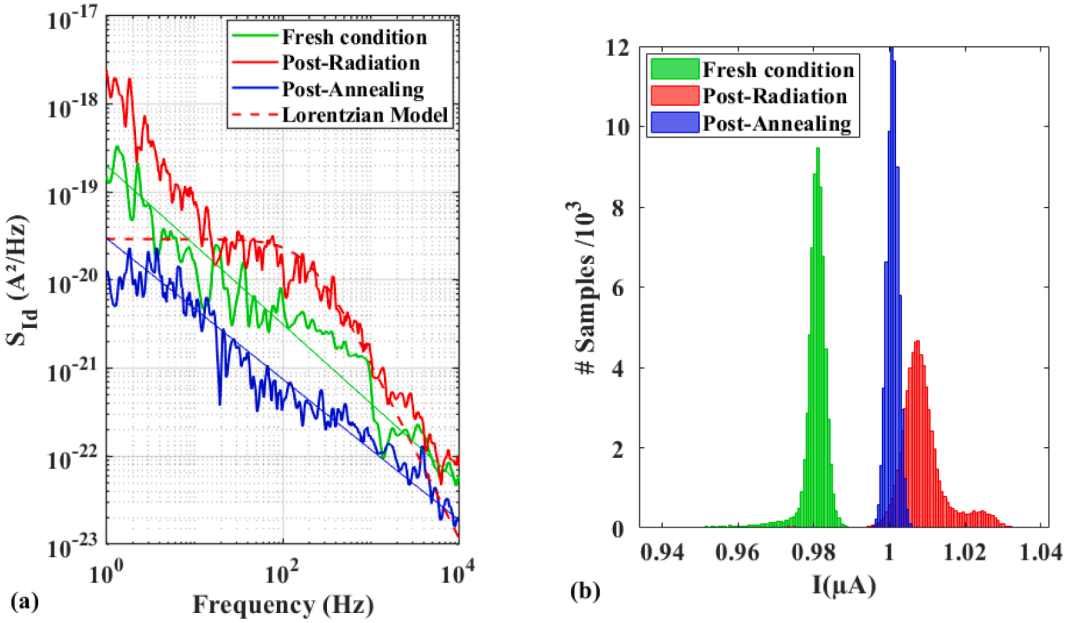

Fig. 10. (a) Power spectral density of noise measurements before radiation, after radiation and after thermal annealing (measured in the saturation regime at Ids = 1 μA and Vds = 3 V). (b) Histogram presentation of the recorded time trace measurements of drain current measured at the same bias conditions.

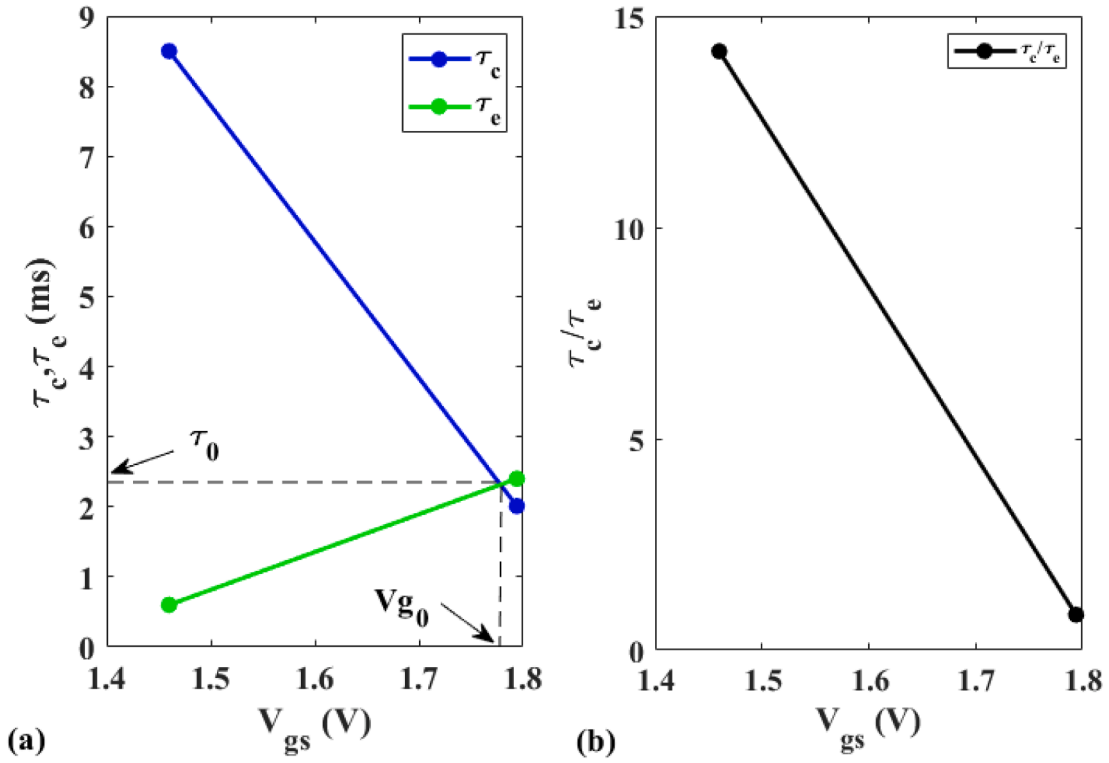

Fig. 11. (a) Time constants and (b) $\overline{\tau}_c/\overline{\tau}_e$ ratio dependences on V_{gs} extracted from time trace measurements at Ids1 = 1 μA and Ids2 = 10 μA.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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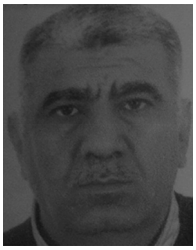

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