# Process-based Life Cycle Assessment of a Vanadium Dioxide spiking neuron

Noémie Bidoul
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Pauline Raux
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Tom Van Aerschot
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Alex Pip
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Christian Renaux
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Sébastien Faniel
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Denis Flandre
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

Jean-Pierre Raskin
*ICTEAM, UCLouvain*
Louvain-la-Neuve, Belgium

***Abstract*—Artificial spiking neurons are one of the building blocks of neuromorphic systems. Such type of hardware is often promised to offer energy-efficient platforms to run Deep Learning algorithms on large datasets. These systems require large numbers of neuronal primitives, raising the question of the environmental footprint of their fabrication. In this work, we propose to address this matter by performing a cradle-to-gate Life Cycle Assessment (LCA) of an artificial neuron based on Vanadium Dioxide, fabricated in a lab-scale fab. We focus on the Cumulated Energy Demand (CED), Global Warming Potential (GWP) and Ultra Pure Water consumption (UPW) metrics. We identify the use of gold for the electrical contacts (the dominant practice in the fabrication of such devices) as the critical step, representing respectively 38 % and 49 % of the total CED and GWP associated to the device fabrication. We further explore the validity of this result by varying key parameters in different scenarios. In an eco-design approach, we propose the replacement of gold by aluminium as a way to curb the total process CED and GWP by respectively 25 % and 43 %, and show first evidence that the device electrical properties are preserved in this case. Finally, we provide a first attempt at comparing the direct environmental footprint and performance of $VO_2$ neuron with CMOS-based implementations.**

***Index Terms*—Life Cycle Assessment (LCA), cradle-to-gate, eco-design, spiking neuron, Vanadium Dioxide, neuromorphic device**

## I. Introduction

Artificial neurons are electronic devices able to emulate the spiking behavior of biological neurons. They form the elementary units of bio-inspired, so called neuromorphic hardware, akin to transistors in conventional Von Neumann processor architectures. Neuromorphic systems are often put forwards as platforms which would allow to run Deep Learning algorithms at lower energy costs, some claiming they could help achieve "Green AI" [1], [2]. These platforms can be implemented using neurons based on CMOS technology [3]–[6], or on new materials with resistive switching properties [7], [8]. Vanadium Dioxide ($VO_2$) is one of such materials, allowing to design artificial neurons that can be referred to as volatile memristors, thanks to their ability to transition from a high to low resistive state in a reversible way [9]–[11]. While several works have been conducted on Life Cycle Assessments (LCAs) of the fabrication process of CMOS technology nodes [12]–[16], there has so far been no research on the environmental cost of fabricating emerging neuromorphic devices. In regard of scenarios in which memristive devices would be used as hardware primitives in new generations of processors, quantifying this impact is relevant, as these systems can contain up to millions of neurons [17]. It is also recognized that performing LCA on technologies with low Technology Readiness Levels (TRLs) allows to reorient design choices to minimize the product environmental footprint prior its market penetration, at which point changes in the process flow would come at higher costs [18]. This work proposes a first attempt in this direction by performing a cradle-to-gate LCA of the fabrication process of a memristor based on $VO_2$, whose functionalities are described in [19]. The LCA goal, scope, and methodology to perform the inventory analysis and impact assessment are detailed in Section II. We focus on the Cumulated Energy Demand (CED), Global Warming Potential (GWP) and Ultra Pure Water consumption (UPW) metrics. The life-cycle impact assessment results are presented in Section III, and allow to identify the process steps that significantly contribute to the different impact categories. The robustness of our conclusions w.r.t. variations of certain parameters is analyzed in Section IV-A. An alternative design route to reduce the total CED of the process is discussed in Section IV-B. Finally, in Section IV-C, the $VO_2$ memristor direct environmental footprint and performances are compared to CMOS-based implementations.

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## II. LCA methodology

### A. Goal and scope

The goal of this LCA is to identify the largest contributors among the different process steps in terms of CED, GWP and UPW consumption, and to investigate alternatives to these process steps to propose eco-design guidelines and reduce the direct environmental footprint associated to the device fabrication. This analysis is aimed at nanotechnology researchers and designers eager to make design choices minimizing the direct footprint or their fabricated device, at the upfront of its development. Results are expressed with respect to a functional unit corresponding to a 3-inch silicon wafer (45.6 cm² surface) on which the memristive devices are fabricated. Our model follows an attributional approach, as recommended in [20] given the context of our work.

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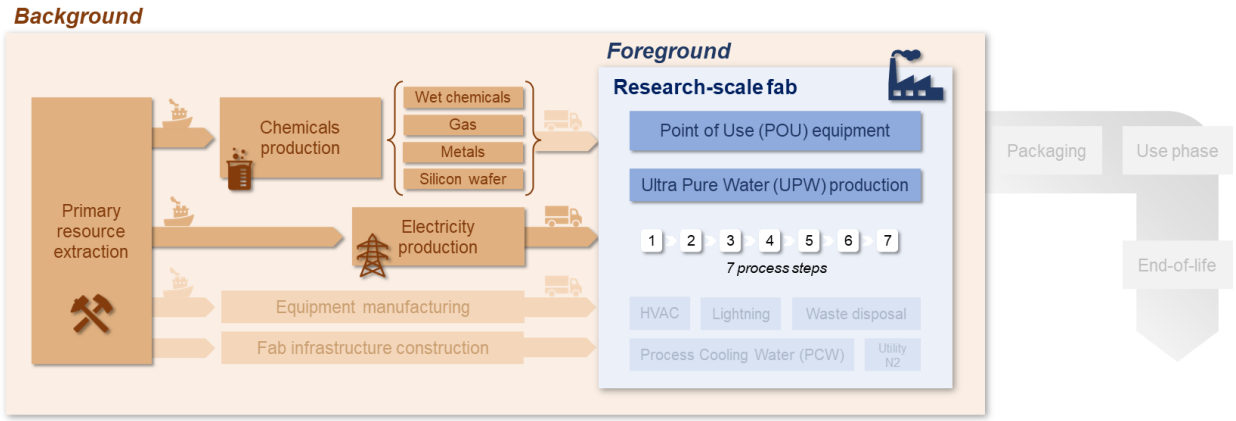


Fig. 1. LCA scope and system boundaries, with distinction between the background and foreground systems. Lighter items are not included in the scope.

The LCA system boundaries are presented in Fig. 1, and correspond to a cradle-to-gate scope which can be divided into the background and foreground systems. The background system includes the manufacturing of upstreams chemicals required for the process (wet chemicals, gas, metals), as well as the the silicon wafer production. This includes extraction of raw materials and transformation processes, but excludes transport of the input products to the fab gate, due to lack of accurate provenance data from suppliers. The foreground system includes on-site processes taking place within the fab, such as the electricity consumption of process tools, point-of-use (POU) equipment and UPW production utilities, quantified for each of the seven process steps. We exclude environmental impacts that can be attributed to the whole fab facility, such as the equipment manufacturing, the construction of the fab, and the electrical consumption of certain utilities (Heating – Ventilation and Air Conditioning or HVAC, lightning, waste disposal and process cooling water). Indeed, the memristive devices studied in this work are fabricated in a research-scale fab where a large number of different fabrication processes are conducted, making it difficult to allocate those environmental impacts in a meaningful way. In addition, in the eco-design approach followed in this work, such impacts are considered as fixed as they currently cannot be optimized to reduce the device direct footprint. The packaging, use phase and end-of-life stages are also neglected: due to the low TRL of the device and associated uncertainty regarding its specific application, the data required to evaluate these stages of the life cycle are yet unknown.

### *B. Inventory*

The fabrication process of the $VO_2$ memristor is detailed in Fig. 2, and is composed of seven steps: (1) standard cleaning of the silicon wafer, (2) thermal oxidation to create an 200 nm - thick electrically insulating $SiO_2$ layer, (3) DC reactive sputtering of a 135 nm - thick amorphous $VO_2$ thin film from a vanadium target, (4) thermal annealing to trigger its crystallization, (5) lithography, (6) evaporation of a 150 nm - thick gold layer (together with a thin 5 nm nickel adhesion layer) and (7) liftoff to define the electrical contacts. The inventory is completed in a bottom-up, process-based approach using data gathered directly within the fab, offering precision and a granularity at the process step level. Quantities of wet chemicals and UPW (used in the standard cleaning, photolithography and liftoff steps) are directly measured, while quantities of gas (used in the thermal oxidation, sputtering, and annealing steps) are extracted from the recipes detailed on the equipment control programs. The exact quantities of metals are either deduced through weighting metallic crucibles before and after the deposition (for gold and nickel), or by estimations based on sputtering chamber volume and film thickness (as for vanadium). Electrical consumption of equipment used in the different process steps are deduced from the rated power indicated on their datasheets, as well as their operation time (excluding stand-by operation). The inventory considers one run of each process step, for which each equipment has a different loading factor (i.e. number of wafers processed simultaneously), which is taken into account into the normalization towards the functional unit. The inventory is detailed for each process steps in Table I.

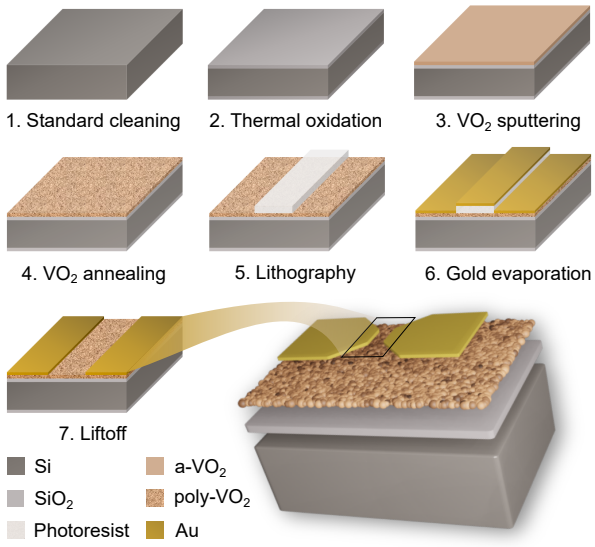


Fig. 2. Process flow of the $VO_2$ memristor microfabrication.

TABLE I
DETAILED INVENTORY

| | | Wafer fabrication | Standard cleaning | Thermal oxidation | VO2 sputtering | VO2 annealing | Lithography | Gold evaporation | Liftoff | |
|---|---|---|---|---|---|---|---|---|---|---|
| Equipment load | (# wafers) | 1 | 25 | 25 | 1 | 30 | 10 | 4 | 2 | |
| ***Gas*** | | | | | | | | | | |
| Ar | (g/wafer) | | | | 2.18E+00 | 2.68E-01 | | | | † |
| H2 | (g/wafer) | | | 1.48E+00 | | | | | | † |
| O2 | (g/wafer) | | | 2.58E+01 | 2.47E-01 | | | | | † |
| N2 | (g/wafer) | | | 3.18E+01 | | | | | | † |
| ***Wet chemicals*** | | | | | | | | | | |
| H2SO4 | (g/wafer) | | 1.27E+02 | | | | | | | † |
| H2O2 | (g/wafer) | | 1.19E+01 | | | | | | | † |
| HF | (g/wafer) | | 7.96E-01 | | | | | | | † |
| HMDS | (g/wafer) | | | | | | 9.68E-01 | | | † |
| Acetone | (g/wafer) | | | | | | 1.58E+01 | | 2.38E+01 | † |
| Methanol | (g/wafer) | | | | | | 1.59E+01 | | | † |
| Isopropanol | (g/wafer) | | | | | | | | 2.36E+01 | † |
| DMSO | (g/wafer) | | | | | | | | 7.70E+02 | † |
| PGMEA | (g/wafer) | | | | | | 1.62E+00 | | | ⋆ |
| TMAH | (g/wafer) | | | | | | 2.02E-01 | | | ⋆ |
| ***Metals*** | | | | | | | | | | |
| V | (g/wafer) | | | | 1.87E-01 | | | | | ◇ |
| Au | (g/wafer) | | | | | | | 2.76E-01 | | ◇ |
| Ni | (g/wafer) | | | | | | | 9.19E-03 | | ◇ |
| ***Others*** | | | | | | | | | | |
| Silicon wafer | (m²) | 4.56E-03 | | | | | | | | † |
| Ultra Pure Water | (l/wafer) | | 8.00E+00 | | | | 1.63E-01 | | 6.43E+00 | |
| ***Electricity*** | | | | | | | | | | |
| POU equipments | (kWh/wafer) | | 2.63E-02 | 2.59E+00 | 9.81E-01 | 2.43E-01 | 1.97E+00 | 3.03E+00 | 5.42E-02 | ○ |
| UPW production | (kWh/wafer) | | 3.14E-01 | | | | 6.38E-03 | | 2.52E-01 | ○ |

***Sources of CED and GWP data for Impact Assessment :*** † *Ecoinvent v3.10,* ⋆ *Boyd [13],* ◇ *Nuss & Eckelmans [21],* ○ *PEF and carbon intensity values from IEA [22][23]*

### C. Impact Assessment

For the majority of chemicals used in the process, the CED and GWP associated to their manufacturing (background data) are gathered from the *EcoInvent* database *v3.10* with cutoff system model, respectively from the Cumulated Energy Demand and EF v3.0 LCIA methods. Exceptions include wet chemicals such as PGMEA and TMAH (found respectively in the composition of photoresist and developer used during lithography), for which CED and GWP values of 3.1 MJ/kg and 0.26 kg$CO_2$-Eq/kg were used based on S. Boyd's work [13]. Since *Ecoinvent* also lacks data for certain metals, we turn to Nuss & Eckelmans's work for CED and GWP values associated to the production of nickel, gold and vanadium [21]. It is noteworthy that these values are possibly underestimates of reality, as metals used in semiconductor fabrication processes such as those considered in this work are of very high purity, while Nuss & Eckelmans do not specify purity levels. All three data sources follow an attributional approach. To compute the equivalent CED and GWP associated to the production of electricity consumed by POU equipment and UPW utilities, we use respectively a Primary Energy Factor (PEF) for electricity of 2.77 [22] and a carbon intensity for electricity of 145 g$CO_2$-Eq/kWh [23], two values estimated by the International Energy Agency (IEA) considering the Belgian electricity production mix. UPW consumption is directly measured on site.

## III. RESULTS

The contribution of each individual process step to the total CED (expressed in MJ) and GWP (expressed in kg$CO_2$-Eq) associated to the fabrication of one wafer of memristors is detailed in Fig. 3. For both impact categories, gold evaporation stands out as the most intensive step. This is largely due to the extraction and manufacturing of gold, which represents the major part of this specific step footprint (65.51 % of its CED and 88.69 % of its GWP). The large energy and carbon intensity of gold production is generally attributed to its relatively low abundance in the earth crust [24], and to the large energy requirements and emissions of some of its refining steps, such as grinding and post-roasting gas treatments [25]. Regarding the overall memristor fabrication process, the CED

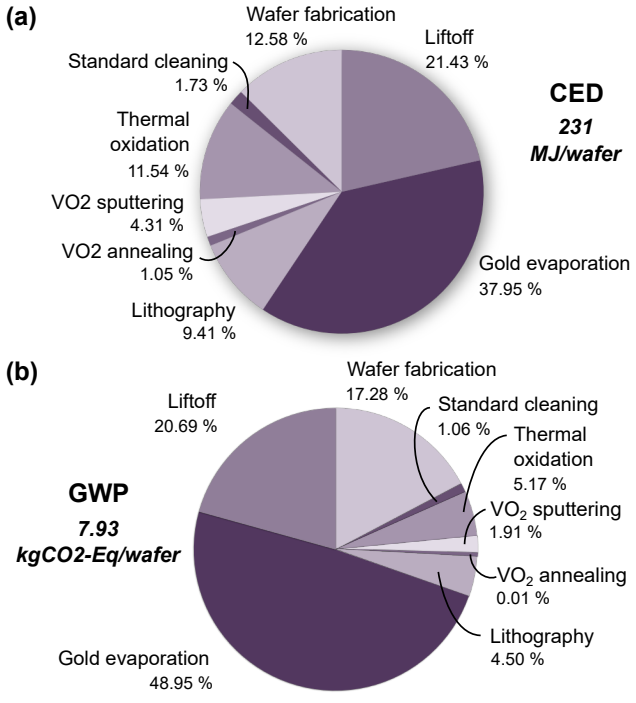


Fig. 3. LCA results regarding (a) the total CED and (b) GWP associated to the production of one wafer of memristive devices, with detailed contributions of individual process steps.

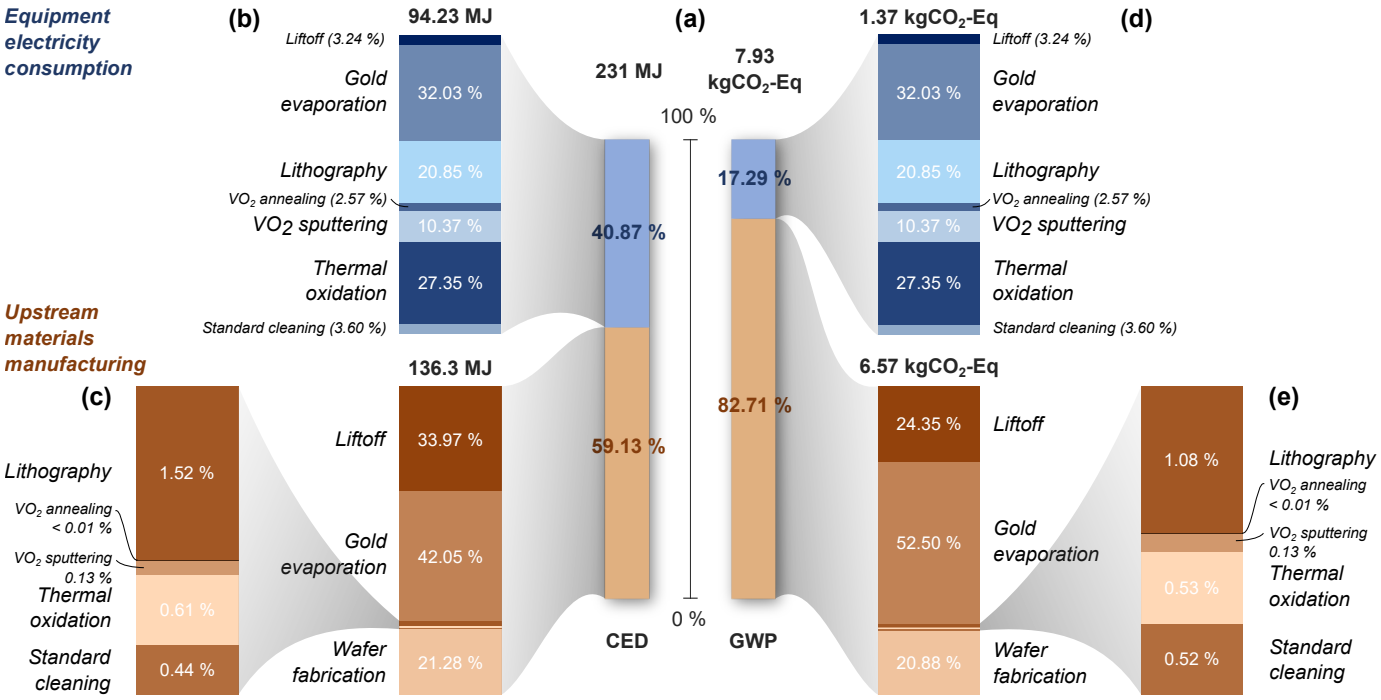


Fig. 4. (a) Decomposition of the total CED and GWP associated to the production of one wafer of memristive devices, by making the distinction between the electrical consumption of equipment within the fab gates (blue) and the manufacturing of upstream materials (orange). In each case, contribution of individual process steps is detailed for CED (b,c) and GWP (d,e).

and GWP impact categories are dominated by the manufacturing of the upstream materials. This trend is highlighted in Fig. 4, where the distinction is made between the contribution of the upstreams material manufacturing and the equipment electricity consumption. The top three globally most intensive steps (Fig. 3) are also the top three contributors of the total CED/GWP associated to upstream materials manufacturing. Following gold evaporation, the second and third most intensive steps are the liftoff and wafer fabrication. Liftoff requires dimethyl sulfoxide (DMSO, a solvent allowing to dissolve the photoresist). Its manufacturing is associated to quite standard CED/GWP values compared to other inputs of the process, but it is used in large quantities (see Table I) to avoid gold particles attaching onto the samples. The fabrication of monocrystalline silicon wafers typically involves low-yield, energy-intensive steps such as the transformation of trichlorosilane into polysillicon, the crystallization of polysilicon and the sawing of ingots into wafers [26]. Regarding the remaining steps, the dominant contribution to the CED/GWP are associated to the production of electricity required by the process tools and POU equipment. The thermal oxidation involves a high temperature furnace (1000 °C) with 17 kW rated power running for almost 4 hours. The lithography step requires a UV lamp consuming up to 2.6 kW, and the gold evaporation step requires pumping a large-volume chamber to low pressure during several hours, further adding to the contribution of the this step. Finally, the consumption of Ultra Pure Water (UPW) in the different process steps is shown in Fig. 5. Only three steps consume UPW: lithography, standard cleaning and liftoff. Standard cleaning and liftoff consume the largest amount of UPW, as large quantities of water are required to rinse remains of acids between cleaning baths during standard cleaning, and remove solvent, resist and gold particles during liftoff.

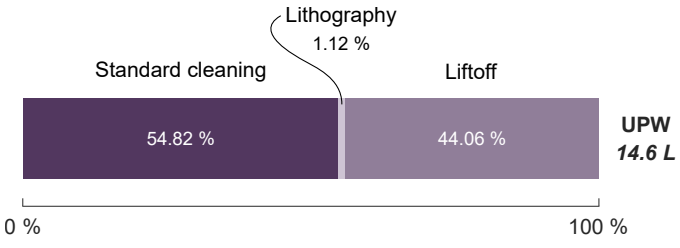


Fig. 5. Decomposition of UPW consumption among the different process steps, for the fabrication of one wafer of memristors.

## IV. Discussion

### A. Uncertainty & scenario analysis

To test the reliability of our conclusions, we discuss uncertainty and vary the value of certain key parameters in different scenarios. A first factor adding uncertainty is the method used to estimate the electricity consumption of the process steps equipment, which likely yields overestimation. Indeed, this consumption was extracted based on datasheet rated power values rather than actual measured instantaneous power consumption. To get insight on the impact of this hypothesis, we performed such measurements during the thermal oxidation step using a power-energy logger. We obtain a capacity factor (actual electricity consumption over rated consumption) of 0.23, confirming our hypothesis of overestimation. Applying such capacity factor uniformly to the electricity consumption

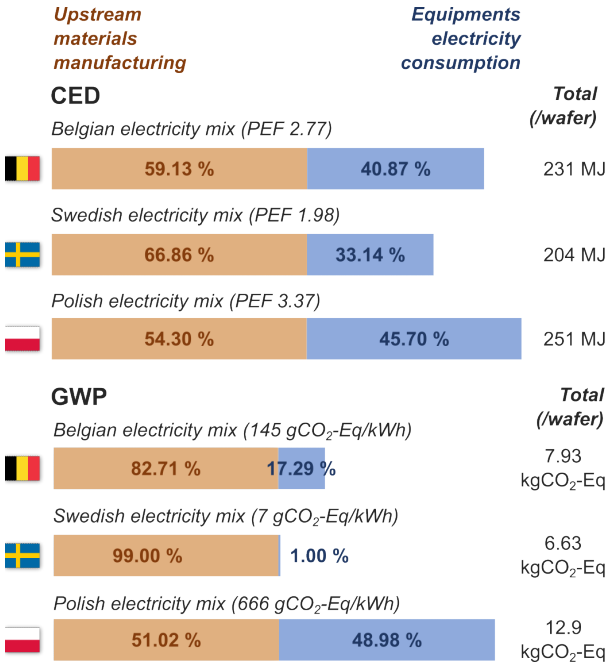


Fig. 6. Evolution of the relative contribution of the upstream materials manufacturing (orange) and the equipment electricity consumption (blue) to the total process CED and GWP, considering different electricity production mixes.

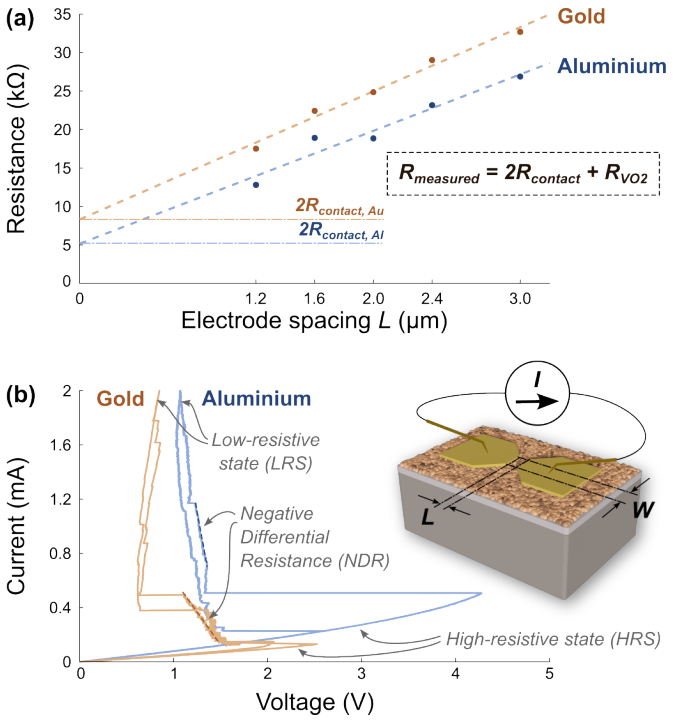


Fig. 7. Comparison of the electrical characteristics of $VO_2$ memristors fabricated with gold (orange) and aluminium (blue) electrical contacts: (a) extraction of the device contact resistance through the transfer length method (TLM), at T = 35 °C (the $VO_2$ film being in its high-resistive state) (b) current-driven I-V characteristic of two memristors of identical dimensions (L = 1.2 μm, W = 15 um). Inset shows the measurement configuration and the dimension notations (since the $VO_2$ layer is not patterned, device dimensions are defined by electrode dimensions).

of all equipment would reduce to total CED and GWP associated to wafer fabrication by respectively 29.87 % and 12.48 %, and reduce the contribution of equipment electricity consumption to 16.05 % and 5.47 % (without affecting the order of the top three contributing steps). Moreover, the energy and carbon intensity of TMAH and PGMEA extracted from S. Boyd's work [13] also carry high uncertainty (from -75 % to +25 %), as they were obtained through Economic Input-Output (EIO) LCA considering different markets than those associated to the semiconductor industry [27]. However, since these two chemicals are used in very small volumes (see Table I), such variations would have a marginal effect on the total CED and GWP of the lithography step, and wouldn't change the ranking of this step in the top contributors. Finally, we consider how the contribution of the equipment electricity consumption to the total process CED and GWP would evolve in different scenarios of electricity production mixes (see Fig. 6). In the case of Sweden, which has a less energy and carbon intensive mix, this contribution would be reduced to 33.14 % and 1 % of the total process CED and GWP, but the top three most intensive steps would remain identical. In the case of Poland, which has a more energy intensive and carbonated mix, the contribution of the equipment consumption would almost equal that of the materials manufacturing. The thermal oxidation step would climb to the third most intensive step (above wafer fabrication), due to the furnace high electricity demand. All things considered, in each of the considered scenarios, the gold evaporation step remains the most intensive in terms of CED and GWP.

### B. *Eco-design perspectives*

There is now clear evidence that the dominant contribution to the CED and GWP associated to the $VO_2$ memristors fabrication process is related to the use of gold for their electrical contacts. Gold and noble metals in general (which have similarly high CED and GWP) are often preferred to contact memristors based on materials such as Vanadium Dioxide [28], due to their low resistivity and to the fact that they do not oxidize over time or at high temperatures. Indeed, during its transition from high-resistive state (HRS) to low-resistive state (LRS), a $VO_2$ memristor can reach significantly high temperatures [29]. However, alternative to noble metals for contacts have barely been investigated so far. Among materials with small energy- and carbon-intensive manufacturing, one finds aluminium, with an energy and carbon intensity of respectively 131 MJ/kg and 8.2 $kgCO_2$-Eq/kg (w.r.t. 208 000 MJ/kg and 12500 $kgCO_2$-Eq/kg for gold [21]). Considering a constant deposited mass, replacing gold contacts by aluminium ones in the fabrication process studied in this work would result in a decrease of the total process CED and GWP by respectively 25.11 % and 43.38 %, down to 173 MJ/wafer and 4.49 $kgCO_2$-Eq/wafer. In addition, aluminium - on the opposite of gold - is a CMOS compatible material, which would be desirable in the case of CMOS integration of $VO_2$ devices. To test if such design choice would impact the

TABLE II
COMPARISON BETWEEN CMOS- AND $VO_2$-BASED SPIKING NEURON IMPLENTATIONS

| Reference | (1) Technology node | (2) CED/cm² (MJ) | (3) GWP/cm² (kgCO2-Eq) | (4) Die area for one neuron (cm²) | (5) Active area for one neuron (µm²) | (6) CED/die (MJ) | (7) GWP/die (kgCO2-Eq) | (8) CED/neuron (MJ) | (9) GWP/neuron (kgCO2-Eq) | (10) Energy efficiency | (11) Static energy consumption |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Indiveri 2006 [3] | CMOS 350 nm | 6.89E+01 | 6.90E+00 | / | 2.57E+03 | / | / | 1.77E-03 | 1.77E-04 | 900 pJ/spike | / |
| Cruz-Albrecht 2012 [4] | CMOS 90 nm | 4.21E+01 | 3.79E+00 | / | 4.42E+02 | / | / | 1.86E-04 | 1.67E-05 | 0.4 pJ/spike | 40 pW |
| Sourikopoulos 2017 [5] | CMOS 65 nm | 4.64E+01 | 4.43E+00 | 1.13E-03 | 3.50E+01 | 5.22E-02 | 4.98E-03 | 1.63E-05 | 1.55E-06 | 4 fJ/spike | 100 pW |
| Nalliboyina 2024 [6] | CMOS 45 nm | 5.36E+01 | 4.46E+00 | / | 4.17E+01 | / | / | 2.23E-05 | 1.86E-06 | 1.32 fJ/spike | 23 pW |
| This work | $VO_2$ | 5.07E+00 | 1.74E-01 | 6.60E-04 | 2.40E+00 | 3.34E-03 | 1.15E-04 | 1.22E-07 | 4.17E-09 | 151 nJ/spike | 2.6 mW |
| Yuan 2022 [9] | $VO_2$ | / | / | / | 4.00E-01 | / | / | | | 2.9 nJ/spike | 5 mW |
| Han 2022 [10] | $VO_2$ | / | / | / | 1.96E+01 | / | / | | | 3 nJ/spike | 100 µW |
| Yi 2018 [11] | $VO_2$ | / | / | / | 3.00E+00 | / | / | | | 100 fJ/spike† | 11 µW† |

† *simulated*

device performances, we fabricated two batches of memristors wafers with identical process parameters, only differing by their contact material (gold or aluminium). Their electrical characteristics are shown in Fig. 7. The contact resistance of the memristive devices was extracted using the transfer length method (TLM), in which the resistances of devices with identical electrode dimensions but varying electrode spacing $L$ are measured. Extrapolating towards zero electrode spacing yields an estimation for the contact resistance. The study shows that despite the fact that aluminium typically has a higher resistivity than gold, the devices with aluminium contacts present smaller contact resistances. This difference could be attributed to the resistance of the metal/semiconductor junction itself, and/or to additional phenomena taking place at the Al/$VO_2$ interface, such as diffusion of aluminium ions into the $VO_2$. Fig. 7b shows that the resistive switching properties are preserved for both types of device: a reversible transition between a high-resistive state and a low-resistive state takes place. Both types of devices present a region of negative-differential resistance (NDR), a necessary condition for the devices to exhibit spiking neuromorphic behavior [30].

### C. Comparison with CMOS-based neuron

Beyond eco-design concerns, one could ask whether the fabrication of $VO_2$ neurons has a larger direct environmental footprint than that of CMOS technologies. Since $VO_2$ neurons are still at low TRL, characteristics of the functional unit required to make a comparison with a CMOS conventional processor (density, yield, number of devices needed to reach equivalent functionalities) are not yet known. To overcome this, we propose to remain in the neuromorphic domain and at device level. Table II compares CMOS implementations of spiking neurons to the $VO_2$ device along 11 criteria. CED and GWP values associated to the CMOS nodes fabrication (with similar scope than ours) [13] must be taken with caution, as large variability exists between distinct LCAs of CMOS processes [15]. Energy and power consumptions of the $VO_2$ neuron have been extracted from our previous work [19]: the neuron dimensions are slightly different from those of the device measured in Fig. 7, but the fabrication process is identical. A first conclusion is that the CED and GWP values associated to the fabrication of the $VO_2$ technology (normalized for 1 cm²) seems to be one order of magnitude below those of CMOS implementations (criteria 2, 3). Indeed, CMOS process flows involve larger numbers of steps (up to 206 for a processor in 130 nm node [12]). In particular, CVD deposition and dry etching steps, which are not present in our process, involve emissions of GHG such as fluorinated gases and $N_2O$ (data exclude abatement). These steps also have large electricity consumption. However, another subsequent part of the electricity consumption of CMOS processes is attributed to the fab infrastructure, which is not included in our study. In addition, it is hard to predict how the footprint of the $VO_2$ fabrication process would evolve with industrialization: equipment loading factors could be optimized (in our case, very few wafers are processed simultaneously during evaporation and sputtering steps), quantities of certain chemicals could increase (larger quantities of acids and UPW per cm² wafer are typically used in industrial cleaning steps in order to increase yield [12]). The area associated to a single neuron also differs (see criteria 4, 5): a smaller die and active area attributed to $VO_2$, since it only requires a single device, yielding even smaller footprint per die and per neuron (criteria 6-9). Finally, the dynamic and static energy consumptions of CMOS-based neurons (criteria 10, 11) are still far below those of $VO_2$ neurons, showing that optimization is still required for the latter to become energy-competitive during in their use phase.

## V. CONCLUSION AND PERSPECTIVES

Several key messages can be taken away from this cradle-to-gate, process-based LCA of a $VO_2$ neuromorphic device. First of all, regarding the CED and GWP metrics, the dominant contribution comes from the use of gold for the electrical contacts. This conclusion is robust to the variation of several parameters, such as the electricity production mix and the estimated consumption of individual equipment. The use of aluminium as an alternative for contacts significantly reduces the process footprint (-25 % CED and -43 % GWP), and seems to preserve the resistive switching properties of the device. More characterization is required to ensure reliability over several switching cycles. Other materials such as nickel, which also has a low energy and carbon intensity [21] and has already been tested in certain works [31], could be investigated. Finally, when comparing CMOS-based neurons implementations to the device studied in this work, the fabrication process of the latter seems to be associated to smaller CED and GWP values per neuron. However, this analysis was performed on a device produced in lab-scale, and these numbers are likely to evolve with industrialization. Our comparison also shows that its use phase energy consumption is still far above that of CMOS neurons.

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## REFERENCES

[1] A. Rao, P. Plank, A. Wild, and W. Maass, "A Long Short-Term Memory for AI Applications in Spike-based Neuromorphic Hardware," *Nature Machine Intelligence*, vol. 4, no. 5, pp. 467–479, 2022.

[2] T. Luo, W.-F. Wong, R. S. M. Goh, A. T. Do, Z. Chen, H. Li, W. Jiang, and W. Yau, "Achieving Green AI with Energy-Efficient Deep Learning Using Neuromorphic Computing," *Communications of the ACM*, vol. 66, no. 7, pp. 52–57, 2023.

[3] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI Array of Low-Power Spiking Neurons and Bistable Synapses With Spike-Timing Dependent Plasticity," *IEEE Transactions on Neural Networks*, vol. 17, no. 1, pp. 211–221, 2006.

[4] J. M. Cruz-Albrecht, M. W. Yung, and N. Srinivasa, "Energy-efficient neuron, synapse and STDP integrated circuits," *IEEE transactions on biomedical circuits and systems*, vol. 6, no. 3, pp. 246–256, 2012.

[5] I. Sourikopoulos, S. Hedayat, C. Loyez, F. Danneville, V. Hoel, E. Mercier, and A. Cappy, "A 4-fJ/Spike Artificial Neuron in 65 nm CMOS Technology," *Frontiers in Neuroscience*, vol. 11, 2017.

[6] K. Nalliboyina and S. Ramachandran, "An energy-efficient hybrid CMOS spiking neuron circuit design with a memristive based novel T-type artificial synapse," *AEU - International Journal of Electronics and Communications*, vol. 173, p. 154982, 2024.

[7] Z. Li, W. Tang, B. Zhang, R. Yang, and X. Miao, "Emerging memristive neurons for neuromorphic computing and sensing," *Science and Technology of Advanced Materials*, vol. 24, no. 1, p. 2188878, 2023.

[8] V. Milo, G. Malavena, C. Monzio Compagnoni, and D. Ielmini, "Memristive and CMOS Devices for Neuromorphic Computing," *Materials*, vol. 13, no. 1, p. 166, 2020.

[9] R. Yuan, Q. Duan, P. J. Tiw, G. Li, Z. Xiao, Z. Jing, K. Yang, C. Liu, C. Ge, R. Huang, and Y. Yang, "A calibratable sensory neuron based on epitaxial VO2 for spike-based neuromorphic multisensory system," *Nature Communications*, vol. 13, no. 1, p. 3973, 2022.

[10] C. Y. Han, Z. R. Han, S. L. Fang, S. Q. Fan, J. Q. Yin, W. H. Liu, X. Li, S. Q. Yang, G. H. Zhang, X. L. Wang, and L. Geng, "Characterization and Modelling of Flexible VO2 Mott Memristor for the Artificial Spiking Warm Receptor," *Advanced Materials Interfaces*, vol. 9, no. 19, p. 2200394, 2022.

[11] W. Yi, K. K. Tsang, S. K. Lam, X. Bai, J. A. Crowell, and E. A. Flores, "Biological plausibility and stochasticity in scalable VO2 active memristor neurons," *Nature Communications*, vol. 9, p. 4661, 2018.

[12] N. Krishnan, S. Boyd, A. Somani, S. Raoux, D. Clark, and D. Dornfeld, "A Hybrid Life Cycle Inventory of Nano-Scale Semiconductor Manufacturing," *Environmental Science Technology*, vol. 42, no. 8, pp. 3069–3075, 2008.

[13] S. B. Boyd, *Life-Cycle Assessment of Semiconductors*. Springer New York, 2012.

[14] M. Garcia Bardon, P. Wuytens, L.-A. Ragnarsson, G. Mirabelli, D. Jang, G. Willems, A. Mallik, A. Spessot, J. Ryckaert, and B. Parvais, "DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies," in *2020 IEEE International Electron Devices Meeting (IEDM)*, 2020, p. 41.4.

[15] T. Pirson, T. P. Delhaye, A. G. Pip, G. L. Brun, J.-P. Raskin, and D. Bol, "The Environmental Footprint of IC Production: Review, Analysis, and Lessons From Historical Trends," *IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING*, vol. 36, no. 1, 2023.

[16] L. Boakes, M. Garcia Bardon, V. Schellekens, I.-Y. Liu, B. Vanhouche, G. Mirabelli, F. Sebaai, L. Van Winckel, E. Gallagher, C. Rolin, and L.- Ragnarsson, "Cradle-to-gate Life Cycle Assessment of CMOS Logic Technologies," in *2023 International Electron Devices Meeting (IEDM)*, 2023, pp. 1–4.

[17] G. Orchard, E. P. Frady, D. B. D. Rubin, S. Sanborn, S. B. Shrestha, F. T. Sommer, and M. Davies, "Efficient Neuromorphic Signal Processing with Loihi 2," 2021. [Online]. Available: http://arxiv.org/abs/2111.03746

[18] M. Buyle, A. Audenaert, P. Billen, K. Boonen, and S. Van Passel, "The Future of Ex-Ante LCA? Lessons Learned and Practical Recommendations," *Sustainability*, vol. 11, no. 19, p. 5456, 2019.

[19] N. Bidoul, T. Rosca, A. M. Ionescu, and D. Flandre, "Static and Dynamic Stochastic Analysis of a Temperature-Sensitive VO $_2$ Spiking Neuron," in *ESSDERC 2023 - IEEE 53rd European Solid-State Device Research Conference (ESSDERC)*, 2023, pp. 81–84.

[20] M. Z. Hauschild and M. A. Huijbregts, *Life Cycle Impact Assessment*. Springer Netherlands, 2015.

[21] P. Nuss and M. J. Eckelman, "Life Cycle Assessment of Metals: A Scientific Synthesis," *PLOS ONE*, vol. 9, no. 7, p. e101298, 2014.

[22] "Iea world energy statistics and balances," https://doi.org/10.1787/enestats-data-en, accessed: 2023-04-08.

[23] "Greenhouse gas emission intensity of electricity generation in europe," https://www.eea.europa.eu/en/analysis/indicators/greenhouse-gas-emission-intensity-of-1?activeAccordion=, accessed: 2023-04-08.

[24] A. A. Yaroshevsky, "Abundances of chemical elements in the Earth's crust," *Geochemistry International*, vol. 44, no. 1, pp. 48–55, 2006.

[25] S. Kadivar, H. Akbari, and E. Vahidi, "Assessing the environmental impact of gold production from double refractory ore in a large-scale facility," *Science of The Total Environment*, vol. 905, p. 167841, 2023.

[26] E. D. Williams, R. U. Ayres, and M. Heller, "The 1.7 Kilogram Microchip: Energy and Material Use in the Production of Semiconductor Devices," *Environmental Science & Technology*, vol. 36, no. 24, pp. 5504–5510, 2002.

[27] S. Kim and M. Overcash, "Energy in chemical manufacturing processes: gate-to-gate information for life cycle assessment," *Journal of Chemical Technology & Biotechnology*, vol. 78, no. 9, pp. 995–1005, 2003.

[28] Y. Ke, S. Wang, G. Liu, M. Li, T. J. White, and Y. Long, "Vanadium Dioxide: The Multistimuli Responsive Material and Its Applications," *Small*, vol. 14, no. 39, p. 1802025, 2018.

[29] J. Lin, K. Alam, L. Ocola, Z. Zhang, S. Datta, S. Ramanathan, and S. Guha, "Physics and technology of electronic insulator-to-metal transition (E-IMT) for record high on/off ratio and low voltage in device applications," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 23.4.1–4.

[30] G. A. Gibson, "Designing Negative Differential Resistance Devices Based on Self-Heating," *Advanced Functional Materials*, vol. 28, no. 22, p. 1704175, 2018.

[31] B.-J. Kim, Y. W. Lee, B.-G. Chae, S. J. Yun, S.-Y. Oh, H.-T. Kim, and Y.-S. Lim, "Temperature dependence of the first-order metal-insulator transition in VO2 and programmable critical temperature sensor," *Applied Physics Letters*, vol. 90, no. 2, p. 023515, 2007.