# Variability and Intrinsic Noise Effects in ULV CMOS SRAM Demystified

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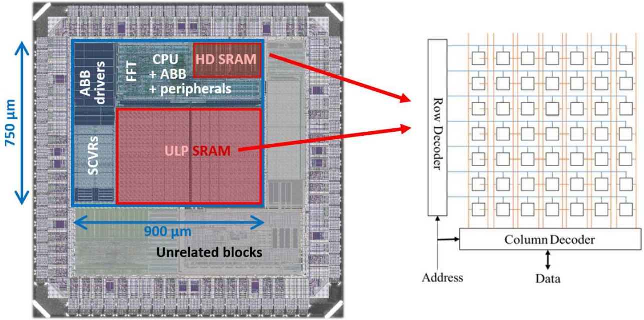
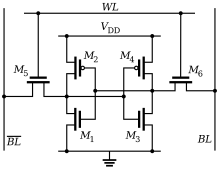
3rd of July

# CMOS SRAM Arrays and Bitcell Failure Probability



SleepRunner ULP MCU [Bol et al., 2021]



32 kB SRAM array = 262 144 *bitcells* implemented with MOS transistors

*Functional* bitcell: capable of retaining a "0" or "1"
*and* not losing this data during operation!

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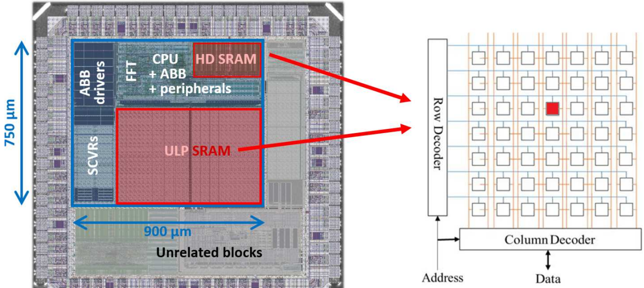

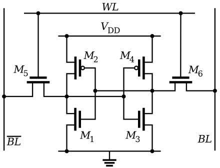

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32 kB SRAM array = 262 144 *bitcells* implemented with MOS transistors

*Functional* bitcell: capable of retaining a “0” or “1”
*and* not losing this data during operation!

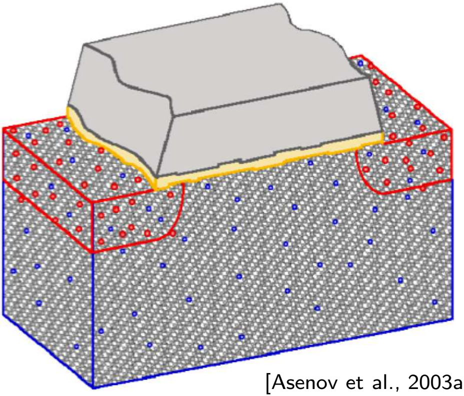
*Failure* “risk” (*probability* $P_{\text{fail}}$) due to uncertainties: *process variability*
*intrinsic noise*

Need to guarantee (estimate) $P_{\text{fail}} \lesssim 1 - 10\,\text{ppm}$ $(1\,\text{ppm} = 10^{-6})$.

# Statistical Process Variability

↪ time-independent *random* variations ($\delta V_{\mathrm{th}}$) in physical parameters ($V_{\mathrm{th}}$) of identically manufactured transistors

Due to the discreteness of the charge and the atomicity of matter:



[Asenov et al., 2003a]

gate *line edge roughness*

oxide thickness fluctuation

*random dopant* ● ● *fluctuations*

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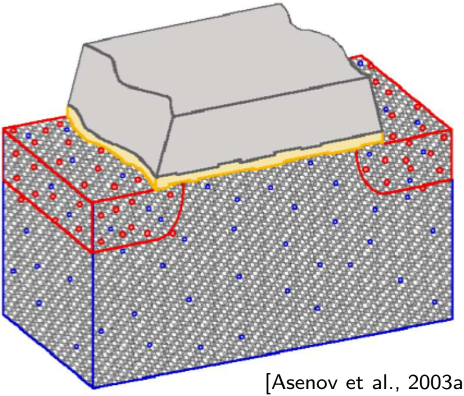

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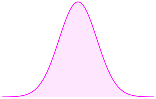
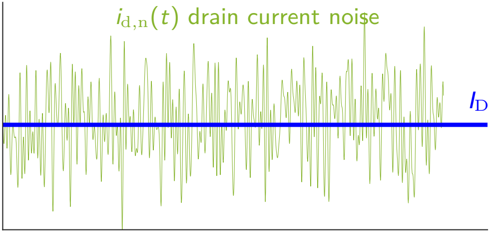
Dominant effect: $\overset{\text{CLT}}{\Longrightarrow}$ $\boxed{V_{\mathrm{th}} \sim \mathcal{N}\left(V_{\mathrm{th0}}, \sigma_{V_{\mathrm{th}}}\right) \text{ with } \sigma_{V_{\mathrm{th}}} = \frac{A_{V_{\mathrm{th}}}}{\sqrt{W \cdot L}}}$



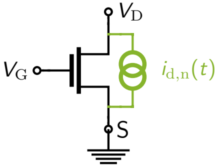
# Intrinsic Noise

↪ *randomly time-fluctuating* signal *generated* within the devices themselves



Interpretation/modelling:

$i_{\mathrm{D}}(t) = I_{\mathrm{D}} + i_{\mathrm{d,n}}(t)$



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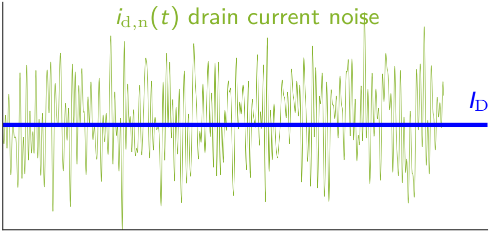

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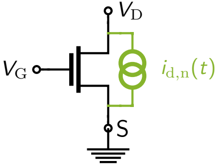
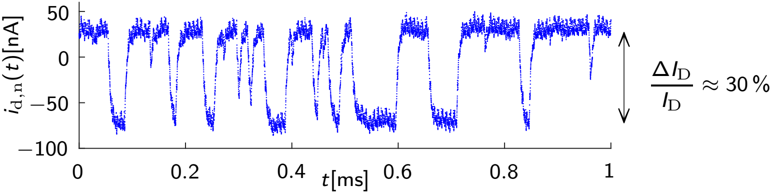


Thermal and flicker noise sources ≈ Gaussian

Random Telegraph Noise (RTN): capture/emission of electrons by single trap



Measured $\Delta I_{\mathrm{D}}/I_{\mathrm{D}} = 30\,\%$ in 28 nm FD-SOI! [Van Brandt et al., 2019]

# ULV CMOS SRAM Design (I)

↪ smallest transistors ($W_{\mathrm{min}}$ and $L_{\mathrm{min}}$) for high integration density

↪ reduction of supply voltage ($V_{\mathrm{DD}}$)

1 V nominal

$\searrow$ 400 – 500 mV *ultra-low voltage* (ULV) operation

$\sim$150 mV extreme (ultimate ?) ULV

✓ reduced power consumption $P^{\searrow\searrow} \propto V_{\overset{\searrow}{\mathrm{DD}}} \cdot I_{\overset{\searrow}{\mathrm{DS}}}$

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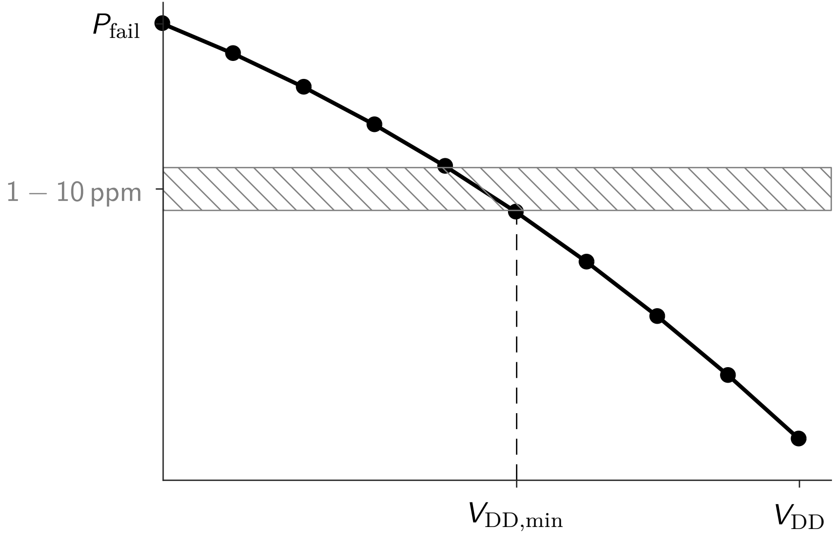
✗ worsened sensitivity to variability and noise

Robustness of SRAM bitcell against read/write/**hold** failures?

# ULV CMOS SRAM Design (II): Functional Yield



How do we define/extract/predict $P_{\text{fail}}$?

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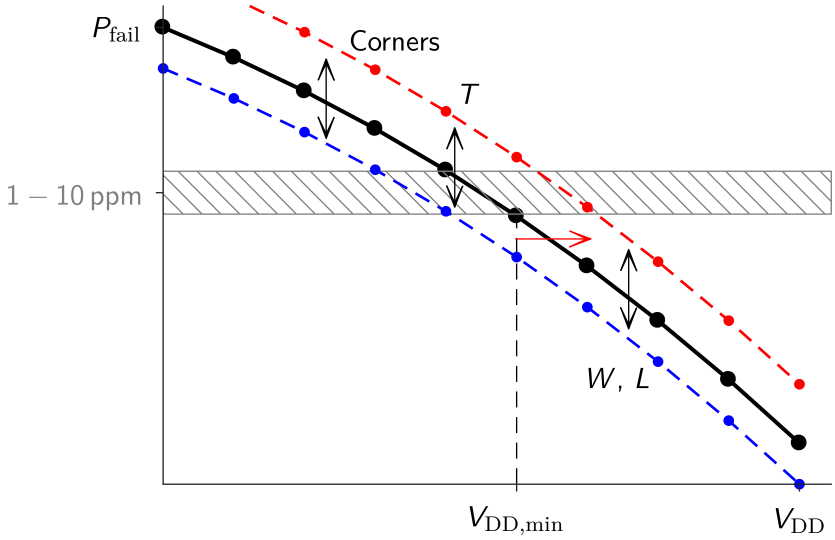

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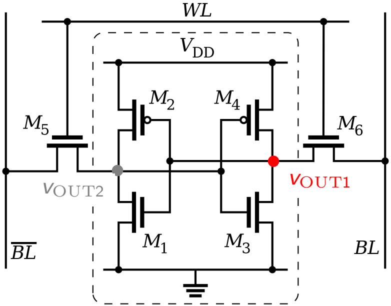
# Outline

1. Context and Motivation
    - CMOS SRAM Arrays and Bitcell Failure Probability
    - Statistical Process Variability
    - Intrinsic Noise
    - ULV CMOS SRAM Design
2. Variability-Induced Failures
    - SRAM Static Stability
    - Monte-Carlo Simulation
    - Semi-Analytical Methodology to Predict Hold Failure Probability
3. Noise-Induced Transient Bit Flips
    - Notion of Dynamic Stability
    - Transient Noise Simulations
4. Discussion and Conclusions
    - Reported Mean Times to Failure in Various Conditions
    - Process Variability + RTN + Gaussian Noise

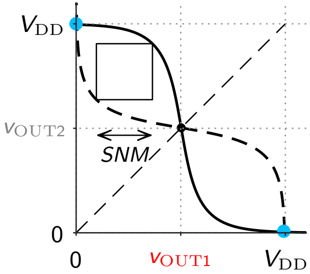
# Variability-Induced Failures

# SRAM Static Stability

↪ stability of "as-fabricated" bitcell at time zero



"Butterfly" [Seevinck et al., 1987]



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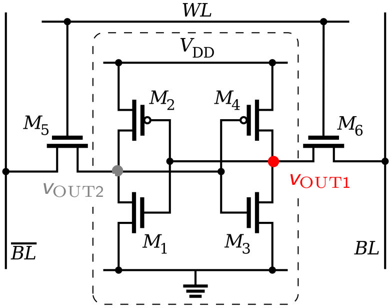

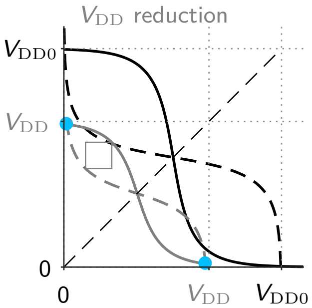

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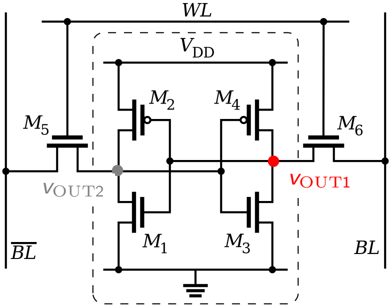

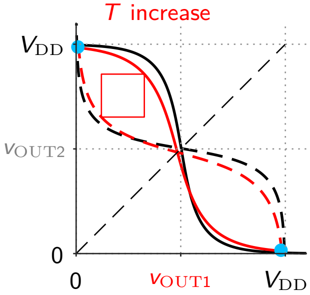

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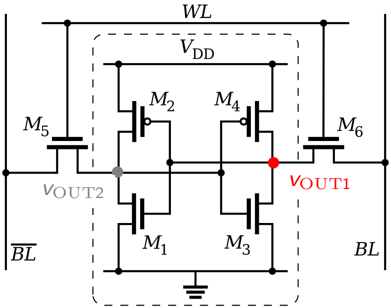

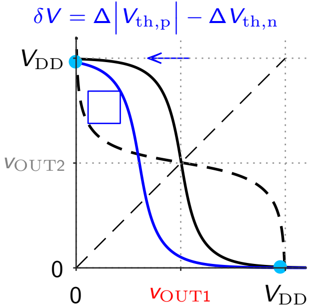

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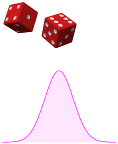
# Monte-Carlo Simulation

Simulate $N_{\mathrm{s}}$ bitcells (latches).
For each latch, "*throw dice*"

- for each transistor parameter ($V_{\mathrm{th}}$), *sampling* from the *distribution*;



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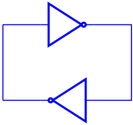

- classify as either functional or defective.
  ↪ iif the two stable logic states "0" and "1" exist

Unbiased estimator of $P_{\mathrm{fail}}$: $\hat{P}_{\mathrm{fail}} = N_{\mathrm{defective}}/N_{\mathrm{s}}$; how many samples ($N_{\mathrm{s}}$)?

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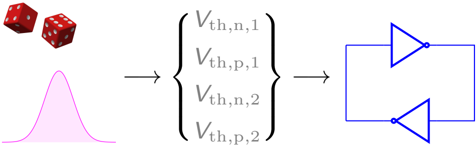

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$$\implies N_\mathrm{s} = \frac{2}{\varepsilon^2}\left(\mathrm{erf}^{-1}(1-\delta)\right)^2 \frac{1}{P_\mathrm{fail}}$$

$(1-\varepsilon) = (1-\delta) = 90\,\%$, target $P_\mathrm{fail} = 10\,\mathrm{ppm} \implies N_\mathrm{s} = 27$ **million**!

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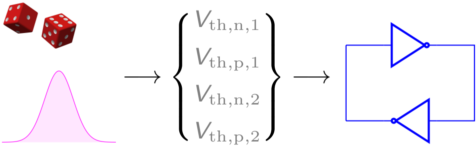

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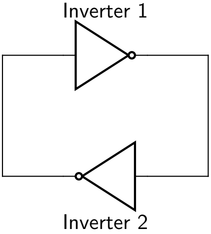
Cheaper but less accurate: accelerated Monte-Carlo (importance sampling);
SRAM analytical modelling (insightful!)

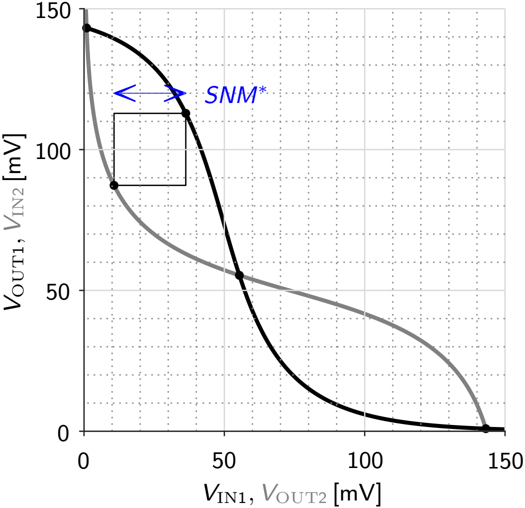
*Methodology* "in between": *deterministic simulations + analytical statistics*

# Static Failure Detection

*Static noise margin* extraction:



"Butterfly plot" [Seevinck et al., 1987]



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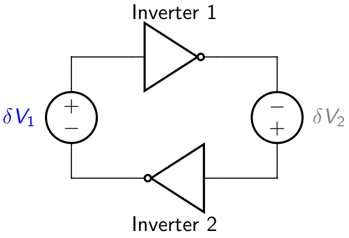

$SNM(\delta V_1, \delta V_2) \overset{>}{\underset{<}{}} 0?$

Cheap **deterministic** simulation ("`DC` sweep") at *circuit* level

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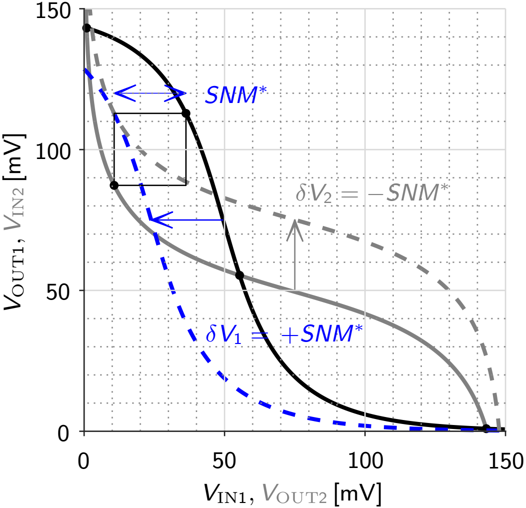

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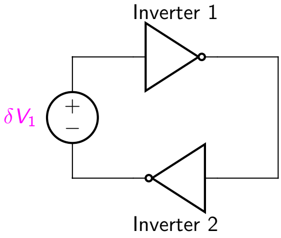

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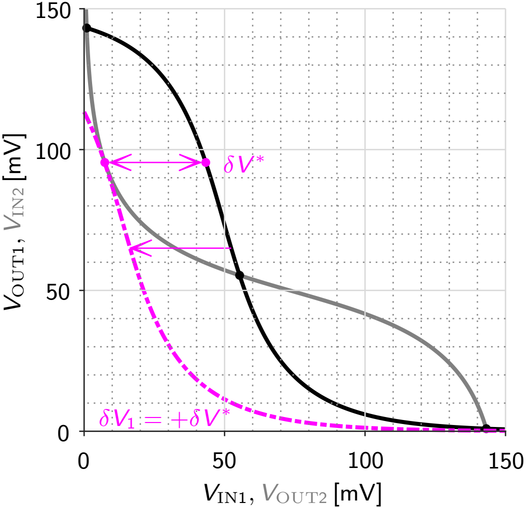

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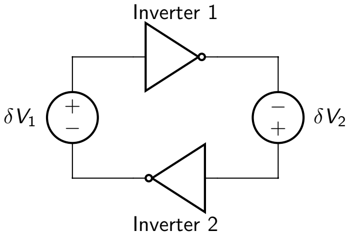

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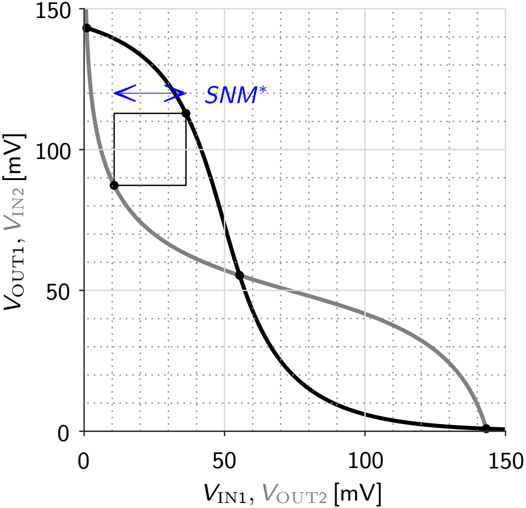

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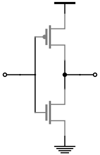
Cheap **deterministic** simulation ("`DC` sweep") at *circuit* level

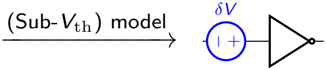
+ knowledge of variability, at the *transistor* level.

"Propagate the *statistics*" ⟶ efficient analytical calculation of $P_{\mathrm{fail}}$!

# Threshold Voltage Imbalance Representation

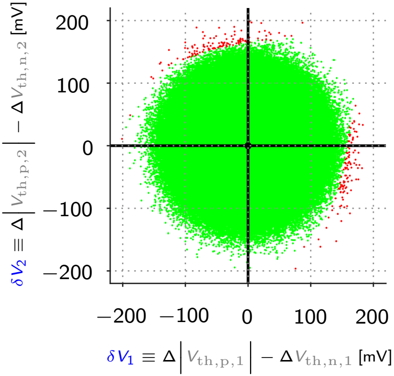
"Transistor to circuit parameter"





$$\delta V = \frac{\left(n_{\mathrm{n}}\, \Delta \left| V_{\mathrm{th,p}} \right| - n_{\mathrm{p}}\, \Delta V_{\mathrm{th,n}}\right)}{n_{\mathrm{n}} + n_{\mathrm{p}}}$$

Illustration with Monte-Carlo simulation:



28 nm FD-SOI SPW latch

RVT nMOS and LVT pMOS transistors

Minimal dimensions ($L_{\mathrm{n}} = L_{\mathrm{p}} = 30$ nm
$W_{\mathrm{n}} = W_{\mathrm{p}} = 80$ nm);

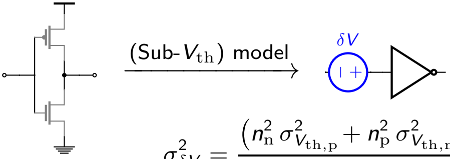
$V_{\mathrm{DD}} = 200$ mV; $T = 300$ K; TT corner.

**Two weeks** of total
simulation + analysis time!

5 M latches
↪ 235 defective ($P_{\mathrm{fail}} = 47$ ppm)

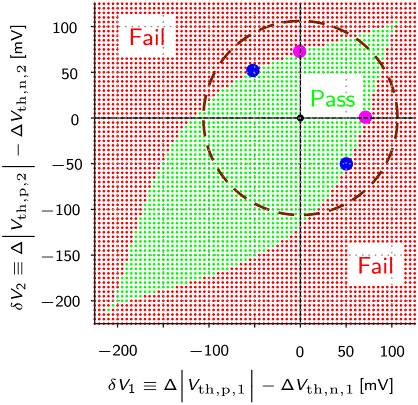
# Failure Probability Prediction

"Propagate the randomness"



$$\sigma_{\delta V}^2 = \frac{\left(n_{\mathrm{n}}^2 \, \sigma_{V_{\mathrm{th,p}}}^2 + n_{\mathrm{p}}^2 \, \sigma_{V_{\mathrm{th,n}}}^2\right)}{(n_{\mathrm{n}} + n_{\mathrm{p}})^2}$$

**Deterministic** simulation ("`DC` sweep"):



Extraction of the failure *boundary* $g(\delta V_1)$

$\implies$ (Almost) *exact* calculation of $P_{\mathrm{fail}}$

$$= 2 \cdot \int_{-\infty}^{+\infty} \mathrm{d}\delta V_1 \, f_{\delta V}(\delta V_1) \int_{-\infty}^{\boldsymbol{g(\delta V_1)}} \mathrm{d}\delta V_2 \; f_{\delta V}(\delta V_2)$$

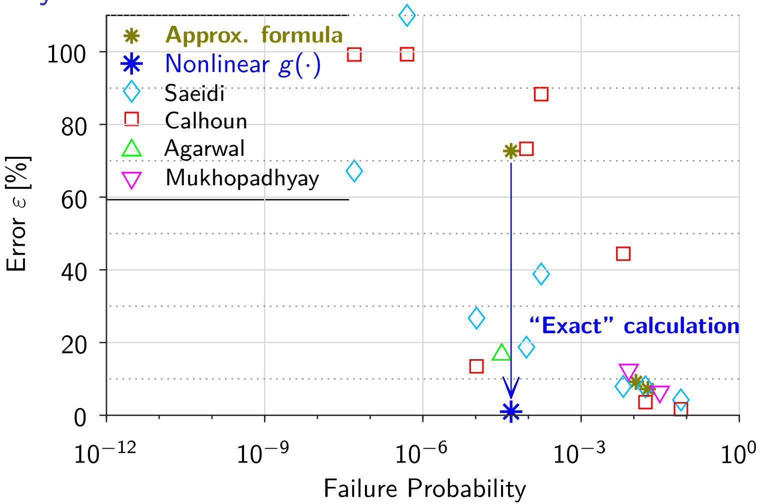
in **less than a minute**!

[Van Brandt et al., 2023a, in preparation for IEEE TCASII]

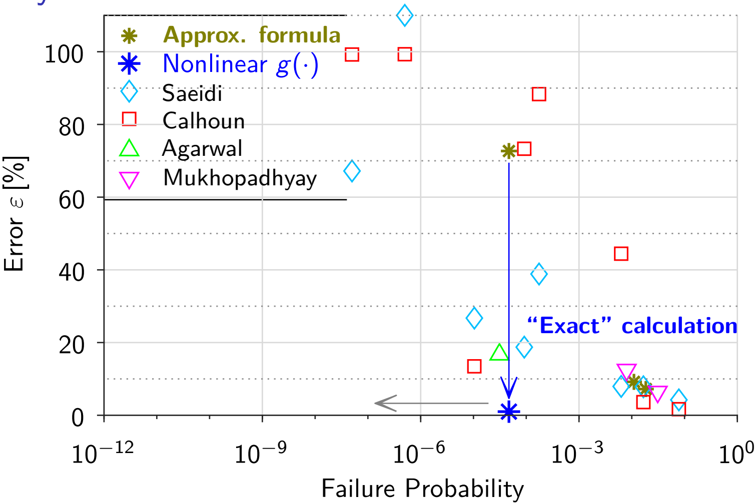
Approximated closed-form formula

[Van Brandt et al., 2022, IEEE TCASI]

# Accuracy: Benchmark with Former Works



# Accuracy: Benchmark with Former Works

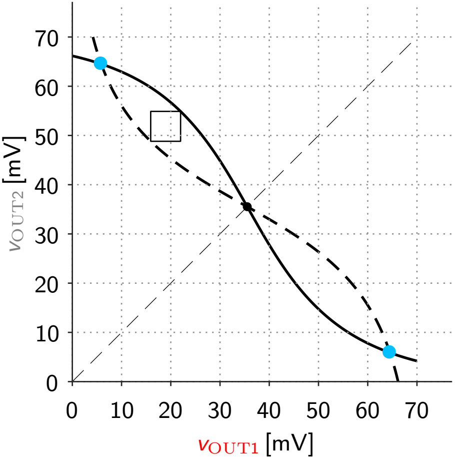


Accuracy for $P_{\mathrm{fail}}$ down to the ppm still to be proven/confirmed
$\hookrightarrow$ further comparison with reliable importance sampling?

# Noise-Induced Transient Bit Flips

# Notion of Dynamic Stability

Ultimate $V_{\mathrm{DD}}$ lowering: 70 mV



28 nm FD-SOI RVT transistors
Minimal dimensions $L_{\mathrm{n}} = L_{\mathrm{p}} = 30\,\mathrm{nm}$
$W_{\mathrm{n}} = W_{\mathrm{p}} = 80\,\mathrm{nm}$;
pMOS back-gate bias $V_{\mathrm{SB}} = 1.6\,\mathrm{V}$;
room temperature; TT corner

Question: Is *this* SRAM bitcell "functional", or not?

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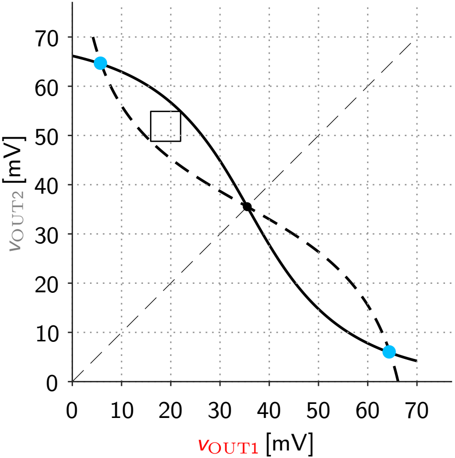

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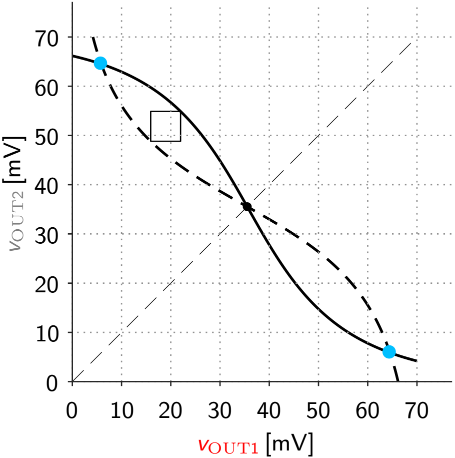

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However, we expect poor noise immunity during *retention* operation.

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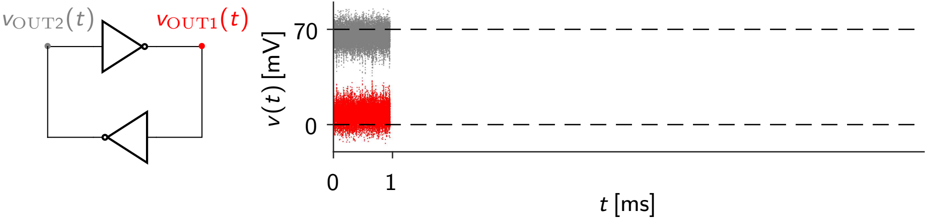
Let us perform a real time-domain simulation of the retention operation:



The bitcell is well functional at time zero.

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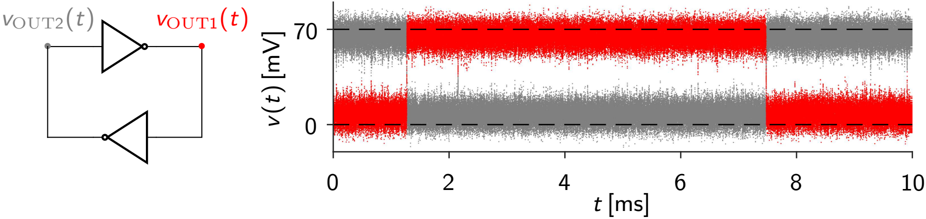

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For *this* experiment, the initial state is retained at least during 1 ms! However...

A *bit flip* due to the *intrinsic transistor noise* here occurs at $t \approx 1.3\,\mathrm{ms}$

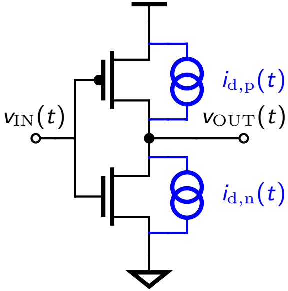
Repeating and/or lengthening experiment $\longrightarrow$ *mean time to failure* ($MTTF$)

The bitcell is dynamically *unstable*, and must be classified as defective!

# Transient Noise Simulation

↪ true noise simulation in the time domain (`NOISETRAN` in SPICE).

↪ **CPU intensive**



[Bolcato and Poujois, 1992]

Random Gaussian noise source

added in parallel to each (noisy) device
generated independently according to
device compact model

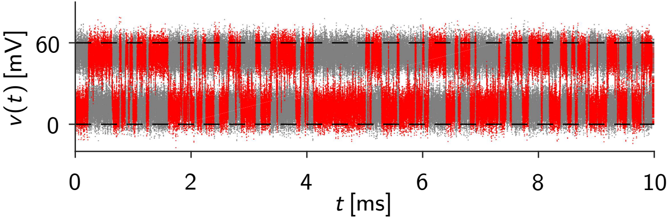
→ General `TRAN` simulation

Simulation methodology described in [Van Brandt et al., 2023b]

# Ultimate $V_{\mathrm{DD}}$ Lowering

[Van Brandt et al., 2023b]

(a) $V_{\mathrm{DD}} = 60\,\mathrm{mV}$: $SNM = 3\,\mathrm{mV}$ $MTTF = 96\,\mathrm{\mu s}$



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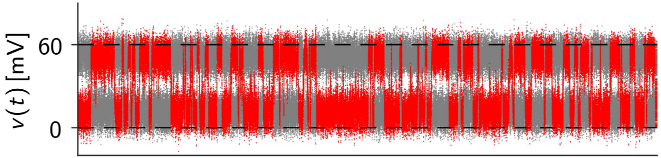
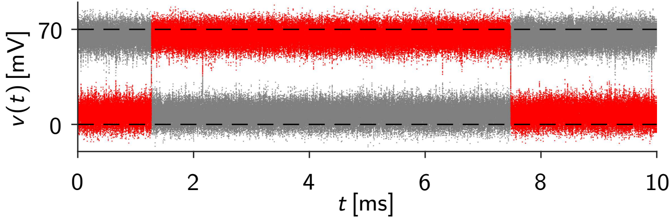


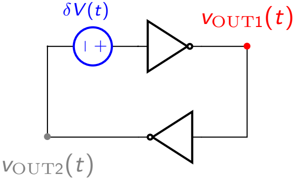
(b) $V_{\mathrm{DD}} = 70\,\mathrm{mV}$: $SNM = 6\,\mathrm{mV}$ $MTTF = 8\,\mathrm{ms}$



# Random Telegraph Noise (RTN)

↪ not incorporated in industrial PDK

$\Longrightarrow$ We introduce it as a series-voltage source $\delta V(t)$ at inverter level:

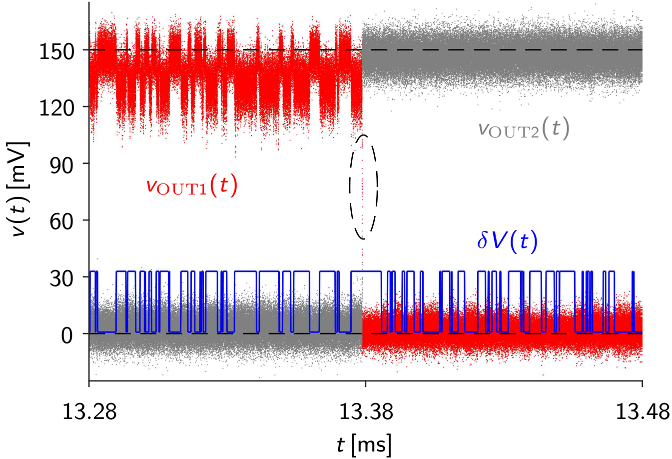


RTN parameters: $\delta V_0 = 32\,\mathrm{mV}$, $\overline{\tau}_{\mathrm{e}} = \overline{\tau}_{\mathrm{c}} = 2\,\mu\mathrm{s}$
$\sim \Delta I_{\mathrm{D}}/I_{\mathrm{D}} \approx 30\,\%$ in 28 nm FD-SOI transistors
[Van Brandt et al., 2019]

Simulated case:
[Van Brandt et al., 2023b]
28 nm FD-SOI Single-P-Well inverter (RVT nMOS and LVT pMOS);
$V_{\mathrm{B}} = 0$; $V_{\mathrm{DD}} = 150\,\mathrm{mV}$; $T = 120\,^{\circ}\mathrm{C}$.

Bandwidth of generated Gaussian noise: $f_{\max} = 500\,\mathrm{MHz}$ ($\mathrm{d}t = 1\,\mathrm{ns}$);
simulation duration $T = 20\,\mathrm{ms}$

# Random Telegraph Noise (RTN)

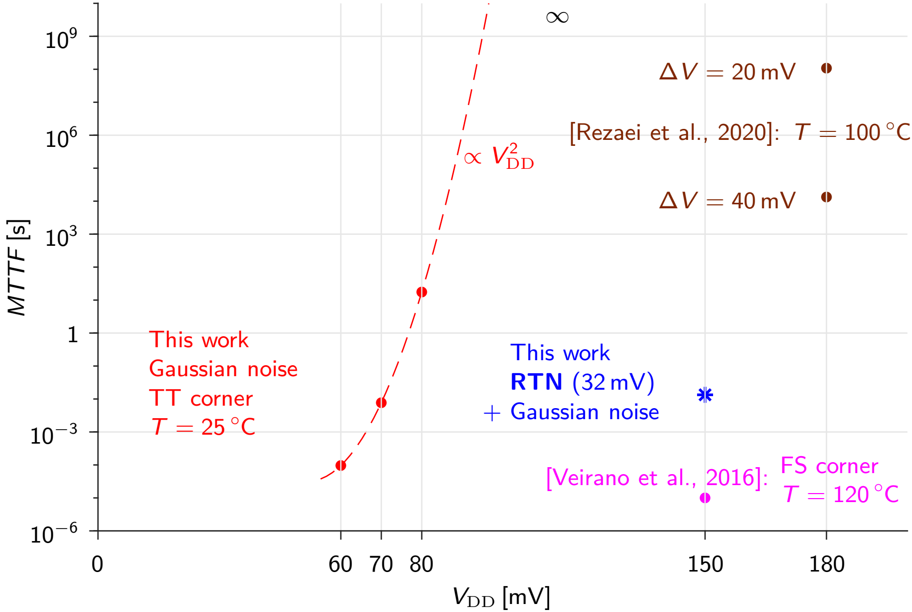


A bit flip has occurred at 13.38 ms!

The large RTN dynamically reduces the Gaussian noise margin:
*SNM* from 29 mV (nominal value) to 15 mV

$\Longrightarrow$ endangers the noise immunity of the SRAM bitcell!

# Reported $MTTF$ in Various Conditions



# Variability vs RTN vs Gaussian Noise?

In 28 nm FD-SOI CMOS technology:

Process variability: estimated $\boxed{\sigma_{V_{\mathrm{th}}} \sim 20 \ldots 30\,\mathrm{mV}}$

Measured large-amplitude RTN: $\Delta I_{\mathrm{D}}/I_{\mathrm{D}} = 30\,\% \longleftrightarrow \Delta V_{\mathrm{th}}$ conversion?
[Van Brandt and Flandre, 2020]

$$\frac{\Delta I_{\mathrm{D}}}{I_{\mathrm{D}}} = \underbrace{\frac{g_{\mathrm{m}}}{I_{\mathrm{D}}}}_{\approx 19\,\mathrm{V}^{-1}} \cdot \Delta V_{\mathrm{th}} \implies \boxed{\Delta V_{\mathrm{th}} \approx 16\,\mathrm{mV}}$$

At inverter level, two transistors in worst-case RTN scenario: $\delta V_0 = 32\,\mathrm{mV}$

Important quantitative conclusion: $\Delta V_{\mathrm{th}} < \sigma_{V_{\mathrm{th}}} \ll 3 - 6 \cdot \sigma_{V_{\mathrm{th}}}$, i.e.
**process variability remains the major concern**

However, together with variability, RTN reduces the noise margins;
Gaussian noise ($\sigma \approx 6\,\mathrm{mV}$) can then induce transient bit flips

# State-of-the-Art and Contributions

Toward efficient assessment of SRAM bitcell reliability

*Process variability* has remained the dominant concern

- Monte-Carlo much too expensive for low failure probability (ppm)
- Quite well covered, notably importance sampling methods
- Novel non-Monte-Carlo methodology:
  deterministic circuit simulations + knowledge of $V_{\mathrm{th}}$ statistics

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For both, we have to think semi-analytical, accelerated statistical methods!

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