LOW-FREQUENCY NOISE ANALYSIS OF ON-MEMBRANE MOSFET AND IN-SITU THERMAL ANNEALING

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***Abstract*—In this work, we discuss the I-V and low-frequency noise characteristics of on-membrane 6µm-wide 1µm-long n-MOSFETs for analog low-power sensor interfaces, in e.g. pressure or gas measurements. After MEMS processing (i.e. bulk Si Deep Reactive Ion Etching), a high power spectral density (PSD) with clear signs of Random Telegraph Noise (RTN) (with ΔId/Id as high as 40%) is observed. Cadence simulations predict lower PSD values. At the same time, the MOSFET I-V measurements show threshold voltage, transconductance and subthreshold slope discrepancies compared to simulations. In order to heal these detrimental effects of DRIE, a high-temperature in-situ thermal annealing (T=265 °C for 2 min) is applied. As a result, the noise power is reduced by a factor of about 10, the MOSFET electrical characteristics are also partially recovered and become close to simulations. An analytical study based on noise and current models fits the interpretation of effects linked to interface traps.**

Keywords—1/f NOISE, MOSFET, Thermal Annealing, DRIE defects, interface traps

I. INTRODUCTION

Local electro-thermal annealing is a promising technique for the recovery of process- or radiation-induced defects in CMOS circuits [1-3]. In recent works, we used micro-heaters located on thermally-insulated MEMS membrane, with Partially-Depleted (PD) SOI (Silicon-on-Insulator) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Such micro-hot-plate is common for gas sensing applications where it showed high performances and good mechanical stability at high temperatures up to 600°C [4]. However, residual charge traps are created in the SOI Buried Oxide (BOX) by the Deep Reactive Ion Etching (DRIE) post-CMOS process used to release the membrane of the micro-heater by etching the substrate back-side and using the BOX as the etch stop layer. These residual charge traps alter the typical MOSFET behavior (e.g. threshold voltage (Vth), transconductance (gm), subthreshold slope…) [5]. In this work we provide a quantitative study on the electrical defects of on-membrane n-MOSFET caused by DRIE, and evaluate the efficiency of thermal annealing in the recovery from residual traps. Firstly, we present the I-V behavior of the transistor before and after thermal annealing and evaluate its parameters. Afterwards, using low-frequency noise measurements we investigate the charge trapping behavior before and after thermal annealing. A detailed analysis based on Power Spectral Density (PSD) noise measurements is provided. An analytical study shows the contribution of RTN noise in the total power noise, which demonstrates the real interference of the oxide traps. For comparison, Cadence simulations are also provided with respect to the same dimensions and technology model as the measured MOSFET but with model parameters valid for MOSFETs on the SOI substrate, not on membranes yet.

II. DESIGN DESCRIPTION

The technology used for fabrication is SOI 1.0 µm – XI10, provided by XFAB. The design consists of a circular Tungsten micro-heater of 200µm diameter, with Body-Tied (BT) n-MOSFETs of different dimensions and a PIN diode of 10x20 µm^2 footprint and intrinsic length of 1µm, both being placed at a few tens of micro-meters away from the micro-heater. A second PIN diode occupies the footprint of the micro-heater. All devices are embedded in 5µm thick Si/SiO_2 membrane including a 0.55µm thick Si_3N_4 passivation layer, where the micro-heater and the interconnections are implemented by a 0.3 µm thick Tungsten metallization layer. The connection pads are designed in a third 0.5µm thick Tungsten metallization layer. The membrane has a circular shape of 600 µm diameter, in order to reduce the stress at the borders, thus improve the mechanical stability (Fig. 1). The electrical characteristics of MOSFETs reached stability after two minutes of post-process stabilization annealing at 265°C. The on-membrane MOSFETs showed good performance under high-temperature conditions up to 280°C. No significant mechanical deterioration was observed on the membrane structure after high-temperature operation [5]. The main

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purpose of the membrane implementation is to avoid the dissipation of Joule energy through the bulk, which would act

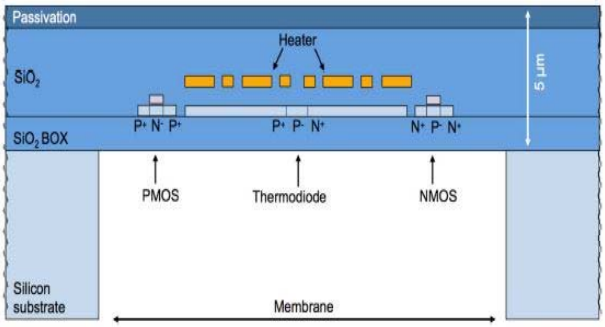

Fig 1. Schematic cross section of the studied device

as a heat sink, thus guaranteeing high-temperature annealing up to 335 °C with reasonable power consumption below 50 mW and fast time response [5].

III. EXPERIMENTAL PROCEDURE

The chip is packaged in a DIL-24 ceramic packages by conductive adhesive at the substrate back-side and gold lead wires bonded to the tungsten pads on the chip, then inserted in a Zero Insertion Force support of a closed test fixture box and connected to the input and output modules of the "*Keysight LFNA noise analyser*" with 1.5m-long triax cables [6]. The PIN diode is used as a temperature sensor during thermal annealing. The measurement consists in applying a constant current bias of 65µA and measuring the forward diode voltage V_d, to obtain the annealing temperature. The diode was previously calibrated using the hot chuck of a probe station, yielding a sensitivity factor d of d=-1.2 mV/°C. Then obtaining the annealing temperature with the following equation where V_0 is the initial voltage at room temperature T_0

$$V_d = V_0 - d\,(T - T_0) \qquad (1)$$

A first set of I-V measurements is performed on the virgin die after DRIE, on the 6µm-wide nMOSFET in linear regime at V_{ds} = 50mV, followed by low-frequency 1/f and RTN noise measurements at drain currents I_{ds} of about 10^{-3}, 10^{-2}, 10^{-1}, 1 and 10 µA. At each current level, PSD measurements were done from 1 Hz to 1 MHz, while time trace measurements were recorded for 5s with a time step of 80µs, to allow extraction of slow trap time constants. Afterwards, a thermal-annealing of 265°C is applied for 2 min by biasing the embedded micro-heater. Next, a 2nd set of measurements is performed, following the same methodology and measurement conditions.

IV. RESULTS AND DISCUSSION

A. I-V Characterization

Compared to the ideal electrical behavior of the simulation results of the on-substrate n-MOSFET, the I_{ds} and g_m versus V_{gs} measurements show a strong deviation due to the defects created by the MEMS DRIE post-CMOS process. These defects are mainly due to a combination of charge traps in the buried oxide (N_{ox}) and Si/SiO_2 interface (N_{it}), where V_{th} depends on (N_{it} - N_{ox}) [7]. After the thermal annealing, a partial recovery of the initial characteristics is obtained because of the decrease of the charge traps density (Fig. 2). The extracted threshold voltage, peak transconductance value (G_{m_max}) and subthreshold swing (SS) show a strong degradation after DRIE but almost fit the simulation results after annealing (Table 1).

The extracted SS values shift from 114 to 79 mV/dec, which means a better control of the channel and becomes close to the Cadence simulation:

$$SS = \frac{dV_{gs}}{d\log(I_{ds})} \qquad (2)$$

TABLE I. ELECTRICAL PARAMETERS OF MEASURED AND SIMULATED N-MOSFETS.

	V_{th} [V]	G_{m_max} [µA.V^{-1}]	SS[mV/dec]
Virgin	1.8	10.2	114
Post-annealing	1.68	12.2	79
Simulation	1.71	13.5	71

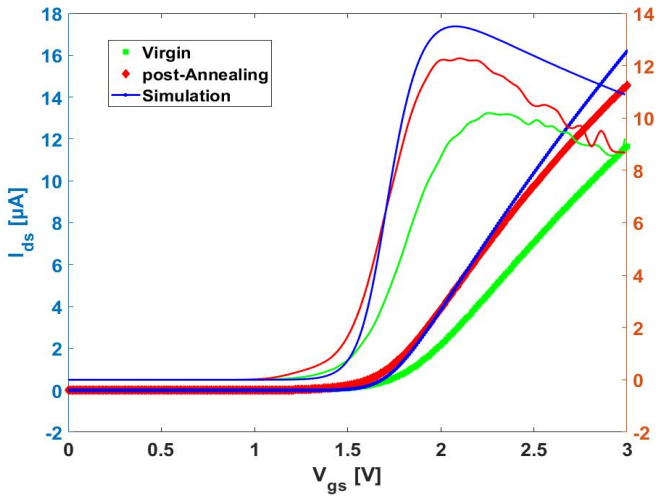

Fig 2. I-V (thick lines) and transconductance g_m (thin lines) measurements of on-membrane n-MOSFET, before and after thermal annealing, compared to Cadence simulation of the ideal MOSFET model in linear regime with V_{ds}=50 mV.

However, a deeper investigation is needed to better understand the physical defects created by DRIE and the recovery efficiency after annealing. Noise measurements are used here to analyze the impact of electrically-active trapping mechanisms.

B. Noise measurements

1) Subthreshold: The drain current time trace measurements id (t) of the virgin n-MOSFET, in weak inversion with Vgs-Vth = -0.55 V, show a multiple-level RTN signal, with a trap yielding a remarkably high current jump of about 40%, i.e. ΔIds ~ 2nA (Fig. 3). The RTN physical property is explained by the electron capture and emission between the channel and the charge traps in the oxide. The emission time τe is the average time to emit a trapped carrier (i.e. low current level), while the capture time τc is the average time to capture the carrier (i.e. high current level).

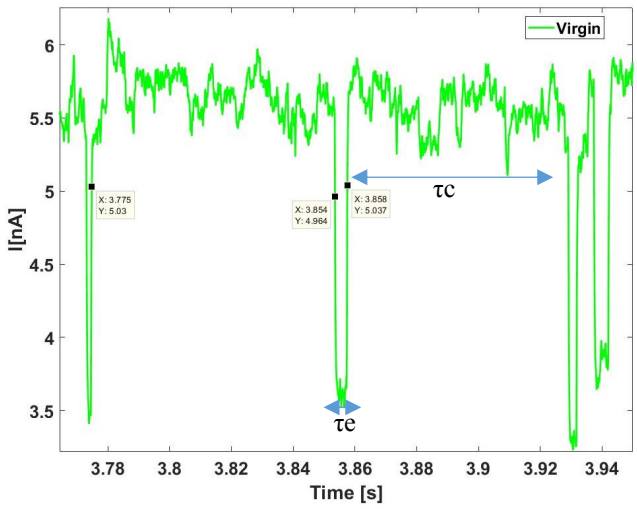

Fig 3. Time domain RTN traces of the on-membrane n-MOSFET after DRIE at V_{ds}=50mV below V_{th}.

The Time Lag Plot (TLD) of i_d (t) clearly demonstrates the strong RTN behavior (Fig. 4). The TLD shows two clear lobes, thus confirming the presence of one main active trap. A cloud of populated regions are spread around the main states, which present the transitions between the two states of the trap. The color weighted presentation shows the frequency of I_{ds} appearance, where the red and blue color indicates the high and low frequency, respectively.

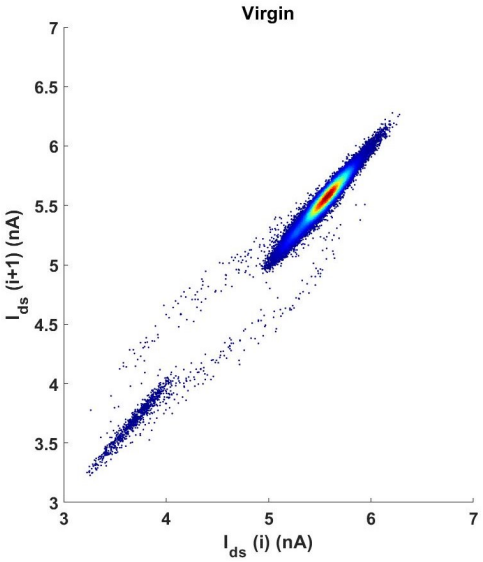

Fig. 4. Lag plot of $i_d(t)$ measurements in weak inversion regime, before annealing resp.

Due to the DRIE back-etching of the substrate, the defects are typically created in the BOX and in the thick isolation oxide on the sides of the channel. It is important to note that this strong RTN behavior is seen in subthreshold regime, at low drain current, where edge effects, known as parasitic edge transistor, highly influence the current in the channel. The mean values of emission and capture time constants, extracted using an extrapolation algorithm, are respectively τ_e = 2.4 ms and τ_c = 153 ms. In order to verify the contribution of the observed strong RTN to the total power noise, we calculate its power spectral density (PSD) using the following model and compare it to the measured total noise spectrum [8] :

$$S_{id,RTN}(f)=\Delta I_d^2 \frac{4\tau^2}{\tau_e+\tau_c}\frac{1}{1+(2\pi f\tau)^2} \qquad (3)$$

with $$\frac{1}{\tau}=\frac{1}{\tau_c}+\frac{1}{\tau_e}$$

The PSD measurements of the virgin MOSFET show the presence of a Lorentzian plateau between 10 and 102 Hz corresponding in amplitude and corner frequency to the RTN estimations based on eq. 3, measured time constants and ΔI_{ds} (i.e. $S_{id,RTN} = 2.4\ 10^{-22}\ A^2Hz^{-1}$).

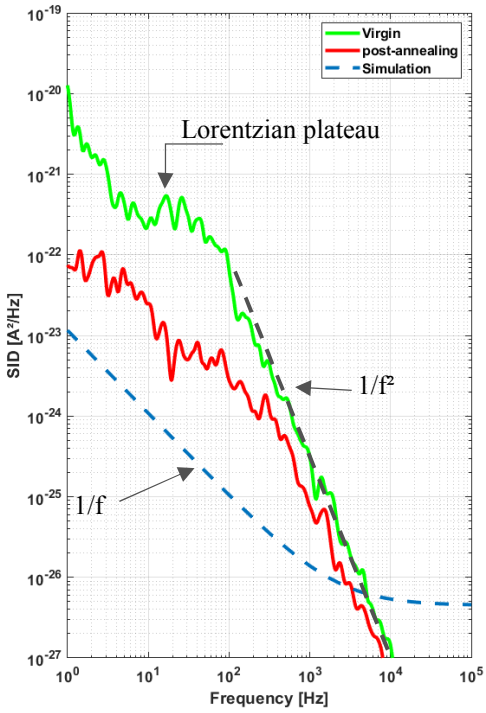

Fig 5. Measured noise power spectral density of the on-membrane n-MOSFET in weak inversion regime, before and after thermal annealing, and compared to 1/f noise Cadence simulation.

At lower frequency, the PSD measurement is dominated by 1/f noise. At higher frequencies, one should take care of the invalid data above the roll-off frequency of the equipment, due to the effect of equivalent capacitance and resistance at the

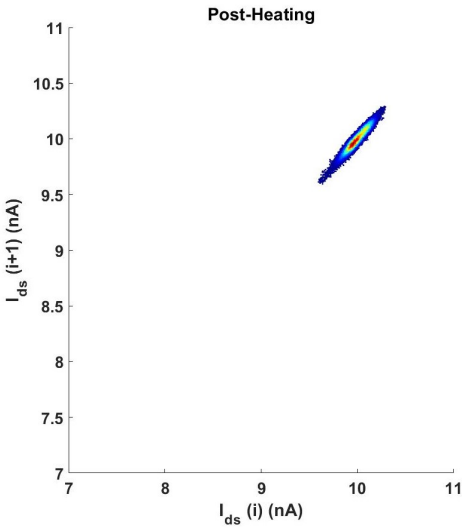

Fig. 6. Lag plot of $i_d(t)$ measurements in weak inversion regime, after annealing resp.

output node; this effect can be noticed by the change in slope in the frequency response of S_{id} measurements.

After thermal annealing, the PSD measurement of I_{ds} noise in subthreshold regime is remarkably reduced by more than one decade, though it does not totally recover the ideal value simulated for the on-substrate n-MOSFET (i.e. without DRIE effects, Fig. 5). On another hand, it is very clear from the lag plot in Fig. 4 and Fig. 6 that the strong RTN has disappeared after the thermal annealing.

2) Above threshold: Typically at I_{ds} = 1µA, no significant RTN is observed in time trace measurements of the virgin n-MOSFET and S_{id} measurements in the frequency range between 10 Hz and 1 kHz show the dominance of 1/f noise (Fig. 7).

After thermal annealing, the noise PSD is reduced by a bit less than one decade. The S_{id} measured above V_{th} approaches the simulation level after annealing. In strong inversion, I_{ds} is indeed dominated by the main channel below the front gate oxide, whereas in sub-threshold, the noise related to defects created in the BOX or at the edges remains dominant, even after annealing.

Integrated noise power: For quantitative analysis, the total integrated noise power is calculated before and after thermal annealing, at the different fixed drain currents, based on the PSD measurements and reference simulations. The following equation is used

$$\sigma_{id}^2 = \int_{f_{min}}^{f_{max}} S_{id}(f)\, df \qquad (4)$$

where the maximum frequency is fixed at the minimum roll-off frequency of the measurement system f_{max} = 613 Hz to avoid the 1/f² effect at high frequency (See Fig. 5 and Fig. 7).

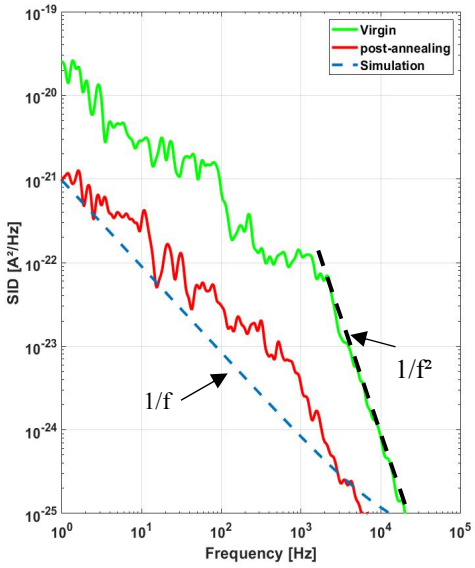

Fig 7. Measured noise power spectral density of the on-membrane n-MOSFET at I_{ds}=1 µA, before and after thermal annealing, and compared to 1/f noise Cadence simulation.

This confirms that the thermal annealing reduces the RTN and 1/f noise at all I_{ds} levels (Table 2). In strong inversion, the total noise measurements almost fit the simulation of 1/f noise, which can be related to the low influence of RTN at high current.

TABLE II. TOTAL POWER NOISE INTEGRATED FROM 1HZ TO 613HZ AT DIFFERENT DRAIN CURRENTS FROM WEAK TO STRONG INVERSION, V_{DS} = 50 mV.

I_{ds} / σ_{id}^2 [A²]	1nA	10nA	100nA	1µA	10µA
Virgin	3.27 10^{-22}	2.9 10^{-20}	2.8 10^{-19}	5.53 10^{-19}	6.6 10^{-18}
Post-annealing	3.71 10^{-23}	1.5 10^{-21}	1.68 10^{-20}	2.22 10^{-19}	1.5 10^{-18}
Simulation	8.8 10^{-25}	7 10^{-23}	5.6 10^{-21}	2.16 10^{-19}	7.6 10^{-19}

V. CONCLUSION

The experimental results showed that in-situ thermal annealing at 265°C for 2 minutes significantly reduces the damage created by the DRIE post-process on on-membrane MOSFETs. The electrical characterization showed a remarkable recovery of threshold voltage and subthreshold swing, which almost fit the ideal simulation results, as well as a partial recovery of the maximum transconductance value. This recovery is confirmed by low-frequency noise measurements, where a strong RTN behavior is recorded in subthreshold after DRIE. The thermal annealing showed an important recovery by about one decade, with noise measurements almost fitting 1/f noise from Cadence simulation above Vth. The recorded strong RTN and its neutralization by thermal annealing have been related the presence of DRIE defects in the BOX and side walls, highly influencing the channel in subthreshold regime.

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