28 GHz Down-Conversion Mixer with RF Back-Gate Excitation Topology in 22-nm FD-SOI

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***Abstract* — This paper presents a novel 28 GHz down-conversion mixer topology using the back-gate terminal in 22 nm FD-SOI as an RF excitation port for the 21 GHz local oscillator (LO) signal. A double balanced architecture with an active load and transimpedance amplifier were implemented in the 22FDX® technology from GlobalFoundries. The mixing functionality is provided at the level of a single FET, that is simultaneously excited at the front- and back-gates by the RF and LO signals, respectively. Under 0.9 V power supply (26 mW DC consumption) the proposed down-conversion mixer exhibits a maximum conversion gain of 3.5 dB by applying 10 dBm of LO power. The 1 dB compression point occurs at -6 dBm of RF input power and the third order intercept (IIP3) point is 15 dBm at nominal LO power. Benchmarking these values against mixer performances from the literature reveals this design to be close to the current state-of-the-art in CMOS and SOI technology, demonstrating the viability of this novel topology employing back-gate excitation at mm-wave frequencies**

***Keywords* — RF CMOS, back-gate contact, low-power, low-voltage, down-conversion mixer, millimeter-wave communication, linearity, conversion gain.**

I. Introduction

In recent years, Silicon-on-Insulator (SOI) technology is decreasing the gap against III-V and bipolar SiGe by the aggressive downscaling of the transistor gate length [1]. High values of f_{max} are presently around 450 GHz [2], this allows design of high-quality circuits such as switches, LNAs, power amplifiers and mixers. Silicon technology has the main advantage to be low cost at very large scale of integration. Millimeter wave circuits are employed mostly in telecommunication systems [3]. Among those circuits, mixers are playing an important role in translating the frequency to/from the baseband (downconverter/ upconverter). Phase detection, modulation, frequency multiplication are a few application examples of general mixers [4].

In this paper, the design of 5G modular radio receivers are considered, as depicted in Fig. 1. In such an architecture, the RF (6-7 GHz) and mm-wave (26.5-29.5 GHz) signal chains share the RF down-converting hardware, as is depicted. The mm-wave receiver chain contains: (i) the RF receiver chain, and (ii) a down-converting step using a mixer that translates from the 26.5-29.5 band to the 5.5-8.5 GHz RF band.

In this work, a 28 GHz to 7 GHz down-conversion mixer was designed, fabricated and measured using GlobalFoundries' 22FDX® technology. This node offers advanced fully-depleted (FD) silicon-on-insulator (SOI) devices with ultra-thin body and BOX (UTBB) with back-gate terminal accesses [5].

The mixer is based on a double-balanced topology, which offers excellent port isolation [6], and includes active loads and a transimpedance amplifier stage, that contribute to improving mixer conversion gain and linearity, respectively [7-8].

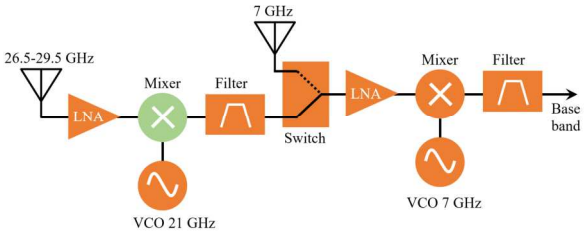

Fig. 1. 5G modular receiver with two stage down conversion architecture.

The major novelty in the proposed circuit is the use of the back-gate as an analog input terminal to which the LO signal is injected (Fig 2). Under this scheme, both the front-gate and back-gate transconductances are actively employed, effectively using the UTBB-FD-SOI transistors as double-gate devices.

First, this paper outlines in Section II the operating principle of such devices, and how they are employed to achieve the desired mixing functionality through dual-gate excitation. Analysis on the optimal biasing conditions at both the front- and back-gate terminals is performed towards maximizing the mixer conversion gain.

Next, a fully differential double-balanced design is proposed in Section III, including an active load, a transimpedance amplification stage, and the balun-based differential feeding and matching circuits. On-wafer measurement results of this fabricated mixer are presented in Section IV.

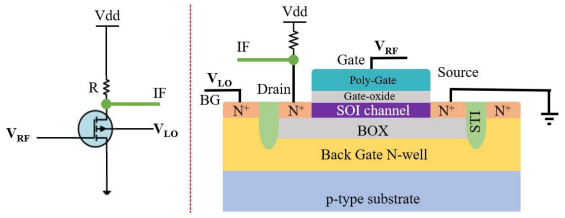

Fig. 2. Basic mixing cell using dual-gate excitation. (a) Schematic diagram. (b) Cross-section of an SLVT-NFET UTBB FD-SOI device.

II. Double-Gate Mixer Operation

A double-gate excited device is depicted in Fig. 2 in a common-source configuration, loaded with a resistor R at the

drain. Analysis based on this simple circuit can serve to describe the mixing function of the signals at the front gate (V_{RF}) and the back-gate (V_{LO}) provided through the non-linear operation of the FET.

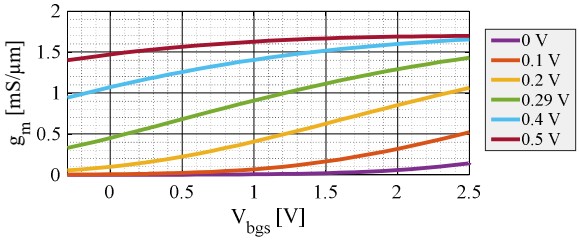

Fig. 3. g_m of the front-gate vs back-gate voltage for multiple front-gate biases, at V_{ds} = 0.5 V.

For this simple branch circuit, we can write the following equation for the current:

$$I_{ds} = \frac{V_{dd}-V_{ds}}{R} = \frac{V_{dd}-V_{IF}}{R} \quad (1)$$

Considering the time-varying RF signal terms, we write:

$$i_{ds} = -\frac{v_{ds}}{R} = -\frac{v_{IF}}{R} \quad (2)$$

Neglecting parasitic elements, the FET's RF drain current can be written as:

$$i_{ds} = g_m(v_{bgs}) \cdot v_{gs} + g_{mb} \cdot v_{bgs} \quad (3a)$$

$$= g_m(v_{LO}) \cdot v_{RF} + g_{mb} \cdot v_{LO} \quad (3b)$$

Where the front-gate transconductance has been written as a function of the back-gate signal. In our case, to implement a mixer, a large-amplitude LO signal will excite the device's back-gate so that it strongly modulates the FET's characteristics (g_m) in time with the LO signal. The device's threshold voltage will then be pulsed in time with $v_{LO}(t)$, and so then will the g_m term. The g_{mb} term is not considered to be dependent on $v_{RF}(t)$ for our application, since the RF signal at the front-gate is considered to be of infinitesimally small-amplitude.

Combining (2) and (3b), we can then write:

$$v_{IF} = -R \cdot g_m(v_{LO}) \cdot v_{RF} - R \cdot g_{mb} \cdot v_{LO} \quad (4)$$

The second term on the right-hand side of Eq. (4) is a signal term at a frequency of f_{LO} (it is usually undesirable at the IF port, and can be avoided using a double-balanced topology, that shall be considered for the full mixer (described in Section III).

The first term however is a multiplication of a term at frequency f_{RF} (voltage v_{RF}) by a term at frequency f_{LO} (term $g_m(f_{LO})$). It then contains a spectrum of frequencies described by $f_{RF} + k \cdot f_{LO}$, where k is an integer. In this work, we wish to use such a mixing principle to design a down-converter, and we are then specifically interested in the signal component of v_{IF} at the frequency of $f_{RF} - f_{LO}$ (i.e. $k = -1$).

The conversion gain of a mixer is defined as the amplitude of the IF signal relative to the RF input's amplitude. It will then be proportional to the first term of the right-hand side of Eq. (4) normalized by the RF input signal's amplitude, and so shall be proportional to $R \cdot g_m(v_{LO})$. We then seek to maximize this term, by appropriately biasing the device's front gate (FG) and back gate (BG), and providing the adequate v_{LO} signal.

Single FET simulations were performed using the PDK models of mm-wave SLVT transistors in order to maximize this $g_m(v_{LO})$ term towards achieving high mixer conversion gain. The results are given in Fig. 3, that plots the device front-gate transconductance g_m for various front- and back-gate DC biasing conditions, for a V_{ds} fixed to 0.5 V.

The back-gate voltage biasing is -0.3 V to +2.0 V. Biasing the DC back-gate point close to +1.0 V then allows for maximum swing in the applied v_{LO} driving the modulation of the FET's behavior.

The front-gate DC bias should then be carefully selected such that the device's current and g_m are strongly modulated by the LO signal at the back-gate. The curves of Fig. 3 show that a front-gate DC bias close to 0.29 V results in the $g_m(V_{bg})$ function with the strongest slope over the -0.3 V to +2.0 V range.

The above analysis of Fig. 3 is performed at a V_{ds} of 0.5 V. Similar analysis was performed at other V_{ds} points. Overall, 0.5 V is chosen, as it is a good compromise between $g_m(V_{bg})$ sensitivity and DC power consumption.

For these reasons, we set the DC operating points of each double-gate excited FET of the mixer topology to V_{ds} = 0.5 V, V_{gs} = 0.29 V and V_{bg} = 1.0 V.

Targeting low power consumption, the V_{dd} point was set to 0.9 V. The FETs and load must then be co-designed to achieve a DC drain-to-source bias of 0.5 V, though too low values of R pull the V_{IF} node towards an RF ground and reduce the conversion gain, and too high values will require very narrow FETs to ensure the bias drop over the devices, which is undesirable as the FET input impedances would then be very high and difficult to match.

Based on these considerations, the width of the mixing FET's width was set to 37.5 µm using a gate length of 20 nm. This width enables the real part of the device's input impedances at the RF, LO and IF ports to be close enough to 50 Ohms to facilitate the matching based on integrated passives available in the technology.

III. A Double-Blanced Desing in 22FDX® with Active Load and Tranimpedance Amplification Stage

Based on the double-gate mixing principles described above, a fully differential double-balanced down-conversion 28 GHz mixer was designed, fabricated and characterized using the 22FDX® node from GlobalFoundries. The FETs sizing, load values and DC bias conditions chosen for the final design correspond to those determined in the above section.

The schematic of the full down-conversion mixer is given in Fig. 5, including the active load and transimpedance amplification stage. As illustrated, the double-balanced topology makes use of four dual-gate excited SLVT nFETs.

A. Double-Balanced Differential Topology

A double-balanced differential topology, shown in Fig. 4, is chosen towards high port isolation between one-another [9].In this topology, the v_{IFp} and v_{IFm} signals do not contain any term proportional to $g_{mb} \cdot v_{LO}$, though that is the case in single-balanced or single-branch topologies (see second term in Eq. (4)). In the double-balanced circuit, a virtual ground is then enforced at the LO frequency at nodes IF_p and IF_m by construction of the circuit, resulting in very high isolation of the

IF port from the LO signal (which can be of substantially higher power than the RF and IF signals).

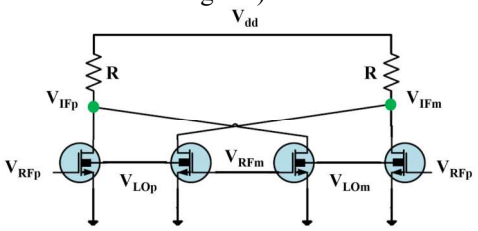

Fig. 4. Double-balanced mixer topology, fully differential at all three ports.

In this topology, the conversion gain is still proportional to the sensitivity of the device's transconductance to the back-gate excitation signal $g_m(V_{bg})$, per the first term of Eq. (4).

B. Active Load

An active load has been used in order to improve the conversion gain. As depicted in Fig. 5, a single pMOS device (FET2) is used in the two side of the double-balanced topology to self-regulate the potential at nodes Y1 and Y2, avoiding the degradation of the conversion gain at higher LO power [8]. By symmetry of the topology, a virtual RF ground appears between the two R1 resistor elements of 5 kΩ. The FET2 devices have a channel length of 20 nm and a total width of 72.5 µm.

C. Transimpedance Amplifier Stage

A transimpedance amplifier (TIA) stage is designed on both sides of the differential circuit, as shown in Fig. 5. Each TIA is composed of: (i) a resistor R2 sized to be 100 Ω, (ii) a pMOS device (FET3) with a total width of 75 µm, and of (iii) an nMOS device (FET4) with a total width of 72.5 µm. The TIA is a buffer that is used as a current evacuator to bleed the drain current at the Y node. The use of a TIA, offers the possibility of using a lower supply voltage (0.9 V in our case targeting low DC consumption) while maintaining sufficient overall conversion gain [10]. Moreover, it has been shown in [8] that the TIA increases the linearity of the mixer.

D. Balun Stages and Port Matching

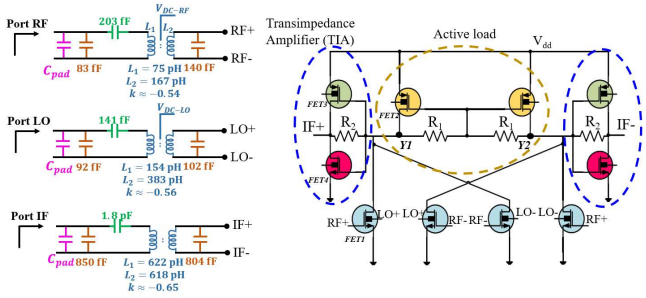

Fig. 5. Schematic diagram of the back-gate topology down-conversion mixer using an active load and a transimpedance amplifier. The baluns at 3 different frequencies are also shown.

On-chip integrated baluns were designed to match and feed the differential terminals of the mixer core to the single-ended GSG pads for the RF, LO and IF ports. Their design provides matching while accounting for the GSG pad capacitance. As shown in Fig. 5, each balun was implemented using (i) a shunt capacitor in parallel with the GSG pad capacitance, (ii) a series capacitance towards a transformer, (iii) an interleaved transformer, and (iv) a shunt capacitance at the core-mixer-side of the transformer. All values determined for these matching baluns are given in Fig. 5, to provide matching at 28, 21 and 7 GHz at the RF, LO and IF ports, respectively.

IV. On-Wafer Measurment Results

A micro-photograph of the mixer is given in Fig. 6. The total area, including the baluns and excluding the pads is 0.150 mm². The core active area (red outline) is around 0.008 mm².

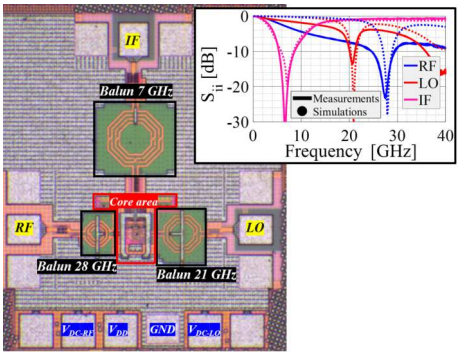

Fig. 6. Photograph of the designed down-conversion mixer. The total area, including the baluns and excluding the pads is 0.150 mm². The core active area (highlighted in blue) is 0.008 mm². Inset: measured and simulated reflection coefficient of each port of the mixer to check to matching of the circuit.

First, S-parameters measurements are calibrated with a Short-Open-Load-Thru calibration performed on an impedance standard substrate to move the reference plane at the probe tips. The measured S-parameters plotted in Fig. 6 demonstrate that the mixer is well matched at the LO port at 21 GHz, at the RF port from 25 to 29 GHz, and at the IF port from 5.5 to 8.5 GHz. Next, large-signal measurements are performed to extract the mixer's FoMs. The conversion gain (CG) is the ratio of the IF power to the available RF power. After calibrating the power of the PNA to the probe tips, an input RF signal at -30 dBm and 28 GHz was injected to the mixer. Then, a power sweep of the LO signal (at 21 GHz) was performed using a separate source from the VNA, while the IF port is connected to one of the VNA's receivers. The conversion gain of the mixer as a function of the LO power is plotted in Fig. 7. The maximum conversion gain achieved is 3.5 dB at an LO power of 10 dBm.

Measurements and simulations agree to within 2 dB for LO powers below 10 dBm and to 3 dB at an LO power of 10 dBm. At higher power, the measured CG degrades starting from 10 dBm, while the simulations predicted a reduction starting from 13.5 dBm. This shift in LO power is as of yet unexplained, but could be attributed to the back-gate RF voltage signal going beyond the specified -0.3 to +2.0 V range. Any voltage below -0.3 V will start to leak current to the substrate through the PN isolation well, resulting in a highly non-linear relationship between g_m and v_{bgs} which causes the conversion gain drop.

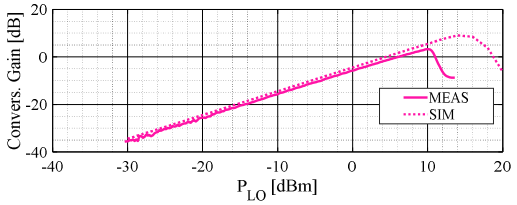

Fig. 7. Measured and simulated conversion gain versus LO power. PRF = -30 dBm, fRF = 28 GHz, fLO = 21 GHz, fIF = 7 GHz.

To evaluate the mixer's bandwidth, the conversion gain is also extracted for other signal frequencies at the RF port, from 24 to 31 GHz. The LO signal is maintained at 21 GHz, and its power is set to the nominal value of P_{LO} = 10 dBm. The IF power is then measured from 3 to 10 GHz. Fig. 8 plots the CG versus RF frequency under these conditions. The results show that peak CG is achieved at 28 GHz, and that the 3-dB bandwidth extends from approximately 27 to 30 GHz.

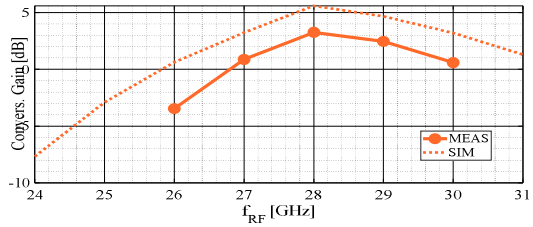

Fig. 8. Measured and simulated conversion gain versus RF signal frequency. PRF = -30 dBm, PLO = 10 dBm, fLO = 21 GHz, fIF = fRF- fLO.

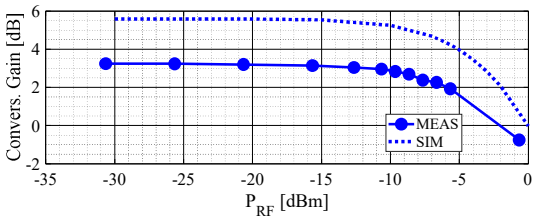

Fig. 9. Measured and simulated conversion gain versus RF signal power. fRF= 28 GHz, PLO = 10 dBm, fLO = 21 GHz, fIF = 7 GHz.

The 1 dB-compression point of the mixer, is extracted by sweeping the RF signal power, and measuring the CG. Those results are plotted in Fig. 9, where the LO power is set to 10 dBm. The compression point is at P_{RF} = -6 dBm where the conversion gain drops to 2.5 dB.

Finally, the third order input intercept point (IIP3) was determined through simulations by defining two tones at the RF port at 28 and 28.3 GHz, both with the same power (P_{RF}), with a 21 GHz LO signal at 10 dBm. The IIP3 is extracted as the intersection of (i) the curve of the fundamental output power at the IF port (7 GHz) plotted vs. P_{RF} and (ii) the curve of the third harmonic output power at the IF port (6.7 GHz) plotted vs. P_{RF}. Simulations reveal that these two curves intercept at a P_{RF} value of 15 dBm. This is defined as the IIP3 metric, and the higher its value, the more linear the mixer.

Table 1 benchmarks these results against the published state-of-the-art down-conversion mixers.

Table 1:State-of-the-art down- conversion mixers operating close to 28 GHz

Work	Techno.	Gain [dB]	f_{RF} [GHz]	P_{DC} [mW]	P_{1dB} [dBm]	IIP3 [dBm]	Area [mm²]	V_{DD} [V]
[11]	180 nm CMOS	-4.5	23-25	16	-5	23	0.72	2
[12]		24	22-26	35	-20	/	0.39	3.3
[13]	90 nm CMOS	10	21-27	38	/	-8.5	0.98	/
[8]		0	20-50	6	-1	9.5	0.48	/
[14]		-3.2	23-30	10	0	21	0.6	1.2
[15]	45 nm SOI	-0.5	28	24	-0.2	17	0.78	/
[16]	**22 nm FD-SOI**	12	25-31	25	-14.8	/	0.64	1.2
This work		**3.5**	**27-30**	**26**	**-6**	**15**	**0.55**	**0.9**

V. Conclusion

A down-conversion mixer using 22 nm FD-SOI technology has been presented, based on a novel topology that makes use of UTBB device back gate nodes as signal input terminals. The circuit is based on a double balanced topology using 4 SLVT nFETs that are excited as dual-gate device, with RF signals (28 GHz) inputted to their front-gates and a simultaneous back-gate excitation of LO signals (21 GHz). An active load was designed to increase the mixer's conversion gain, and a transimpedance amplification stage was included to provide higher linearity. The low-power (25 mW) low-voltage (0.9 V) design provides competitive performances compared to state-of-the-art mm-wave CMOS mixers, achieving a peak conversion gain of 3.5 dB, an IIP3 point of 15 dBm, and a P1dB of -6 dBm.

Aknowledgement

The authors would like to thank GlobalFoundries chip fabrication and research report. This work was partially supported via Beyond5 ECSEL project.

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