Low-Frequency Noise Transistor Performance for UTBB FDSOI MOSFET-C Filters

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***Abstract*— This work investigates the low-frequency noise performance of a long-channel UTBB FD SOI nMOS transistor operated in triode region as typically used for MOSFET-C filter applications. Measurements of the low-frequency noise have been performed over a large temperature range (25–125ºC) at different constant currents above threshold, as a function of the back-gate bias. It is highlighted that in such case, 1/f noise power is dominant, however sufficiently low, in the frequency range of interest for the filters, i.e. below 1 MHz. Noise power strongly reduces with temperature and slightly with positive back-gate bias, which is adequate for the filter tuning.**

Keywords— UTBB-FDSOI; Low-Frequency Noise; MOSFET-C filter

I. Introduction

Ultra-Thin Body and Buried oxide (UTBB) Fully Depleted Silicon on Insulator (FDSOI) CMOS technology has shown great promise for low-power operation of digital, analog and RF circuits [1-3] such as in future Internet of Things (IoT) or 5G applications. Notable advantages for analog circuits are the significant reduction of mismatch and 1/f noise thanks to the low-doped channel, increase of the intrinsic analog gain resulting from the excellent electrostatic control of the channel as well as potential threshold-voltage tuning using the back gate, e.g. to improve operating voltage range or mitigate Process-Voltage-Temperature (PVT) variations [4].

A particular case of analog circuits concerns the MOSFET-C structures typically used to integrate active continuous-time CMOS filters in frequency bands ranging up to 1 MHz [5]. Fig. 1 shows the basic schematic of a MOSFET-C integrator using MOS transistors operated as resistors, i.e. in triode region with a tunable DC gate voltage to achieve a constant on-resistance (R_{on}) over all PVT variations. The typical RC specifications of such filters impose a R_{on} in the range of 100 kΩ. In addition, mismatch, third-order harmonic distortion (HD3) and low-frequency noise have to be minimized. Long-channel transistors are hence preferred. In [6], we have investigated and demonstrated, by circuit-level simulations, the capability of UTBB n- and p-MOSFETs to achieve the specified R_{on} with an HD3 below -60 dB, over a large range of temperatures from -25 to 150°C combining front- and back-gate tunings.

In this paper, we focus on the low-frequency noise of the nMOS transistor which exhibited lower HD3 in a suitable range of front and back-gate voltages. To our best knowledge, the 1/f noise characteristics of such large and long UTBB MOS transistors operating in triode region and under such high temperature range have not been discussed previously.

This work was partially funded by Eniac “Places2Be”, Ecsel “Waytogofast” and ARC “Nanosec” projects

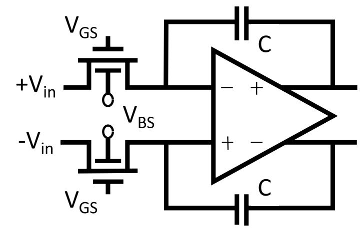

Fig. 1. MOSFET-C filter concept.

II. Measurements

A typical UTBB long-channel nMOS transistor was measured in 28 nm FDSOI CMOS process from ST-Microelectronics [1]. Equivalent gate oxide, Si body and BOX thicknesses are 1.3 nm, 7 nm and 25 nm respectively. Ground plane was implemented under buried oxide, allowing back-gate biasing. Further process details can be found in [1]. Gate length is 2 µm and width is 1 µm. The transfer and transconductance characteristics were measured in triode regime at drain-to-source voltage V_{DS} = 50 mV and back-gate voltages V_{BS} = -0.5, 0 and 0.5 V, at three temperatures, T = 25, 75 and 125°C (Fig. 2).

The low-frequency noise power spectral density (PSD) was measured using Keysight ALFNA noise analyzer [7]. In order to correspond to a constant R_{on} when varying V_{BS} and T, noise measurement were performed at constant DC currents of 2 or 4 µA, respectively corresponding to biases close to the zero-temperature coefficient (ZTC) point (fig. 2.a) or to the maximum transconductance value (fig. 2.b). Minimum HD3 is achieved for such bias range, as determined in [6].

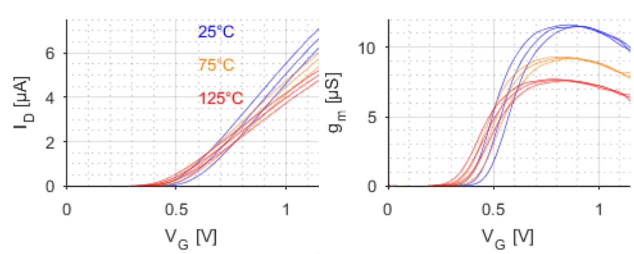

Fig. 2. Drain current and Transconductance of the DUT versus V_{GS} at V_{DS} = 50 mV and V_{BS} = 0.5, 0 and -0.5 V (curves from left to right), for 3 different temperatures (colors).

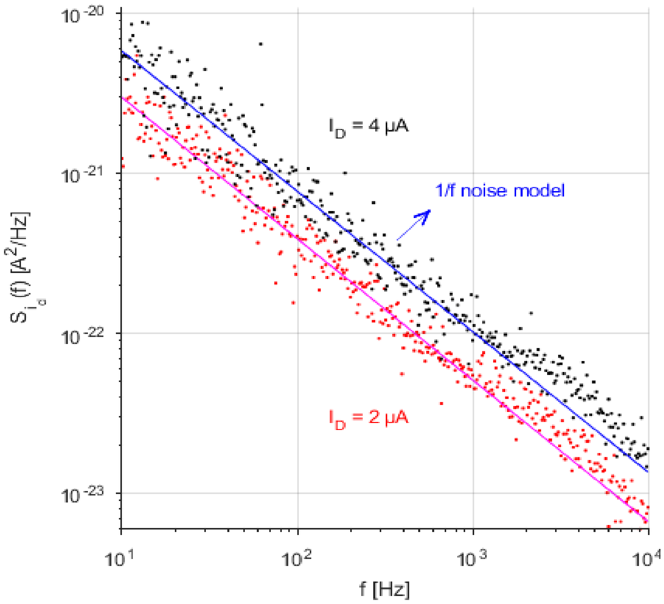

Fig. 3. Measured and fitted PSD at room temperature and V_{BS} = 0 V for the two current levels.

The measured and fitted room-temperature PSD are depicted in Fig. 3, at V_{BS} = 0 V, demonstrating a dominant 1/f noise characteristic as expected for long-channel transistors in strong inversion. The noise amplitude well corresponds to circuit simulations using the compact model of the industrial design kit for a typical device operating at the drain current. The 1/f dominance has been confirmed in the whole back-gate bias and temperature ranges considered here.

III. Temperature and Back-gate bias effects on Noise Power

To avoid an impact of noise measurement fluctuations on the V_{BS} and T trends, the total noise power is considered as the relevant figure of merit for MOSFET-C filters, and is obtained by integrating the PSD over their typical frequency bandwidth from 10 to 1000 Hz (Fig. 4). In all cases, the noise power dependence on current level, back-gate bias and temperature follows the carrier number with correlated mobility fluctuations model, due to the contribution of the front and back channel interfaces [8]:

- the noise reduction with temperature is strongly correlated with the transconductance;
- the stronger V_{BS} dependence at lower current level can be explained by the larger contribution of the back-channel conduction closer to threshold.

Similarly to our previous observations on HD3, at constant current, noise can be lowered when applying a positive back-gate bias with a higher importance at lower temperature and reduced current level. In the operation range of interest, the worst-case signal to noise ratio is about 80 dB, which is very suitable for the targeted circuits.

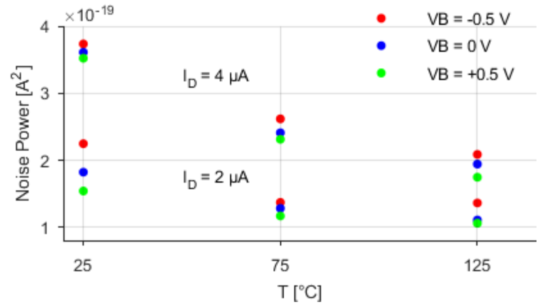

Fig. 4. Integrated noise power measured at various current levels, back-gate biases and temperatures.

IV. Conclusions

The low-frequency noise performances of a large-size UTBB FDSOI nMOS transistor operating in triode region have been investigated at different temperatures, current levels and back-gate voltages. The effects observed on the measured 1/f noise power have been related to the transconductance dependence and back-interface contribution according to [8]. Along with their low mismatch and HD3 properties, the devices exhibit excellent low-frequency noise performance, thus suggesting them as promising candidates for MOSFET-C filter applications.

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