

Triple-Gate FinFETs for Very High Frequency Applications

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1. Abstract

This last decade silicon MOSFETs have demonstrated their potentialities for very high frequency applications. Thanks to the successful shrinkage of transistor size, cut-off frequencies (f_T) in the order of 500 GHz have been achieved. In this scenario, the International Technology Roadmap of Semiconductors (ITRS) has established that the analog performance of the MOSFETs will continue growing as the channel length will be shrunk beyond a few nm [1]. Fig. 1 shows the projections of the cut-off frequency, according with the ITRS, for two technologies: Ultra Thin Body transistors (UTB) and Multiple-Gate Transistors (MuGFETs). As can be seen from Fig. 1, the projections on MuGFET indicate that f_T will reach the THz range for technology nodes about 10 nm [1]. Nowadays, triple-gate FinFET transistors which exhibit high immunity against SCE [2] are promising candidates to pursue the downscaling of CMOS transistors beyond 22-nm node, emerging as a suitable MuGFET device. However, it has been also shown that, due to its tridimensional nature, FinFETs exhibit very large parasitic gate capacitance (C_{gge}), which is even higher than its intrinsic counterpart for sub-100 nm technology nodes [3]. As a consequence the transistor's f_T is dramatically reduced due to those fringing parasitic capacitances [4].

2. Extrinsic Gate Capacitance

Fig. 2 shows the comparison of the extracted cut-off frequency, for different channel length devices, including the whole parasitic effects (f_{Te}), the cut-off frequency with the extrinsic series resistances removed (f_{TR}) and the cut-off frequency after withdrawing the parasitic resistances and capacitances (f_{Ti}) as a function of the FinFET channel length [4]. As it can be observed, intrinsic cut-off frequency of about 400 GHz can be achieved for 60-nm devices, however when the parasitic capacitance is included, a strong reduction of f_T is measured, with values of about 100 GHz [4].

Therefore, in order to meet the ITRS projections, it is of

first importance to reduce as much as possible C_{gge} . In this context a new semi-analytical model for C_{gge} has been presented in [5]. This model considers five different components which are directly linked to the 3D physical architecture of FinFET. Fig. 3a shows the comparison of C_{gge} obtained from the model and from 3-D numerical simulations for different channel lengths and Fig. 3b for different fin widths [5].

3. FinFET Modeling

Recently, an analytical compact model for SOI Symmetric Doped Double Gate MOSFETs (SDDGM) was implemented in Verilog-A, where its applicability for SOI FinFETs was demonstrated in [6] as well as its capability to reproduce the small-signal parameters from dc characteristics [7]. The SDDGM compact model considers the doping concentration of the silicon layer from lowly to highly doped, which provides good agreement with numerical calculation of the potentials. Field dependent mobility as well as SCEs, such as DIBL, channel length modulation and velocity saturation, have been included [7]. Additionally, the parasitic gate capacitances as well resistances have been included.

Fig. 4 shows the comparison between the experimental and modeled transfer and output characteristics (a), as well as the comparison for the transconductance and conductance (b), for 250 and 500 nm devices. Fair agreement is achieved.

4. Conclusion

As the channel length of FinFETs is reduced below sub-100 nm, their extrinsic capacitances become larger than their intrinsic ones. As a consequence, the total gate capacitance is dominated by the extrinsic parasitic components which lead to an important degradation of their RF performance. A semi-analytical model for describing the total parasitic gate capacitance as been shown and included in a compact model which is extended in a Verilog-A implementation of the SDDGM

compact model for SOI FinFETs in a SPICE simulator.

References

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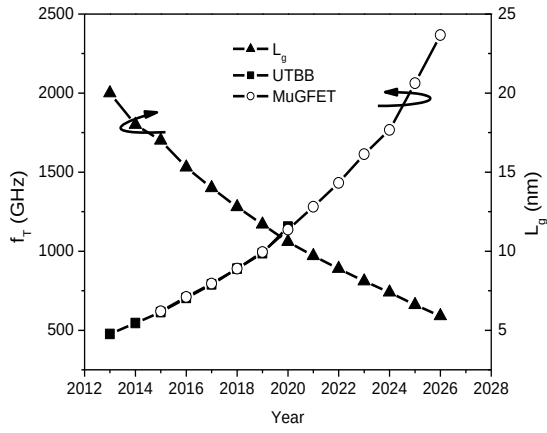


Fig. 1. Cut-off frequency projection according with the ITRS [1].

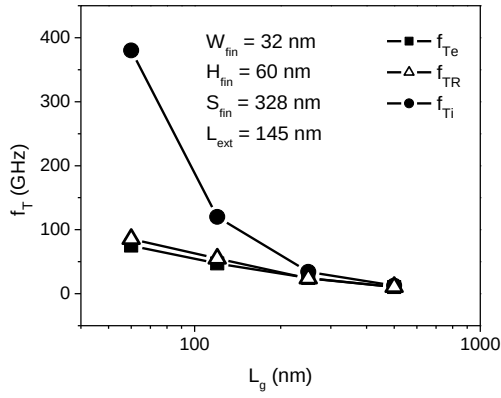


Fig. 2. Measured cut-off frequencies versus channel length [4].

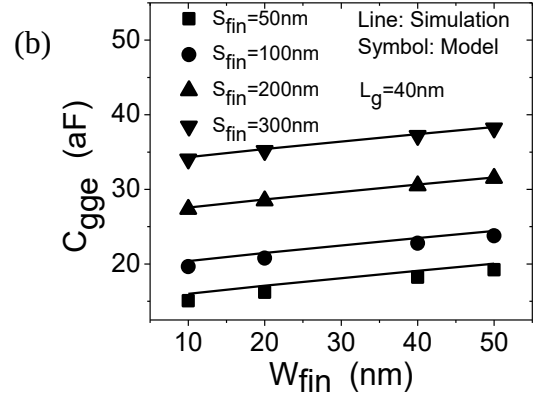
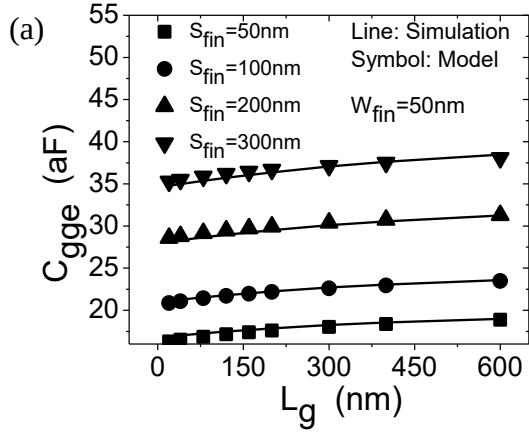


Fig. 3. Measured cut-off frequencies vs. (a) channel length and (b) fin width [5].

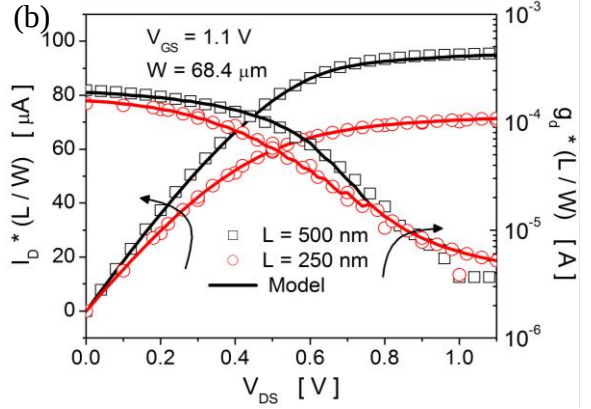
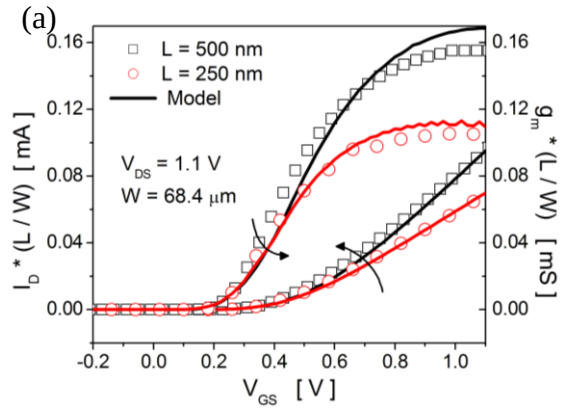


Fig. 4. (a) I-V characteristics, (b) transconductance and conductance [7].