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SOIPIX R&D programme and applications

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ABSTRACT: SOIPiX is a R&D project targeting the development of monolithic pixel detectors with Silicon On Insulator technology for future high energy physics experiments, X-ray experiments, and other applications. It integrates both radiation sensors and LSI circuits in one chip to achieve high resolution and intelligent detectors. After a short introduction about the advantages of monolithic active pixel sensors, the main characteristics of SOI monolithic sensors will be discussed: technological process, response to incident radiation and radiation hardness. Special attention will be given to the description of the so-called "back-gate" effect and the different techniques developed to mitigate it. Finally, various applications of this technology will be presented.

KEYWORDS: Solid state detectors; Radiation-hard detectors; Materials for solid-state detectors; Silicon On Insulator.

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1. Introduction

Semiconductors have been used as radiation sensors for more than 50 years. A comprehensive description on how semiconductors can be used as a particle detectors can be found elsewhere[1, 2, 3]. In the following it is assumed that the reader is familiar with semiconductor physics and its use in particle detection.

The first semiconductor detectors in the 1960's were designed for high count rate and energy resolution. At that time semiconductor radiation detectors were based on highly pure materials, such as Ge. Most of the time these detectors were cooled down to cryogenic temperatures, had little or no spatial resolution and were readout by large electronic boxes. These detectors were composed of a large fully depleted diode and they were a major step forward in spectrometry improving energy resolutions by orders of magnitude with respect to scintillation detectors [4]. These kind of detectors are also referred to as pad detectors.

It was only in the 1980's that microelectronic industry techniques were applied to semiconductor sensors [5, 6, 7, 8], allowing for micron-scale patterning and the development of position sensitive detectors.

Semiconductor tracking devices make intensive use of planar technology based in oxide passivation, micro photolithography and ion implantation. When we talk about position resolution in

semiconductor devices we have to think of positions in a 2D plane. The third coordinate is obtained by the positioning of the semiconductor device.

To obtain spatial information two basic structures have been used in the design of semiconductor radiation detectors:

- Strip, or microstrip, detectors, in which several relatively narrow ($\sim 10\mu$m) and long (~ 10 cm) implants are made on a high resistivity substrate. This kind of detectors are at the origin of the development of semiconductor detectors as tracking devices [9] and since then they have become the standard detectors in particle tracking systems in High Energy Physics. Strips detectors provide a precise measurement in one dimension. In order to obtain two dimensions we need to use two planes with non-collinear strip orientation or double sided strip detectors where the two surfaces of a planar detector are processed with (micro)pattern strips. Typical sizes for the pitch between strips are 25-100 μm.

- Pixel detectors, where high granularity is achieved in two dimensions, are most of the time arranged in a grid layout although other layouts such as honeycomb are also used. Pixel semiconductor detectors are nowadays ubiquitous such as those used if CCD digital cameras. Pixel detectors automatically provide the position in a plane and no further external information is needed to solve ambiguities. Typical sizes for pixels are 20-200 μm

1.1 Hybrid and Monolithic Devices

Along with the detector structures themselves, readout techniques have been developed to deal with the density of readout channels which explodes with increasing granularity. For the three types of structures described above the number of readout channels is $\sim$1/cm^2 for pad detectors, $\sim$100/cm^2 for microstrips and $\sim$ 10000/cm^2 for pixel detectors.

With this large readout channel density the use of microelectronics chips is needed. The current state of the art are hybrid detectors in which the detector (high resistivity substrate) is fabricated separately from the readout electronics (low resistivity substrate).

In case of microstrips the connection of individual strips to readout electronics can be done by wire bonding pads on the detector side to a readout electronics chip placed at the edge of the detector. This technique requires precise machining as the distance between wires can be only a few tens of micrometers.

For pixel detectors the size and density of the connection of individual pixels to readout electronics making wire bonding impractical. Basically two techniques can be applied: sharing of readout circuitry and bump-bonding.

- Sharing of readout electronics circuitry by many pixels. This technique implies the measurement of each pixel should be stored locally and transferred when needed to be readout. One common technique is to readout all pixels in a column with the same readout circuit. In this case, a wire bonding technique can be used to connect each column to an external readout chip. Another technique is to use just one electronics circuit to readout the whole sensor, as is the case of CCDs [10]. The price to pay is on the one hand the need for transmission lines and control structures to connect each individual pixel to readout electronics and on the other hand an increase of the readout time. Lowering the number of electronic channels increases the amount of readout time.

- The second technique is the bump-bonding technique in which each individual pixel is connected to an individual readout channel that lies in an independent chip through a solder ball. This technique [11] requires the deposition and treatment of the solder material in one of the chips, the careful alignment of both chips to be connected and the control of the good planarity of both chips in order to have an almost 100% yield on all bump-bonds when large surfaces (>5-10cm^2) have to be bonded. This technique is limited by the alignment accuracy and the complexity of the process. Only a few technological centres and companies can perform it with reasonable yields.

In the case of High Energy Physics, the bump bonding technique is the one favored so far. However it has some shortcomings that will be quite difficult to overcome. The first is that pixel size is limited by the bump-bonding technique. In current experiments the pixels sizes are of the order of $100\mu\text{m}\times100\mu\text{m}$. The second problem is that it introduces extra passive material that may cause problems in tracking devices. Last but not least it is a relatively complicated and costly procedure both in terms of time and money.

In order to solve these problems an intensive research program in the so called monolithic active pixel detectors (or MAPS) where electronics and detector are in the same substrate has been carried out since $\sim$10 years. Pixel sizes may be reduced down to tens of microns per side, the material budget introduced by the readout can be reduced to a few microns and the expensive step of bump bonding may be avoided.

However, to benefit from these advantages, one has to overcome the challenges of building a monolithic detector . Constructing the detector often involves extra non-standard process steps that have to be optimized. Since the sensor and the electronics are now on the same substrate, they may interfere electrically with each other. Placing the electronics close to the detector will also expose the electronics to high levels of radiation. These challenges have to be overcome before the potential of monolithic detectors can be fully realized.

Research in monolithic pixel sensors has been ongoing since the 1990's [14] although large scale applications are only starting to be built. Some of the more important research projects in monolithic pixel sensors are DEPFET, MIMOSA, HVMOS and Through Silicon Via (TSV) or 3D-integration [15].

In the following we will focus on monolithic detectors based in the Silicon On Insulator technology (SOI). We will describe the basis of the SOI technology, how a monolithic detector can be realized with this technique and the description of the problems that showed up as well as the solutions to overcome them provided by the SOIPIX collaboration [12].

2. SOI Technology

SOI (Silicon on Insulator) technology is a well known technique that has long been used to build field-effect transistors on thin semiconductor film. In fact, the first field-effect transistor patent issued in 1928 was for a device similar to current SOI devices, although due to technology limitations there is no evidence this device ever worked [13]. In the 1960's when planar processing technology became available, circuits built on a bulk silicon wafer dominated the industry although SOI circuits appeared in niche applications such as the military and space industries due to their

higher radiation hardness to single event effects. The mass production of SOI circuits occurred in 1998 when IBM decided to use the technology for its PowerPC MPU. Currently, SOI is used in the RF wireless communications industry by companies such as Peregrine, RFMD, and Skyworks with technologies down to $0.13\mu m$ in 2013. ST Microelectronics already has 28nm FD-SOI technology in production for use in low power mobile applications, with 20nm and 14nm FD-SOI technology in development.

2.1 SOI Wafer

An SOI wafer consists of a thin top active silicon layer on top of an insulating layer. The top active silicon layer can range from less than ten nanometers to a few hundreds of nanometers thick. The buried oxide (BOX) layer is on the order of a few tens of nanometers thickness with advanced processes developing thin buried oxide layers 15nm to 20nm thick. The bottom handle wafer is typically 300-500 μm thick and can be thinned down as required.

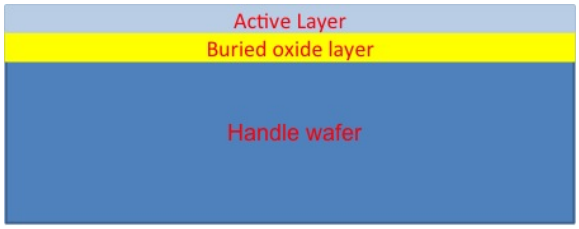

Figure 1. Schematic of an Silicon-on-Insulator wafer

The first SOI wafers for large commercial integrated circuits use were produced in 1978 by K. Izumi. His method called SIMOX (Separation by Implanted Oxygen) involves implanting a silicon wafer with a high fluence of oxygen atoms. The wafer is then annealed, allowing a SiO_2 layer to form under a thin silicon layer. The SIMOX method produces high quality wafers but is an expensive process due to the large oxygen implantation.

Another method of SOI production called Smart Cut^{TM}was patented by M. Bruel [16]. This method begins with two different wafers. The first wafer is oxidized to create a top insulating layer and then implanted with H+ ions which forms a weakened layer inside the wafer, near the top. The first wafer is then bonded to the second wafer and cleaved along the weakened layer, leaving behind the insulating layer and a thin silicon layer. A wafer formed with this technique is called a UNIBOND^{TM}wafer.

The UNIBOND^{TM}wafer is of particular interest to detector development because the top and bottom silicon layers can be different. In most applications, the bottom layer only acts as a mechanical support for the electronics in the thin top active layer, but for detector development, the bottom handle wafer may be used as the sensor active volume. Having two different wafers allows the optimization of layers: high resistivity for the sensor layer and low resistivity for the CMOS circuitry layer. These wafers are now available commercially, notably from SOITEC [16] amongst others.

2.2 SOI CMOS vs. Bulk CMOS

There are several advantages to using SOI CMOS technology over standard bulk CMOS. As shown

in Figures 2 and 3, in a standard bulk process each transistor is insulated by a well structure with a pn reversed biased diode. In SOI, each transistor is better insulated with an oxide insulator, thereby reducing parasitic effects. For high speed circuits, the capacitive coupling of the source and drain to the bulk substrate may limit performance; in SOI this coupling is reduced by the BOX. The absence of the well structures in SOI enables more compact circuit layout so that more circuitry can be included in the same die area.

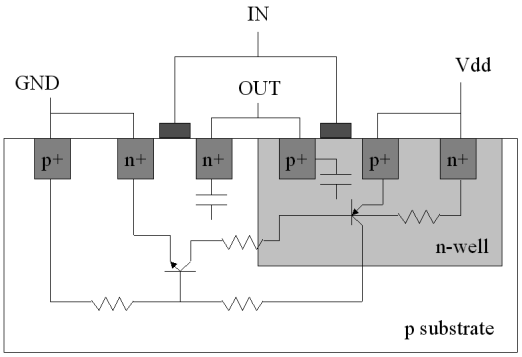

Figure 2. Bulk CMOS

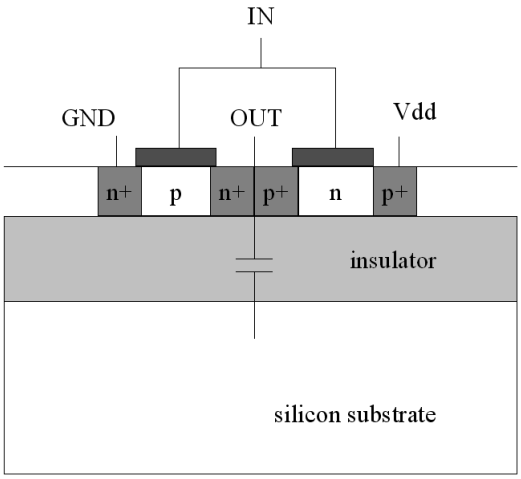

Figure 3. SOI CMOS

In regards to radiation performance, bulk CMOS are known to have a parasitic PNPN device in the substrate which may cause latch-ups; this parasitic device does not exist in SOI devices. The thin active layer in SOI devices reduces the amount of charge generated in the active area, making SOI devices less susceptible to single event effects. However, SOI devices may be more susceptible to total ionizing dose (TID) due to the numerous Si and SiO_2 interfaces and thick BOX. SOI devices have been shown to withstand up to Mrads of radiation. At higher doses however, charge buildup in the BOX can lead to transistor threshold voltage shifts [17].

Two types of SOI transistors exist: partially depleted (PD-SOI) and fully depleted (FD-SOI). PD-SOI has a thicker top active layer (often around 70-200 nm) while the FD-SOI has a thinner active layer. Figure 4 illustrates the two. In PD-SOI transistors, a neutral region in the body exists, which can lead to floating body effects such as kink[1] and history[2] effects [18]. While the kink effect increases the drivability of the circuit making it useful for high-speed digital circuits, the body effects are not desirable in analog circuits and require careful design techniques. In FD-SOI, the entire body under the gate is depleted, resulting in significantly reduced body effects. However, the fully depleted body presents more coupling to the buried oxide resulting in more susceptibility to TID effects in the buried oxide. Thick buried oxides present more TID effects but BOX thicknesses are decreasing, down to less than 100nm. In advanced processes, BOX thicknesses close to 10nm are being studied [19]. As the first stage in a detector readout chain is always analog, FD-SOI is the natural choice to build monolithic pixel sensors.

[1] Kink effect: Appearance of an "kink" in the output characteristics of SOI MOSFET (I_d vs V_d)

[2] History effect: dependence of the threshold voltage of the transistor on its previous state

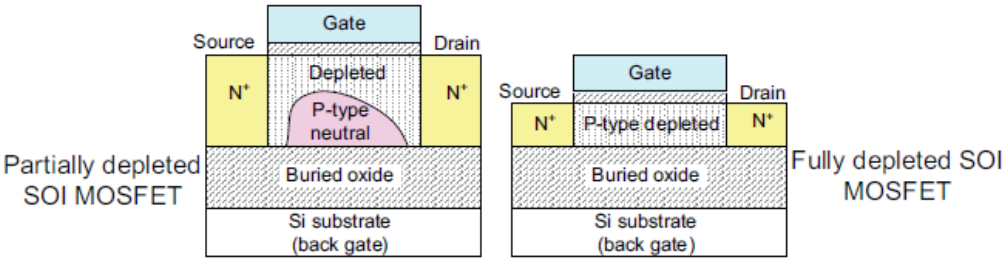

Figure 4. Partially depleted and Fully depleted SOI MOSFETs [18]

2.3 Main features of SOI technology features

The main features of the SOI technology that make it appealing for particle detection are [20]

- Small Junction Capacitance. Junction capacitance in FD-SOI is $\sim \frac{1}{10}$ of bulk technology. Notably gate capacitance in MOS transistors is 30-40% lower than in bulk technology. Both effects combined allow higher speeds in SOI.
- Low Power Consumption. As gate voltage is not wasted to deplete the bulk, lower threshold voltage can be achieved without increasing the leakage current. Slopes of 68 mV/dec have been measured on I_{ds} vs V_{gs} plots (∼85-95 mV/dec in case of bulk technologies)
- Radiation Tolerance. As the active layer is quite thin and isolated from the bulk of the handle wafer, SOI devices are almost immune to single event effects. On the other hand, the presence of the BOX layer is a charge trap, making these devices sensitive to total ionisation dose. The main effect is a change in the electric field configuration and a drift of the transistors threshold voltage.
- TID Damage Compensation. TID effects can be corrected by changing the electric field. This can be done polarising the back plane as shown in Figure 5, where it has been shown that threshold voltage and leakage current can be almost completely corrected.
- Operation at Cryogenic temperatures. Contrary to bulk CMOS where kink effects and hysteresis appears when operating at cryogenic temperatures, SOI devices continue to work. The reason is that the channel formation is much less dependent of the temperature than in bulk CMOS devices due to the thin active layer.

3. SOI for Particle Detection

SOI technology can be used to create a particle detector by the realization of a diode in the bottom handle wafer and the integration of the readout electronics in the top active layer. The two parts are separated by the middle oxide layer so that vias are required to connect the two parts, as shown in Figure 6. Each layer can be optimized for its intended application; the bottom handle layer for the sensor can be made of high resistivity silicon and the top active layer holding the electronics can be made of lower resistivity silicon. This structure avoids the need for complicated bump bonding procedures.

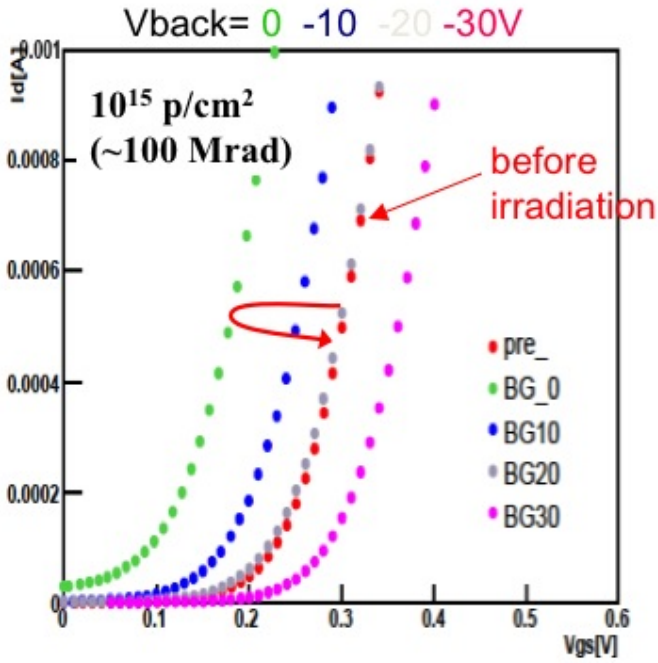

Figure 5. TID damage compensation by biasing the back side. This test was done by irradiating a standard SOI wafer with a flux of 10^{15} p/cm^2 with transistors in the active layer

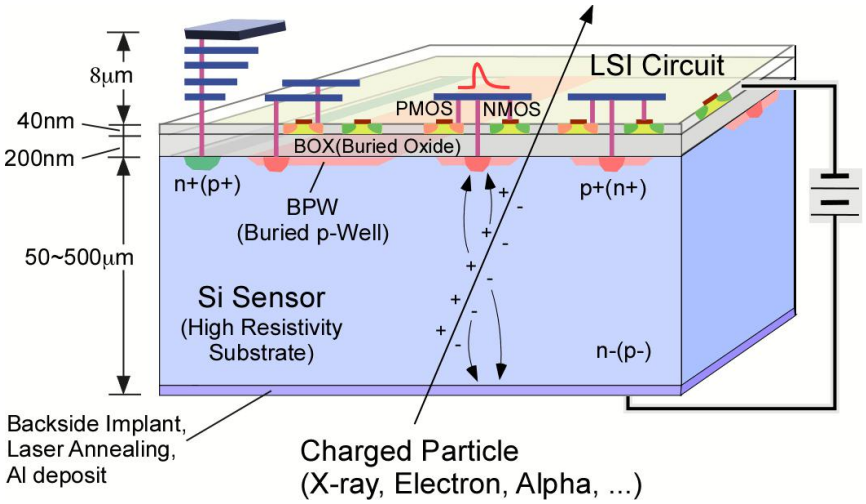

Figure 6. SOI wafer used as a monolithic detector. A sensor is created in the bottom handle layer and connected to the readout in the active layer with metal vias.

As a result, the detector and readout electronics may be processed together in one monolithic device. Complications arising from this device include the extra processing steps required to create the diode and through vias.

Three main issues arise with this configuration related to the SOI configuration

- Back-Gate effect (figure 8-left). In order to operate the detector, the sensor in the bottom

layer should be depleted. This requires biasing of the detector where a voltage is applied to the bottom substrate. This voltage generates an electric field throughout the bottom layer which may affect the electronics in the top active layer. To solve this problem, the electric potential at the bulk-buried oxide interface should be fixed. This means the introduction of extra structures.

- Charge carrier trapping in the buried oxide layer due to total dose irradiation effects. It's almost impossible to avoid this charge trapping, but it has been demonstrated that by changing the electrical configuration their effects can be corrected. Again the solution involves the control of the electric field in the oxide region.

- Cross Talk induced by capacitive coupling of the pixel implant with electronics structures in the active layer through the bulk. In order to avoid this cross-talk, suitable shielding should be placed locally.

If we want to use an SOI device as radiation detector all three issues should be solved or minimized.

4. SOIPIX collaboration

Research in using SOI to build a monolithic detector was first published in 1993 by Diebrickx and others [22]. However, due to limitations in SOI wafer processing techniques at the time, a complete working detector was not built. In the 2000's, the SUCIMA project has investigated the use of SOI to build monolithic detectors for medical applications [23]. In 2005, monolithic detector development in SOI technology began at KEK in Japan. KEK initiated the SOIPIX collaboration [12], an international collaboration of research organizations with a common interest of developing pixel detectors in SOI technology. The foundry at OKI Semiconductor based in Japan was used to produce the first prototypes. OKI Semiconductor was acquired by ROHM Semiconductor in 2008 and has since been renamed LAPIS Semiconductor [21].

In 2006, the first multi-project wafer (MPW) of the SOIPIX collaboration was performed. MPW runs permit several research institutions to share the cost of manufacturing by placing several project layouts on one wafer. The first SOI detectors were developed in $0.15\mu m$ OKI technology [24]. In 2007, the $0.15\mu m$ process line was shut down and pixel development was moved to a $0.2\mu m$ process line. Current SOIPIX participants include mainly Japanese institutions, but also institutes from the United States and Europe. About two MPW runs are performed per year.

Besides the management of MPW runs, SOIPIX has also steered the technological advancements mainly in the mitigation of the backgate effect with the development of various shielding structures: the buried wells and the double SOI. Although there are other developments on shielding structures, as the so called nested wells, these two are the most important and the ones that the community has more widely implemented.

As important as the microelectronic processing is the quality of the SOI wafers. In the case of SOIPIX process, the wafers, as well as all the innovative developments, have been provided by SOITEC. Microelectronics processing has been assured by LAPIS.

4.1 LAPIS-SOI technology

In Table 1 the main characteristics of LAPIS-SOI technology used by the SOIPIX collaboration for MPW runs are shown.

Process	0.2 μm low-leakage FD SOI CMOS 1 Poly, 5 Metal layers MIM Capacitor (1.5 fF/μm^2), DMOS Core (I/O) Voltage = 1.8 V (3.3 V)
SOI wafer	Diameter: 200 mm; 720 μm thick Top Si: Cz $\sim$18 Ω-cm, p-type, $\sim$40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz(n)$\sim$700Ω-cm FZ(n)$\sim$7kΩ-cm FZ(p)$\sim$25kΩ-cm
Backside	Thinned to 100-500 μm mechanical grinding, chemical etching Back side implant, laser annealing and Al plating (200 nm)
Transistors	Normal and low threshold transistors for both core and IO Three structures: body floating, source-tie and body-tie

Table 1. Summary of SOIPIX process technology properties.

4.2 Buried Wells

This shield technique consists of extending the implants of high doping regions in the sensor side with low doping regions. High doping regions are for instance present in the pixel implants or in dedicated implants for biasing purposes and always require a via through the BOX. The extension of these regions can be done with implantations that do not need an opening in the BOX. Depending of the bulk substrate we will use buried p-wells (BPW) for n-type bulks and buried n-wells (BNW) for p-type bulks.

This technique has the advantages that it allows for the shrinkage of the pixel implant without losing sensitive area as well as increasing the breakdown voltage because of the low doping regions. To properly operate these wells, they should be fixed to a voltage. Biasing the wells solves the back-gate effect (Figure 8), but it does not avoid the charge carrier trapping in the BOX, so it does not solve the radiations issue as shown in figure 9.

4.3 Double SOI

As it can be seen in the figures, the effect on the transistors transfers characteristics in Figures 8 and 9 is almost the same as, although the origin is different. In the end the result is the same: a modification of the electric field in the channel region. One possibility to solve this is to have two voltages close to the electronics that can be controlled, one to screen to back gate effect and another to correct for the charge concentration in the BOX. This is the main idea of the double SOI structure (also called SOI2). Basically it consists in having a stack with two SOI structures, as

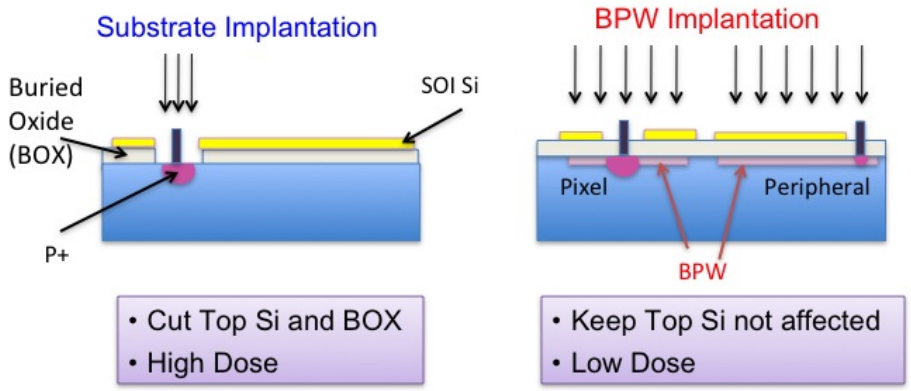

Figure 7. Buried P-Well. For substrate implantation an aperture in the BOX is needed (left panel). This substrate implantation defines the core of the pixel. In order to enlarge this, ion implantation can be done (right panel).

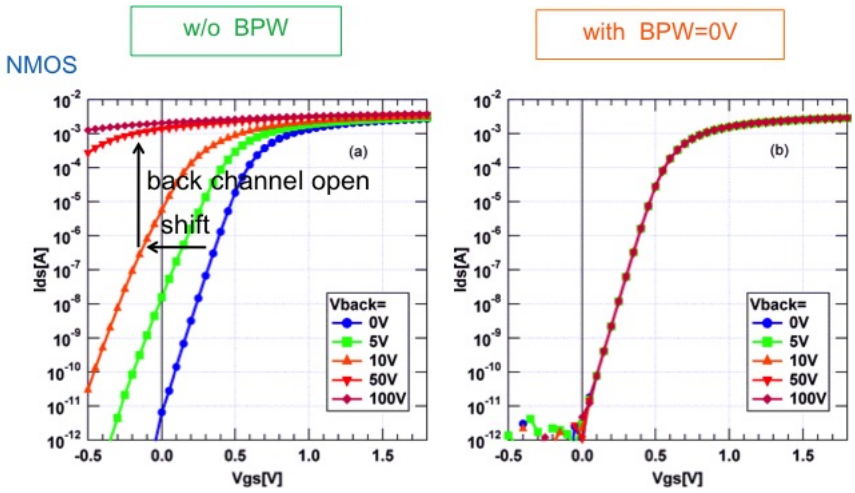

Figure 8. Back gate effect (left pannel) in which is seen the drift of the threshold voltage as a function of the back voltage. In case BPW is presented and fixed to a potential this effect disappears (right panel).

shown in Figure 10, with two BOX layers and one silicon layer buried among them. Technological implications are not easy to solve such as opening vias through the bulk to the buried silicon layer and assuring a good electrical conductivity in this layer. All these technological issues have been solved with a dedicated research program both at the SOI wafer supplier (SOITEC) as with the foundry (LAPIS).

In Figures 11 and 12 show that by controlling the middle Si layer both effects (back gate and TID) can be solved. In combining both screening techniques, buried wells with SOI2, both effects could be corrected. The buried wells will fix a potential that will solve the back-gate effect and the middle Si layer voltage can be adapted to correct the charge trap in the BOXes.

5. SOIPIX projects

Research projects in which SOI technology for particle detection as described above is used can be

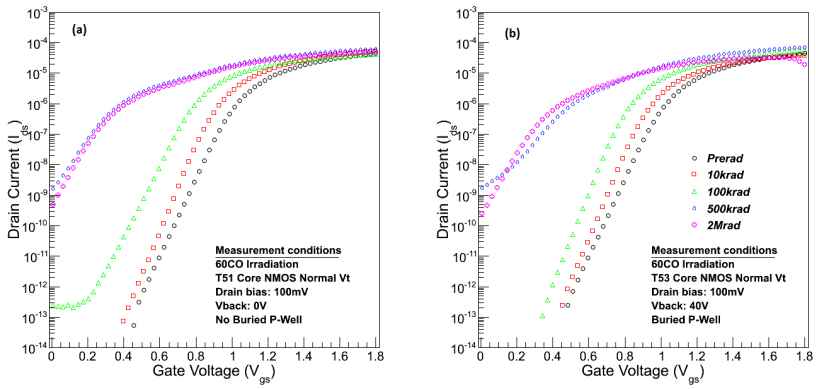

Figure 9. Effect of TID in a transistor with and without BPW. As charge trapping occurs after BPW shielding, TID effects are seen clearly in both cases.

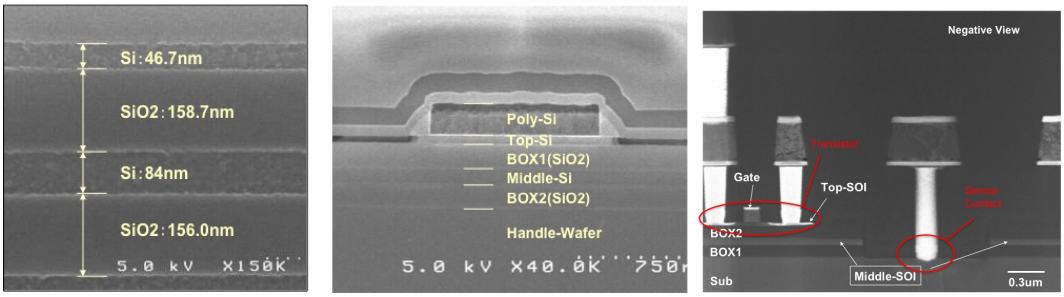

Figure 10. Double SOI SEM

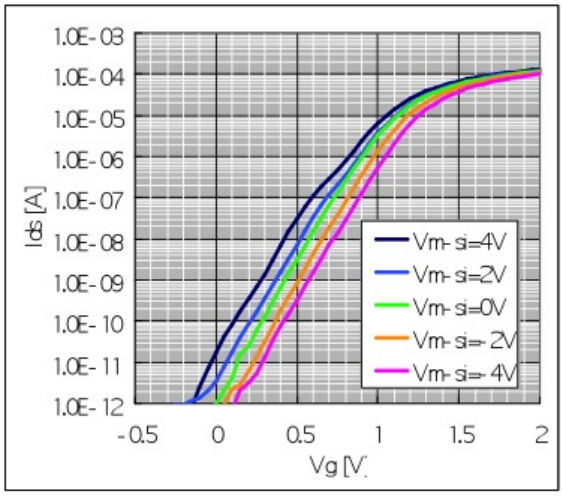

Figure 11. Back gate solving with middle Si layer

divided in four categories (see [20] and references therein): integration type pixel detectors, X-ray detectors, Vertex detectors and cryogenic detectors.

The integration type pixel sensors (INTPIX) are the main SOI detector development so far.

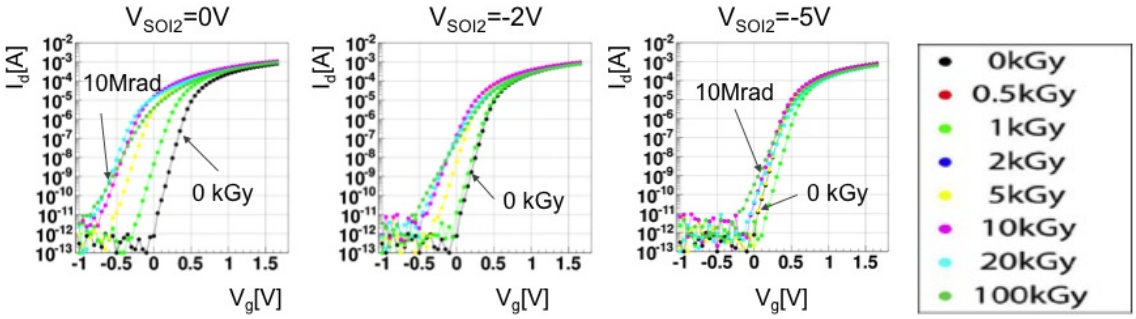

Figure 12. TID solving with middle Si layer

It is based on relatively basic circuitry (source follower+capacitance) together with a correlated double sampling technique (CDS). Several circuits has been built during last eight years, resulting in $>$1 Mpixel matrices and pixels sizes down to 12μm$\times$12μm.

Scientific X-ray detectors is the other big family of detectors in SOIPIX: they have been developed to be used in space borne experiments (XRPIX) or in free electron lasers facilities (SOPHIAS). Besides the simple source follower circuitry they have also included a charge sensitive amplifier readout, both of them with an on-pixel CDS technique. One of the main technological advancements done with these kind of detectors is the development of a stitching technique to build large formats with one mask. Indeed masks in LAPIS technology are limited to 24.6 mm $\times$ 30.8 mm. With the technology developed a buffer between different masks as thin as 10μm with a limited number of layers connected (up to 3) has been achieved so that large format pictures such as the one shown in Figure 13 can be obtained.

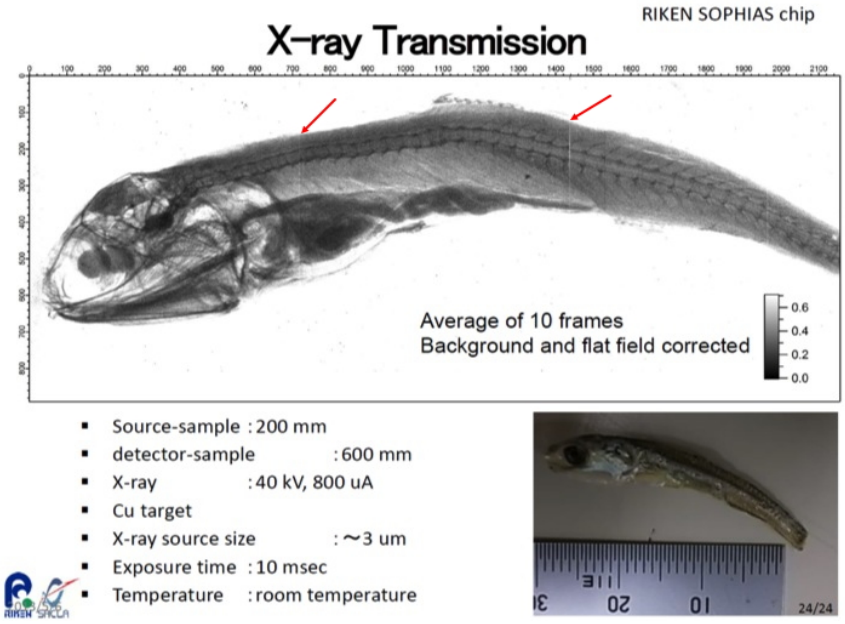

Figure 13. Small fish X-ray Transmission radiography taken with the RIKEN SOPHIAS chip. The 10 μm buffer region ($\sim$1 pixel wide) can be seen between the three chips used with the stitching technique.

An R&D project for a future vertex detector in Belle-II experiment is PIXOR, in which ORed signals from rows and columns of NxN pixel matrices are processed locally. This technique results in the reduction of the number of readout channels from N^2 to 2N allowing high resolution, low occupancy and on-sensor signal processing.

One of the main characteristics of SOI is its ability to work at cryogenic temperatures. Japanese Space Agencies JAXA/ISIS have developed in SOI technology, both amplifiers and Superconducting Tunnel Junctions able to work at 4.2K and $<$1K respectively, paving the way for SOI monolithic sensors that will work in these temperatures where other CMOS devices cannot.

6. Overview

SOI technology is a mature technology and it has been demonstrated during last years that it is suitable to build monolithic pixel sensors. The main advantages of SOI monolithic detectors are:

- No mechanical bump bonding, resulting in a reduction of material budget and smaller pixel sizes.
- Low parasitic capacitances, allowing higher speeds and lower noise.
- Ability to work at cryogenic temperatures.
- Full CMOS circuitry can be implemented in the pixel, with technology based in industry standards.
- Small cross section to SEE and possibility to reduce TID effects changing the electric field configuration around the BOX.

Probably the most important contribution of SOIPIX project has been the development of shielding structures (buried wells and double SOI) that solve the effects of electrostatic fields (needed to operate the detector) as well as the radiation effects. Nowadays the main stream of thought in SOIPIX devices is the use of p-doped substrates with SOI2 and buried wells. The first prototypes are arriving at different institutes and their characterization is taking place.

The whole project is a successful history in the collaboration between academia and industry. The formers are pushing the limits of the technology in order to fulfil the constraints by the experiments, and the latters are providing new technological features such as the development of buried wells (LAPIS) or the fabrication of double SOI wafers (SOITEC). Without any of these actors, this project would have not been possible.

Acknowledgments

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