Double Buried Oxide Trap-Rich Substrates for High Frequency Applications

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***Abstract*— Measurements of a new type of substrate for the integration of the trap-rich interface passivation solution with the below-buried oxide functionalities required in fully-depleted (FD) Silicon-on-Insulator (SOI) nodes is presented. This is achieved by adding a second thin buried oxide (BOX2) layer in between the substrate and the trap-rich/BOX1/SOI stack. It is shown that the trap-rich layer above BOX2 can effectively passivate the parasitic surface conduction that would be induced below BOX2 if BOX2 remains thinner than 20 nm. This is proven through measurements of substrate losses and non-linearity of coplanar waveguide transmission lines, comparing the fabricated double-BOX samples to reference trap-rich and unpassivated high-resistivity substrates.**

***Index Terms*— Double-BOX (DB) SOI, effective resistivity (ρ_{eff}), Harmonic Distortion (HD), oxide charges, RF CMOS, Trap-Rich substrate (TR).**

I. Introduction

In the past decade, silicon-on-insulator (SOI) technology has taken the radio-frequency (RF) world by storm [1]. Partially depleted (PD) SOI on trap-rich enhanced signal integrity (eSI™ [2]) substrates has been the mainstream technology for RF switches in mobile phones, having displaced Gallium-arsenide and silicon-on-sapphire technologies. Choosing the right substrate for SOI is of high importance to achieve high performance circuits [3]. The standard silicon (std) substrate (10 Ω·cm) is attractive due to its low price. However, it lacks in performance for RF applications since it induces high losses and non-linear signal distortion in passive devices implemented atop it [1]**.** The high-resistivity (HR) substrate improves the RF performance of the passive devices and reduce crosstalk [4]. However, due to positive oxide charges, electrons are attracted to the Si-SiO_2 interface forming a conductive layer called parasitic surface conduction (PSC). The effective resistivity (ρ_{eff}) of the substrate, is then lowered [5, 6], limiting the RF performances as it translates into high losses and high harmonic distortion of the RF signal [7].

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In order to overcome the PSC effect, UCLouvain and SOITEC developed the trap-rich (TR) substrate that introduces a thin layer of polysilicon between the insulating buried oxide (BOX) layer and the handle Si bulk wafer [1]. Thanks to the high density of trapping states in the polysilicon, the interface Fermi level is effectively pinned near the mid-gap [8]. This translates into lower losses and higher linearity of the substrate [1, 7, 9]. Passive devices such as Coplanar Waveguide (CPW) lines, filters and inductors on TR substrates show excellent RF performances [10].

Nowadays, TR substrates are employed in practically 100% of the switching circuits between the RF front-end and the antenna in modern day smartphone devices [11-13]. While the trap-rich passivation solution has seen great success in PD-SOI nodes [14], its compatibility with fully depleted (FD) SOI is foreseen as challenging. Indeed, many FD-SOI devices include electrical functionalities that are defined below the BOX layer (such as back-gate terminals). P and N isolation wells implemented within the semiconductor substrate with low reverse-leakage current are required. Forming these wells in a trap-rich type substrate is expected to lead to high leakage currents from the biased back gates to the substrate, facilitated by recombination centers associated to the traps of the polysilicon [15-17].

To overcome that reverse current leakage problem, a substrate structure solution is proposed in this letter, by introducing an insulating layer of SiO_2 between the trap-rich layer and the bulk silicon called *double-BOX* (DB) substrate. The objective of this DB-SOI substrate architecture is to provide DC isolation for the back-gate wells, implemented in the trap-rich layer, while maintaining the efficient passivation of the PSC. Another type similar to this substrate called double SOI has been reported previously in [18].

II. Substrates Description

To demonstrate the effectiveness of this proposed passivation scheme, 2.1 mm-long CPW lines have been designed on top of three types of substrates: (a) high-resistivity (HR), (b) conventional trap-rich (TR) and (c) Double-BOX substrates (DB).

These substrates are illustrated in Fig. 1. Basic HR wafers were cleaned using Piranha solution (3:1: H_2SO_4:H_2O_2 for a duration of 20 min at 110°C). After the Piranha cleaning, all the wafers were dipped in dilute HF solution (1:50, HF: Deionized water) to remove the native oxide. The insulating layer (silicon dioxide, SiO_2) BOX2 was thermally grown at a temperature of 900°C. Several samples were fabricated with

various thicknesses of that BOX2 layer. Next, for all samples, 500 nm (T_{poly}) of polysilicon was deposited by Low Pressure-Chemical Vapor Deposition (LPCVD), followed by, 200 nm of SiO_2, also by PECVD. This oxide layer emulates the combined presence of the BOX1 layer along with the first insulating layers of the back-end of line (BEOL) dielectrics. Finally, a 1-µm-thick Al layer was deposited on the backside of the Si wafer using E-gun evaporation. After each growth and deposition, the thicknesses were mapped by ellipsometry over the wafer. The proposed industrial process of double BOX SOI substrate is reported in [19].

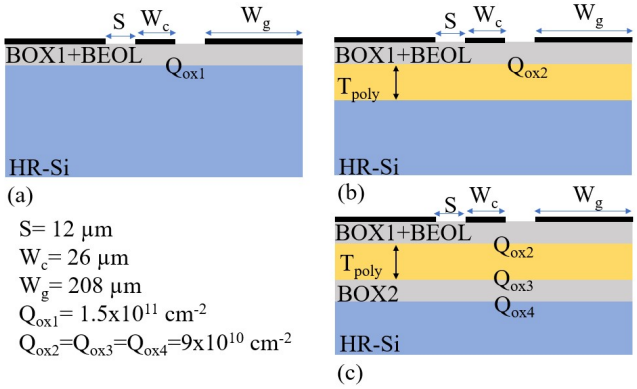

Fig. 1. The different substrates fabricated: (a) HR, (b) TR, and (c) DB substrate with different BOX2 thicknesses of 2, 10, 20, 50 and 500 nm.

The dimensions of the CPW lines are: the width of signal track W_c = 26 µm, the spacing between the signal and the ground plane S = 12 µm and the width of the ground line W_g = 208 µm. For all samples, the bulk silicon is p-type and has a nominal resistivity of 10 kΩ·cm. The DB substrates have different BOX2 thicknesses: 2, 10, 20, 50 and 500 nm.

Simulations are performed using Silvaco TCAD software, accurately accounting for the effects of oxide charges Q_{ox} in the insulating layers, along with those of interface and volume traps in the polysilicon. The interface oxide charge Q_{ox1} was extracted as $1.5 \cdot 10^{11}$ cm^{-2} for the HR. At the SiO_2-polysilicon interface Q_{ox2} was extracted as approximately $9 \cdot 10^{10}$ cm^{-2} for the DB and TR samples through simulation fitting using the modelling methodology described in [8, 9].

The polysilicon layer was simulated using tail distributions for donor and acceptor as in [20]. The simulated DB structures include three semiconductor-insulator interfaces are Q_{ox2}, Q_{ox3} and Q_{ox4}, as depicted in Fig. 1c.

III. Small Signal Characterization

The small-signal measurements of the CPW line were performed using 2-port Performance Network Analyzer (PNA)-X and a pair of ground signal ground (GSG) 100 µm-pitch |Z| probes. The effective resistivity has been extracted as described in [5, 6]. After that, a CPW line is measured on-wafer, along with dedicated open and short de-embedding structures that are used to remove the pad parasitics [21].

Fig. 2 shows the extracted effective resistivity as a function of frequency for HR, TR and DB substrates, at V_{DCline} = 0 V (V_{DCline} is the voltage applied to the CPW signal line relative to 0 V reference voltage). The HR substrate has a low effective resistivity of around 80 Ω·cm at 2 GHz due to the PSC effect. A conductive layer below the insulating layer is formed which makes the substrate's electrical properties non-uniform over space.

The TR substrate has an effective resistivity higher than 10 kΩ·cm at 2 GHz. The traps from the polysilicon layer capture the electrons attracted to the Si-SiO_2 interface and pin the Fermi level near mid-gap [8] (i.e. the interface is in a highly resistive state).

The DB substrate with 2 nm of BOX2 shows an effective resistivity close to that of the reference TR wafer. In that case, even with the presence of the 2 nm-thick BOX2 layer in between the bulk and the polysilicon, the traps are able to compensate the electrons created by the fixed oxide charges and passivate the BOX2-Si interface. This is confirmed by TCAD simulations, that reveal a robust passivation of the below-BOX2, particularly for thin BOX2 layers.

The DB substrates with 10 nm and 20 nm of BOX2 achieve effective resistivity metrics of 10 kΩ·cm and 2 kΩ·cm at 2 GHz, respectively. With the increase in BOX2 thickness, the trap-rich polysilicon layer becomes further away from the BOX2-bulk interface, and the passivation is less effective.

Then, the DB substrates with BOX2 thicknesses of 50 nm and 500 nm show 400 Ω·cm and 200 Ω·cm, respectively. The decrease in effective resistivity for these samples is due to the traps in the polysilicon being electrostatically far from the Si-SiO_2 interface. The traps are not able to compensate the PSC effect locally, and the RF performance results resemble more those of the HR reference sample than those of the TR reference sample.

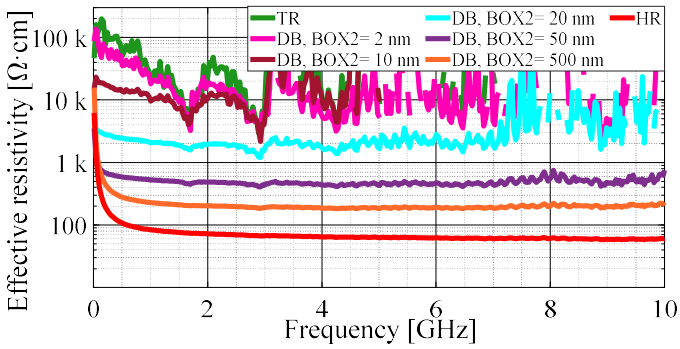

Fig. 2. Measured effective resistivity as a function of the frequency for the TR, HR and DB substrates with different BOX-2 thicknesses.

IV. Large Signal Characterization

Large-signal measurements were performed using a single tone (H'1) at 900 MHz injected into one port of the CPW line with its power swept from -25 to 25 dBm. The fundamental (H1), second (H2) and third (H3) harmonics were measured at the second port of the CPW. Large-signal simulations have been performed using the transient model described in [8, 9].

Fig. 3 shows the measured power of the second and the third harmonics versus the fundamental output power H1 at 900 MHz frequency. The HR is the least linear substrate due to the PSC effect and shows -50 dBm of H2 at a fundamental output power H1 of 15 dBm. The large signal applied to the CPW line modulates a large amount of free carriers at the Si-SiO_2 interface, and this translates to a high power of harmonics [10].

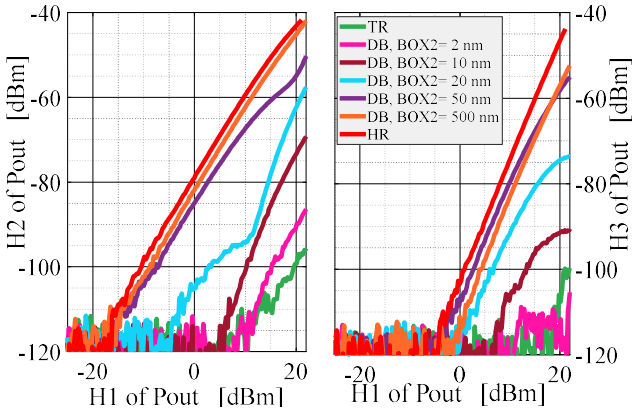

Fig. 3. Second and third harmonics versus fundamental H1 output power at 900 MHz and at V_{DCline} = 0 V, for the studied substrates HR, TR and DB with different BOX2 thicknesses.

The TR is the most linear substrate because of the traps in the polysilicon that ensure a low quantity of free carriers in the substrate, and consequently, a low variation of the local resistivity below the signal line at RF frequencies [8, 9]. This low variation translates to a low harmonic level for the TR substrate. The DB substrate with a BOX2 of 2 nm shows a H2 power around 10 dB higher than the TR. The thicker the BOX2 layer, the more free carriers are at the Si-SiO_2 interface to be modulated by the large-signal stimulus.

V. Discussion

Fig. 4 shows both the effective resistivity extracted at 2 GHz and the second harmonic H2 for the different BOX2 thicknesses, under the condition V_{DCline} = 0 V. It illustrates how the effective resistivity and linearity strongly depend on the thickness of the BOX2.

When the free carriers are less than 10 nm away from the polysilicon, the interface BOX2-polysilicon is well passivated and effective resistivities higher than 10 kΩ·cm are achieved thanks to the Fermi level below the signal line being deep in the bandgap. When the traps are far away from the Si-SiO_2 interface (more the 20 nm), the traps are not able to overcome the PSC effect, and this translates into a low effective resistivity and higher non-linearity. TCAD simulation results are overlaid in Fig. 4, and demonstrate very good agreement to the measured data.

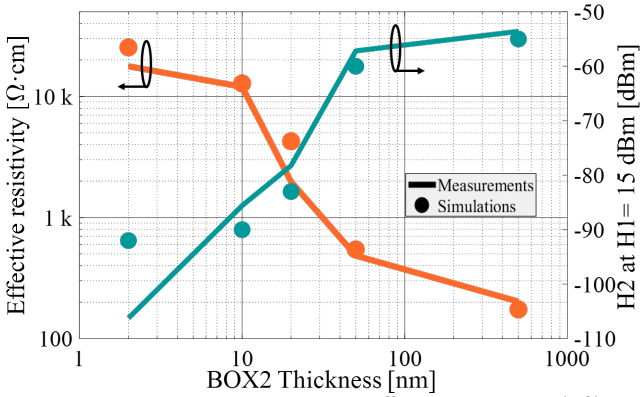

Fig. 4. Measured and simulated effective resistivity (left) and second harmonic power (right) as a function of the BOX2 thickness of the DB substrates at V_{DCline} = 0 V.

Overall, the strong correlation between ρ_{eff} and the signal distortion levels (H2 and H3) are well observed, as expected [7-9]. This is due to the fact that the large-amplitude RF signal modulates free carriers that are present in the substrate, and less well the PSC is passivated, the more the interfacial impedance can vary through time [8], increasing the HD components, and, the more the PSC is present, the lower the ρ_{eff} metric.

The TR interface passivation is uniquely compatible with PD-SOI technology and is widely regarded as the state-of-the-art benchmark silicon-based RF substrate solution. However, when moving to the FD-SOI, in which below-BOX functionalities are required from the devices (back gate contacts, isolation wells, substrate diodes, etc.), compatibility issues are foreseen when wanting to implement these in a defect-rich polysilicon layer instead of the bulk Si. For example, it is expected that the reverse current of a biased back-gate well formed in such a polysilicon layer will be orders of magnitude larger than in a crystalline Si material, as depicted by the diode leakage current in Fig. 5a (BOX1 has a thickness of 20 nm in the case of active devices). This motivates the interest for the DB substrates presented in this work, that propose a trap-rich passivation integration scheme with FD-SOI while maintaining excellent DC isolation thanks to the presence of the dielectric BOX2 layer (Fig. 5b).

As presented throughout this paper, well-designed DB substrates can offer good RF performances for RF passives.

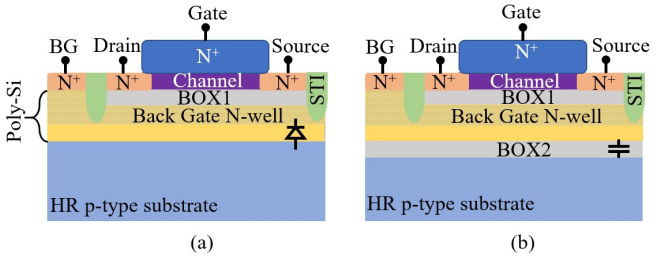

Fig. 5. Schematic view of a fully depleted SOI MOSFET on (a) TR substrate and (b) on DB substrate. BOX1 = 20 nm.

VI. Conclusion

In this work, the RF performance of a novel type of SOI trap-rich-based substrate solution employing two BOX layers was evaluated, both through RF measurements of several fabricated samples as well as using TCAD simulations. The RF characteristics of these double-BOX (DB) substrates were benchmarked against conventional trap-rich and high-resistivity reference substrates in terms of both small-signal (effective resistivity) and large-signal (non-linear distortion levels) performances. It was demonstrated that implementing a trap-rich layer between the BOX1 and BOX2 layers can provide effective passivation of all BOX-semiconductor interfaces. It was shown that the interface *below* BOX2 is well passivated by the polysilicon layer *above* it as long as the BOX2 thickness is less than approximately 20 nm. This type of substrate is a promising solution to enable the co-integration of FD-SOI nodes with a trap-rich-based RF substrate solution, and can offer a new range of well biasing options with decreased substrate leakage current.

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