

High-Frequency modeling of SOI transistors with BSIM3SOI

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Abstract - In this paper, the suitability of the commercially available SOI model, BSIM3SOI, for the High Frequency regime is studied. The performance of the internal model is improved by adding an external lumped model in order to fit the simulated S-parameters with measured ones, in a frequency range of 0.5-20GHz.

1. Introduction

Fully-Depleted Silicon-on-Insulator (FD-SOI) CMOS devices offer several advantages over ordinary CMOS transistors, such as higher transconductance, sharper subthreshold slope and higher cut-off frequency [1],[2]. With SOI, low-voltage low power analog RF blocks required in portable communication circuits can be realized together with high-performance digital circuits enabling the design of complete radio systems on chip.

The use of SOI in the Gigahertz region is no longer limited by the device operation, but in order to get full advantage of these devices, reliable models have to be available for circuit designers. Several models have been developed for SOI MOSFETs, but most of them are limited to the DC and low-frequency regime only [3],[4]. In this paper, the SOI version of the BSIM3 MOSFET model, BSIM3SOI, is studied in RF regime. First the validation in DC regime will be shown, and after this the Scattering (S) parameters will be fitted by adding an external lumped model.

The results will be shown for a device of 240 μ m/1 μ m, with a gate of 10 fingers, fabricated at the Universite Catholique de Louvain, Belgium, and a discussion will follow about the validity of the model for circuit simulations.

2. Modeling of a RF CMOS transistor

The layout of a multi-finger microwave SOI CMOS transistor is shown in Fig. 1. The transistor is embedded inside a microwave probing structure. The impact of the probing structure on the measured is de-

embedded using an on-wafer TRL calibration. The layout in Fig. 1. shows the structure inside the calibration reference planes [5].

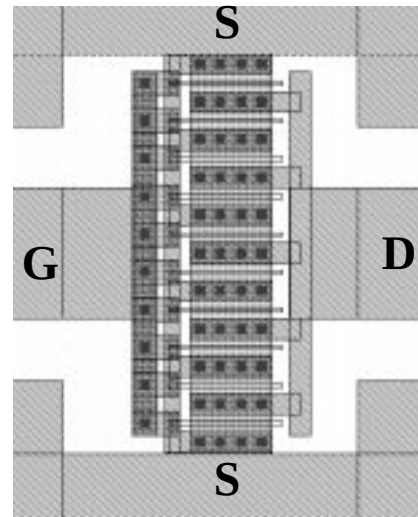


Figure 1. The layout of a multi-finger SOI CMOS transistor, with gate length of 240 μ m and gate width of 1 μ m.

The layout structure can be divided into 3 different sections, the access, external and internal [6]. The access section is required for the signal to travel to and from the device, and the parameters for this section are independent of both biaspoint and device geometry. The second section is the external part, consisting of structures caused by the elements depending on the layout structure, such as gate resistance, external gate-source capacitances, wire inductances, etc. Finally, the internal section is dependent on both the layout structure and the bias point.

In [6], a lumped element model has been developed, which makes very strict boundaries between each of the previously mentioned sections. A very detailed extraction routine has been given, with which each element on this model can be found. However, even though this model is very suitable for S-parameter simulations, the DC I-V characteristics can not be fully modeled with this model. Hence, the internal section of this model is now replaced by a commercial SOI CMOS model, the BSIM3SOI, which is used to model the DC curves. For this, a model BISM3SOIDD, a dynamic depletion model found in SmartSpice is used [7]. This model has been chosen, since it has a few improvements over the original BSIM3SOI, such as improved impact ionization

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current and self heating. The obtained model is used as an internal section for the High Frequency model and an external model based on the model presented in [6] is added to this.

In this work, the extraction routine for the external and access parameters is taken from [6]. However, this routine makes an assumption, that the internal section can completely be neglected in the cut-off region. Since there is a finite response of the BSIM3SOIDD model even in cut-off, the values obtained by the extraction routine have to be modified afterwards in order to get a perfect fit.

3. Results

The extraction of the DC parameters of the BISM3SOIDD model was based according to the procedure given in [3] and [8]. The acquired IV curves of a $240\mu\text{m}/1\mu\text{m}$ transistor are shown in Fig. 2.

The dynamic depletion operation of the model can be seen in the subthreshold slope with large back gate bias. Except of this, the model shows very good matching with measured values.

The BSIM3SOIDD model has a number of AC and capacitance paramters, but with those, the S-parameters could not be fitted. Thus they were all set to 0 for the High Frequency model extraction.

The S -parameters of the intrinsic model, with all AC parameters set to 0 fot both saturation ($V_{gs}=1\text{V}$, $V_{ds}=2\text{V}$) and cut-off ($V_{gs}=V_{ds}=0\text{ V}$) are shown in Fig. 3.

As can be noted from Fig. 3a, the model has a finite response in cut-off, and thus the values obtained by the extraction routine can not be valid. The obtained model with modified component values is shown in Fig. 4 and Table 1. The main difference between the original model presented in [6] and the model presented in this work is the absense of the inductors in the external section. As noted in Fig. 3,

the BSIM3SOI model has a very strong High-Frequency response itself, and thus the removal of the inductors can be explained with the intrinsic operation

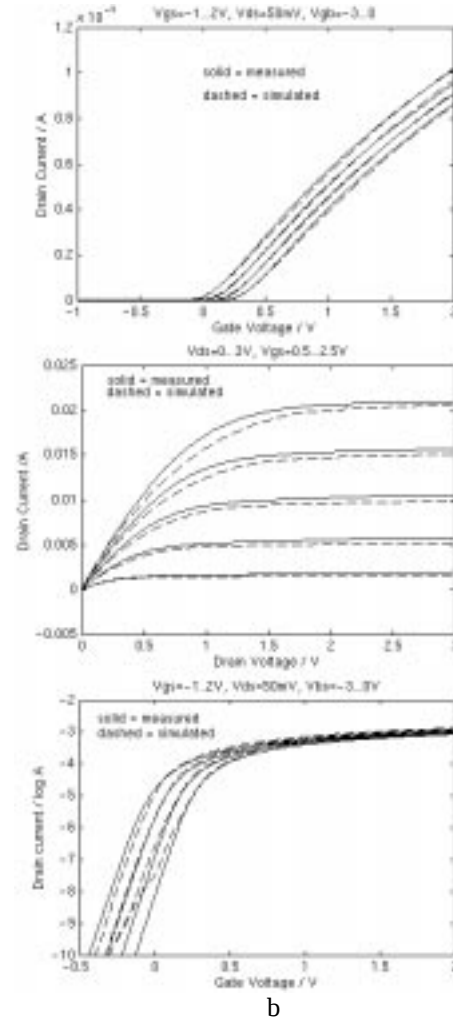


Figure 2. I-V curves of a $240\mu\text{m} / 1\mu\text{m}$ transistor.

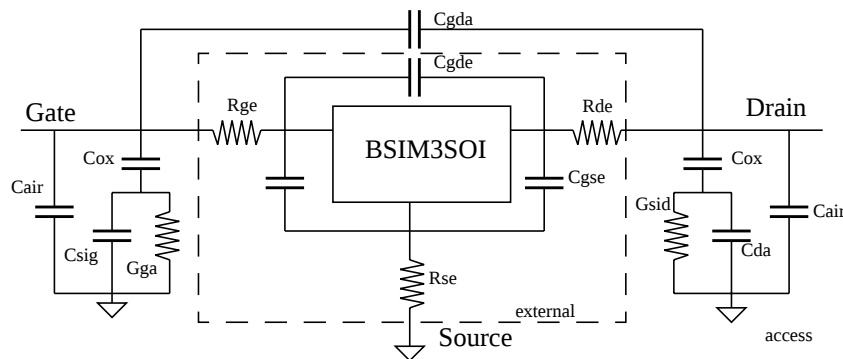


Figure 4. BSIM3SOI with external model

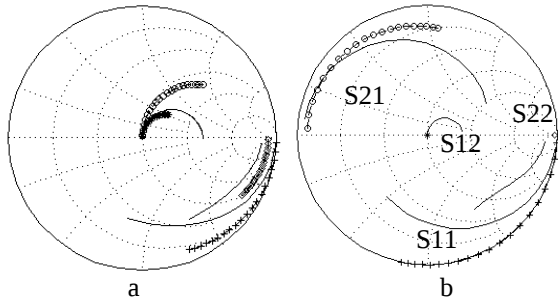


Figure 3. S-parameter response of the BSIM3SOIDD model for 240 μ m/1 μ m with AC parameters set to 0. a) cut-off response, b) saturation response.

Parameter	Value	Parameter	Value
Cox	110e-15	Rse	1
Cgda	10.3e-15	Rge	12
Cda	49.2e-15	Rde	50
Cga	3.1e-14	Cgse	5e-14
Cair	0.71e-15	Cgde	6e-14
Gga	1.5e-6	Cdse	0.2e-14
Gda	4.4e-7		

Table 1. Obtained parameter values for the external model. Parameters for the access section are denoted with an *a* and parameters of the externa section are denoted with *e*.

The fitted S-parameters are shown in Fig.

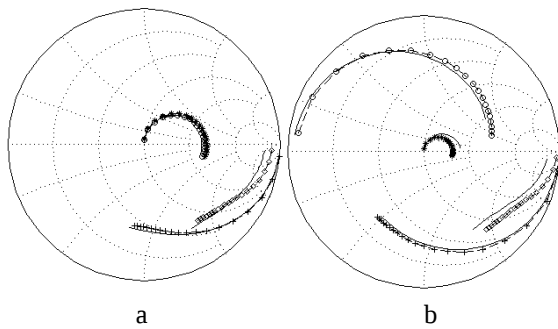


Figure 5. Fitted S-parameters of the complete model. a) in cut-off b) in saturation.

4. Conclusions

In this paper it has been shown, that the BSIM3SOI model can be used in the High Frequency regime, if it is extended with an external model. The simulated S-parameters fit reasonably well with the measured values. Further work has to be done to develop an extraction routine for the external components.

References

- [1] Chen C.L. et al., "High Frequency Characterization of Sub-0.25- μ m Fully-Depleted Silicon-on-Insulator MOSFETs", IEEE Electron Device Letters, Vol. 21, pp. 497-499, 2000.
- [2] Colinge J.-P., "Fully-Depleted SOI CMOS for analog applications", IEEE Transactions of Electron Devices, vol. 45, pp. 1010-1016, 1998.
- [3] BISMOSI v2.1 MOSFET Model - User's Manual for BSIMFD2.1. 1999.
- [4] [19] Fossum J., SOISPICE-5.0. SPICE2 with UFSOI MOSFET Models. User's Guide. University of Florida, 2000.
- [5] Gillon R, 'Modelling and Characterisation of teh SOI MOSFET for MMIC Applications.', PhD Thesis, .Universite Catholique de Louvain, 1998.
- [6] Jean-Pierre Raskin, 'Modeling, Characterization and Optimization of MOSFET's and Passive Elements for the Synthesis of SOI MMIC's', Ph.D. Thesis, Universite Catholique de Louvain, 1997.
- [7] Silvaco International, SmartSpice/UTMOST III Modeling Manual - Volume 3. 1999.
- [8] BSIM3v3.2.2 MOSFET Model. Users' Manual. University of California, Berkeley, 1999.