

# Advanced Interface Characterization for RF SiGe-engineered Substrates and Al<sub>2</sub>O<sub>3</sub> Gate Dielectric

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## Abstract

In this work, Metal-oxide-semiconductor (MOS) capacitors with different dielectric stacks and SiGe buried substrates with coplanar technology are studied, under both small- and large-signal conditions. The core methodology of the thesis relies on capacitance–voltage (C–V) characterization of MOS capacitors. Different device configurations and multiple extraction approaches for determining the interface trap density are examined. In addition, several admittance-related phenomena that can lead to under- or overestimation of the interface trap density when using the conductance method are discussed.

The classical C–V electrical characterization technique is used in two contexts. The first concerns the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  MOS capacitors, where it serves to evaluate interface passivation and extract key parameters such as fixed charge and doping concentration. This provides valuable feedback for improving interface passivation, which remains a key challenge in MOSFET development and scaling. Negative fixed charges in the dielectric stack result in a positive shift of the threshold voltage ( $V_{\text{th}}$ ) in nMOS devices. This effect can be leveraged to reduce the channel doping concentration, thereby compensating the  $V_{\text{th}}$  shift, enhancing carrier mobility, and potentially reducing device variability. Meanwhile, the effective carrier lifetimes were measured by the contactless photoconductance decay method, which implied the quality of interface passivation.

High-resistivity Silicon has drawn great attention for the radio-frequency (RF) and millimeter wave integration. One efficient way to reduce free carriers near the Si surface and preserve the substrate's high resistivity is to leverage the high density of interface traps ( $D_{\text{it}}$ ) at the  $\text{SiO}_2/\text{Si}$  interface. High interface trapping states lead to deep Fermi level pinning in the band gap, so that the concentration of free carriers remains low, ensuring a state of high resistivity. In this work, one novel interface passivation schemes of HR-Si are presented, SiGe buried high resistivity Si based on substrate interface potential control through high interface trap density at  $\text{SiGe}/\text{SiO}_2$ . An epitaxial SiGe layer is inserted between the buried oxide (BOX) and the handle Si substrate. A  $\text{SiO}_2/\text{SiGe}$  interface tends to exhibit higher  $D_{\text{it}}$  values than  $\text{SiO}_2/\text{Si}$ , which is attributed to the formation of Ge–O bonds at the interfacial layer. Consequently, it is valuable to investigate  $D_{\text{it}}$  and the effective resistivity ( $\rho_{\text{eff}}$ ) on various buried SiGe stressor substrates. At the same time, a buried SiGe layer can be a useful layer being able to induce tensile strain in the channel of an SOI MOSFET if both the SOI and BOX layers are extremely thin (FDSOI), thereby boosting

transistor mobility.

To comprehensively evaluate SiGe buried substrates, the interface trap density ( $D_{it}$ ), effective resistivity, and linearity are defined as the key substrate figures of merit, and their corresponding extraction procedures are detailed. The second application of C-V characterization focuses on SiGe-buried standard-resistivity Si MOS capacitors. Once the  $\text{SiO}_2/\text{SiGe}$  interface is analyzed and  $D_{it}$  is extracted, the study is extended to SiGe-buried high-resistivity Si MOS capacitors. In this case, however, the C-V characteristics measured on high-resistivity silicon (HRS) differ significantly from those on low-resistivity silicon (LRS). A simple parallel RC network is no longer sufficient to model the substrate at high frequencies in HRS.

In terms of RF characterizations, the effective resistivity and linearity parameters are defined as RF substrate figures of merit, and their extraction procedures are described. These figures of merit serve as reliable indicators of substrate loss, coupling, and induced signal distortion. It is required that such considerations be kept under careful control in front-end circuitry for advanced telecommunication applications that have stringent spectral cross-contamination specifications between adjacent communication bands.

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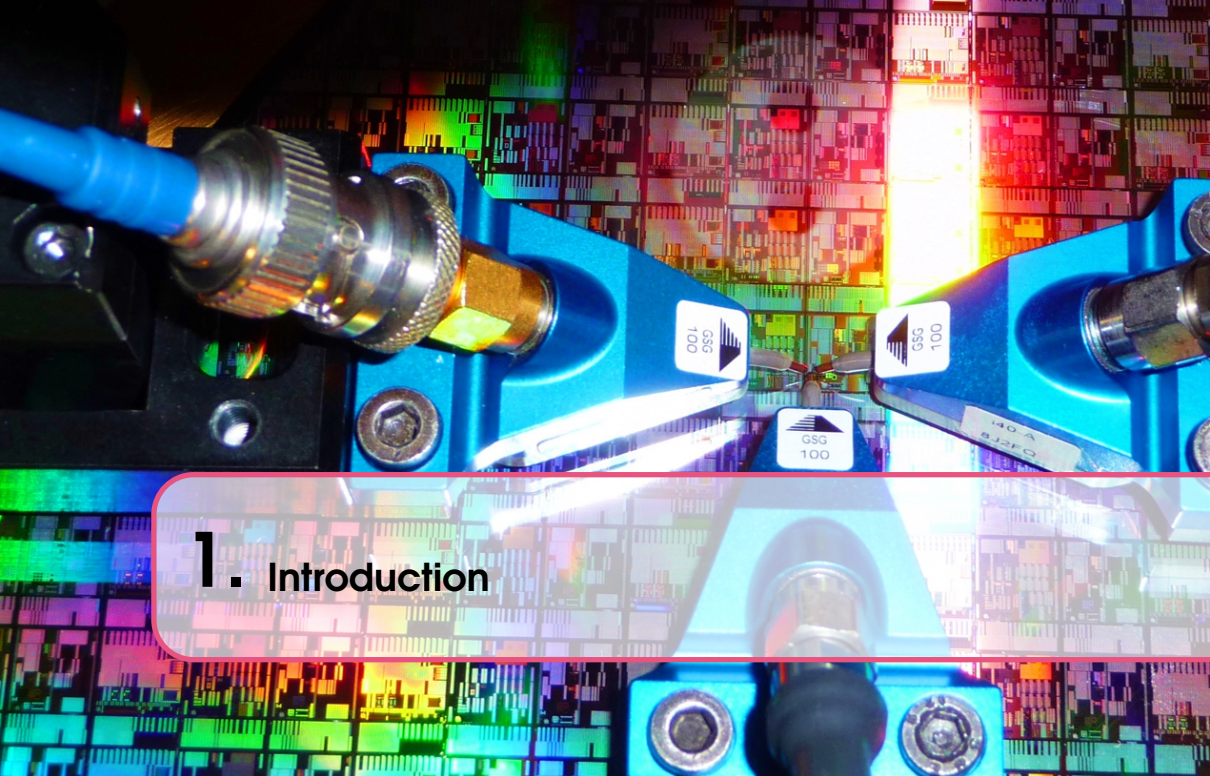


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# 1. Introduction

## 1.1 Context

High-resistivity silicon (HRS) has been used for the integration of frequency and millimeter wave integrated circuits. The low conductivity of HRS effectively suppresses RF bulk losses but leads to pronounced losses caused by a parasitic conductive layer at the  $\text{SiO}_2/\text{Si}$  interface. It has been shown that those parasitic surfaces can be suppressed by reducing the free carriers in the trap-rich polysilicon layer or by damaging the silicon surface through ion implantation. The characterization of both pristine and modified silicon surfaces will be essential in developing future silicon RF technologies that rely on the HRS substrates. The capacitance–voltage characteristics of MOS capacitors provide comprehensive information on semiconductor surface properties, making MOS capacitors particularly suitable test structures for this purpose. Therefore, this thesis aims to highlight the fundamental differences between MOS capacitors fabricated on standard-resistivity and high-resistivity silicon substrates, and to establish reliable admittance-based methodologies for interface trap characterization in

CMOS scaling and RF substrate engineering.

As RF and mm-wave operating frequencies continue to increase, transistor gate lengths must be aggressively scaled to sustain performance. In this context, RF-SOI technologies based on partially depleted SOI (PD-SOI) transistors have demonstrated excellent RF characteristics and have become a cornerstone of modern wireless electronics. A major advancement was achieved through the integration of trap-rich (TR) polysilicon layers beneath the buried oxide. By effectively suppressing parasitic surface conduction, these engineered substrates significantly reduce RF losses, substrate coupling, and nonlinear distortion. While the TR substrates are fully compatible with PD SOI nodes, the FD SOI remains a challenge to integrate with the defect-rich poly Si. Indeed, the back-bias features cannot be preserved with TR integration in FDSOI due to potential leakage current and fabrication difficulties. The development of novel passivation solutions applicable to FD SOI is an active topic of research.

One additional advantage of FD SOI resides in the possibility to improve the technology's performance by employing boosters. In particular, the application of strain to the Si channel can significantly improve the transistor's metrics. The edge relaxation of a buried SiGe layer beneath the BOX, enabled through shallow trench isolation (STI) structures, was shown to transfer tensile strain into the channel of FD SOI device. The strain significantly enhances  $I_{\text{dsat}}$  and  $g_{\text{m}}$ . When implemented in RF transistors, the strained channel should improve  $f_{\text{T}}$  and  $f_{\text{max}}$ , allowing the operation of RF ICs with higher frequency and lower current. In addition, high interface trap density ( $D_{\text{it}}$ ) values were found at the  $\text{SiO}_2/\text{SiGe}$  interface. High  $D_{\text{it}}$  hints to the potential of using the SiGe layer as an interface passivation layer for improved RF performance and is compatible with FD SOI technology, as an additional bonus of its use as a strain layer.

## 1.2 Objectives

The objective of this thesis is to experimentally characterize interface traps on different substrates using admittance-based methods. For RF substrates in particular, the lack of an established characterization approach can be attributed to both their high trap density and high resistivity. The large concentration of defects causes Fermi-level pinning, which prevents the application of conventional capacitance-based electrical measurements directly on RF-SOI structures for trap analysis.

Rather than relying solely on predicted figures of merit derived from hypo-

thetical trap profiles used in modeling polysilicon or other materials, this work aims to experimentally validate and extend our understanding of these traps. In addition, we seek to evaluate the sensitivity and limitations of conventional admittance methods, and to determine whether they can directly probe traps within the materials. Such an approach would ultimately support the development of next-generation RF-SOI substrates designed for emerging application domains not yet addressed by existing RF-SOI technologies.

In parallel, the proposed characterization framework can be extended to assess the feasibility and reliability of advanced high- $k$  dielectric stacks in CMOS gate architectures. By providing a unified methodology to evaluate interface quality, fixed charge, and leakage mechanisms, it enables the systematic optimization of dielectric stacks and thereby contributes to performance enhancement in advanced MOS technologies.

## 1.3 Structure of the Thesis

This thesis is organized as follows:

**Chapter 2** describes substrate properties on coplanar technology at RF frequencies. It outlines the key substrate requirements for RF applications, emphasizing their effects on parasitic coupling, RF losses, and non-linear signal distortion. In addition, the chapter discusses the challenges related to alternative solutions for FD-SOI integration and the characterization of traps in high-resistivity silicon-based substrates.

**Chapter 3**, a detailed description of various characterization methodologies (DC and RF) will be provided. The setups for key measurements, including Capacitance-voltage (C-V), S-parameters, and harmonic distortion, will be illustrated and explained.

**Chapter 4** This part describes the core work of this thesis: Using TCAD simulation to understand the electrical properties of interface traps at play in diverse semiconductor substrates. It also provides the different widely used extraction methods of interface traps based on the metal-oxide-semiconductor (MOS) capacitor. The energy distribution, density of interface states, capture cross sections for holes and electrons, and so on, can be accessed by the admittance of the MOS capacitor. Besides, the limitations of the methods have been assessed.

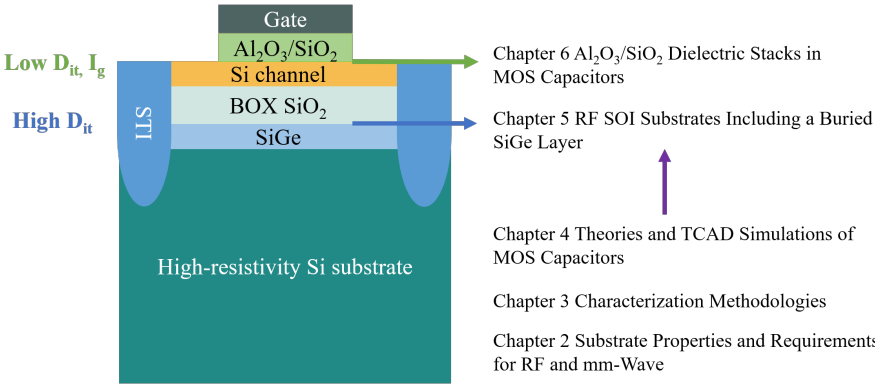
**Chapter 5** is dedicated to exploring and presenting an alternative silicon-based

RF substrate solution incorporating SiGe, leveraging the inherently high interface trap density at the SiO<sub>2</sub>/SiGe interface, as opposed to the conventional high-resistivity or trap-rich substrates. It includes C–V, small-signal, and large-signal characterizations of SiGe-buried silicon substrates, which show strong potential for RF applications while offering an additional advantage — enhanced carrier mobility.

**Chapter 6** systematically investigates the electrical properties of thin Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> (with a target equivalent oxide thickness of 4.9 nm) as a gate dielectric stack in the metal–oxide–semiconductor (MOS) capacitor. Different deposition techniques, i.e., thermal oxidation, thermal atomic layer deposition (ALD), and plasma-enhanced atomic layer deposition (PEALD), are employed in the fabrication of MOS capacitors. The second-derivative, Terman, and conductance methods are used to extract the fixed oxide charges and interface trap densities in the MOS capacitors. Furthermore, to evaluate the reliability of the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> gate dielectric stack, the leakage current is analyzed. Contributions from Poole–Frenkel emission, trap-assisted tunneling, and Fowler–Nordheim mechanisms to the leakage current are detailed.

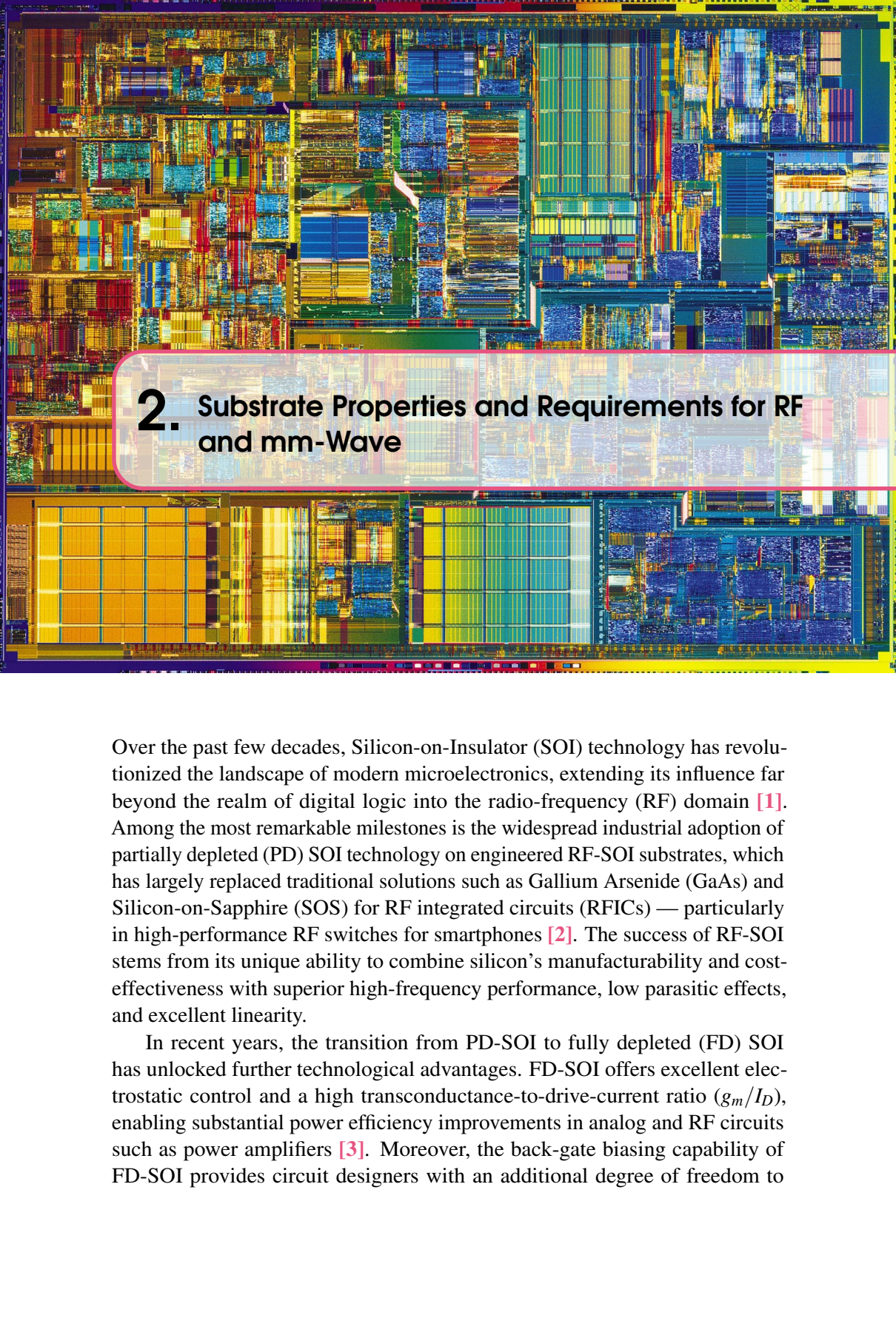
**Chapter 7** is dedicated to reviewing the global conclusions of this thesis and offering perspectives on future endeavors in line with the presented work. Combining **Chapter 5** and **Chapter 6**, a particularly promising extension is the application of the 5-nm EOT Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> dielectric stack to RF power switches fabricated on SiGe buried high-resistivity RF SOI substrates, the cross-section as seen in **Figure 1.1**.





**Figure 1.1:** The cross-sectional schematic of RF SOI CMOS illustrates the structure of this thesis, progressing from characterization methodologies and TCAD simulations at the foundation to SiGe-buried RF SOI substrates and high-k gate dielectric stacks in MOS capacitors.

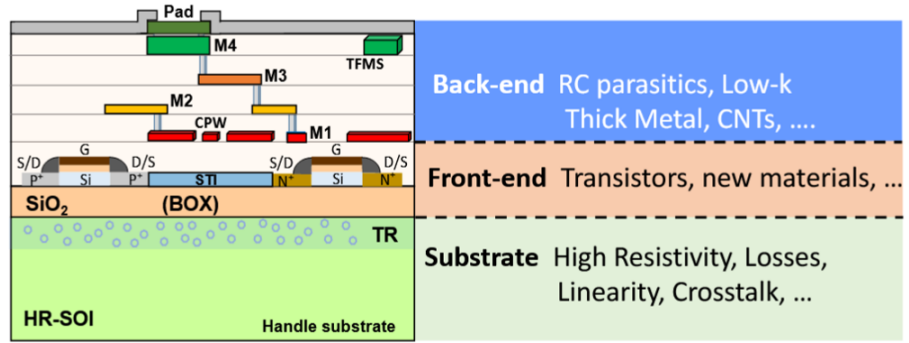




## 2. Substrate Properties and Requirements for RF and mm-Wave

Over the past few decades, Silicon-on-Insulator (SOI) technology has revolutionized the landscape of modern microelectronics, extending its influence far beyond the realm of digital logic into the radio-frequency (RF) domain [1]. Among the most remarkable milestones is the widespread industrial adoption of partially depleted (PD) SOI technology on engineered RF-SOI substrates, which has largely replaced traditional solutions such as Gallium Arsenide (GaAs) and Silicon-on-Sapphire (SOS) for RF integrated circuits (RFICs) — particularly in high-performance RF switches for smartphones [2]. The success of RF-SOI stems from its unique ability to combine silicon's manufacturability and cost-effectiveness with superior high-frequency performance, low parasitic effects, and excellent linearity.

In recent years, the transition from PD-SOI to fully depleted (FD) SOI has unlocked further technological advantages. FD-SOI offers excellent electrostatic control and a high transconductance-to-drive-current ratio ( $g_m/I_D$ ), enabling substantial power efficiency improvements in analog and RF circuits such as power amplifiers [3]. Moreover, the back-gate biasing capability of FD-SOI provides circuit designers with an additional degree of freedom to



**Figure 2.1:** The schematic representing the three important levels of optimization for an RF IC. Some key parameters important to improve the back-end and front-end of line processes, as well as the substrate electromagnetic properties, are mentioned.

optimize the DC operating point, allowing the simultaneous enhancement of the transition frequency ( $f_T$ ) and the maximum oscillation frequency ( $f_{max}$ ). This back-bias tunability also facilitates the co-integration of digital, analog, and RF functions on a single die, fostering compact and energy-efficient system-on-chip (SoC) architectures.

### 2.1 Substrate Influence in RF Circuits

The three important levels of optimization for a RF IC are shown in **Figure 2.1**. The substrate plays a critical role in defining both active and passive device performance, as it strongly affects the electromagnetic environment in which the circuits operate. When conventional low-resistivity silicon is used as a handle wafer, integrated passive components, such as inductors and tunable capacitors, experience significant substrate losses, resulting in a low quality factor (Q). In addition, signal coupling through the substrate causes crosstalk and non-linearity, which further degrades the performance of high-frequency circuits [4].

In SOI technologies, the substrate losses and parasitic coupling depend primarily on the resistivity of the handle silicon and the thickness of the buried oxide (BOX) layer. Modern SOI wafers are manufactured using the Smart Cut™ process [5], which offers a key advantage: it allows transferring various semiconductor materials as the handle substrate. This makes it possible

to use low-loss, high-resistivity substrates such as HR-Si, sapphire, quartz, or glass—materials that remain fully compatible with standard SOI CMOS processing.

The use of such high-resistivity substrates enables the suppression of conduction paths and improves RF isolation. It also enables the fabrication of high-quality passive components and RF circuits suitable for wireless communication systems. Additionally, their low crosstalk characteristics facilitate efficient mixed-signal integration, allowing digital and analog/RF blocks to coexist on the same chip. This capability further extends to system-on-chip (SoC) platforms that integrate power management and wireless communication functionalities.

## 2.2 Substrate Impact on Coplanar Technology

It is well known that standard high-resistivity silicon-on-insulator (HR-SOI) handle wafers suffer from parasitic surface conduction (PSC) [6], [7], [8], [9]. This effect arises due to fixed oxide charges at the  $\text{SiO}_2/\text{Si}$  interface, which induce a highly conductive accumulation or inversion layer at the surface of the HR silicon handle wafer, as seen in **Figure 2.1**. PSC degrades the intrinsic high-resistivity properties of the handle wafer, increasing substrate losses and crosstalk, and thus limiting the RF performance of standard HR-SOI substrates.

Despite this issue, HR-SOI still significantly reduces substrate losses and crosstalk compared to conventional SOI wafers. In fact, its RF potential was first demonstrated in 1997 [10]. Before then, the consensus in the scientific community was that silicon substrates were fundamentally unsuitable for RF integrated circuits (ICs) [11].

In the early 2000s, a significant advancement in SOI technology was achieved through the integration of a thin polysilicon layer containing a high density of traps beneath the buried oxide [12]. Polysilicon is widely used in the semiconductor industry and is well understood. It has a resistivity similar to intrinsic or lightly doped silicon and introduces numerous interface states and deep-level defects within the silicon bandgap [13]. These defects act as recombination centers and traps, effectively suppressing PSC by pinning the Fermi level near the midgap at the interface in a highly resistive state. It restores the high-resistivity behavior of the HR-Si substrate to values above  $3 \text{ k}\Omega\text{cm}$  [14]. These traps can be created through several techniques [15], [16]. But the integration of a thin polysilicon (poly-Si) layer is emerging as one of the most

robust and efficient solutions.

Polysilicon's key advantages over other methods include:

- High trap density,
- Thermal stability up to 1100°C,
- Compatibility with existing wafer bonding techniques used in the fabrication of trap-rich (TR) SOI wafers for system-on-chip (SoC) applications [17].

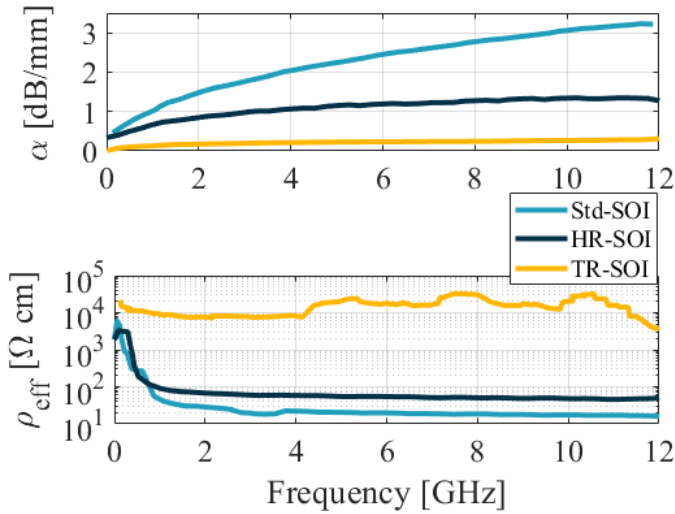
### Substrate Effective Electrical Parameters

To experimentally validate the benefits of the trap-rich layer, both high-resistivity (HR) and trap-rich (TR) samples were fabricated from high-resistivity float-zone silicon wafers with a nominal resistivity above 5 k $\Omega$ cm. For comparison, a standard (Std) sample was prepared using a 10  $\Omega$ cm silicon wafer. The TR sample incorporated a 500 nm polysilicon layer, while a 500 nm oxide layer was deposited by PECVD on all three samples, followed by a 1  $\mu$ m aluminum metallization and front-side lithography and etch to pattern the RF structures.

The first RF structure investigated is a coplanar waveguide (CPW) transmission line. Through RF measurements and/or simulations of these lines, the effective substrate electrical parameters can be extracted. Since the substrate is a heterogeneous stack composed of multiple materials with non-uniform properties, direct evaluation of its influence on device performance is not straightforward. Therefore, the concepts of effective resistivity and effective permittivity are employed to describe the overall electromagnetic behavior of the substrate in RF circuit design. This procedure will be mentioned in the **Section 3.6.1**.

The effective resistivity and RF losses of the CPW lines fabricated on the three SOI substrates are presented in **Figure 2.2**. The coplanar waveguide (CPW) lines fabricated on standard (Std) resistivity SOI substrates exhibit an effective resistivity of approximately 10  $\Omega$ ·cm. Consequently, their lineic RF losses reach about 3.0 dB/mm at 10 GHz. The HR-SOI substrate exhibits a performance comparable to that of the Std-SOI. Although the nominal resistivity of HR-SOI exceeds 1 k $\Omega$ ·cm, the presence of fixed charges in the buried oxide layer induces parasitic surface conduction (PSC) by attracting free electrons at the SiO<sub>2</sub>/Si interface. As a result, the effective resistivity  $\rho_{\text{eff}}$  is reduced to approximately 68  $\Omega$ ·cm, leading to lineic RF losses of about 1.4 dB/mm at 10 GHz. The TR-SOI substrate suppresses parasitic surface conduction (PSC) through the introduction of a thin polysilicon layer. Free carriers are trapped by the defects induced within this layer, maintaining a depleted region and ensuring a high



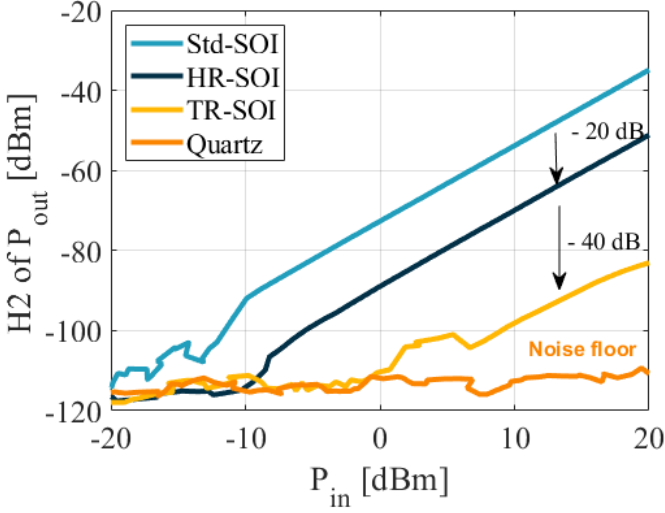


**Figure 2.2:** Effective electrical substrate parameters  $\alpha$  and  $\rho_{eff}$  extracted from CPWlines S-parameters obtained by on-wafer measurements .

interfacial resistivity. As a result, the effective resistivity  $\rho_{eff}$  remains as high as 10 k $\Omega \cdot \text{cm}$ , while the lineic RF losses at 10 GHz are minimized to approximately 0.24 dB/mm.

We have to mention the reasons why we have the frequency-dependent trend of the effective resistivity and losses related to Std and HR substrates. At low frequencies, the electromagnetic wave “sees” the substrate as a large capacitor formed by the thin oxide layer (acting as the dielectric) and the conductive silicon beneath it (acting as the bottom plate). Because the current cannot easily flow through the insulating oxide, the system behaves mainly as a capacitor with almost no resistive loss. This explains why the effective resistivity appears very high and the effective permittivity increases — the electric field is mostly stored in the thin oxide, enhancing the capacitive effect. As the frequency increases, the electric field starts to penetrate deeper into the substrate, reducing this capacitive dominance and making  $\rho_{eff}$  and  $\epsilon_{eff}$  stabilize to their intrinsic, frequency-independent values. In this thesis, all effective substrate parameters are extracted in the high-frequency regime—beyond the slow-wave region, where they become frequency-independent.

### Substrate Linearity: Signal Distortion



**Figure 2.3:** Measured harmonic distortion along a CPW line lying on standard SOI (10  $\Omega$ -cm) and HR based-Si substrates (10 k $\Omega$ -cm) with and without the trap-rich layer, compared to the insulator substrate quartz [18].

To evaluate and compare the substrate-induced nonlinearities, a single-tone excitation at a fundamental frequency  $f_0 = 900$  MHz is applied to one port of the CPW transmission line. The input power of this tone, denoted as  $H'1$ , is swept from  $-20$  dBm to  $+20$  dBm with  $50 \Omega$  reference port impedances. The output signal is then analyzed in the frequency domain, as illustrated in **Figure 3.11**.

Because of the nonlinear response of silicon-based substrates, signal distortion occurs, resulting in a multi-tone output that contains the fundamental component ( $f_0 = 900$  MHz), denoted as  $H'1$ , along with harmonic components at integer multiples of the fundamental frequency—namely  $H2$  at 1.8 GHz,  $H3$  at 2.7 GHz, and so forth. Among these, the second harmonic  $H2$  is typically the most significant component in CPW structures and is therefore used as the primary indicator of substrate linearity.

**Figure 2.3** presents the measured  $H2$  level as a function of the fundamental output power  $H'1$ , obtained from on-wafer characterization of a 2.1 mm-long CPW line fabricated on the three investigated SOI substrate types. The harmonic



levels originating from the substrate are reduced by at least 20 dB when moving from a standard-resistivity SOI substrate ( $\sim 10 \Omega\cdot\text{cm}$ ) to a high-resistivity SOI ( $\sim 1 \text{ k}\Omega\cdot\text{cm}$ ). More importantly, an additional reduction of about 40 dB is achieved with the innovative trap-rich high-resistivity SOI (TR-SOI) substrate, as illustrated in **Figure 2.3**. The resulting harmonic level is comparable to that observed in fully insulating substrates. The quartz substrate as an insulator substrate has a very low harmonic level under the noise floor, which can not be detected by our test bench.

The physical mechanisms explaining the trapping behavior are discussed in detail in [19]. The electrical characteristics of Std and HR SOI substrates are strongly voltage-dependent due to the presence of free carriers. This dependence arises because the substrate impedance varies with the applied signal amplitude. Under large-signal excitation, the free-carrier distribution in the silicon changes dynamically as the substrate cycles through accumulation, depletion, and inversion regimes. As a result, these voltage-sensitive substrates introduce significant harmonic distortion at the output of the CPW line.

The integration of a thin polysilicon trap-rich layer beneath the buried oxide (BOX) in nominally high-resistivity substrates effectively mitigates this problem. The traps at the Si/SiO<sub>2</sub> interface pin the Fermi level close to midgap, making it far less sensitive to voltage variations. Consequently, the substrate linearity is substantially improved, and distortion induced by the substrate in the overlying transmission lines is reduced by 40 dB.

These trap-rich (TR) SOI substrates, commercialized by Soitec under the name RFeSI™ (for RF enhanced Signal-Integrity), have become a standard in the RF domain [20]. Different versions of RFeSI™ wafers are available on the market. The RFeSI80™ product exhibits a second-harmonic ( $H2$ ) distortion level as low as  $-80 \text{ dBm}$  for a fundamental component  $H1$  of  $+15 \text{ dBm}$  [21] while the RFeSI100™ achieves an even lower distortion level of  $-100 \text{ dBm}$ . In general throughout this thesis, harmonic levels will be analyzed at a fundamental output power of  $H1 = +15 \text{ dBm}$ , and plotted against the DC bias, to show the dependence of bias. In summary, many studies have demonstrated that TR passivation leads to significant reductions in substrate losses and improvements in linearity [22], [23], [24]. Passive RF components such as CPW lines, filters, and inductors fabricated on TR substrates consistently show superior quality factors and insertion loss performance compared to those on unpassivated HR silicon. Besides, it has been demonstrated that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors

[22].

## 2.3 Challenges and Emerging Alternatives for FD-SOI Integration

Despite the effectiveness of the trap-rich scheme for PD-SOI technologies, integrating such layers within FD-SOI remains challenging. The presence of a defect-rich polycrystalline layer underneath the BOX may introduce leakage currents, unwanted interface states, and fabrication complexities that are incompatible with the thin and highly controlled nature of FD-SOI stacks. Furthermore, the back-bias functionality — a key advantage of FD-SOI, can be severely degraded by the introduction of such layers.

To overcome these limitations, the community has proposed several alternative passivation strategies, including buried PN junctions [25], [26], deep-level impurity passivation [23], double-BOX substrate architecture [27], and locally formed polysilicon trap-rich regions via ion implantation [24]. Each of these approaches aims to suppress parasitic conduction while preserving the back-bias capability and compatibility with existing CMOS processes.

## 2.4 Challenges of Trap Characterizations for High-resistivity Si-Based Substrates

### 2.4.1 Defects and Traps: Fatal or Vital

In MOSFET devices, traps located within the bulk and at the interface can induce several detrimental effects, including degradation of carrier mobility and long-term stability and reliability issues. Hence, effective interface passivation is crucial to preserve device performance, as discussed in **Chapter 6**.

Interestingly, deliberately introducing defects and traps in semiconductors—although seemingly counterintuitive—can be highly beneficial in specific applications. Examples include charge-trapping flash memories [28] and RF substrates, such as trap-rich, gold-doped silicon [29], and other material solutions that benefit from a high density of traps. The latter forms one of the central motivations of the present thesis, as further detailed in **Chapter 5**.

Polycrystalline silicon (polysilicon) consists of numerous small silicon grains with different crystal orientations. These grains are separated by grain boundaries that are rich in defects and surface states. The development of processes for obtaining the trap-rich (TR) layer has so far been carried out in a largely qualitative manner, while the quantitative characterization of traps is investigated in [30].

In addition to bulk traps, interface traps located at the interface between two materials can also capture the free carriers and thus eliminate the PSC. Various admittance methods have been simulated for interface trap analysis in both standard- and high-resistivity silicon and subsequently extended to other material interfaces, where their reliability and convenience have been widely demonstrated, as presented in **Chapter 4**. However, interface traps on high-resistivity silicon have never been systematically investigated.

Similar to the study of polysilicon, we aim to gain detailed insights into:

- the nature of the traps (e.g., energy distribution, capture cross-section, donor or acceptor behavior),
- their densities,
- their evolution throughout the various processing steps during the fabrication of the SOI substrate (i.e., thermal budget during annealing).

## 2.5 Chapter Summary

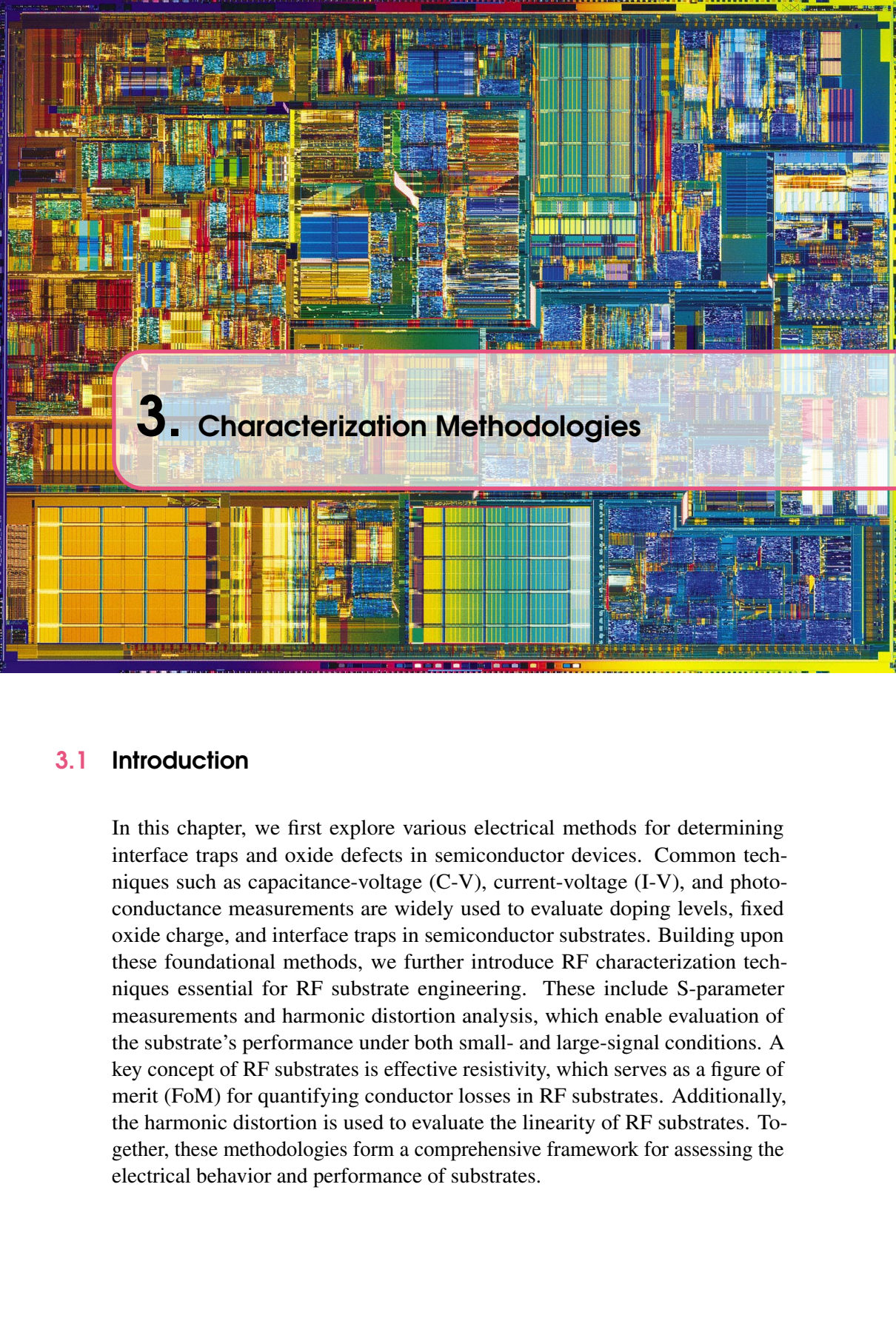
This chapter examined the role of the substrate in RF and mm-wave SOI technologies, emphasizing its impact on RF losses, crosstalk, and linearity. While high-resistivity silicon significantly improves RF performance compared to standard silicon, its benefits are often limited by parasitic surface conduction (PSC) induced by fixed oxide charges at the  $\text{SiO}_2/\text{Si}$  interface, which drastically reduces the effective substrate resistivity.

Trap-rich SOI substrates were introduced as an effective solution to suppress PSC. By integrating a defect-rich polysilicon layer beneath the buried oxide, free carriers at the interface are trapped and the Fermi level is pinned near midgap, restoring high-resistivity behavior. RF measurements on coplanar waveguide structures demonstrate that this approach substantially reduces substrate losses and improves linearity, with harmonic distortion levels comparable to insulating substrates. The physical origin of substrate-induced nonlinearities was discussed, highlighting the voltage-dependent redistribution of free carriers in standard and high-resistivity silicon. In contrast, trap-rich substrates stabilize the substrate impedance under large-signal excitation, leading to a strong reduction in harmonic distortion. These advantages have enabled the industrial adoption of trap-rich RF-SOI substrates.

Finally, the challenges associated with integrating trap-rich concepts into fully depleted SOI (FD-SOI) technologies were addressed. While highly effec-

tive for PD-SOI, defect-rich layers are not readily compatible with FD-SOI due to leakage, back-bias degradation, and process integration constraints. Emerging alternatives, including buried PN junctions, deep-level impurity passivation, and advanced substrate architectures, were therefore introduced.

This chapter also motivated the central theme of this thesis: although defects and traps are traditionally viewed as detrimental in MOS devices, they can be deliberately engineered to enhance RF substrate performance. However, despite their critical role, traps in high-resistivity and RF-oriented substrates remain poorly quantified. This gap motivates the experimental investigation of interface traps using admittance methods, which are developed in the following chapters.



## 3. Characterization Methodologies

### 3.1 Introduction

In this chapter, we first explore various electrical methods for determining interface traps and oxide defects in semiconductor devices. Common techniques such as capacitance-voltage (C-V), current-voltage (I-V), and photo-conductance measurements are widely used to evaluate doping levels, fixed oxide charge, and interface traps in semiconductor substrates. Building upon these foundational methods, we further introduce RF characterization techniques essential for RF substrate engineering. These include S-parameter measurements and harmonic distortion analysis, which enable evaluation of the substrate's performance under both small- and large-signal conditions. A key concept of RF substrates is effective resistivity, which serves as a figure of merit (FoM) for quantifying conductor losses in RF substrates. Additionally, the harmonic distortion is used to evaluate the linearity of RF substrates. Together, these methodologies form a comprehensive framework for assessing the electrical behavior and performance of substrates.

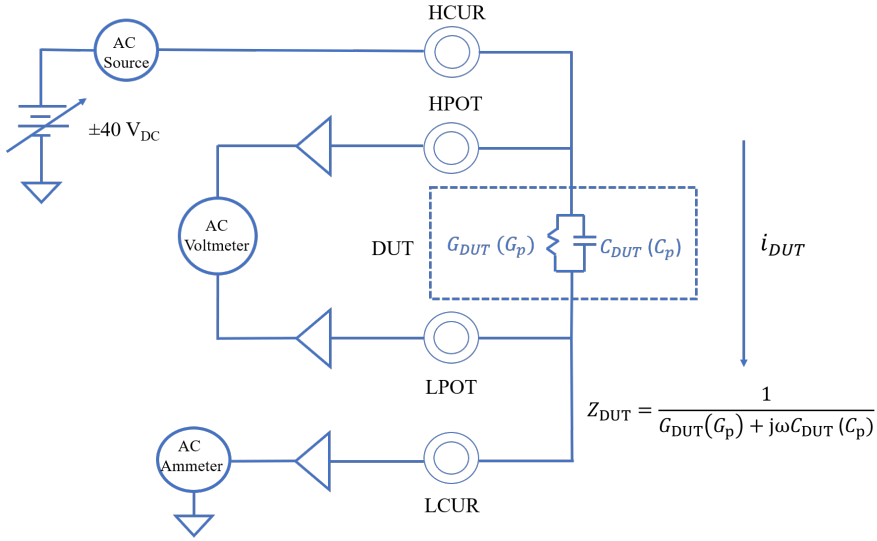


## 3.2 Capacitance-Voltage Characterization

### 3.2.1 Setup Details

#### Basic Test Setup for C-V Measurements

**Figure 3.1** is the basic diagram of a C-V measurement setup. Since the C-V measurements are made at AC frequencies, the capacitance for the DUT is calculated with the following:

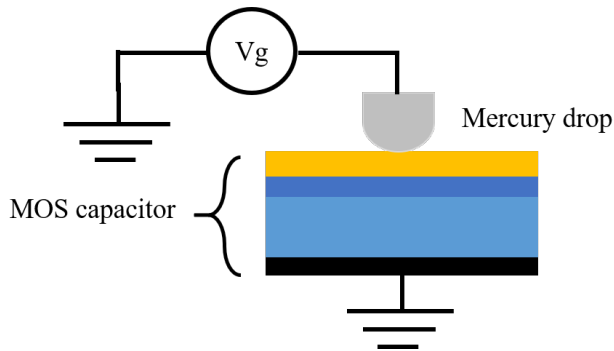


**Figure 3.1:** Basic test setup for C-V measurements.

$$C_p = C_{DUT} = \frac{\text{Im}(i_{DUT})}{2\pi f v_{AC}}, \quad G_p = G_{DUT} = \frac{\text{Re}(i_{DUT})}{v_{AC}} \quad (3.1)$$

$$Z_{DUT} = \frac{1}{Y_{DUT}} = \frac{1}{G_{DUT} + j\omega C_{DUT}} \quad (3.2)$$

where  $i_{DUT}$  is the magnitude of the AC current through the DUT,  $f$  is the test frequency, and  $v_{AC}$  is the magnitude and phase angle of the measured AC voltage,  $C_p$  and  $G_p$  are the parallel capacitance and conductance we will use in **Section 3.2.1**. It measures AC impedance by supplying an AC voltage out of the



**Figure 3.2:** Schematic representation of the mercury probe measuring the MOS capacitor.

high current terminal (HCUR). The current through the device is measured by the low current terminal (LCUR), and the voltage across the device is measured by the high and low potential terminals (HPOT and LPOT). The high leaky capacitor and bad back contact could lead to bad results. Moreover, the back contact should be ohmic.

### Mercury Probe Station

Capacitance-voltage (C-V) measurements can be performed using an HP 4284A LCR meter and a mercury probe station, which provides temporary contact to either the sample's top or bottom, as shown in **Figure 3.2**. The mercury probe eliminates the need for metal electrode deposition on the wafer, simplifying the MOS capacitor fabrication process. With a  $907\ \mu\text{m}$  diameter, the probe's contact area is well-defined for profile measurements. The mercury probe allows lateral capacitance profiling by moving the wafer across the station without damaging the surface or leaving mercury residues. The HP 4284A LCR meter operates over frequencies ranging from 1 kHz to 1 MHz and can evaluate LCR components, materials, and semiconductor devices. Parallel connection ( $C_p - G_p$ ) modes was used for measuring the C-V curves, as shown in **Figure 3.1**.

### Probe Station PM8PS

C-V measurements can also be performed using B1500 and probe station PM8PS. Unlike Mercury probe station, this setup requires samples to be patterned with front-side electrodes to enable proper contact with the probe tips.

While this approach offers greater flexibility in mask design—an advantage for our substrate engineering needs that involve diverse characterization structures. But it also introduces the complexity in the fabrication process.

### 3.2.2 Conductance Method

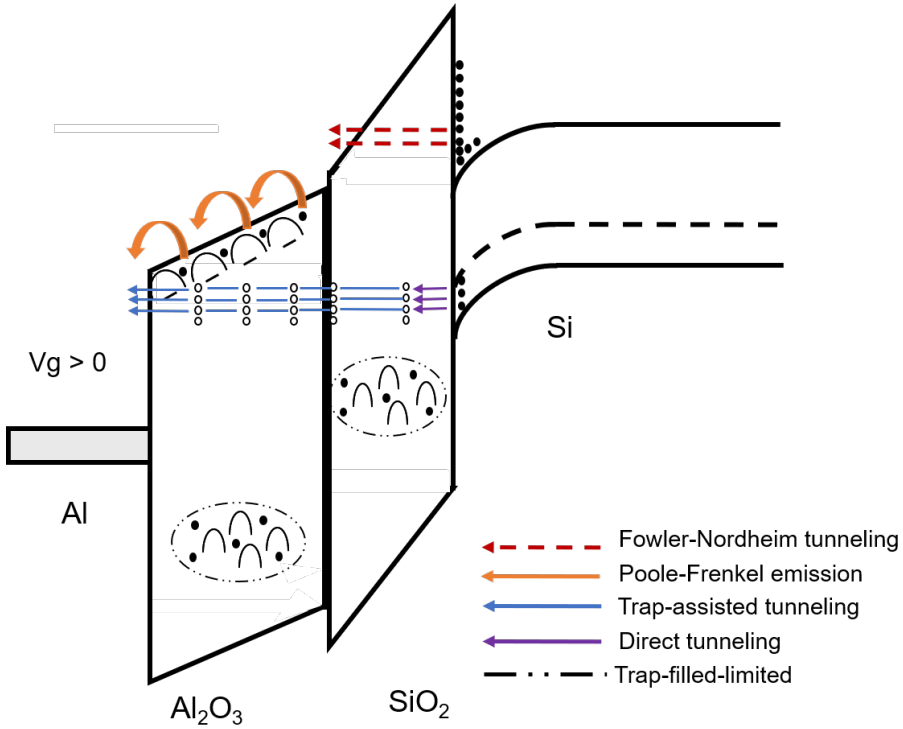
The conductance method, proposed by Nicollian and Goetzberger [31], is one of the most sensitive methods to determine  $D_{it}$ . Interface trap densities of  $10^9 \text{ cm}^{-2}\text{eV}^{-1}$  and lower can be measured. The admittance contribution of interface traps results from the charging and discharging of interface traps by AC bias. The DC bias determines which traps in the bandgap will be charged and discharged by AC bias. It is also the most complete method, because it yields  $D_{it}$  level, the energy distance of the trap to the majority carrier band edge, the capture cross-section for majority carriers, and information about surface potential fluctuations. The technique is based on measuring the equivalent parallel conductance  $G_p$  of a MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

### 3.2.3 Terman Method

The Terman method determines the interface trap density by looking at the stretch-out of a high-frequency C-V curve. The method assumes the absence of interface trap capacitance in the C-V at a sufficiently high frequency. Therefore, they should not contribute any capacitance. How can one measure interface traps if they do not respond to the applied ac signal? Although interface traps do not respond to the ac probe frequency, they do respond to the slowly varying dc voltage and cause the HF C-V curve to stretch out along the gate voltage axis as the occupancy of interface traps changes with gate bias.

The limitation of the Terman method is that the frequency needs to be high enough to ensure a true high-frequency C-V curve is measured. For instance, Silicon carbide (SiC) [32], in which fast interface traps still respond at the usual 1 MHz frequency. This means that the Terman method with conventional frequency up to 1 MHz cannot be applied. It is necessary to increase frequencies to "freeze" fast interface traps. The Terman method cannot be used for traps near the band edges, which have interface trap frequencies that are too high to allow the high-frequency C-V condition.





**Figure 3.3:** Energy band diagram of the semiconductor/dielectric interface in Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> MOS capacitor with leakage mechanisms that can contribute to the charge leakage through the gate dielectric stack.

### 3.3 Current-Voltage Characterization

#### 3.3.1 Fowler-Nordheim Tunneling

The Fowler–Nordheim (FN) tunneling mechanism is a one-step process, illustrated in **Figure 3.3**. When the applied electric field is sufficiently high, the electron wave function can tunnel through the triangular potential barrier into the dielectric conduction band. According to quantum mechanics, if the barrier thickness is small enough (typically <10 nm), the electron wave function has a finite probability of penetrating it. Consequently, the likelihood of finding electrons on the opposite side of the barrier is nonzero due to tunneling. The expression for the tunneling current in the FN tunneling regime is written as below [33]:

$$J_{FN} = \frac{q^3}{8\pi h \phi_B} E_{ox}^2 \exp\left(-\frac{8\sqrt{2m_{ox}}}{3hqE_{ox}} \phi_B^{3/2}\right) \quad (3.3)$$

This equation **Equation 3.3** leads to a characteristic dependence between current density and electric field:

$$\ln\left(\frac{J_{FN}}{E_{ox}^2}\right) \propto -\frac{1}{E_{ox}} \quad (3.4)$$

In the FN tunneling regime, a plot of the logarithm of **Equation 3.4** (known as the FN plot) yields a straight line.

### 3.3.2 Poole-Frenkel Emission

The Poole-Frenkel (PF) transport process describes electrons being released from traps into the conduction band of the dielectric, after which they flow across the dielectric and into the metal through the metal–dielectric interface, as seen in **Figure 3.3**. This mechanism becomes dominant at higher bias compared to trap-assisted tunneling (TAT). The expression for PF tunneling is written as below [34]:

$$J_{PF} = qCE_{ox} \exp\left[\frac{-q\left(\phi_T - \sqrt{\frac{qE_{ox}}{\pi\epsilon}}\right)}{kT}\right] \quad (3.5)$$

This leads to a characteristic dependence between current density and electric field:

$$\ln\left(\frac{J_{PF}}{E_{ox}}\right) \propto E_{ox}^{1/2} \quad (3.6)$$

In the PF tunneling regime, a plot of the logarithm of **Equation 3.6** (known as the PF plot) yields a straight line.

### 3.3.3 Trap-Assisted Tunneling

Instead of one-step FN tunneling through the potential barrier directly, the electron transport process of trap-assisted tunneling (TAT) considers that electrons

first tunnel into the traps in the dielectric from silicon or metal, and subsequently tunnel into metal or silicon under a low bias, illustrated in **Figure 3.3**. The presence of traps inside the dielectric splits the energy barrier into several parts, thus allowing consecutive tunneling through thinner energy barriers, thereby increasing the tunneling probability. The expression of TAT tunneling is demonstrated as below [35]:

$$J_{TAT} = A \exp \left( \frac{-8\pi\sqrt{2qm^*}}{3hE_{ox}} \phi_t^{3/2} \right) \quad (3.7)$$

This leads to a characteristic dependence between current density and electric field:

$$\ln(J_{TAT}) \propto 1/E_{ox} \quad (3.8)$$

In the TAT tunneling regime, a plot of the logarithm of **Equation 3.8** (known as the TAT plot) yields a straight line.

In leakage current measurements of MOS capacitors, different conduction mechanisms may contribute to the observed behavior. If Fowler–Nordheim (FN) tunneling, Poole–Frenkel (PF) emission, or trap-assisted tunneling (TAT) dominate the leakage process, the corresponding FN, PF, or TAT plots will exhibit a linear relationship, where the slope provides the parameters defined by their respective models.

**Table 3.1:** Model Parameters and their Symbols/Units

| Model Parameters                        | Symbol     | Units                           |
|-----------------------------------------|------------|---------------------------------|
| Dynamic dielectric constant             | $\epsilon$ | –                               |
| Electron effective mass                 | $m_e^*$    | kg                              |
| Equilibrium free electron concentration | $n$        | $\text{cm}^{-3}$                |
| Barrier height                          | $q\phi_B$  | eV                              |
| Conduction band Urbach energy           | $W_{TA}$   | meV                             |
| Peak conduction band tail state energy  | $N_{TA}$   | $\text{cm}^{-3} \text{eV}^{-1}$ |
| Series resistance                       | $R_S$      | $\Omega \cdot \text{cm}^2$      |
| Poole-Frenkel pre-exponential constant  | $C$        | –                               |
| Trap ionization potential               | $q\phi_T$  | eV                              |
| Planck's constant                       | $h$        | -                               |
| Temperature                             | T          | K                               |

### 3.4 Photoconductance Characterization

#### Illumination source and spectral filtering

In a photoconductance lifetime measurement, the absorption depth in silicon is a strong function of wavelength. Short (visible) wavelengths are absorbed within a few micrometers of the surface, whereas long (near-infrared) wavelengths penetrate deep into the wafer and generate carriers almost uniformly throughout its thickness. The choice of spectrum, therefore, determines whether the measured signal is dominated by surface or bulk recombination.

##### • White (visible) Illumination

With the visible band-pass filter, or with no infrared filter in place, the excitation is concentrated in the visible part of the spectrum, approximately 400 nm to 700 nm. Because these photons are absorbed close to the surface, the measurement is comparatively sensitive to surface recombination.

##### • Infrared Illumination

With the infrared-pass filter, only the long-wavelength part of the flash reaches the wafer, nominally above 700 nm. Since crystalline silicon becomes transparent beyond its band edge at  $\lambda \approx 1100$  nm, the spectral range that is effective for carrier generation in a silicon wafer lies between approximately 700 nm and 1100 nm. These near-infrared wavelengths penetrate deeply and produce a nearly uniform generation profile across the wafer, which is why infrared illumination is preferred for bulk-lifetime measurements and for thicker wafers, where surface-dominated effects are to be minimized.

#### Carrier Lifetime

Nagel et al. [36] developed a generalized model to analyze the relationship between the effective carrier lifetime ( $\tau_{\text{eff}}$ ) and the excess carrier density ( $\Delta n$ ) by illumination:

$$\tau_{\text{eff}}(\Delta n) = \frac{\Delta n}{G_{\text{bulk}} - \frac{\partial \Delta n}{\partial t}} \quad (3.9)$$

Here  $G_{\text{bulk}}$  is the charge carrier generation rate. In the quasi-steady-state (QSS)

case,  $\frac{\partial \Delta n}{\partial t} \approx 0$ , this gives

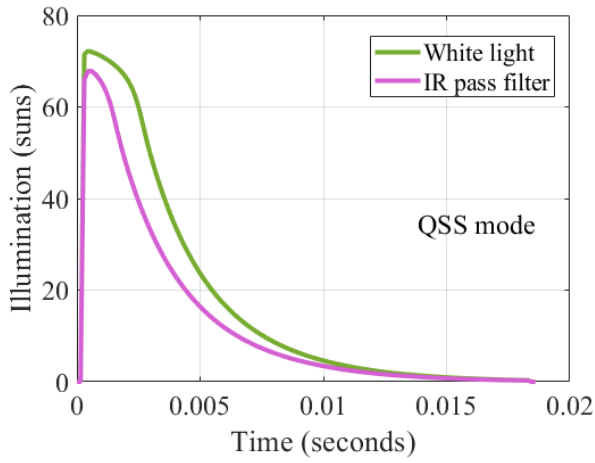
$$\tau_{\text{eff,QSS}}(\Delta n) = \frac{\Delta n}{G_{\text{bulk}}} \quad (3.10)$$

By considering  $G_{\text{bulk}} = 0$  in the transient (trans) case, **Equation 6.27** can be rewritten as:

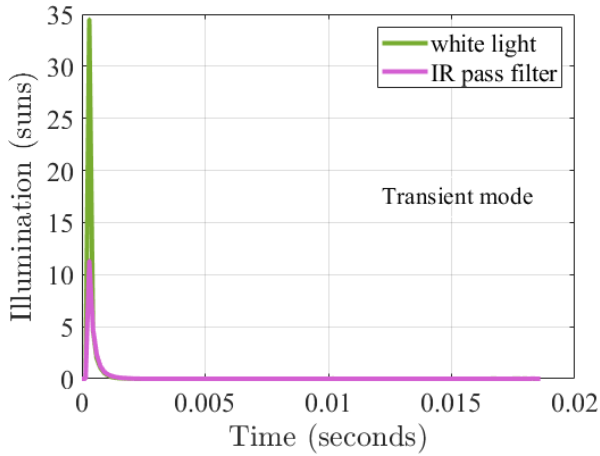
$$\tau_{\text{eff,trans}}(\Delta n) = - \frac{\Delta n}{\frac{\partial \Delta n}{\partial t}} \quad (3.11)$$

Here, note that the lifetime refers specifically to the recombination lifetime. When a flash injects excess carriers into the sample, the sample conductance relaxes as these carriers recombine. Effective surface passivation reduces the surface recombination velocity, thereby slowing down this carrier decay. While the generation lifetime measured via pulsed *C-V* is mostly sensitive to near-midgap traps, the recombination lifetime is influenced by traps spanning a wide energy range. Additionally, the interface trap time constant ( $\tau_{\text{it}}$ ) characterizes the speed at which a trap exchanges carriers with either the conduction or valence band.

For low-lifetime samples ( $< 200 \mu\text{s}$ ), the QSS mode is more suitable, whereas for high-lifetime samples ( $> 200 \mu\text{s}$ ), the transient mode is preferred. For our measurements in the following section, we adopt the QSS mode. To illustrate the distinction between the two modes, we use a single reference sample: thermal atomic layer deposition  $\text{Al}_2\text{O}_3$  (T-ALD) deposited on double-polished standard Si. In a QSS measurement, as shown in **Figure 3.4**, the light intensity should follow a smooth, exponentially decaying curve after a rapid initial rise. The time axis should extend far enough to capture the termination of the flash at about 12 ms, after which both signals decay to zero. In a transient measurement, by contrast, the light intensity appears as a sharp spike on the left of the graph, seen in **Figure 3.5**.



**Figure 3.4:** The light intensity in suns with respect to a time with white light and infrared pass filter at QSS mode for T-ALD  $\text{Al}_2\text{O}_3$  sample.



**Figure 3.5:** The light intensity in suns with respect to a time with white light and infrared pass filter at transient mode for T-ALD  $\text{Al}_2\text{O}_3$  sample.

### Surface Recombination Velocity

When the effective carrier lifetime ( $\tau_{\text{eff}}$ ) is obtained by the measurement

mentioned above, the surface recombination velocity,  $S_{\text{eff}}$ , can be calculated using the following equation [37]:

$$\frac{n_{\text{av}}}{\tau_{\text{eff}}} = \frac{1}{W} \left[ \int_{-W/2}^{W/2} \frac{n(x)}{\tau_{\text{bulk}}(n)} dx + S_{\text{front}} n(-W/2) + S_{\text{back}} n(W/2) \right] \quad (3.12)$$

where  $W$  is the silicon wafer thickness ( $W = 380 \mu\text{m}$  in this work),  $\tau_{\text{bulk}}$  is the bulk carrier lifetime,  $n$  is the excess carrier concentration,  $S_{\text{front}}$  and  $S_{\text{back}}$  are the surface recombination velocity for the front and back surfaces, respectively. The  $\tau_{\text{bulk}}$  is independent of injection level, the integral term becomes  $n_{\text{av}}/\tau_{\text{eff}}$ .

One should note that as the sample structure is symmetrical (i.e., the dielectric stack was deposited on both sides of the double side polished silicon wafer), the surface recombination velocity is identical for the front and back surfaces ( $S_{\text{front}} = S_{\text{back}} = S_{\text{eff}}$ ). Therefore, the Equation 3.12 is simplified as below:

$$\frac{n_{\text{av}}}{\tau_{\text{eff}}} = \frac{n_{\text{av}}}{\tau_{\text{bulk}}} + \frac{S[n(-W/2) + n(W/2)]}{W} \quad (3.13)$$

With the assumption of a uniform carrier concentration, the average excess concentration is the mean of the two surface values:

$$n_{\text{av}} = \frac{n(-W/2) + n(W/2)}{2} \quad (3.14)$$

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + 2 \left( \frac{S_{\text{eff}}}{W} \right) \quad (3.15)$$

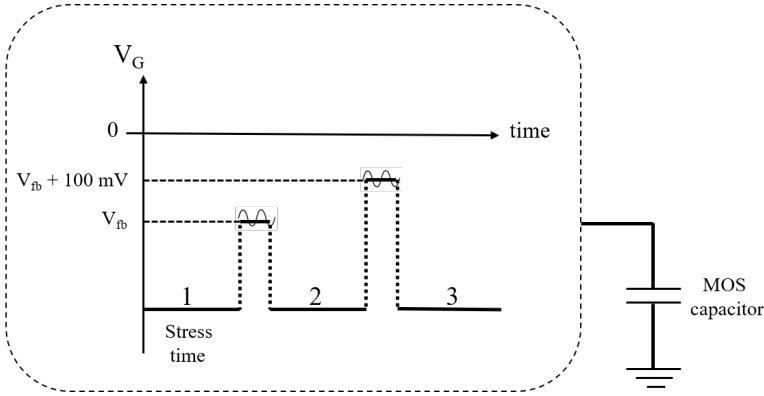
$$S_{\text{eff}} = \frac{W}{2} \left( \frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}} \right) \quad (3.16)$$

and  $\tau_{\text{bulk}} \rightarrow \infty$  due to the high quality of the FZ wafer. In this case, Equation 6.30 can be approximated to:

$$S_{\text{eff}} \approx \frac{W}{2\tau_{\text{eff}}} \quad (3.17)$$

### 3.5 Negative Bias Time Instability (NBTI) Characterization

Device under test (DUT) was subjected to NBTI degradation using the measure/stress/measure (MSM) protocol, illustrated in **Figure 3.6**. The protocol sequentially applies a constant negative voltage stress on the gate electrode of MOS capacitor for a certain period of time at elevated temperatures ranging from 75 to 150 °C. The whole stress time was fixed to 3,600 s, and a C-V measurement was done at each 100 s step at 500 kHz frequency. To extract the flat-band voltage  $\Delta V_{fb}$ , two capacitance values were extracted at  $V_{fb}$  and  $V_{fb} + 100$  mV, respectively [38]. The extraction of  $V_{fb}$  and  $N_a$  is based on the slope of the linear part of the measured capacitance  $C$  versus gate voltage [39].



**Figure 3.6:** Schematic illustration of MSM-CV protocols used during NBTI stress measurements.

The C-V curves are measured at 500 kHz, and the constant stress voltage is applied at the gate. The C-V curve is observed to shift towards positive voltage with stressing time. The shift in flatband voltage ( $\Delta V_{fb}$ ) is measured with respect to the C-V curve obtained before stressing at  $t = 0$  s. Since  $\Delta V_{fb}$  is attributed to the trapping of charges by the gate dielectric film, the trapped charge density ( $N_t$ ) can be calculated as below:

$$N_t = \frac{\Delta V_{fb} \cdot d}{k' \cdot \epsilon_0} \quad (3.18)$$

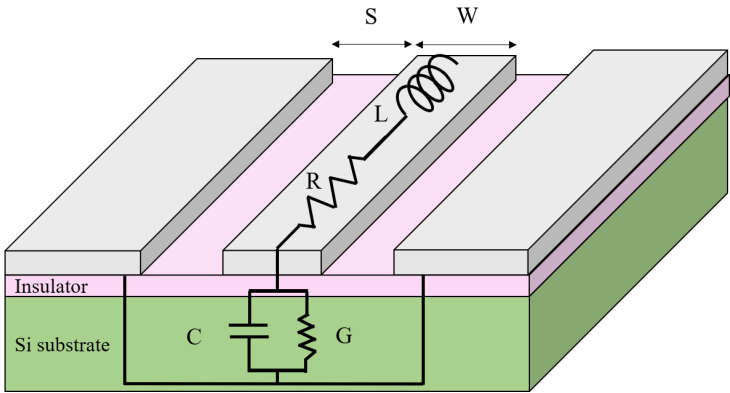
where  $\epsilon_0$  is the permittivity of free space,  $d$  is the physical thickness, and  $k'$  is the dielectric constant of the dielectric film.



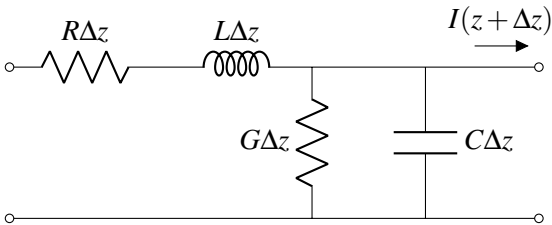
3.6 Small-Signal Characterization

3.6.1 Substrate Parameters Extraction

In this section, a coplanar waveguide (CPW) is depicted in **Figure 3.7** above the conductive metal layer atop an insulator-semiconductor stack. Ideally, a transmission line or waveguide would have a unity transmission coefficient, with 100% of the input power reaching the output. However, materials always have some degree of loss associated with them. Due to finite metal conductivity, the propagation of the signal through the metal lines leads to energy dissipation within the metal. Another source of loss is due to finite substrate resistivity, as RF fields penetrating these materials induce RF currents within them.



**Figure 3.7:** Schematic representation of a CPW line and the RLGC equivalent circuit elements representing it. The important dimensions of signal conductor width ( $W$ ) and slot width ( $S$ ) are also indicated.



**Figure 3.8:** Infinitesimal length  $\Delta z$  of the line in **Figure 3.7**.

### Extraction of $\gamma$ and $Z_c$

The first step involves using the measured S-parameters to extract the propagation constant  $\gamma$  and characteristic impedance  $Z_c$  based on established methods by Eo and Dehan.

1. Eo's Method [40]: Eo's method provides the following expressions to compute  $\gamma$  and  $Z_c$ :

$$e^{-\gamma L} = \frac{1}{\left(\frac{1-S_{11}^2+S_{21}^2}{2S_{21}} + K\right)} \quad (3.19)$$

$$K = \sqrt{\frac{((S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2)}{(2S_{11})^2}} \quad (3.20)$$

The characteristic impedance is given by:

$$Z_c^2 = Z_0^2 \cdot \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \quad (3.21)$$

2. Dehan's Method [41]: Alternatively, Dehan proposes the following expression for the propagation constant:

$$\gamma = 2 \cdot \tanh \left( \sqrt{\frac{(1 - S_{11} - S_{12})(1 + S_{11} - S_{12})}{(1 + S_{11} + S_{12})(1 - S_{11} + S_{12})}} \right) \quad (3.22)$$

### RLGC Extraction

After computing the characteristic impedance  $Z_c$  and the propagation constant  $\gamma$ , these quantities are utilized to extract the equivalent lumped-element parameters of the CPW transmission line. The RLGC parameters— $R$  (series resistance per unit length),  $L$  (series inductance per unit length),  $C$  (shunt capacitance per unit length), and  $G$  (shunt conductance per unit length)—constitute a distributed model that accurately characterizes the electrical behavior of the line.

These RLGC parameters are essential for analyzing the performance and signal integrity of the CPW structure. A detailed representation of the RLGC elements for the CPW line is illustrated in **Figure 3.8**.

As demonstrated in [42] and [43], the characteristic impedance  $Z_c$  and the propagation constant  $\gamma$  can be expressed in terms of the RLGC parameters as:

$$Z_c = \sqrt{\frac{j\omega L + R}{j\omega C + G}} \quad (3.23)$$

$$\gamma = \sqrt{(j\omega L + R)(j\omega C + G)} \quad (3.24)$$

where  $\omega$  is the angular frequency, defined as  $\omega = 2\pi f$ .

From equations (3.23) and Equation 3.24, the RLGC parameters can be calculated as:

$$R = \operatorname{Re}\{\gamma Z_c\} \quad (3.25)$$

$$L = \frac{\operatorname{Im}\{\gamma Z_c\}}{\omega} \quad (3.26)$$

$$G = \operatorname{Re}\left\{\frac{\gamma}{Z_c}\right\} \quad (3.27)$$

$$C = \frac{\operatorname{Im}\left\{\frac{\gamma}{Z_c}\right\}}{\omega} \quad (3.28)$$

Furthermore, the propagation constant  $\gamma$  can be expressed as:

$$\gamma = \alpha + j\beta \quad (3.29)$$

where  $\alpha$  is the attenuation constant (representing losses per unit length) calculated by Equation 3.30, and  $\beta$  is the phase constant (representing the electrical phase shift) expressed by Equation 3.31. This form is commonly used in transmission line characterization to extract the frequency-dependent loss behavior.

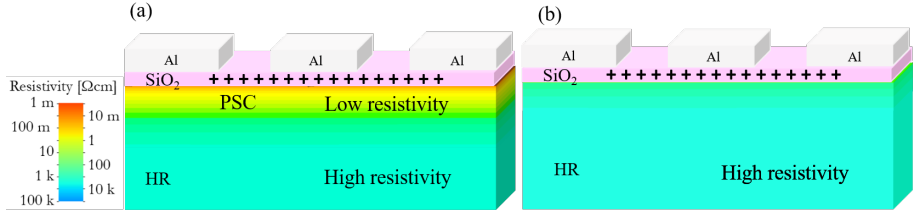
$$\alpha = \frac{1}{2} \left( \frac{R}{Z_0} + GZ_0 \right) \quad (3.30)$$

$$\beta \approx \omega \sqrt{LC} \quad (3.31)$$

where  $Z_0 = \sqrt{\frac{L}{C}}$  is the characteristic impedance of the line.

### Effective Resistivity Extraction

The full extraction procedure can be found in Lucas Nyssens's thesis [44]. Here we just briefly demonstrate the procedure. High-resistivity substrates often exhibit an inhomogeneous resistivity distribution, characterized by a lower resistivity near the interface and a significantly higher resistivity deeper in the bulk. This gradient is primarily caused by positive oxide charges, as illustrated



**Figure 3.9:** CPW transmission line atop of a real inhomogeneous substrate in (a) and atop of a modeled homogeneous substrate in (b).

in **Figure 3.9 (a)**.

To simplify analysis, the concept of *effective resistivity* is employed, as introduced in [12]. The effective resistivity  $\rho_{\text{eff}}$  serves as a representative electrical parameter that captures the overall resistive behavior of the non-uniform substrate, assuming an equivalent homogeneous material, as shown in **Figure 3.9 (b)**.

### Extraction Procedure

The extraction procedure of  $\rho_{\text{eff}}$  and  $\epsilon_{r,\text{eff}}$  of the substrate material stack below the CPW line is as follows.  $C_{\text{data}}$  and  $G_{\text{data}}$  include contributions from the material substrate stack of interest, below the CPW line, but also contributions from materials above (and between) the CPW line. Referring to **Figure 3.10**, these contributing terms are expressed as:

$$C_{\text{data}} = C_{\text{top}} + C_{\text{bot}} \quad [\text{F/m}] \quad (3.32)$$

$$G_{\text{data}} = G_{\text{top}} + G_{\text{bot}} \quad [\text{S/m}] \quad (3.33)$$

To extract the effective resistivity, the substrate below the CPW line is equated to a uniform material, as depicted by **Figure 3.10**. We are interested in the electrical parameters of the substrate stack below the CPW line  $C_{\text{bot}}$  and  $G_{\text{bot}}$ , including oxide capacitance. They can be extracted from the data if the material parameters of the material above the CPW line are known<sup>1</sup>. To extract the effective electrical properties of the material stack below the line, the extraction

<sup>1</sup>In this thesis, the above material is air, so  $\epsilon_{r,\text{eff},\text{top}} = 1$  and  $\sigma_{\text{top}} = 1/\rho_{\text{top}} = 0$ . Note that the extraction of  $\rho_{\text{eff}}$  does not depend on  $\epsilon_{r,\text{eff},\text{top}}$  (see **Equation 3.41**), though the extraction of  $\epsilon_{r,\text{eff}}$  does.

procedure requires the knowledge of material parameters above the line. We then write:

$$C_{\text{bot}} = C_{\text{data}} - C_{\text{top}} \quad [\text{F/m}] \quad (3.34)$$

$$G_{\text{bot}} = G_{\text{data}} - G_{\text{top}} \quad [\text{S/m}] \quad (3.35)$$

Knowing the dimensions of the CPW line, the impedance parameters  $C_{\text{top}}$ ,  $G_{\text{top}}$ ,  $C_{\text{bot}}$ ,  $G_{\text{bot}}$  can be related to the material parameters, in the case of uniform materials, using the closed form expressions from [45]:

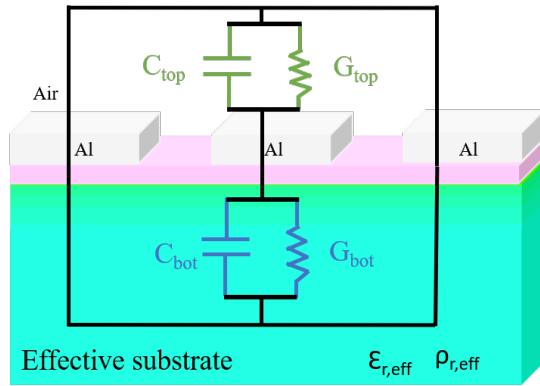
$$C_{\text{top}} = \epsilon_0 \epsilon_{r,\text{eff},\text{top}} \cdot F_{\text{top}}(\text{DIMS}) \quad [\text{F/m}] \quad (3.36)$$

$$G_{\text{top}} = \frac{1}{\rho_{\text{eff},\text{top}}} \cdot F_{\text{top}}(\text{DIMS}) \quad [\text{S/m}] \quad (3.37)$$

$$C_{\text{bot}} = \epsilon_0 \epsilon_{r,\text{eff},\text{bot}} \cdot F_{\text{bot}}(\text{DIMS}) \quad [\text{F/m}] \quad (3.38)$$

$$G_{\text{bot}} = \frac{1}{\rho_{\text{eff},\text{bot}}} \cdot F_{\text{bot}}(\text{DIMS}) \quad [\text{S/m}] \quad (3.39)$$

where  $F_{\text{top}}$  and  $F_{\text{bot}}$  are geometrical functions of the dimensions *DIMS* of the CPW line (conductor width, spacing and thickness)<sup>2</sup>, calculated according to [45].



**Figure 3.10:** A modeled homogeneous substrate with uniform effective relative permittivity ( $\epsilon_{r,\text{eff}}$ ) and uniform effective resistivity ( $\rho_{r,\text{eff}}$ ).

<sup>2</sup>Analogous example: for a parallel plate capacitor,  $C$  is related to  $\epsilon$  through the following well-known formula:  $C = \epsilon \cdot F(\text{DIMS}) = \epsilon \cdot F(A, d) = \epsilon \cdot A/d$ , where  $A$  is the area of the parallel plates, and  $d$  is the distance between the two plates. In that case, the geometrical factor is  $F = A/d$ .

we finally write:

$$\epsilon_{r,eff,bot} = \frac{C_{data} - \epsilon_0 \epsilon_{r,eff,top} \cdot F_{top}(DIMS)}{\epsilon_0 \cdot F_{bot}(DIMS)} \quad [\text{F/m}] \quad (3.40)$$

$$\rho_{eff,bot} = \frac{F_{bot}(DIMS)}{G_{data} - \sigma_{eff,top} \cdot F_{top}(DIMS)} \quad [\Omega\text{m}] \quad (3.41)$$

These equations are equivalent to the original formulation from [12]<sup>3</sup>, and require the knowledge of the electrical parameters of the top material, along with the CPW line geometry.

### 3.7 Large-Signal Characterization

In the previous **Section 3.6**, a small-signal setup was employed with an input power of -5 dBm to measure the S-parameters of the device, providing a linear analysis of its performance. The S-parameters were measured to understand the device's behavior under low-power conditions, which ensures that the passive device remains within its linear operating range. However, passive devices can exhibit non-linear behavior when subjected to large signals, particularly due to substrate-related effects. In this section, the focus shifts to the non-linear effects observed in a CPW line when exposed to large signal levels, specifically what is the setup used to quantify the generated non-linearities.

#### 3.7.1 Description of the HD 900 MHz On-Wafer Measurement Setup

In order to evaluate harmonic distortion originating from the substrate, a simple CPW line structure is employed. Large-signal measurements of the CPW lines are performed on-wafer using a dedicated setup [46] based usually on a Performance Network Analyzer (PNA) or on a spectrum analyzer and signal generator.

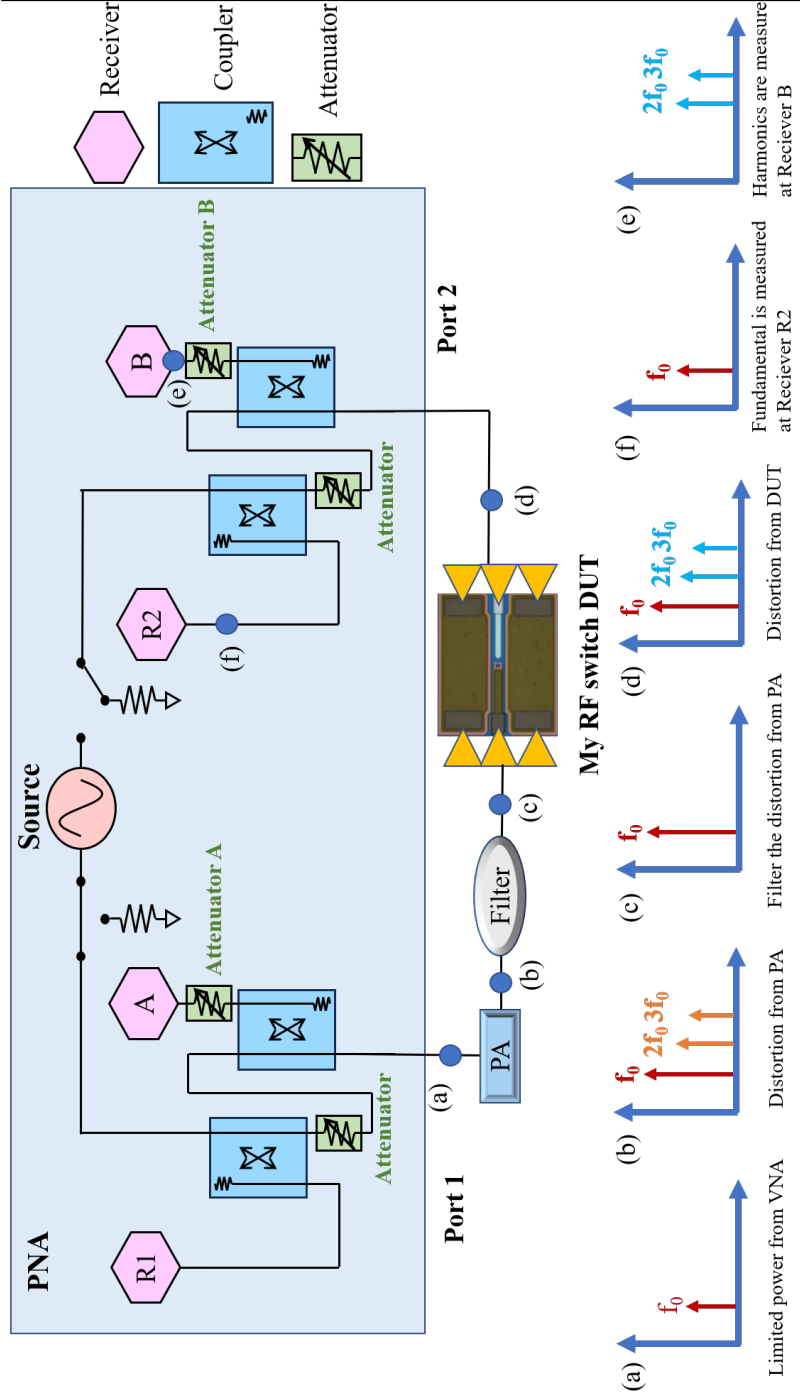
The large-signal measurement setup used for the extraction of harmonic distortion in **Section 5.3.5** is shown in **Figure 3.11**. Key points of the setup are labeled from (a) to (f), each point is explained below the schematic. The main objective is to sweep the power from small-signal levels up to 24 dBm. Since the VNA<sup>4</sup> is unable to reach such high power levels, an RF power amplifier

<sup>3</sup>In that work, parameter  $C_0$  and  $q$  (filling factor) are used together instead of  $F_{top}$  and  $F_{bot}$ . They are linked in the following way:  $C_0 = \epsilon_0 \cdot F_{bot}$ ,  $q = F_{bot} / (F_{bot} + F_{top})$ . Furthermore, in the original paper,  $\epsilon_{r,eff,top}$  was assumed to be equal to unity and  $\sigma_{eff,top}$  was assumed to be zero.

<sup>4</sup>In our case, we utilize the Keysight PNA-X 26.5 GHz vector network analyzer [46].

(PA) is inserted between Port 1 of the VNA and the input of the device under test (DUT). The VNA delivers a pure signal at 900 MHz, which is ideal for this application. However, the power sweep of the fundamental is relatively low and insufficient to reach the desired high power levels (see **Figure 3.11 (a)**).

Following this, the signal at point **(a)** is amplified by the PA, allowing the power sweep to reach levels up to approximately 24 dBm. However, due to the inherent non-linearities of the PA, harmonics components are introduced at 1.8 GHz ( $2f_0$ ) and 2.7 GHz ( $3f_0$ ) as observed at point **(b)**. To ensure that a clean fundamental tone is applied to DUT, passive band-pass filters are used. These filters allow the 900 MHz signal to pass through while suppressing all other frequencies, resulting in the signal at point **(c)**. When the pure signal passes through the DUT, it generates harmonics H2 at  $2f_0$  and H3 at  $3f_0$  (see **Figure 3.11 (d)**). These harmonics are the primary focus of this study. Before analyzing them, it is essential to ensure they are properly received by each receiver of the VNA. The signal at **(d)** is routed through the coupler via Port 2. At this point, the signal is directed to receiver B through a high-pass filter that allows only the frequencies  $2f_0$  and  $3f_0$  to pass. Attenuator B is set to zero since the fundamental frequency is eliminated, and the harmonic levels are not large enough to damage the VNA. If the signal from **(d)** is directed to point **(e)** through Attenuator B. At the same time, Receiving fundamental output properly at Receiver R2 is crucial. A careful choice of the attenuator value ensures the fundamental signal is properly measured at **(f)**. The measurements are performed twice. First, the input power at the DUT is swept, and the fundamental H1 is measured at Receiver R1. Second, the input power at the DUT is swept again to measure H2 and H3 at Receiver B.



**Figure 3.11:** Practical setup for the on-wafer harmonic distortion measurement using an RF single-tone signal.



### 3.8 Chapter Summary

This chapter presents the characterization methodologies employed throughout this thesis to electrically evaluate MOS capacitors and CPW line test structures. The emphasis is placed on establishing reliable and physically meaningful extraction techniques for key material, interface, and substrate parameters.

Capacitance–voltage ( $C$ – $V$ ) characterization is first introduced as a fundamental tool for MOS capacitor analysis. Measurement setup details are described, followed by the conductance methods and the Terman for extracting interface trap density. These approaches provide complementary information on the energy distribution and dynamic response of interface states and form the basis for interface quality assessment in subsequent chapters.

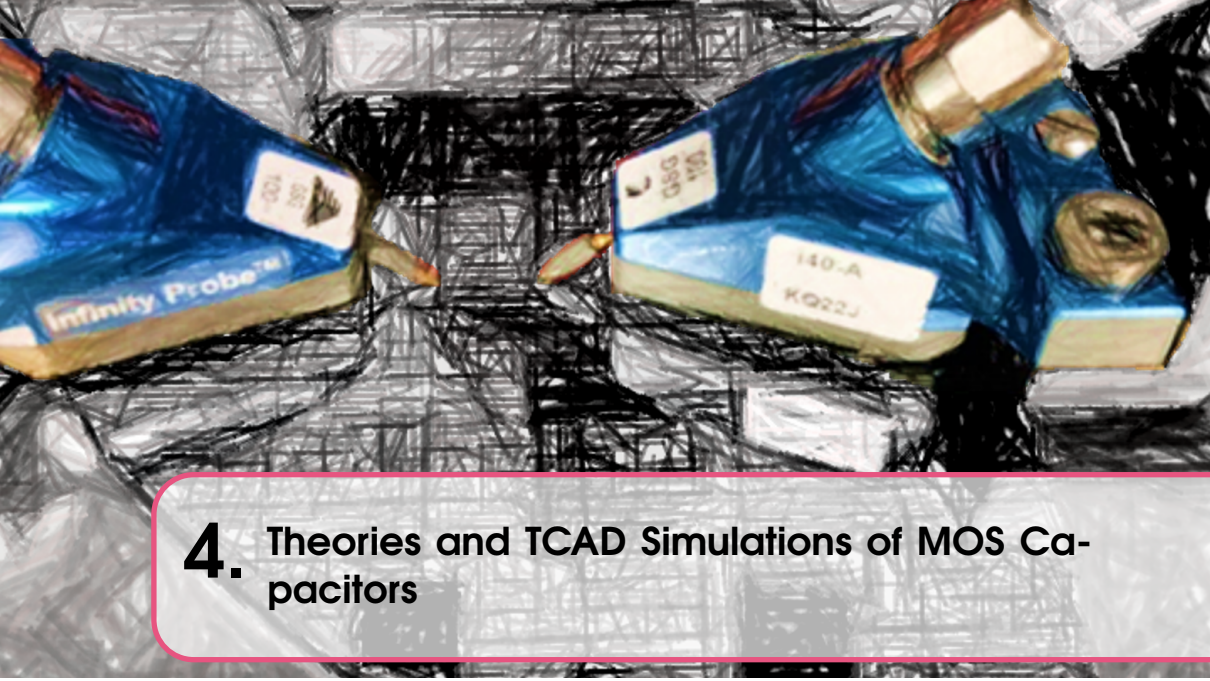
Current–voltage ( $I$ – $V$ ) characterization is then discussed to analyze dielectric leakage mechanisms. Fowler–Nordheim tunneling, Poole–Frenkel emission, and trap-assisted tunneling models are introduced to identify dominant conduction processes under different electric-field regimes and to correlate leakage behavior with defect-related phenomena.

Photoconductance measurements using the Sinton technique are presented to extract effective carrier lifetime, enabling the evaluation of bulk and interface recombination effects. Reliability aspects are addressed through Negative Bias Temperature Instability (NBTI) characterization, providing insight into charge trapping dynamics and long-term dielectric stability.

Finally, small-signal and large-signal characterization methodologies are detailed. Small-signal measurements detailed the process of extracting effective resistivity and explained how the DC bias is applied to the CPW line, while large-signal characterization, including on-wafer harmonic distortion measurements, allows the assessment of nonlinear behavior under RF excitation.

Overall, this chapter establishes a comprehensive and consistent experimental framework that supports the quantitative analysis of interface quality, dielectric integrity, substrate effects, and linearity throughout the remainder of the thesis.





## 4. Theories and TCAD Simulations of MOS Capacitors

### 4.1 Introduction

Admittance characteristics, such as C-V and conductance characteristics, are frequently used in CMOS to characterize crucial parameters of Si MOS capacitors, including the flatband voltage, fixed charge, work function, effective oxide thickness, doping level, and the quality of the semiconductor-dielectric interface passivation (which depends on the interface trap density). C-V measurements, particularly conductance measurements, are regarded as the most effective tools for investigating interface trap density, owing to their high inherent sensitivity of the electrical measurements, methodological simplicity, broad availability of measurement equipment, and the relative ease of capacitor structures.

This chapter presents the core theory of this thesis, focusing on the physical mechanisms of interface traps and the modeling of MOS capacitors with different substrate resistivities. It also applies various admittance-based techniques to extract the interface trap density.

### 4.2 Interface Trap Modeling In MOS Capacitors

#### 4.2.1 What Are Interface Traps ?

Interface traps (also called interface states) are energy levels located at the boundary between silicon and silicon dioxide ( $\text{Si-SiO}_2$ ) or silicon and other dielectrics in MOS capacitors. Think of the interface as a “border” between

two materials. Ideally, this border is smooth and perfect, but in reality, there are imperfections — like dangling bonds, a common source of interface traps. These imperfections create energy levels inside the silicon band gap at the interface. These levels can trap or release electrons or holes, depending on their energy relative to the Fermi level. They act like small energy wells: they can “catch” a charge carrier (electron or hole) from the semiconductor. Whether a trap is filled or empty depends on:

- Trap position in the bandgap
- The Fermi level: if the Fermi level is above the trap, the trap tends to be filled with an electron. If the Fermi level is below the trap, the trap tends to be empty
- The band bending (which is affected by gate voltage)

### 4.2.2 Energy Loss Mechanism

#### Positive Half-Cycle

For P-type substrate, during the positive half-cycle of the AC voltage, the conduction band in silicon moves closer to the Fermi level at the surface. This causes the free electrons near the surface to gain energy — their average energy increases. However, interface traps (energy levels at the Si–SiO<sub>2</sub> interface) don’t respond immediately at certain frequencies — they lag behind the AC signal. Some of these traps are empty, even though they lie below the Fermi level, where they would normally be filled. High-energy electrons from the silicon get captured by these lower-energy traps, and this energy difference is dissipated in the form of heat (transferred to phonons). This process helps equalize the energy between free and trapped electrons, but the lost energy comes from the AC signal.

#### Negative Half-Cycle

For P-type substrate, during the negative half-cycle, the conduction band moves away from the Fermi level at the surface. Now, trapped electrons in interface states above the Fermi level get released into the silicon. These electrons lose energy as they enter the conduction band and become part of the free electron population. The energy needed to release them comes from phonons. After emission, the free electrons have a slightly higher average energy, but they quickly lose this energy to phonons, again heating the lattice.

Thus, the energy loss occurs during both halves of the AC cycle and must be

supplied by the signal source. This energy loss is observed as an equivalent parallel conductance  $G_p$ , which will be used in the conductance method to extract interface traps.

### 4.2.3 Interface Trap Energy Distribution

#### Continuous Trap Distribution

To better understand the mechanism and characterization of interface traps, we return to the trap models used in Silvaco manual. The model considers two tail bands: a donor-like valence band  $g_{TD}(E)$  and an acceptor-like conduction band  $g_{TA}(E)$ . Additionally, it includes two deep-level gaussian bands: one acceptor-like  $g_{GA}(E)$  and the other donor-like  $g_{GD}(E)$ .

The formulas used to describe Gaussian distributions and tail distributions for acceptor-like and donor-like traps in Atlas are given as:

$$g_{GA}(E) = N_{GA} \exp \left[ - \left( \frac{E_{GA} - E}{W_{GA}} \right)^2 \right] [\text{cm}^{-2} \cdot \text{eV}^{-1}] \quad (4.1)$$

$$g_{GD}(E) = N_{GD} \exp \left[ - \left( \frac{E - E_{GD}}{W_{GD}} \right)^2 \right] [\text{cm}^{-2} \cdot \text{eV}^{-1}] \quad (4.2)$$

$$g_{TA}(E) = N_{TA} \exp \left[ \frac{E - E_c}{W_{TA}} \right] [\text{cm}^{-2} \cdot \text{eV}^{-1}] \quad (4.3)$$

$$g_{TD}(E) = N_{TD} \exp \left[ \frac{E_v - E}{W_{TD}} \right] [\text{cm}^{-2} \cdot \text{eV}^{-1}] \quad (4.4)$$

Here,  $E$  is the trap energy,  $E_c$  is the conduction band energy,  $E_v$  is the valence band energy, and the subscripts (T, G, A, D) stand for tail, Gaussian (deep level), acceptor, and donor-like trap states, respectively. The quantities  $N_{TA}$ ,  $N_{TD}$ ,  $N_{GA}$ ,  $N_{GD}$  and  $W_{TA}$ ,  $W_{TD}$ ,  $W_{GA}$ ,  $W_{GD}$  are defined in **Table 4.1**. For an exponential tail distribution, the density of states is described by their conduction and valence band edge intercept densities ( $N_{TA}$  and  $N_{TD}$ ), and by their characteristic decay energies ( $W_{TA}$  and  $W_{TD}$ ) in **Equation 4.3** and **Equation 4.4**. For Gaussian

**Table 4.1:** Typical tail and gaussian trap distribution parameters for interface, as reported in [47].

| Parameter | Description                                                                                                      | Value (e.g.)                                                        |
|-----------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| NGA       | Peak value of the Gaussian acceptor trap distribution $g_{GA}(E)$                                                | $1 \cdot 10^{10}$ - $1 \cdot 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ |
| EGA       | Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution $g_{GA}(E)$ | 0.55 eV                                                             |
| WGA       | Characteristic decay energy of the Gaussian acceptor trap distribution $g_{GA}(E)$                               | 0.15 eV                                                             |
| NGD       | Peak value of the Gaussian donor trap distribution $g_{GD}(E)$                                                   | $1 \cdot 10^{10}$ - $1 \cdot 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ |
| EGD       | Energy position from the valence band edge of the peak of the Gaussian donor trap distribution $g_{GD}(E)$       | 0.55 eV                                                             |
| WGD       | Characteristic decay energy of the Gaussian donor trap distribution $g_{GD}(E)$                                  | 0.15 eV                                                             |
| NTA       | Value of the Tail acceptor trap distribution $g_{TA}(E)$ at the conduction band edge                             | $1 \cdot 10^{10}$ - $1 \cdot 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ |
| WTA       | Characteristic decay energy of the Tail acceptor trap distribution $g_{TA}(E)$                                   | 33 meV                                                              |
| NTD       | Value of the Tail donor trap distribution $g_{TD}(E)$ at the valence band edge                                   | $1 \cdot 10^{10}$ - $1 \cdot 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ |
| WTD       | Characteristic decay energy of the Tail donor trap distribution $g_{TD}(E)$                                      | 49 meV                                                              |

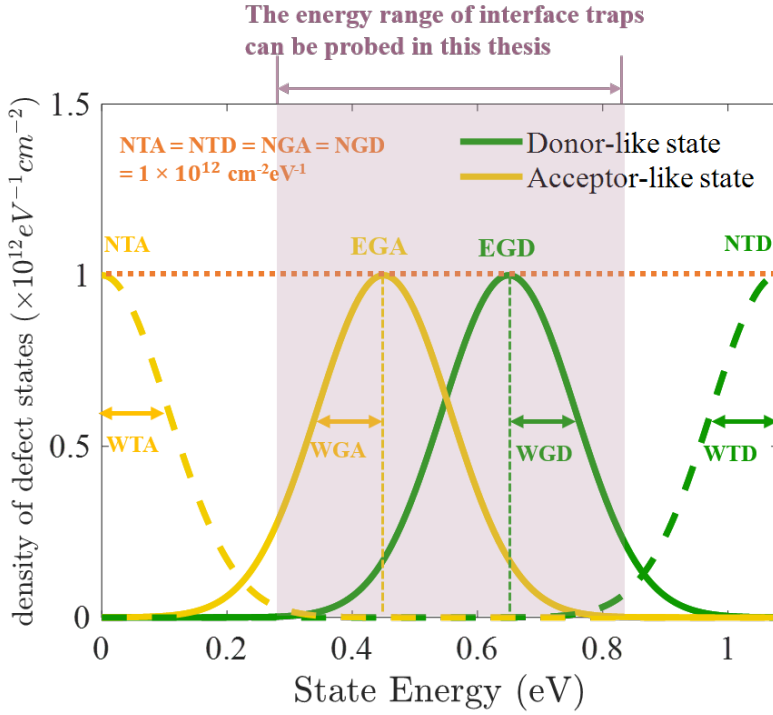
distributions, the density of states is described by their total density of states ( $N_{GA}$  and  $N_{GD}$ ), their characteristic decay energy ( $W_{GA}$  and  $W_{GD}$ ), and their peak energy/peak distributions ( $E_{GA}$  and  $E_{GD}$ ) in **Equation 4.1** and **Equation 4.2**. **Equation 4.1** to **Equation 4.4** are graphically represented in **Figure 4.1**.

**Table 4.2:** Typical capture cross-sections of tail and gaussian-type trap distributions associated with Si, as reported in [47].

| Parameter      | Description                                                                             | Value (in simulations)            |
|----------------|-----------------------------------------------------------------------------------------|-----------------------------------|
| $\sigma_{GAe}$ | Capture cross-section for electrons of the acceptor traps of the Gaussian distribution. | $2.0 \cdot 10^{-16} \text{ cm}^2$ |
| $\sigma_{GAh}$ | Capture cross-section for holes of the acceptor traps of the Gaussian distribution.     | $2.0 \cdot 10^{-15} \text{ cm}^2$ |
| $\sigma_{GDe}$ | Capture cross-section for electrons of the donor traps of the Gaussian distribution.    | $2.0 \cdot 10^{-15} \text{ cm}^2$ |
| $\sigma_{GDh}$ | Capture cross-section for holes of the donor traps of the Gaussian distribution.        | $2.0 \cdot 10^{-16} \text{ cm}^2$ |
| $\sigma_{TAe}$ | Capture cross-section for electrons of the acceptor traps of the Tail distribution.     | $1.0 \cdot 10^{-17} \text{ cm}^2$ |
| $\sigma_{TAh}$ | Capture cross-section for holes of the acceptor traps of the Tail distribution.         | $1.0 \cdot 10^{-15} \text{ cm}^2$ |
| $\sigma_{TDe}$ | Capture cross-section for electrons of the donor traps of the Tail distribution.        | $1.0 \cdot 10^{-15} \text{ cm}^2$ |
| $\sigma_{TDh}$ | Capture cross-section for holes of the donor traps of the Tail distribution.            | $1.0 \cdot 10^{-17} \text{ cm}^2$ |

If  $W_{GA}$  and  $W_{GD}$  are assigned very large values (e.g., 1000 eV), the Gaussian trap distributions effectively approximate a uniform and continuous distribution across the bandgap.

In the steady-state, the probability of occupation of a trap level at energy  $E$  for the tail and Gaussian acceptor and donor states is given by the Fermi–Dirac (FD) occupation function [47]:



**Figure 4.1:** Tail (in dash) and Gaussian (in solid) density distributions of acceptor and donor-like trap states of  $\text{SiO}_2/\text{Si}$  interface.  $\text{WGA} = \text{WGD} = \text{WTA} = \text{WTD} = 0.15 \text{ eV}$ ,  $\text{EGA} = 0.45 \text{ eV}$ ,  $\text{EGD} = 0.65 \text{ eV}$  (the interface traps can be probed in the energy range of 0.24 to 0.85 eV in this thesis).



$$f(E) = \frac{1}{1 + d_g \exp\left(\frac{E - E_F}{kT}\right)}, \quad (4.5)$$

where  $E_F$  is the equilibrium Fermi level,  $k$  is the Boltzmann constant,  $d_g$  is the ground-state degeneracy (which has a value of two for donor-like traps and four for acceptor-like traps), and  $T$  is the lattice temperature.

Combining **Equation 4.1 - Equation 4.4**, the ionized densities of acceptor and donor-like states ( $n_T$  and  $p_T$ , respectively) are expressed as:

$$n_T = \int_{E_V}^{E_C} (g_{TA}(E) \cdot f_{TA}(E) + g_{GA}(E) \cdot f_{GA}(E)) dE, \quad (4.6)$$

$$p_T = \int_{E_V}^{E_C} (g_{TD}(E) \cdot (1 - f_{TD}(E)) + g_{GD}(E) \cdot (1 - f_{GD}(E))) dE, \quad (4.7)$$

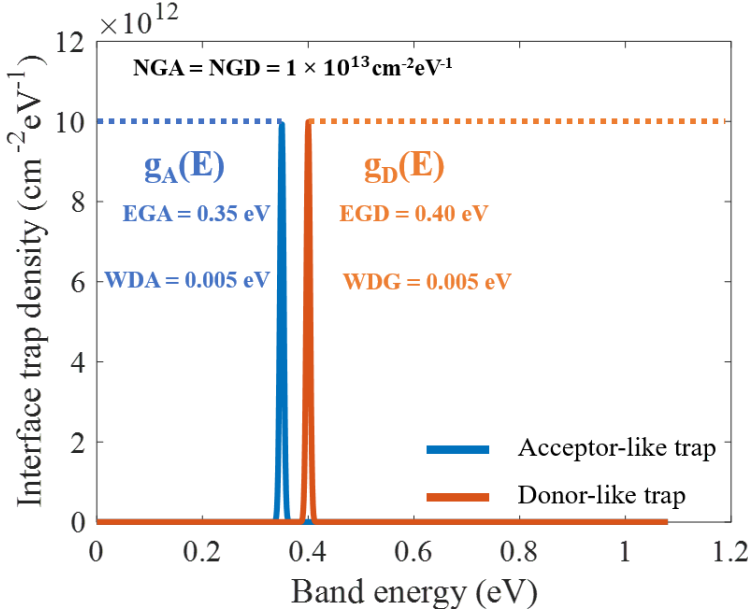
where  $f_{TA}$ ,  $f_{GA}$  and  $f_{TD}$ ,  $f_{GD}$  denote the FD functions of tail and Gaussian acceptor and donor-like traps, respectively. There are two methods available to ATLAS users for handling the integrals **Equation 4.6** and **Equation 4.7**. They are named CONTINUOUS and DISCRETE methods. The CONTINUOUS method evaluates  $n_T$  and  $p_T$  by using a numerical integral scheme adopted from [48]. In the DISCRETE method, however, the integrals **Equation 4.6** and **Equation 4.7** are replaced by summations, which run over the number of discrete energy levels (NUMA and NUMD).

In the simulation of our work, we specified NUMA and NUMD (= 1000) to simulate the continuous distribution of acceptor and donor states. The ionized densities of acceptor and donor-like states,  $n_T$  and  $p_T$ , respectively, can be expressed in a discrete form as:

$$n_T = \sum_{i=0}^{\text{NUMA}} \left[ f_{TA}(E) \cdot \int_{-\infty}^{+\infty} g_{TA}(E) dE + f_{GA}(E) \cdot \int_{-\infty}^{+\infty} g_{GA}(E) dE \right], \quad (4.8)$$

$$p_T = \sum_{i=0}^{\text{NUMD}} \left[ (1 - f_{TD}(E)) \cdot \int_{-\infty}^{+\infty} g_{TD}(E) dE + (1 - f_{GD}(E)) \cdot \int_{-\infty}^{+\infty} g_{GD}(E) dE \right]. \quad (4.9)$$

### Discrete Trap Distribution



**Figure 4.2:** Discrete trap distribution simulated by Gaussian distributions with WGA and WGD = 0.005 eV, EGA = 0.35 eV, and EGD = 0.40 eV.

In addition to continuous trap distributions (mainly for interface traps), discrete traps are introduced by certain materials within the silicon bandgap, such as gold [29]. In order to investigate discrete traps at the interface, two discrete trap distributions shown in **Figure 4.2** are simulated by the Gaussian distribution with very small WGD and WGA. The discrete distribution could be expressed using the following equation:

$$g(E) = g_A(E) + g_D(E) \quad (4.10)$$

Where  $g_A(E)$  and  $g_D(E)$  could be written as:

$$g_A(E) = N_A \cdot \delta(E - E_A) \text{ [cm}^{-2} \text{ eV}^{-1}] \quad (4.11)$$

$$g_D(E) = N_D \cdot \delta(E - E_D) \text{ [cm}^{-2} \text{ eV}^{-1}] \quad (4.12)$$

The finite widths of  $g_A(E)$  and  $g_D(E)$  are governed by the parameters WGD and WGA, while their positions within the silicon bandgap are determined by EGD and EGA, as illustrated in Figure **Figure 4.2**. However, in the discrete trap model, these energy distributions are not represented with finite widths. Instead, they are idealized as Dirac delta functions, as defined in equations **Equation 4.11** and **Equation 4.12**. This approach assumes that the discrete traps are perfectly localized at specific energy levels, with no energy spread.

#### 4.2.4 Interface Trap Time Constant

The interface trap time constant is a measure of the time needed to exchange charges between the trap and, respectively, the valence or conduction bands. The gate voltage determines which trap energy is addressed by setting the interface Fermi level position at a certain trap position. The energy distance of the trap to the majority carrier band edge,  $\Delta E$ , exponentially determines  $\tau_{it}$ . The interface trap time constant decreases toward accumulation over several orders of magnitude as the Fermi level sweeps traps at different locations in the bandgap. The time constant varies exponentially with temperature and also varies inversely proportional to the capture cross section in the **Equation 4.13**. The time constant corresponds to the frequency  $\left(\frac{1}{2\pi\tau_{it}}\right)$  at which the trap in a certain position in the bandgap dissipates the most energy per cycle.

$$\tau_{it} = \left[ v_{th} \sigma N_{eff} \exp\left(-\frac{q\Delta E}{kT}\right) \right]^{-1} \quad (4.13)$$

where  $v_{th}$  is the thermal velocity of the carriers (electrons or holes), in cm/s;  $\sigma$  is the capture cross-section of the trap (either  $\sigma_n$  or  $\sigma_p$ ), in  $\text{cm}^2$ ;  $N_{eff}$  is the effective density of states (DOS) in the corresponding band (either  $N_C$  for the conduction band or  $N_V$  for the valence band), in  $\text{cm}^{-3}$ ;  $\Delta E$  is the energy difference between the trap level ( $E_t$ ) and the band edge ( $E_c$  or  $E_v$ ). Given the measurement frequencies between 1 kHz and 1 MHz, the  $D_{it}$  closer to the band edges could potentially be probed by measuring the impedance at lower temperatures, as seen in **Figure 4.3**. This will increase the trap response time and shift the response frequency into the experimentally available frequency range. As for interface traps located near the midgap, we can probe them at higher temperatures, as seen in **Figure 4.3**. The determination of the interface trap energy using **Equation 4.13** fixes a constant capture cross section  $\sigma$  that is independent of trap type and position in the band gap, which may not be the

case.

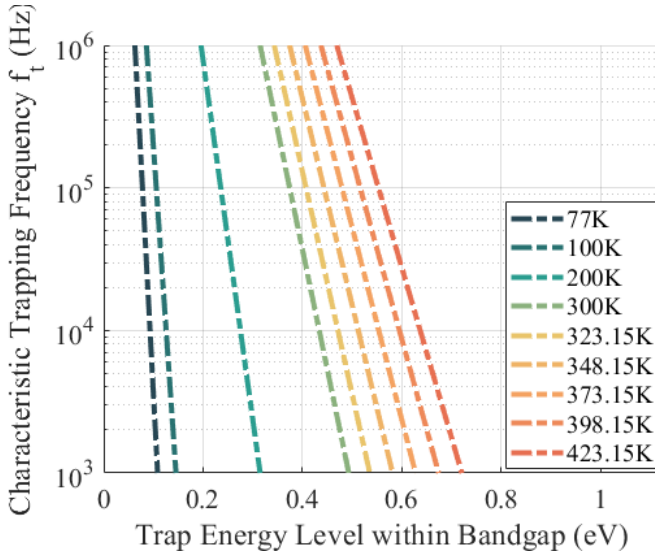
**Table 4.3:** Summary of thermal velocities and density of states at different temperatures.

| Temperature (K) | $v_{t,e}$ (cm/s)   | $v_{t,h}$ (cm/s)   | $N_c$ (cm <sup>3</sup> ) | $N_v$ (cm <sup>3</sup> ) |
|-----------------|--------------------|--------------------|--------------------------|--------------------------|
| 77              | $1.16 \times 10^7$ | $9.47 \times 10^6$ | $3.64 \times 10^{18}$    | $1.35 \times 10^{18}$    |
| 100             | $1.32 \times 10^7$ | $1.08 \times 10^7$ | $5.39 \times 10^{18}$    | $2.00 \times 10^{18}$    |
| 200             | $1.87 \times 10^7$ | $1.53 \times 10^7$ | $1.52 \times 10^{19}$    | $5.66 \times 10^{18}$    |
| 300             | $2.29 \times 10^7$ | $1.87 \times 10^7$ | $2.80 \times 10^{19}$    | $1.04 \times 10^{19}$    |
| 323.15          | $2.38 \times 10^7$ | $1.94 \times 10^7$ | $3.14 \times 10^{19}$    | $1.16 \times 10^{19}$    |
| 348.15          | $2.46 \times 10^7$ | $2.00 \times 10^7$ | $3.51 \times 10^{19}$    | $1.29 \times 10^{19}$    |
| 373.15          | $2.55 \times 10^7$ | $2.07 \times 10^7$ | $3.89 \times 10^{19}$    | $1.43 \times 10^{19}$    |
| 398.15          | $2.63 \times 10^7$ | $2.14 \times 10^7$ | $4.30 \times 10^{19}$    | $1.58 \times 10^{19}$    |
| 423.15          | $2.71 \times 10^7$ | $2.20 \times 10^7$ | $4.72 \times 10^{19}$    | $1.73 \times 10^{19}$    |

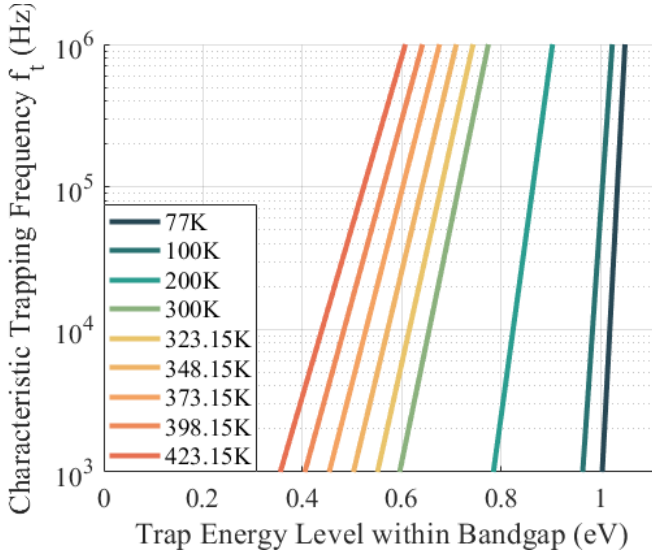
#### 4.2.5 Interface Trap Density ( $D_{it}$ ) Signatures in C-V Curves

##### The Impact of $D_{it}$ on C-V Curves

Here we use TCAD simulation to show that the impact of different level of  $D_{it}$  on C-V curves. Low  $D_{it}$  causes small bumps illustrated by  $D_{it}$  in **Figure 4.4 (a)** and **Figure 4.4 (b)**, while high  $D_{it}$  leads to a noticeable frequency dispersion in **Figure 4.4 (c)**. For small  $D_{it}$ , the interface capacitance distribution to C-V will not be distinguishable. As the frequency increases, the frequency dispersion decreases to zero for higher frequencies since the interface traps do not respond to ac signals. The simulated MOS capacitor consists of a 1  $\mu\text{m}$ -thick aluminium gate contact (work function  $\phi_M = 4.1 \text{ eV}$ ), a 200 nm oxide carrying a fixed charge  $N_{ox} = Q_{ox}/q = +10^{11} \text{ cm}^{-2}$ , and a 700  $\mu\text{m}$  silicon substrate doped at  $N_A = 4.5 \times 10^{14} \text{ cm}^{-3}$  (nominal resistivity  $\rho_{nom} = 30 \Omega\text{cm}$ ). The interface traps are described by Gaussian acceptor and donor distributions,  $g_{GA}(E)$  and  $g_{GD}(E)$ , both with a characteristic decay energy of  $W_{GA} = W_{GD} = 1000 \text{ eV}$ , indicating a continuous distribution; the acceptor density is  $N_{GA} = 1 \times 10^{10}, 1 \times 10^{11}, 1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  with their peak located 0.55 eV from the conduction



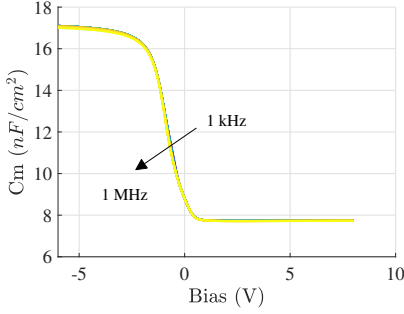
(a) Characteristic trapping frequency for holes (valence band,  $N_v$ ).



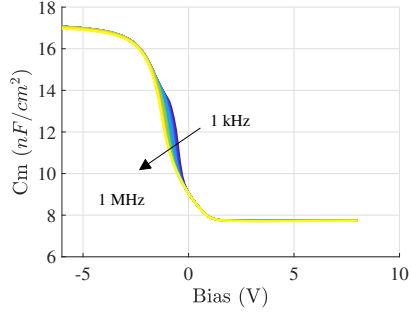
(b) Characteristic trapping frequency for electrons (conduction band,  $N_c$ ).

**Figure 4.3:** Characteristic trap frequency  $f$  calculated from Equation 4.13 using a capture cross section  $\sigma = 1 \times 10^{-15} \text{ cm}^{-2}$  and values for average thermal velocity and the effective density of states (DOS) for the conduction and valence bands as given in Table 4.3.

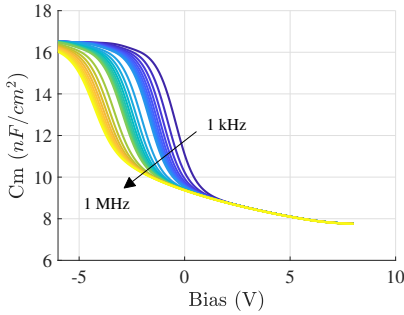
band edge, while the donor density is set to zero ( $N_{GD} = 0$ ), with its nominal peak 0.55 eV from the valence band edge.



(a)  $D_{it} = 1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ .



(b)  $D_{it} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ .



(c)  $D_{it} = 1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ .

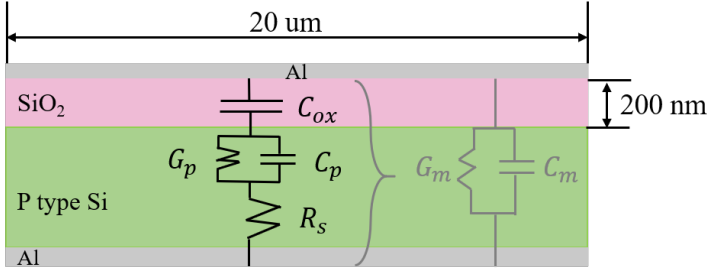
**Figure 4.4:** TCAD simulations of a P-type  $\text{SiO}_2/\text{Si}$  MOS capacitor showing the influence of interface trap density on the C-V characterizations.

In **Appendix Section C**, the influence of interface trap densities of  $1 \times 10^{10}$  and  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  on the conductance method is investigated.

#### 4.2.6 Series Resistance $R_s$

**Figure 4.5** shows a classic equivalent circuit of the MOS capacitor. Here,  $C_{ox}$  is the capacitance of the dielectric stack,  $R_s$  is the series resistance of the Si substrate and the back contact to the Si,  $G_p$  and  $C_p$  are the parallel equivalent conductance and capacitance, respectively, corresponding to the  $\text{SiO}_2/\text{Si}$  inter-

face.  $R_s$  can lead to serious errors in the extraction of interface traps and doping profiles from admittance measurements. So series resistance should be minimized by the fabrication process and corrected from the measured admittance before extracting useful information.



**Figure 4.5:** The equivalent circuit of the MOS capacitor.

Series resistance can come from two sources in our cases: (1) the back contact deposition; (2) the resistance of the bulk silicon between the back contact to the silicon and the depletion layer edge at the silicon surface underneath the gate. The way of minimizing series resistance from the first source is to anneal the samples with the forming gas ( $N_2/H_2$ ) for the formation of ohmic contact. But in the case of high-resistivity substrate Si, it is not possible to neglect the series resistance. Before extracting the desired information, measuring the series resistance and applying a correction to the measured admittance is necessary. In the equivalent circuit of the standard MOS capacitor shown in **Figure 4.6**, when  $R_s$  is properly removed, the capacitance in strong accumulation is solely determined by  $C_{ox}$ . Thus, the corrected C-V in accumulation has no frequency dispersion. The  $R_s$  extraction employs high-frequency measurement (1 MHz) in the accumulation regime of gate bias. In high-frequency measurements, the effect of interface traps on electrical measurements can be eliminated because the charge trapping by interface traps will not be fast enough to respond to the AC signal. The admittance  $Y_{ma}$  in strong accumulation, in terms of the capacitance  $C_{ma}$  and the equivalent parallel conductance  $G_{ma}$ , is given by:

$$Y_{ma} = G_{ma} + j\omega C_{ma}. \quad (4.14)$$

The series resistance is the real part of the impedance  $Z_{ma}$ , which is defined

as:

$$Z_{ma} = \frac{1}{Y_{ma}}. \quad (4.15)$$

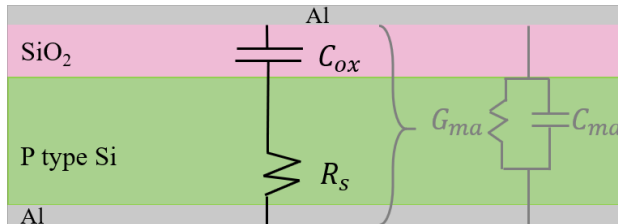
$R_s$  can be determined by either the real part of the impedance  $Z_{ma}$  or the derived from:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} @ 1\text{MHz in the strong accumulation region} \quad (4.16)$$

where  $G_{ma}$  and  $C_{ma}$  are the measured conductance and capacitance in the accumulation region, respectively. To observe the effect conveniently, we take the value of the substrate resistivity around  $30 \Omega \cdot \text{cm}$ . The  $R_s$  caused frequency dispersion in accumulation is seen in **Figure 4.7 (a)**. All the capacitance curves converge to  $C_{ox}$ , as seen in **Figure 4.7 (b)**. To justify the reliability of extracted  $R_s$ , we calculated the semiconductor bulk resistor as below:

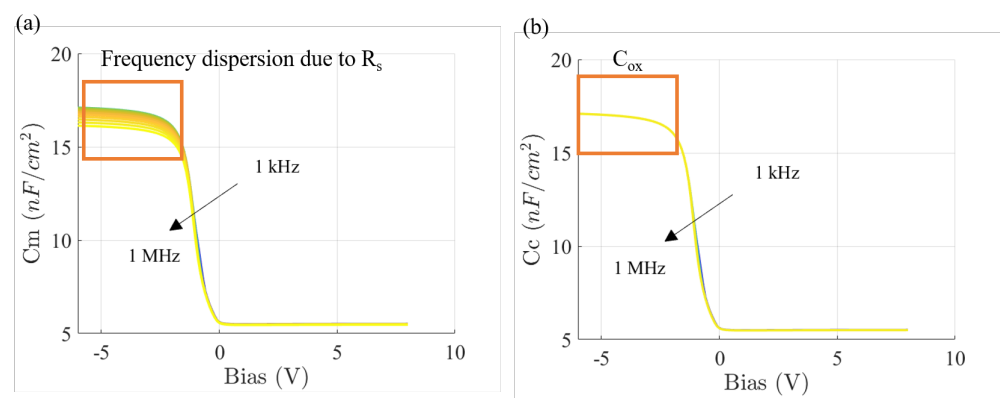
$$R_s = \rho_{bulk} \frac{l}{A} \quad (4.17)$$

where  $\rho_{bulk}$  is the nominal resistivity of the substrate in Silvaco TCAD,  $30 \Omega \cdot \text{cm}$ ,  $l$  is equal to  $t_{sub} = 700 \mu m$ , and  $A$  is the gate electrode area  $2 \times 10^{-7} \text{cm}^2$ . From the calculation,  $R_s$  is around  $1.15 \times 10^7 \Omega$ , which is close to the extracted  $R_s$  seen in **Figure 4.8**.

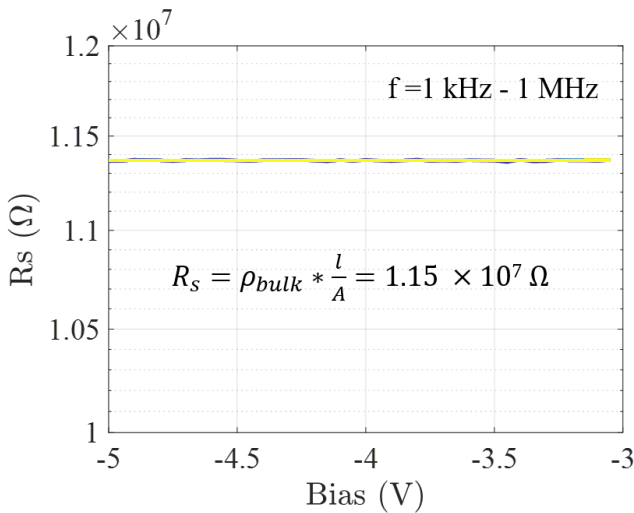


**Figure 4.6:** The equivalent circuit of the MOS capacitor in the strong accumulation.





**Figure 4.7:** (a) simulated original  $C_m$  and (b) simulated corrected capacitance  $C_c$  versus applied bias from 1 kHz to 1 MHz after the withdrawal of  $R_s$ .



**Figure 4.8:** The extracted  $R_s$  of the MOS capacitor in strong accumulation without bias and frequency dependence, compared with calculated bulk resistance.

In **Figure 4.7**, the value of  $C_{ox}$  can be calculated as below:

$$C_{ox} = \frac{C_{c,acc}}{1 + \left( \frac{G_{c,acc}}{\omega C_{c,acc}} \right)^2} \quad (4.18)$$

where  $C_{c,acc}$  and  $G_{c,acc}$  are, respectively, the corrected capacitance and conductance in the strong accumulation region, 17 nF/cm<sup>2</sup>.  $C_{ox}$  from dimension calculation is 17.2 nF/cm<sup>2</sup>.

### 4.3 The Extraction of Interface Trap Density: Conductance Method

#### 4.3.1 Standard Resistivity Si MOS Capacitor Analysis

To evaluate the reliability of the conductance method on standard resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:

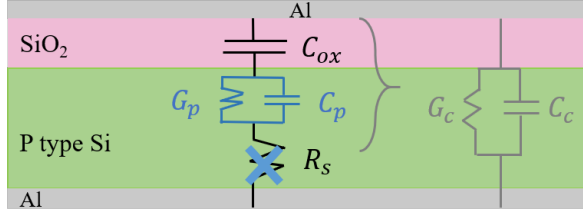
1. Metal thickness of Al contact:  $t_{Al} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{ox} = 200 \text{ nm}$ .
  - (a) With  $N_{ox} = \frac{Q_{ox}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{GA}(E)$  and  $g_{GD}(E)$ .
  - (a) Characteristic decay energies:  $W_{GA} = W_{GD} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{GA} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{GD} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{GA}(E)$ :  $E_{GA} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{GD}(E)$ :  $E_{GD} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{sub} = 700 \mu\text{m}$ .
  - (a)  $N_A = 4.5 \times 10^{14} \text{ cm}^{-3}$ , i.e.,  $\rho_{nom} = 30 \Omega \cdot \text{cm}$ .

Based on this MOS capacitor, the substrate performances are simulated at 25°C.

#### Discussion

The conductance method aims at probing the variation of occupancy of interface trap levels located in the Si bandgap around the Fermi level, following the variation of gate voltage. According to **Section 4.2.2**, the capture and emission of majority carriers by interface traps causes an energy loss mechanism observed at all the frequencies except at the lowest frequencies (no lag behind the AC signal, no energy loss occurs) and at the highest frequencies (no interface trap response occurs). This energy loss is measured as an equivalent parallel

conductance  $G_p$  (in our work) as a function of frequency.  $G_c$  can be extracted from  $G_m$  the schematic as seen in **Figure 4.9** and **Figure 4.10**, and calculated as follows [49]:



**Figure 4.9:** The equivalent circuit after removing  $R_s$  consists of the corrected capacitance  $C_c$ , corrected conductance  $G_c$  in depletion region.

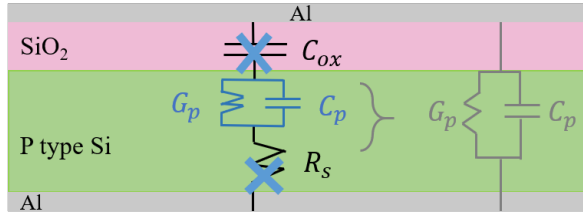
$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} + C_c)^2} \quad (4.19)$$

An approximate expression for the interface trap density in terms of the measured maximum conductance is [49], [50]:

$$D_{it} \approx \frac{2.49}{qA} \cdot \left( \frac{G_p}{\omega} \right)_{\max}^1 \quad (4.20)$$

where  $\omega = 2\pi f$ ,  $q = 1.6 \times 10^{-19} \text{ C}$ , and the mercury probe contact area  $A = 0.0065 \text{ cm}^2$ . **Figure 4.11** represents all the successive steps of the conductance method as applied to a standard-silicon MOS capacitor over a range of frequencies. According to the peaks of  $G_p/\omega$  as a function of  $\omega$  in the depletion region, we can calculate  $D_{it}$  by **Equation 4.20**.

<sup>1</sup>The derivation of the constant value 2.49 can be found in **Appendices Section A**.



**Figure 4.10:** The equivalent circuit after removing  $R_s$  and  $C_{ox}$  consists of the parallel capacitance  $C_p$  and parallel equivalent conductance  $G_p$ .

### Interface Trap Time Constant and Energy Gap Position

The accessible trap energy can be calculated for any temperature and frequency according to Shockley-Read-Hall statistics of the capture and emission rate [51]:

$$\tau = \frac{1}{\omega} = \frac{\exp\left(\frac{\Delta E}{kT}\right)}{\sigma v_t N_V} \quad (4.21)$$

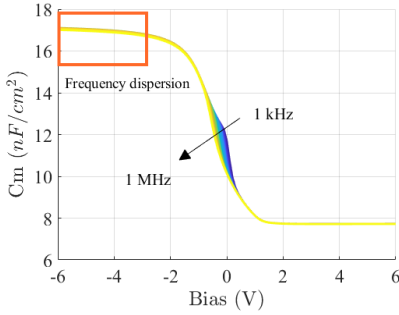
where  $\tau$  is the time constant of the interface trap,  $v_t$  is the average thermal velocity,  $\sigma$  is the capture cross-section,  $N_V$  is the density of states in the valence band,  $k$  is the Boltzmann constant, and  $\Delta E$  ( $\Delta E = E_T - E_V$ ) is the energy difference between the trap energy level ( $E_T$ ) and the top of the Si valence band ( $E_V$ ) in p-type Si.  $\Delta E$  can be calculated using Equation 4.21 from the angular frequency  $\omega$  corresponding to the peak of the  $G_p/\omega$  vs.  $\omega$  curve.

Table 4.4 summarizes the thermal velocity and density of states at different temperatures. The thermal velocity,  $v_t$ , is given by:

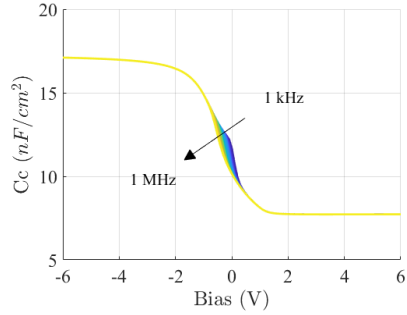
$$v_t = \sqrt{\frac{3kT}{m^*}}, \quad (4.22)$$

where  $m^*$  ( $0.36 m_0$ ) is the transport effective mass for holes. The density of states,  $N_V$ , is given by:

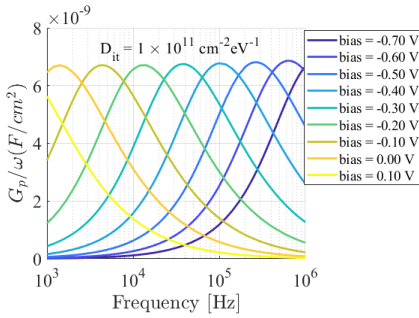
$$N_V = 2 \left( \frac{2\pi m_v^* kT}{h^2} \right)^{3/2}, \quad (4.23)$$



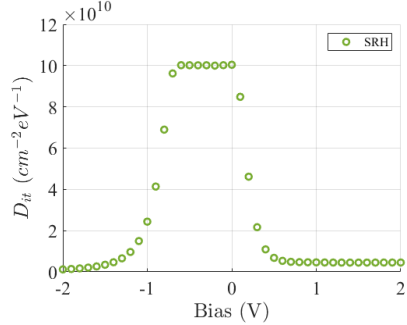
(a) Simulated original capacitance  $C_m$  with frequency dispersion in accumulation.



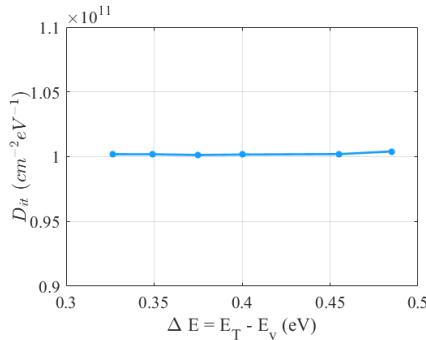
(b) Corrected capacitance  $C_c$  after  $R_s$  withdrawal, showing the disappearance of frequency dispersion in accumulation.



(c) Equivalent parallel  $G_p/\omega$  as a function of frequency with bias voltage variations.



(d) Interface trap density  $D_{it}$  as a function of bias voltage.



(e) The distribution of  $D_{it}$  in the energy band of the Si.

**Figure 4.11:** Illustrations of the conductance method applied to MOS capacitor based on standard Si (resistivity around  $30 \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.

where  $m_{\text{dv}}^*$  is the density-of-states effective mass in the valence bands in silicon [52]. Table 4.4 presents the average thermal velocity,  $v_t$ , and density of states,  $N_v$ , for the calculation of trap response time  $\tau$  under different temperatures. By combining Equation 4.20 and Equation 4.21, we obtain the  $D_{\text{it}}(\Delta E = E_T - E_V)$  profile for DUT as shown in Figure 4.11 (e). At room temperature, the trap energy states can only be measured in the narrow range of energy bandgap from 0.32 to 0.48 eV above the top of the Si valence band.

**Table 4.4:** Summary of thermal velocity and density of states at different temperatures.

| Temperature (°C) | $v_t$ (cm/s)       | $N_v$ (cm <sup>3</sup> ) |
|------------------|--------------------|--------------------------|
| 25               | $1.95 \times 10^7$ | $3.10 \times 10^{19}$    |
| 50               | $2.02 \times 10^7$ | $3.59 \times 10^{19}$    |
| 75               | $2.10 \times 10^7$ | $4.13 \times 10^{19}$    |
| 100              | $2.17 \times 10^7$ | $4.69 \times 10^{19}$    |
| 125              | $2.24 \times 10^7$ | $5.30 \times 10^{19}$    |
| 150              | $2.31 \times 10^7$ | $6.02 \times 10^{19}$    |

### 4.3.2 Limitations and Sensitivity of Conductance Method

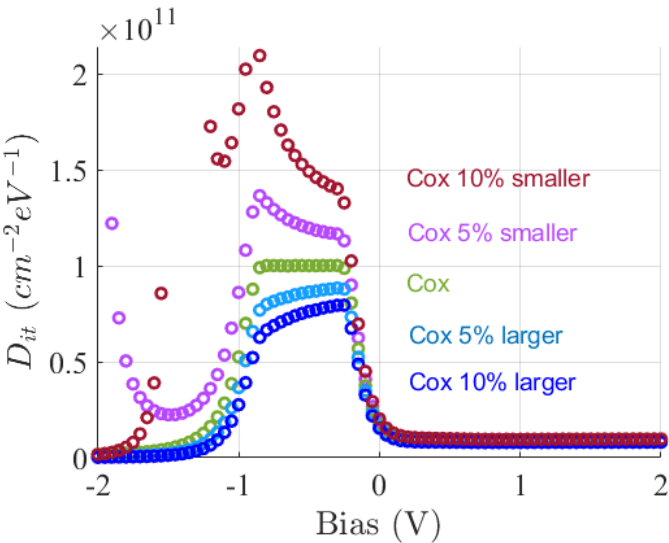
We will take the same TCAD simulation from Section 4.3.1 to analyze the limitations and sensitivity.

#### **C<sub>ox</sub> Errors**

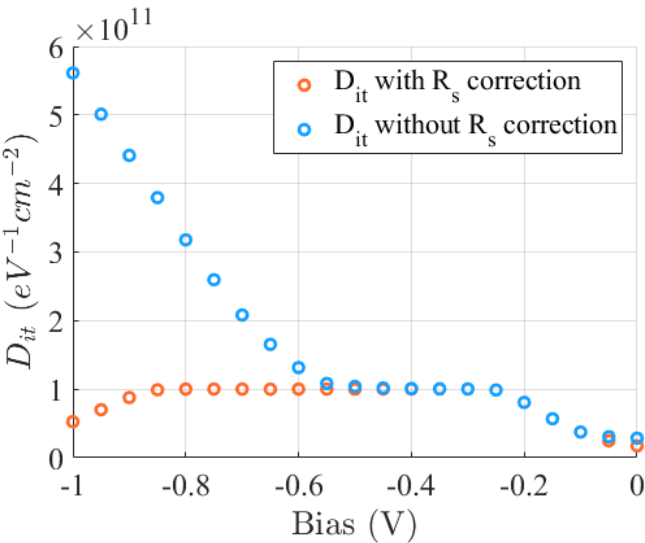
Figure 4.12 shows that the reasonably accurate  $D_{\text{it}}$  is obtained by the conductance method, even with a  $\pm 10\%$  error on  $C_{\text{ox}}$ . Errors in the extracted  $D_{\text{it}}$  increase with  $C_{\text{ox}}$  error, especially if  $C_{\text{ox}}$  is underestimated.

#### **R<sub>s</sub> Correction**

Figure 4.13 shows that if  $R_s$  is not well corrected, the  $D_{\text{it}}$  obtained by the conductance method can be deformed. At the beginning of the depletion regime, the blue  $D_{\text{it}}$  curve reaches values that significantly exceed the imposed trap density, suggesting that the extraction becomes unreliable in this region. This fact indicates the necessity of  $R_s$  correction in the conductance method.



**Figure 4.12:**  $D_{it}$  extracted by the conductance method versus bias with different imposed  $C_{ox}$  errors within  $\pm 10\%$ .



**Figure 4.13:**  $D_{it}$  extracted by the conductance method versus bias with (in orange dots) and without (in blue dots)  $R_s$  correction.

### 4.3.3 High Resistivity Si MOS Capacitor Analysis

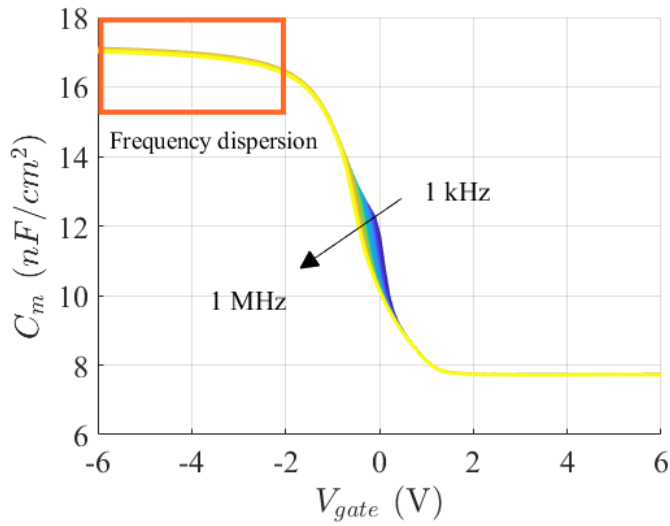
To evaluate the reliability of the conductance method on high resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:

1. Metal thickness of Al contact:  $t_{Al} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{ox} = 200 \text{ nm}$ .
  - (a) With  $N_{ox} = \frac{Q_{ox}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{GA}(E)$  and  $g_{GD}(E)$ .
  - (a) Characteristic decay energies:  $W_{GA} = W_{GD} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{GA} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{GD} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{GA}(E)$ :  $E_{GA} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{GD}(E)$ :  $E_{GD} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{sub} = 700 \mu\text{m}$ .
  - (a)  $N_A = 2.8 \times 10^{12} \text{ cm}^{-3}$ , i.e.,  $\rho_{nom} = 5 \text{ k}\Omega \cdot \text{cm}$ .

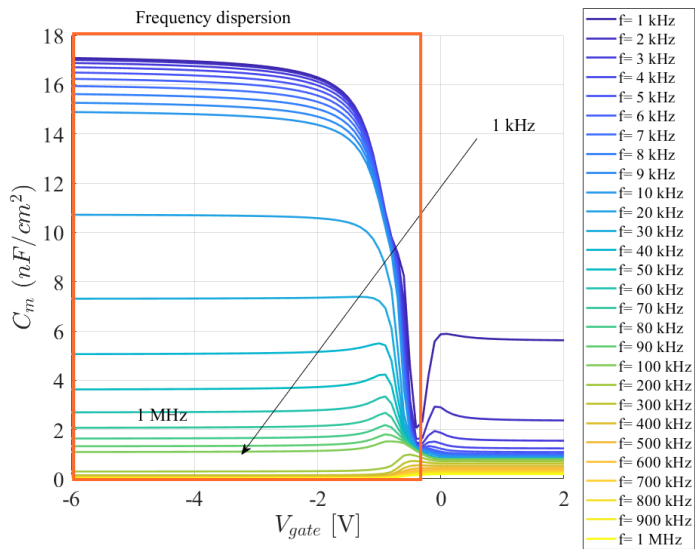
Based on this MOS capacitor, the substrate performance is simulated at  $25^\circ\text{C}$ .



Standard-Resistivity-Si vs High-Resistivity Si MOS Capacitor



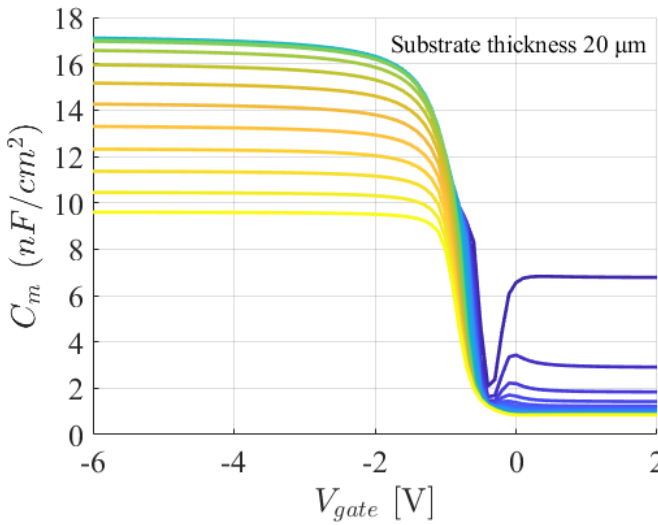
(a) The simulated original C-V characteristics of STD ( $30 \, \Omega \cdot \text{cm}$ ) MOS capacitor.



(b) The simulated original C-V characteristics of HRS ( $5 \text{ k} \, \Omega \cdot \text{cm}$ ) MOS capacitor.

**Figure 4.14:** The TCAD simulations of the C-V characteristics of STD and HRS MOS capacitors with full substrate thickness  $700 \, \mu\text{m}$ .

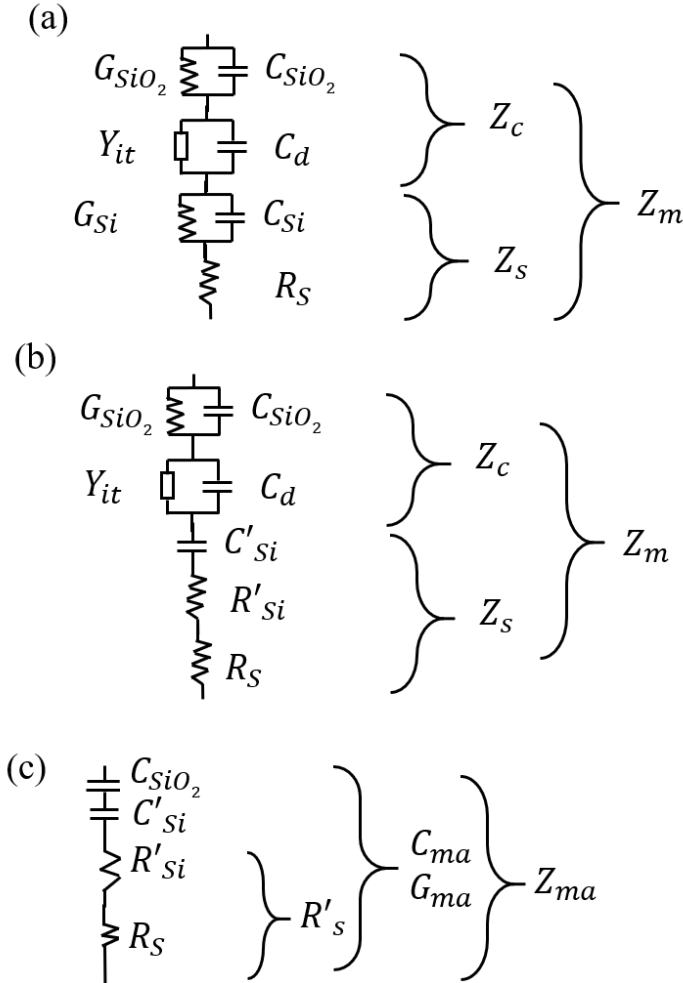
The characteristics of the high-resistivity Si (HRS) MOS capacitor, however, are very different from those of the standard resistivity-Si (STD) MOS capacitor, as shown in **Figure 4.14**. At frequencies above 100 kHz, the C–V characteristics of HRS even appear non-physical: the measured capacitance in accumulation becomes smaller than that in inversion, which is the opposite of what classical MOS theory predicts. In addition, the strong frequency dispersion observed in the accumulation regime of HRS MOS capacitors cannot be corrected using conventional series-resistance ( $R_s$ ) extraction, which is effective for STD MOS capacitors in the previous section **Section 4.2.6**. This behavior highlights the dominant role of the substrate impedance in HRS structures. The C–V characteristics are considerably affected by a potential drop across the HRS substrate. This motivates the need to develop a dedicated de-embedding methodology for accurate admittance analysis.



**Figure 4.15:** High-resistivity Si ( $5\text{k } \Omega \cdot \text{cm}$ ) with a reduced substrate thickness 20  $\mu\text{m}$ , which is larger than the maximum depletion width.

To demonstrate the impact of substrate impedance and validate our de-embedding model, we simulated an HRS MOS capacitor with the substrate thickness reduced to 20  $\mu\text{m}$ , which is slightly wider than the maximum depletion width, thereby effectively excluding the contribution of substrate impedance. As shown in **Figure 4.15**, suppressing the substrate impedance reduces the

frequency dispersion, although a residual dispersion remains. We will discuss the details in **Section 4.3.3**.



**Figure 4.16:** (a) Equivalent circuit of high-resistivity Si substrate. Since the 200 nm  $SiO_2$  layer exhibits low leakage, the conductance  $G_{SiO_2}$  can be neglected. (b) Simplified circuit of (a). (c) Simplified circuit in the strong accumulation region.

### The Procedure of Substrate De-embedding

**Figure 4.16 (a)** presents the equivalent circuit of the HRS MOS capacitor, where  $C_{\text{SiO}_2}$  and  $G_{\text{SiO}_2}$  denote the capacitance and conductance of the  $\text{SiO}_2$  layer, respectively;  $C_d$  represents the depletion capacitance; and  $Y_{\text{it}}$  is the admittance due to interface traps at the  $\text{SiO}_2/\text{Si}$  interface, consisting of equivalent parallel conductance  $G_p$  and capacitance  $C_p$ . The high-resistivity Si substrate is modeled by a parallel RC network ( $C_{\text{Si}}$  and  $G_{\text{Si}}$ ), which is equivalently transformed into a series configuration comprising  $C'_{\text{Si}}$  and  $R'_{\text{Si}}$ , as illustrated in **Figure 4.16 (b)**.

In the strong accumulation regime, the equivalent circuit is illustrated in **Figure 4.16 (c)**, where the measured capacitance ( $C_{\text{ma}}$ ) and conductance ( $G_{\text{ma}}$ ) reflect the behavior of the device. Since the oxide capacitance ( $C_{\text{SiO}_2}$ ) is known from the capacitor geometry, and both depletion capacitance ( $C_d$ ) and interface trap admittance ( $Y_{\text{it}}$ ) are negligible in this regime, we derive the following relations:

$$Z_{\text{ma}} = \frac{1}{G_{\text{ma}} + j\omega C_{\text{ma}}} = R'_s + \frac{1}{j\omega C_{\text{SiO}_2}} + \frac{1}{j\omega C'_{\text{Si}}} \quad (4.24)$$

Comparing the real and imaginary parts of equation **Equation 4.24**, we can extract the series resistance:

$$R'_s = R_s + R'_{\text{Si}} = \frac{G_{\text{ma}}}{G_{\text{ma}}^2 + \omega^2 C_{\text{ma}}^2} \quad (4.25)$$

Additionally, as  $C_{\text{SiO}_2}$  is known from the geometry of the structure, we have:

$$C'_{\text{Si}} = -C_{\text{SiO}_2} \cdot \frac{G_{\text{ma}}^2 + \omega^2 C_{\text{ma}}^2}{\omega^2 (C_{\text{ma}}^2 - C_{\text{ma}} C_{\text{SiO}_2}) + G_{\text{ma}}^2} \quad (4.26)$$

Using **Equation 4.25** and **Equation 4.26**, we extract  $R'_s$  and  $C'_{\text{Si}}$  directly from the measured  $C_{\text{ma}}$  and  $G_{\text{ma}}$  in strong accumulation. As a result, the impedance  $Z_s$  in **Figure 4.16 (a)** can be estimated from measurements in strong accumulation. This allows for a correction to be applied to the measured impedance  $Z_m$ , yielding the corrected impedance  $Z_c$ :

$$Z_c = \frac{1}{G_c + j\omega C_c} = Z_m - Z_s \quad (4.27)$$

$$C_c = \frac{(\omega^2 C_m C'_{Si} - G_m^2 - \omega^2 C_m^2)(G_m^2 + \omega^2 C_m^2) C'_{Si}}{(\omega^2 C'_{Si})^2 [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C'_{Si})^2} \quad (4.28)$$

$$G_c = \frac{[G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2] (G_m^2 + \omega^2 C_m^2)(\omega^2 C'_{Si})^2}{(\omega^2 C'_{Si})^2 [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C'_{Si})^2} \quad (4.29)$$

### Discussion

Assuming a p-type substrate with a resistivity of  $\rho = 5 \text{ k}\Omega \cdot \text{cm}$  and a hole mobility of  $\mu_p \approx 450 \text{ cm}^2/(\text{V} \cdot \text{s})$ , the net doping concentration can be estimated as

$$N \approx \frac{1}{q\mu_p\rho} \approx 2.8 \times 10^{12} \text{ cm}^{-3}. \quad (4.30)$$

Using  $\epsilon_s \approx 11.7, \epsilon_0$  and  $T = 300 \text{ K}$ , the corresponding extrinsic Debye length is

$$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 N}} \approx 2.5 \text{ }\mu\text{m}. \quad (4.31)$$

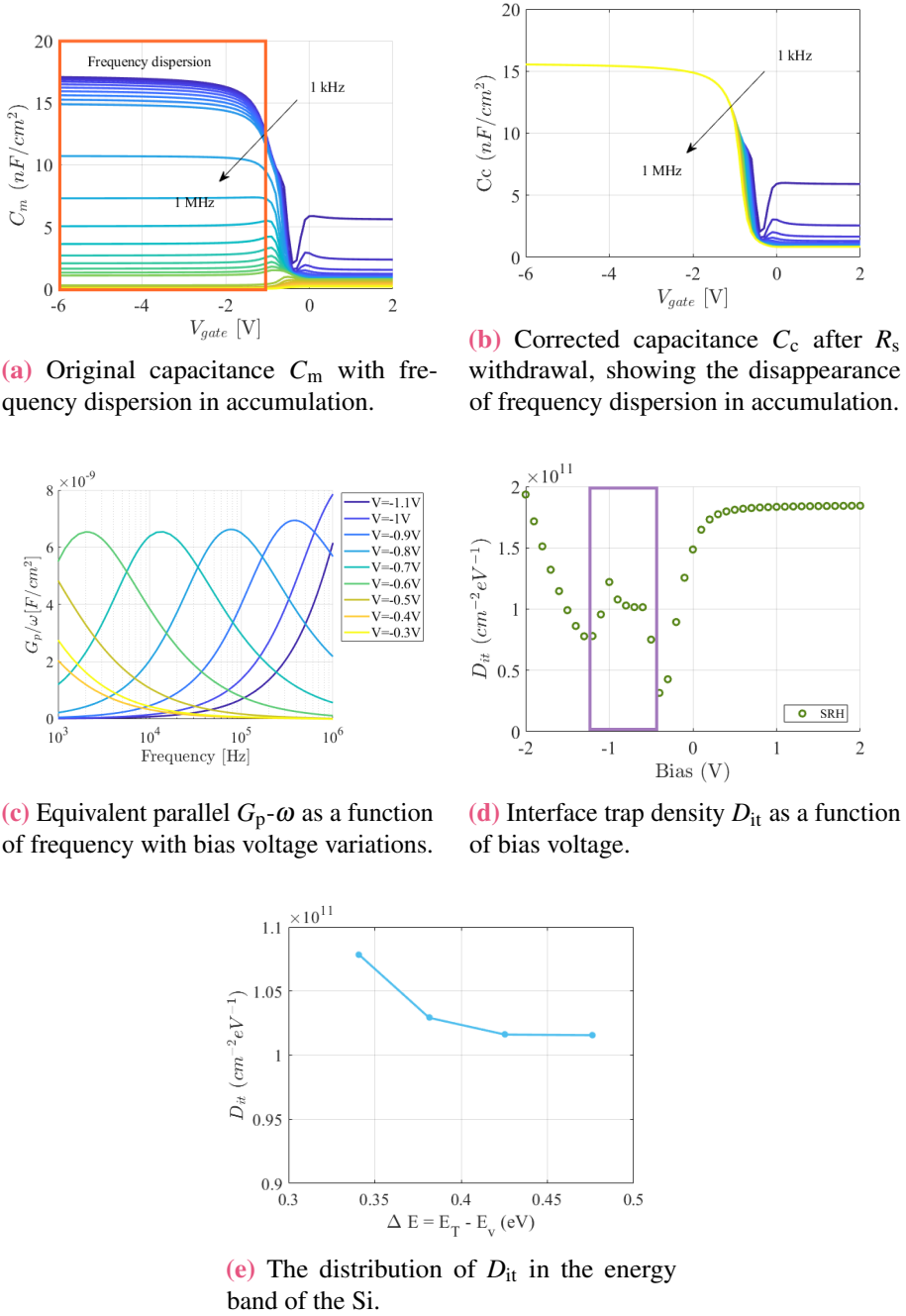
For an intrinsic carrier concentration of  $n_i \approx 10^{10} \text{ cm}^{-3}$ , the Fermi potential is given by

$$\phi_F = \frac{kT}{q} \ln \left( \frac{N}{n_i} \right) \approx 0.15 \text{ V}. \quad (4.32)$$

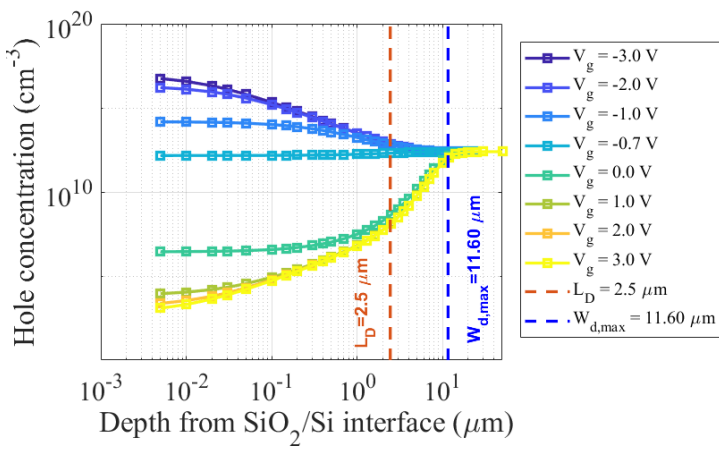
The corresponding maximum depletion width at  $\psi_s = 2\phi_F$  is

$$W_{\max} \approx \sqrt{\frac{4\epsilon_s \phi_F}{qN}} \approx 12 \text{ }\mu\text{m}, \quad (4.33)$$

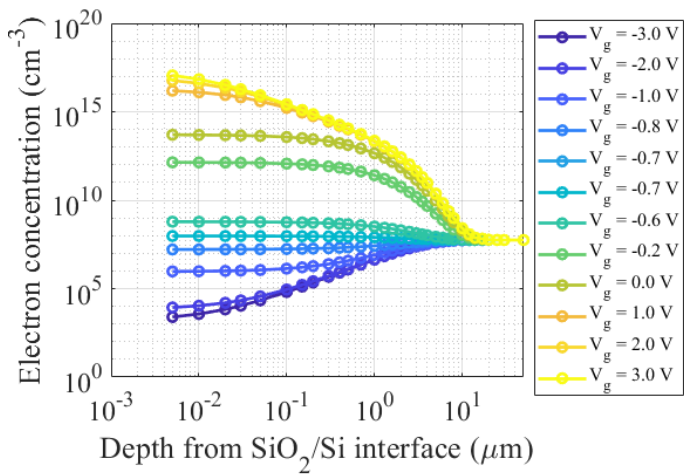
Physically, the Debye length  $L_D$  represents the characteristic distance over which the surface potential decays to  $1/e$  of its surface value. A large  $L_D$



**Figure 4.17:** Illustrations of the conductance method applied to MOS capacitor based on HR Si (resistivity around  $5\text{ k } \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.

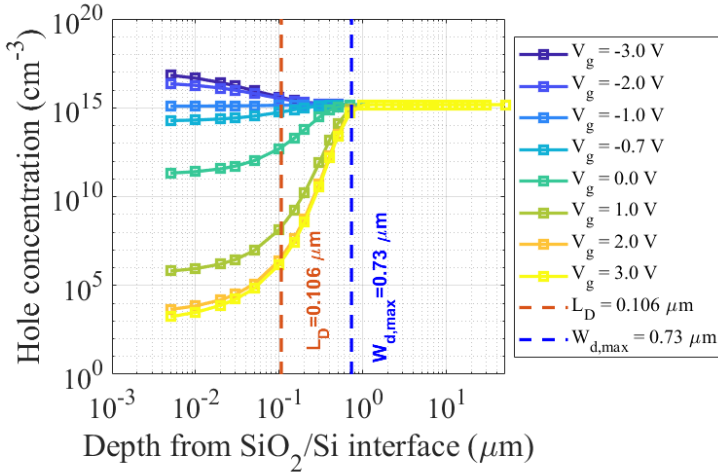


(a) Hole concentration as a function of depth from the SiO<sub>2</sub>/Si interface at several gate biases, showing the spread-out accumulation layer near the surface.

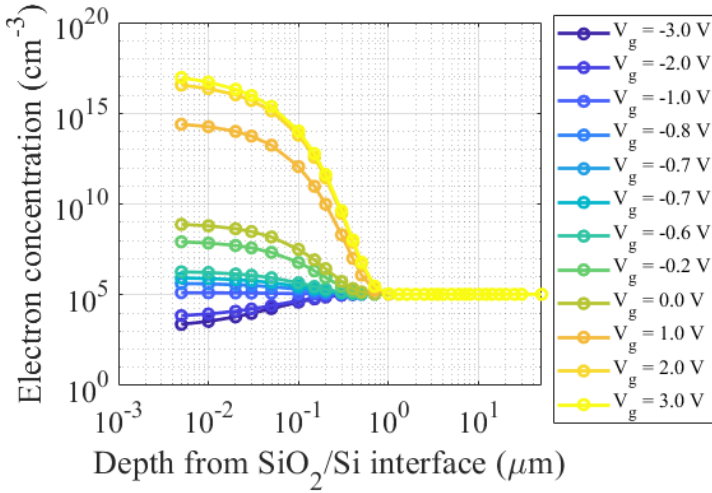


(b) Electron concentration as a function of depth at several gate biases, showing inversion-layer formation at the surface under positive bias.

**Figure 4.18:** Simulated carrier distributions in the HRS MOS capacitor. All depth curves converge to the bulk doping level around 12 μm in (a) and (b).



(a) Hole concentration as a function of depth from the SiO<sub>2</sub>/Si interface at several gate biases, showing a highly concentrated layer at the interface.



(b) Electron concentration as a function of depth at several gate biases, showing inversion-layer formation at the surface under positive bias.

**Figure 4.19:** Simulated carrier distributions in the STD MOS capacitor. All depth curves converge to the bulk doping level around 0.73 μm in (a) and (b).



therefore implies weak screening and a deep penetration of the electric field into the substrate, resulting in a wide depletion region.

To isolate the effect of substrate impedance on the C–V characteristics, **Figure 4.15** presents simulations of an HRS MOS capacitor with a reduced substrate thickness of 20  $\mu\text{m}$ . From **Equation 4.33**, the maximum depletion width is approximately 12  $\mu\text{m}$  seen in **Figure 4.18 (a)**, confirming that the reduced substrate thickness is still sufficient to fully accommodate the depletion region. Under these conditions, C–V curves measured above 100 kHz are no longer influenced by substrate impedance effects.

Nevertheless, as shown in **Figure 4.15**, the high-frequency C–V curves do not fully recover the oxide capacitance  $C_{\text{ox}}$ . Compared to **Figure 4.14 (b)**, the capacitance increases at high frequency but remains below  $C_{\text{ox}}$ . This behavior can be explained by the spatial distribution of the surface potential [53]:

$$\phi = \phi_s e^{-\frac{x}{L_D}}. \quad (4.34)$$

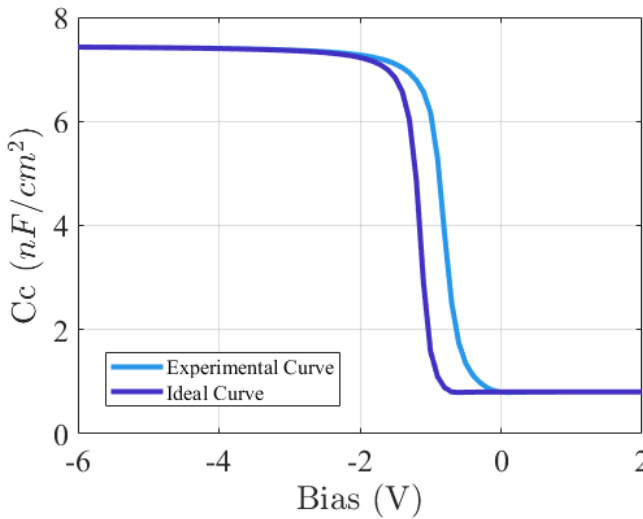
For HRS,  $L_D = 2.5 \mu\text{m}$ , which is comparably large to  $t_{\text{ox}}$  and indicates that the holes in silicon is spaced away from the Si/SiO<sub>2</sub> interface, seen in **Figure 4.18 (a)**, rather than being a sharp and highly concentrated layer at the interface in STD MOS capacitor seen in **Figure 4.19 (a)** ( $L_D = 0.106 \mu\text{m}$ ,  $W_{\text{max}} = 0.73 \mu\text{m}$ ). This charge distribution reduces the effective capacitance at high frequency and should therefore be taken into account in the equivalent circuit model. Applying the new de-embedding model in **Figure 4.16** on C–V curves seen in **Figure 4.14 (b)**, the corrected C–V curves reach to calculated  $C_{\text{ox}}$  by dielectric constant and thickness without frequency dispersion in the accumulation, as shown in **Figure 4.17 (b)**. **Figure 4.17** shows the full procedure of the conductance method on the HRS MOS capacitor. The  $D_{\text{it}}$  extracted by the conductance method in **Figure 4.17 (e)** is  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , in agreement with the value defined in TCAD simulation and thereby confirming the validity of the new de-embedding model.

## 4.4 The Extraction of Interface Trap Density: Terman Method

The room-temperature, high-frequency capacitance method developed by Terman was one of the first methods for determining the interface trap density [54]. The method relies on a high-frequency C–V measurement at a frequency sufficiently high that interface traps are assumed not to respond. They should therefore not contribute any capacitance. Although interface traps do not respond to the ac probe frequency, they do respond to the slowly varying dc gate

voltage. This causes the high-frequency C–V curve to stretch out along the gate voltage axis as the interface trap occupancy changes with gate bias.

**Figure 4.20** illustrates the  $D_{it}$  extraction using Terman method, which is based on the stretch-out phenomenon in the experimental high-frequency C–V curve compared to the theoretically simulated high-frequency C–V curve (i.e. ideal) with no interface traps  $D_{it}$ . The experimental curves are reproduced by TCAD simulations that include the  $D_{it}$  and fixed charge. The stretch-out produces a non-parallel shift of the C–V curve.



**Figure 4.20:** Terman method: the ideal and measured corrected capacitance curves comparison (TCAD simulated without and with  $D_{it}$ , respectively).

#### 4.4.1 Constructing the $\phi_s$ vs. $V_G$ Curve

Knowing surface potential ( $\phi_s$ ) for a given  $C_{HF}$  in a device without  $Q_{it}$  allows us to construct a  $\phi_s$  versus  $V_G$  curve for the actual capacitor:

1. From the ideal MOS-C C–V curve, find  $\phi_s$  for a given  $C_{HF}$ .
2. Find  $V_G$  on the measured curve for the same  $C_{HF}$ , giving one point of the  $\phi_s$  versus  $V_G$  curve.
3. Repeat for other points until a satisfactory  $\phi_s$ – $V_G$  curve is constructed, as shown in **Figure 4.21 (c)**.  $\phi_s$  reaches almost saturated values (in the depletion region: from  $-2$  to  $1$  V).

The experimental  $\phi_s$  versus  $V_G$  curve is a stretched-out version of the theoretical curve, and the interface trap density is determined from this curve using:

$$D_{it} = \frac{C_{ox}}{q^2} \frac{d\Delta V_G}{d\phi_s} \quad (4.35)$$

where  $\Delta V_G = V_G(\text{measured}) - V_G(\text{ideal})$  is the voltage shift of the measured curve from the ideal curve.

#### 4.4.2 Standard Resistivity Si MOS Capacitor Analysis

To evaluate the reliability of the Terman method on standard resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:

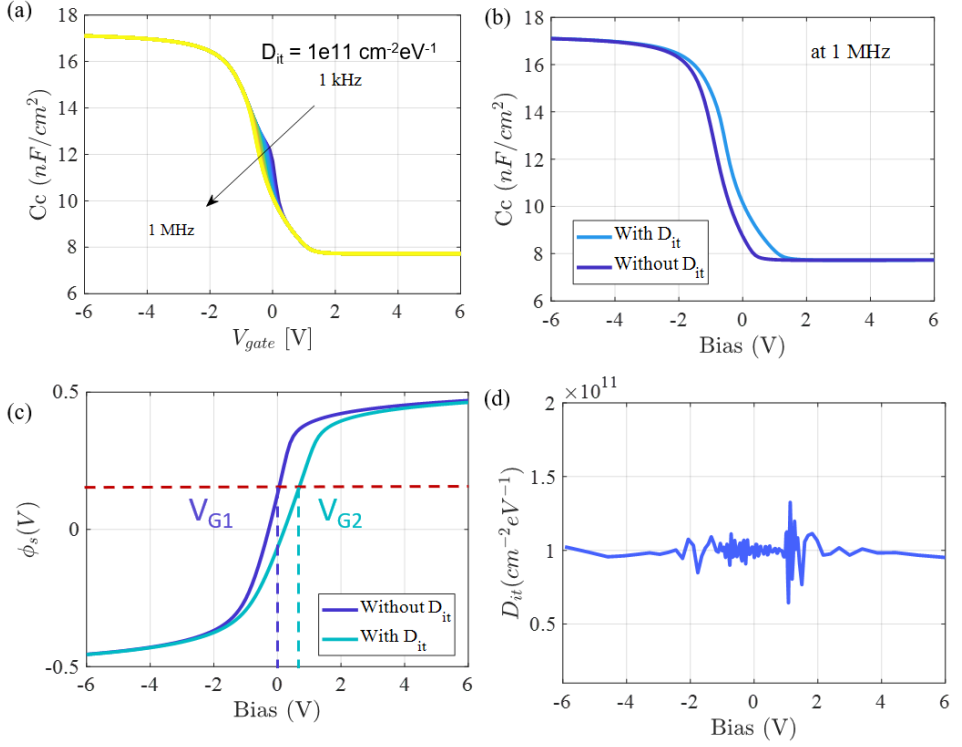
1. Metal thickness of Al contact:  $t_{Al} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{ox} = 200 \text{ nm}$ .
  - (a) With  $N_{ox} = \frac{Q_{ox}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{GA}(E)$  and  $g_{GD}(E)$ .
  - (a) Characteristic decay energies:  $W_{GA} = W_{GD} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{GA} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{GD} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{GA}(E)$ :  $E_{GA} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{GD}(E)$ :  $E_{GD} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{sub} = 700 \mu\text{m}$ .
  - (a)  $N_A = 4.5 \times 10^{14} \text{ cm}^{-3}$ , i.e.,  $\rho_{nom} = 30 \Omega \cdot \text{cm}$ .

Based on this MOS capacitor, the substrate performance is simulated at  $25^\circ\text{C}$ .

By applying the Terman surface-potential construction ([Section 4.4.1](#)) to the C–V curves obtained from TCAD simulations, the extracted interface trap density  $D_{it}$  is found to be approximately  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , in excellent agreement with the value imposed in the TCAD model, as shown in [Figure 4.21](#).

#### 4.4.3 High Resistivity Si MOS Capacitor Analysis

To evaluate the reliability of the Terman method on high resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:



**Figure 4.21:** (a) The simulated corrected capacitance  $C_c$  versus applied bias from 1 kHz to 1 MHz after the withdrawal of  $R_s$  from STD MOS capacitor. (b) The ideal and experimental corrected capacitance curves for comparison. (c)  $\phi_s$  versus applied bias or band bending. (d) The extracted  $D_{it}$  extracted by Equation 4.35.

1. Metal thickness of Al contact:  $t_{Al} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{ox} = 200 \text{ nm}$ .
  - (a) With  $N_{ox} = \frac{Q_{ox}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{GA}(E)$  and  $g_{GD}(E)$ .
  - (a) Characteristic decay energies:  $W_{GA} = W_{GD} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{GA} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{GD} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{GA}(E)$ :  $E_{GA} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{GD}(E)$ :  $E_{GD} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{sub} = 700 \mu\text{m}$ .
  - (a)  $N_A = 2.8 \times 10^{12} \text{ cm}^{-3}$ , i.e.,  $\rho_{nom} = 5 \text{ k}\Omega \cdot \text{cm}$ .

Based on this MOS capacitor, the substrate performances are simulated at  $25^\circ\text{C}$ .

By applying the Terman surface-potential construction (**Section 4.4.1**) to the C–V curves obtained from TCAD simulations, the extracted interface trap density  $D_{it}$  is found to be approximately  $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , in excellent agreement with the value imposed in the TCAD model, as shown in **Figure 4.22**.

#### 4.4.4 Limitations and Precision of the Terman Method

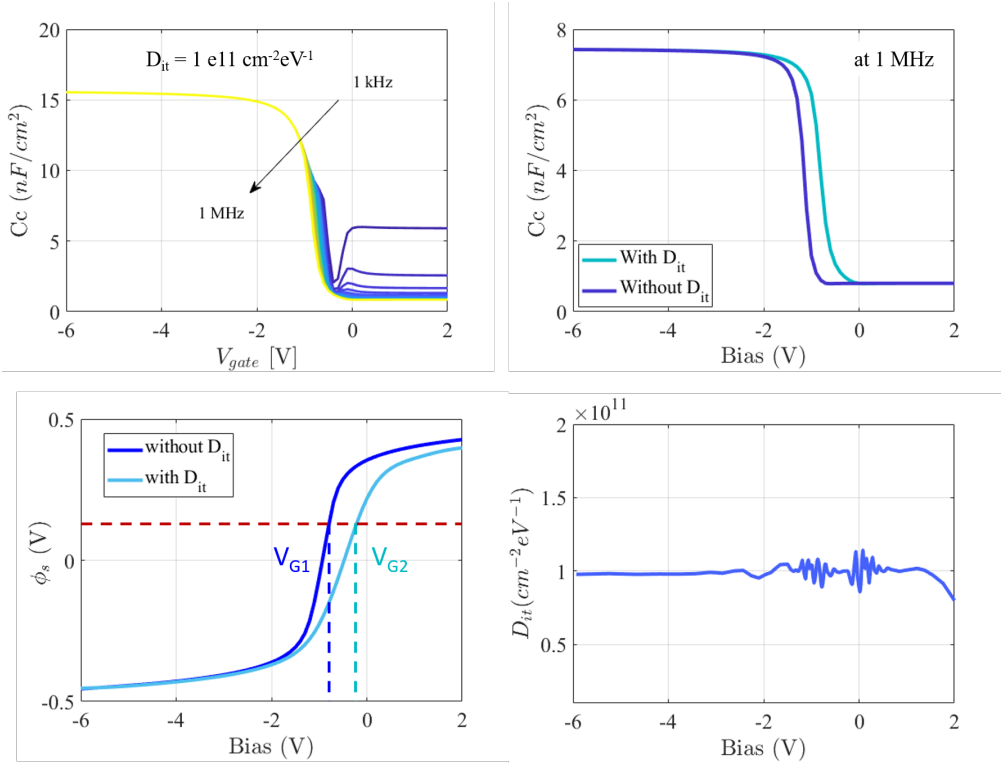
The method is generally considered useful for measuring interface trap densities of  $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  and above. Since the Terman method does not rely on the response, its limitations were originally attributed to inaccurate capacitance measurements and insufficiently high frequencies.

#### Doping Concentration

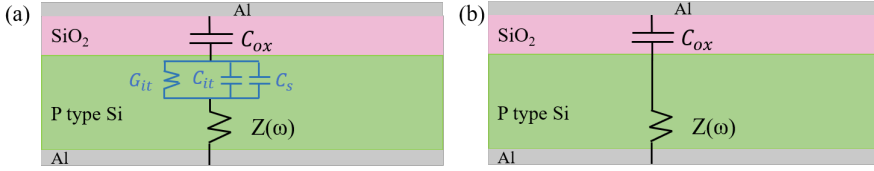
The correct doping concentration is essential for generating ideal C–V curves in TCAD. Using an incorrect value introduces additional stretch-out in the simulated C–V characteristics, which in turn leads to a significant overestimation of the surface potential and consequently to an underestimation of  $D_{it}$ .

### 4.5 The Extraction of Interface Trap Density: High-Low Frequency Capacitance Method

There are two cases to consider: standard and high-resistivity Si substrates, both illustrated using the same schematic in **Figure 4.23**. This figure presents



**Figure 4.22:** (a) The simulated corrected capacitance  $C_c$  versus applied bias from 1 kHz to 1 MHz after the withdrawal of  $R_s$  from HRS MOS capacitor. (b) The ideal and experimental corrected capacitance curves for comparison. (c)  $\phi_s$  versus applied bias or band bending. (d) The extracted  $D_{it}$  extracted by Equation 4.35.



**Figure 4.23:** The equivalent circuits for the MOS capacitor in (a) weak accumulation to depletion and (b) strong accumulation, where  $C_{ox}$ ,  $C_s$ ,  $C_{it}$ ,  $G_{it}$ , and  $Z$  are the oxide capacitance, the semiconductor capacitance, the interface-state capacitance, the interface-state conductance, and series parasitic impedance, respectively.

the equivalent circuits of the MOS capacitor in (a) weak accumulation to depletion and (b) strong accumulation, where  $C_{ox}$ ,  $C_s$ ,  $C_{it}$ ,  $G_{it}$ , and  $Z$  denote the oxide capacitance, semiconductor capacitance, interface-state capacitance, interface-state conductance, and the series parasitic impedance (including  $C_s$ ), respectively. In strong accumulation, as shown in (b),  $C_s$ ,  $C_{it}$ , and  $G_{it}$  can be neglected. The series parasitic impedance is treated using the same de-embedding approach applied to both standard and high-resistivity MOS capacitors in the Conductance method section **Section 4.3**.

The procedure of extracting the interface trap density is as below for both cases:

$$C_{it} = \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \quad (4.36)$$

where  $C_{it}$  is the interface trap capacitance,  $C_{LF}$  is the capacitance at low frequency, and  $C_{HF}$  is the capacitance at high frequency. In the high-low frequency capacitance method, capacitance is measured as a function of gate bias with frequency fixed at a high enough value so that interface traps do not respond. At low frequency, all traps should contribute to capacitance.

$$Q_{it} = D_{it} \cdot q^2 \quad (4.37)$$

where  $q$  is the electronic charge. So,  $Q_{it}$  can be expressed from equation (2) as:

$$D_{it} = \left[ \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right] \frac{q^2}{A} \quad (4.38)$$

where  $\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} = C_s + C_{it}$ ,  $\left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} = C_s$  when  $C_{it} = 0$  the interface traps cannot respond to high frequency. Here,  $C_s$  is the semiconductor capacitance and  $A$  is the area of electrode Al in  $\text{cm}^2$ .

#### 4.5.1 Standard Resistivity Si MOS Capacitor Analysis

To evaluate the reliability of the high-low frequency method on standard resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:

1. Metal thickness of Al contact:  $t_{Al} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{ox} = 200 \text{ nm}$ .
  - (a) With  $N_{ox} = \frac{Q_{ox}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{GA}(E)$  and  $g_{GD}(E)$ .
  - (a) Characteristic decay energies:  $W_{GA} = W_{GD} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{GA} = 4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{GD} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{GA}(E)$ :  $E_{GA} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{GD}(E)$ :  $E_{GD} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{sub} = 700 \mu\text{m}$ .
  - (a)  $N_A = 4.5 \times 10^{14} \text{ cm}^{-3}$ , i.e.,  $\rho_{nom} = 30 \Omega \cdot \text{cm}$ .

Based on this MOS capacitor, substrate performances are simulated at  $25^\circ\text{C}$ .

#### Discussion

Before applying the high-low frequency capacitance comparison, the simulated C-V curves must first be de-embedded to remove the series parasitic impedance. The resulting  $C_c$ - $V_g$  characteristics, shown in **Figure 4.24 (a)**, include the low-frequency (100 Hz) and high-frequency (1 MHz and 100 MHz) capacitances used for the high-low frequency extraction of  $D_{it}$ . The 100 Hz curve reflects the quasi-static response of the MOS capacitor, including the contribution of interface states, and exhibits the expected big bump in the depletion region (highlighted by the purple dashed square).

**Figure 4.24 (b)** shows the  $D_{it}$  extracted using **Equation 4.38** in the depletion region (highlighted by the purple dashed square). The high-frequency curves progressively suppress the interface-state response. At 1 MHz, the depletion-region capacitance still deviates slightly from the ideal high-frequency behavior, indicating that some fast interface states can still respond at this fre-



quency. In contrast, the 100 MHz curve approaches the ideal high-frequency limit, with a flatter and deeper depletion minimum, confirming that the interface traps no longer respond. As a result, 100 MHz provides an appropriate high-frequency reference for the high–low method, producing a wide and stable plateau in the extracted  $D_{it}$  within the depletion region. The extracted curves form the plateau of the 100 MHz C–V curve around  $D_{it} = 4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , which corresponds to the trap density defined in the simulation. Outside the depletion region,  $D_{it}$  increases sharply with  $V_{\text{gate}}$  for both curves, as expected due to the loss of validity of the method in strong accumulation.

#### 4.5.2 High Resistivity Si MOS Capacitor Analysis

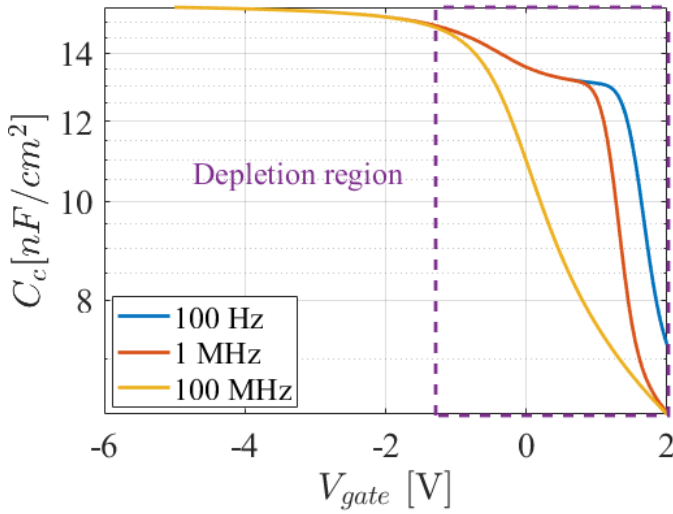
To evaluate the reliability of high-low frequency method on high resistivity MOS capacitors, Atlas Silvaco TCAD simulations were conducted for MOS capacitors with physical parameters as follows:

1. Metal thickness of Al contact:  $t_{\text{Al}} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{\text{ox}} = 200 \text{ nm}$ .
  - (a) With  $N_{\text{ox}} = \frac{Q_{\text{ox}}}{q} = +10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{\text{GA}}(E)$  and  $g_{\text{GD}}(E)$ .
  - (a) Characteristic decay energies:  $W_{\text{GA}} = W_{\text{GD}} = 1000 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{\text{GA}} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ ,  $N_{\text{GD}} = 0 \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{\text{GA}}(E)$ :  $E_{\text{GA}} = 0.55 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{\text{GD}}(E)$ :  $E_{\text{GD}} = 0.55 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{\text{sub}} = 700 \mu\text{m}$ .
  - (a)  $N_{\text{A}} = 2.8 \times 10^{12} \text{ cm}^{-3}$ , i.e.,  $\rho_{\text{nom}} = 5 \text{ k}\Omega \cdot \text{cm}$ .

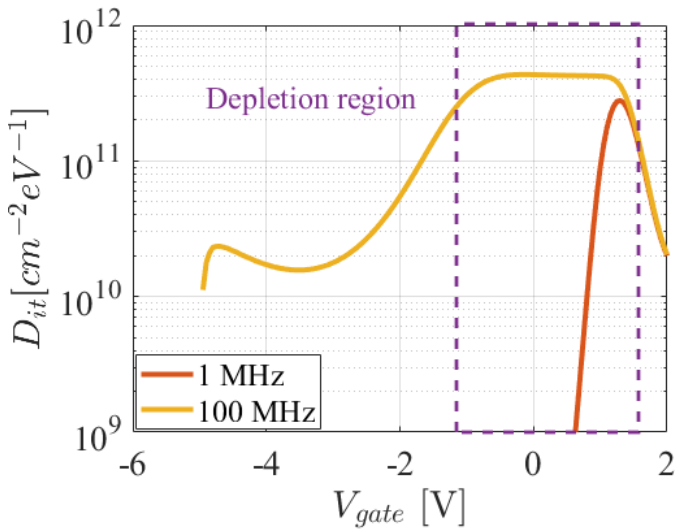
Based on this MOS capacitor, the substrate performances are simulated at  $25^\circ\text{C}$ .

#### Discussion

It is essential to emphasize the choice of a sufficiently low measurement frequency, such that both minority carriers and interface traps can respond effectively. As shown in **Figure 4.25**, the corrected C–V curves measured from 100 to 900 Hz exhibit a clear interface-trap-related plateau in the depletion region around  $-0.65 \text{ V}$ . Among these, the 100 Hz C–V curve presents the widest plateau, indicating that a larger fraction of interface traps is able to respond at this frequency. The main limitation arises from the measurement equipment,



(a) Corrected capacitance  $C_c$  versus bias at various frequencies for STD MOS capacitor at 100 Hz, 1 MHz, and 100 MHz.



(b)  $D_{it}$  extraction in the depletion region from Equation 4.38, compared with C-V curves at 1 MHz and 100 MHz.

**Figure 4.24:** The TCAD simulations of the C-V characteristics of the STD MOS capacitor for the high-low frequency method.

which currently prevents performing reliable measurements below 1 kHz in Welcome. We only show the possibility in the thesis. The simulated C-V curves will be de-embedded for the series parasitic impedance before performing the high-low frequency capacitance comparison, shown in **Figure 4.26 (a)**. At high frequencies (1 MHz and 100 MHz), the series resistance will dominate the loss, and no information on interfacial properties can be extracted from either measured capacitance or equivalent parallel conductance. **Figure 4.26 (b)** shows the  $D_{it}$  extracted using **Equation 4.38** in the depletion region (highlighted by the purple dashed square). The extracted curves form plateaus around  $N_{GA} = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  at the same bias -0.65 V, which corresponds to the trap density defined in the simulation.

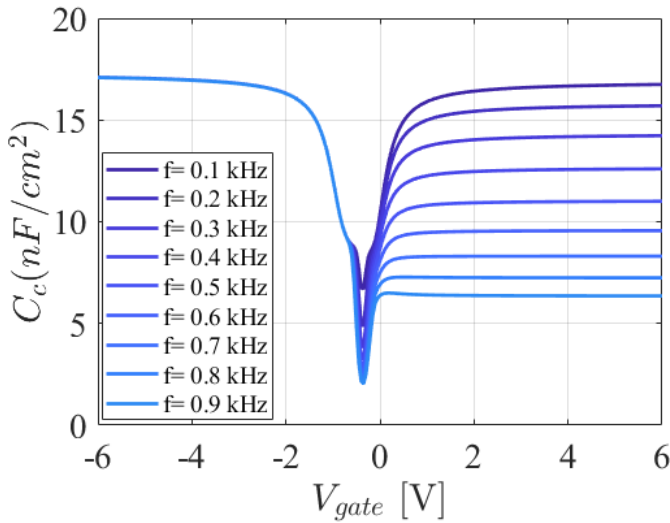
In the depletion region (purple dashed box), both the 1 MHz and 100 MHz curves exhibit a clear and nearly flat plateau around  $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . The two frequencies give very similar values in this bias range, which is a strong indication that the high-low frequency method is operating under its intended conditions: the low-frequency capacitance fully includes the interface-state response, while the high-frequency capacitance is only weakly affected by it. Outside the depletion region,  $D_{it}$  increases sharply with  $V_{gate}$  for both curves, as expected from the loss of validity of the method in strong accumulation or strong inversion. Overall, the comparison shows that high-resistivity Si enables a robust and physically meaningful  $D_{it}$  extraction using the high-low frequency technique.

### 4.5.3 Limitations and Precision of the High-Low Frequency Capacitance Method

#### Frequency Selection

The error might come from the selection of a true high frequency. A measured high-frequency C-V curve is rarely a good approximation to a true high-frequency C-V over its bias range. As the flatband condition is approached, the reduction of band bending increases the majority carrier concentration at the semiconductor interface, which accelerates carrier capture by interface traps and shortens their response time, allowing them to partially follow the AC excitation even at high measurement frequencies. In **Figure 4.23** and **Equation 4.36** shows that

$$C_s + C_{it} = C_{LF} - C_{ox}, \quad (4.39)$$



**Figure 4.25:** The corrected capacitance for HRS MOS capacitor at low frequencies from 100 - 900 Hz. At -0.65 V, the bump exhibits the signature of interface traps.

and

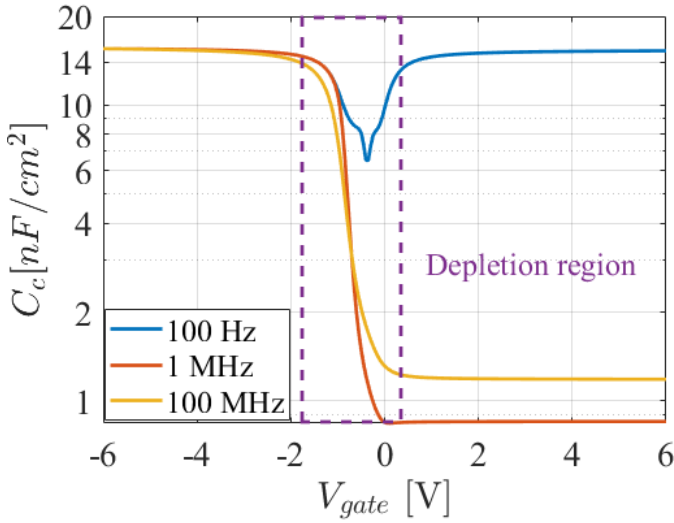
$$C_s = C_{HF} - C_{ox}. \quad (4.40)$$

If the measurement frequency is not sufficiently high, the interface-trap capacitance  $C_{it}$  is not fully suppressed and therefore remains included in the extracted high-frequency capacitance. This will induce the error into the extraction.

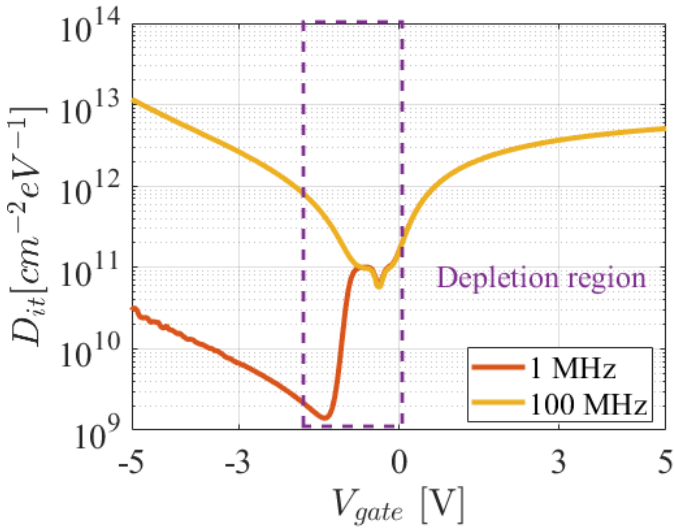
#### 4.5.4 Comparison of Interface Trap Extraction Methods

##### Conductance Method

The conductance method enables a more accurate and sensitive extraction of interface-trap properties from admittance measurements than capacitance methods. An additional advantage of the conductance method is that it provides a well-defined loss peak whose magnitude is directly proportional to the interface-trap density, as described in **Equation 4.20**, allowing a more reliable and energy-resolved extraction of  $D_{it}$  and reducing sensitivity to oxide thickness variations and parasitic capacitances. Besides, the conductance method is particularly sensitive to fast interface traps with short response times, especially



(a) Corrected capacitance  $C_c$  versus bias at various frequencies for HRS MOS capacitor at 100 Hz, 1 MHz, and 100 MHz.



(b)  $D_{it}$  extraction in the depletion region from Equation 4.38, compared with C-V curves at 1 MHz and 100 MHz.

**Figure 4.26:** The TCAD simulations of the C-V characteristics of the HRS MOS capacitor for the High-low frequency method. At -0.65 V, the bump exhibits the signature of interface traps.

those located near midgap. In contrast, capacitance-based methods rely on the subtraction of the semiconductor capacitance  $C_s$  from the measured total capacitance ( $C_s + C_{it}$ ), making them more susceptible to experimental uncertainties. For small interface trap densities, the capacitance-based extraction breaks down because the semiconductor capacitance  $C_s$  contribution dominates the total capacitance and masks the interface trap contribution. The conductance method instead extracts  $D_{it}$  from the peak of  $G_p/\omega$ , which remains distinguishable even at low trap densities since interface traps are the sole contributor to this quantity.

### **Terman Method (High Frequency Capacitance Method)**

The main advantage of the Terman method is its experimental simplicity, as it requires only a single high-frequency C–V measurement, typically performed at 1 MHz, without the need for low-frequency C–V or conductance measurements. The interface-trap density  $D_{it}$  is extracted from the deviation between the measured high-frequency C–V curve and the ideal theoretical C–V response. The resulting stretch-out of the C–V curve directly reflects the presence of interface traps. This method is generally considered to be useful for measuring interface trap densities of  $10^{10} \text{ cm}^{-2}\text{eV}^{-1}$  and above. It is also sensitive to slow traps that contribute to the stretch-out and can be located at the interface or even in the dielectric. Its limitations were originally pointed out to be due to inaccurate capacitance measurements and insufficiently high frequencies.

### **High-Low Frequency Capacitance Method**

The advantage of the high-low frequency capacitance method is that  $C_s$  is determined experimentally from a high frequency C–V measurement for the same gate bias at which ( $C_s + C_{it}$ ) is measured using a low frequency C–V measurement. Therefore, the subtracted  $C_s$  automatically corresponds to the correct band bending. However, it requires larger frequency ranges. A more detailed accounting of errors in this method is given by Nicollian [49].

### **Common Problem: Series Resistance**

Series resistance constitutes a common limitation for both the conductance and capacitance methods. When the interface-trap density  $D_{it}$  is low, losses due to series resistance may dominate the measured equivalent parallel conductance, thereby obscuring the interface-trap contribution. In the high–low frequency capacitance method, series resistance can also cause the C–V curve measured at 1 MHz to deviate from a true high-frequency C–V curve. Consequently, correction for series resistance is required before a reliable extraction of  $D_{it}$  can

be performed.

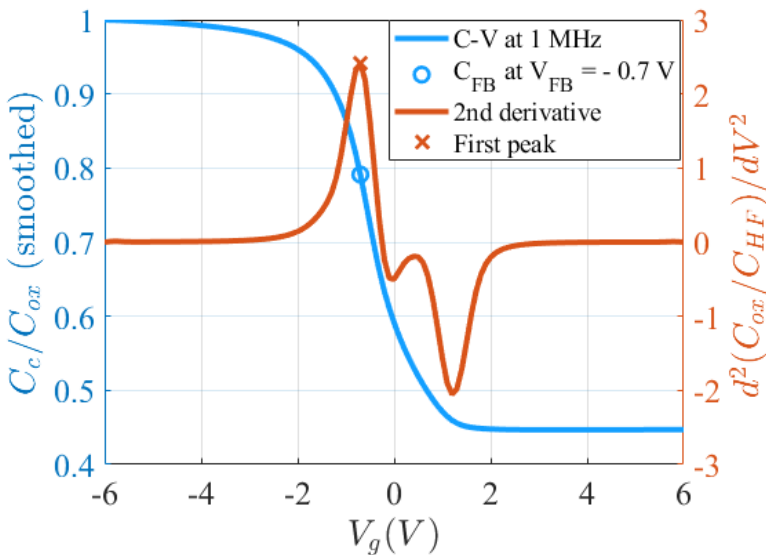
## 4.6 The Extraction of Flatband Voltage and Fixed Charge

### 4.6.1 The Extraction of Flatband Voltage $V_{FB}$

In the following, the simulation of a standard MOS capacitor (STD) is taken from [Section 4.3.1](#) as an example.

#### First Solution: Second Derivative of C-V

One solution can be graphically obtained by finding the maximum of the second derivative of the C-V curve at high frequency 1 MHz, as seen in [Figure 4.27](#). The normalized C-V characteristic (blue curve) and its second derivative with respect to gate voltage (orange curve) are shown. The flatband capacitance  $C_{FB}$  is identified at  $V_{FB} = -0.7$  V on the C-V curve, corresponding to the first peak of the second-derivative curve (marked by the cross).



**Figure 4.27:**  $C_c$  -V measurement at 1 MHz of a  $\text{SiO}_2/\text{Si}$  MOS capacitor (blue color curve). The second derivatives of the capacitance as a function of gate voltage (orange color curve). The first peak of the second derivative is located at  $V_{FB} = -0.7$  V.

$$\frac{d^2}{dV_G^2} \left( \frac{C_{ox}}{C_{HF}} \right)^2 \quad (4.41)$$

The method based on **Equation 4.41** relies on the fact that the C–V curve reaches its maximum curvature at the flatband voltage. However, this curvature can be distorted by the horizontal stretching of the C–V characteristics induced by the existence of  $D_{it}$ . In contrast, horizontal shifts caused by fixed charge ( $Q_f$ ) do not alter the curve shape, and the extracted  $V_{FB}$  shifts accordingly. Therefore, curve fitting provides a more reliable approach for accurately determining the flatband voltage, as demonstrated in the subsequent extraction.

### Second Solution: Curve-fitting Extraction

To verify the second extraction easily, we need an ideal C–V curve without any fixed charge. Thus, we impose a fixed charge  $Q_f$  equal to  $0 \text{ cm}^{-2}$ . A measurement frequency of 1 MHz is required to ensure that the response of  $D_{it}$  is negligible.

To extract the flatband voltage from a measured C–V curve, for a given oxide thickness and dopant concentration, the flatband capacitance is first calculated, as shown below **[50]**:

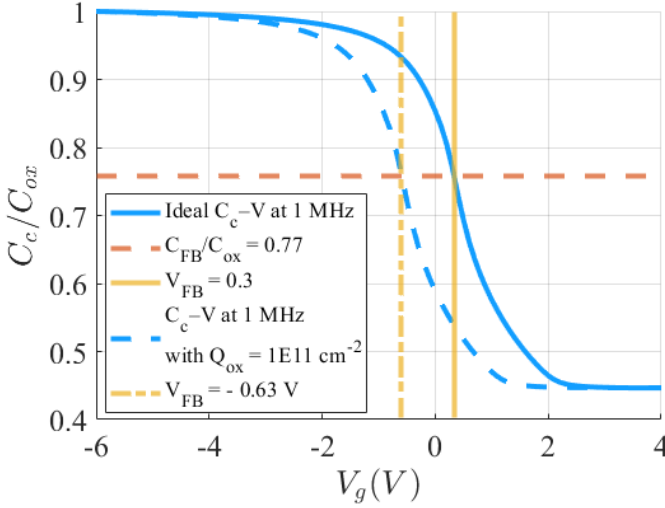
$$\frac{C_{FB}}{C_{ox}} = \left( 1 + \frac{136 \sqrt{T/300}}{t_{ox} \sqrt{N_A \text{ or } N_D}} \right)^{-1} \quad 2 \quad (4.42)$$

In this expression,  $t_{ox}$  is expressed in cm, while the doping concentration  $N_A$  or  $N_D$  is given in  $\text{cm}^{-3}$ . The equivalent gate voltage  $V_{FB}$  corresponding to the calculated  $C_{FB}$  can then be identified from the measured C–V curve, at -0.63 V in **Figure 4.28**. This method is applied to substrates with a uniform doping density and a sufficiently thick semiconductor layer. When many substrate parameters are unknown and prevent reliable simulation, the first solution—the second-derivative C–V method—is recommended.

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<sup>2</sup>Here the calculation of 136 can be found in **Appendices Section B**.





**Figure 4.28:**  $C_c$ - $V$  characteristics of a  $\text{SiO}_2/\text{Si}$  MOS capacitor at 1 MHz for  $Q_{\text{ox}} = 0 \text{ cm}^{-2}$  and  $Q_{\text{ox}} = 1 \times 10^{11} \text{ cm}^{-2}$  (blue solid and dashed curves, respectively).  $C_{\text{FB}}/C_{\text{ox}} = 0.85$  calculated from Equation 4.42 (orange dash line) at  $V_{\text{FB}} = 0 \text{ V}$  (yellow solid line). The equivalent  $V_{\text{FB}}$  for the  $C$ - $V$  curve with  $Q_{\text{ox}} = 1 \times 10^{11} \text{ cm}^{-2}$  is therefore  $-0.63 \text{ V}$  (yellow dash line).

#### 4.6.2 The Extraction of Fixed Charge $Q_f$

After  $V_{\text{FB}}$  has been obtained from two extractions, the density of  $Q_f$  can be calculated as follows:

$$Q_f = \frac{\phi_{\text{MS}} - V_{\text{FB}}}{C_{\text{ox}} \cdot q} \quad (4.43)$$

where  $\phi_{\text{MS}}$  is the work function difference between the metal gate and silicon,  $C_{\text{ox}}$  is the capacitance of  $\text{SiO}_2$ , and  $q$  is the electron charge ( $1.6 \times 10^{-19} \text{ C}$ ). To calculate  $\phi_{\text{MS}}$ , the doping type and density must be specified. For p-type substrates,

$$\phi_{\text{MS}} = \phi_M - \left( \chi + \frac{E_C - E_i}{q} \right) - \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) \quad (4.44)$$

where the electron affinity  $\chi$  of silicon is  $4.15 \text{ eV}$  [50], the bandgap energy is  $E_g = 1.12 \text{ eV}$ , the doping density is  $N_A = 4.5 \times 10^{14} \text{ cm}^{-3}$ , and the intrinsic carrier concentration is  $n_i = 10^{10} \text{ cm}^{-3}$  at  $300 \text{ K}$ .  $C_{\text{ox}} = 17.3 \text{ nF/cm}^{-2}$ ,

$V_{fb} = -0.7$  V and  $-0.63$  V, calculated using the second derivative technique and curve-fitting technique [55] from Figure 4.27 and Figure 4.28, respectively. Therefore, we obtain a positive oxide charge ( $Q_f = 1.04 \times 10^{11} \text{ cm}^{-2}$  from the second derivative method,  $Q_f = 9.66 \times 10^{10} \text{ cm}^{-2}$  from the curve-fitting method), close to the imposed  $Q_f = 1 \times 10^{11} \text{ cm}^{-2}$  in the simulation.

## 4.7 Chapter Summary

This chapter presents the theoretical background and TCAD simulation framework for the electrical characterization of MOS capacitors, with a particular emphasis on interface trap phenomena and their impact on capacitance-voltage (C-V) characteristics. After a brief introduction to MOS capacitor operation, the physical origin of interface traps is discussed, including their energy distribution within the bandgap, associated loss mechanisms, and characteristic time constants. The signatures of interface traps in C-V measurements are analyzed, and the influence of series resistance is addressed, as it impacts the accuracy of the parameter extraction.

The chapter then details the principal techniques used to extract the interface trap density ( $D_{it}$ ). The conductance method is first introduced and applied to standard-resistivity silicon MOS capacitors, followed by an extension to high-resistivity silicon substrates. The sensitivity, assumptions, and limitations of the conductance method are critically assessed, particularly in the context of substrate impedance effects.

Subsequently, the Terman method is presented, including the construction of the surface potential-gate voltage relationship and its application to standard-resistivity and high-resistivity MOS capacitors. The accuracy and limitations of this method are discussed, highlighting the conditions under which reliable  $D_{it}$  extraction can be achieved.

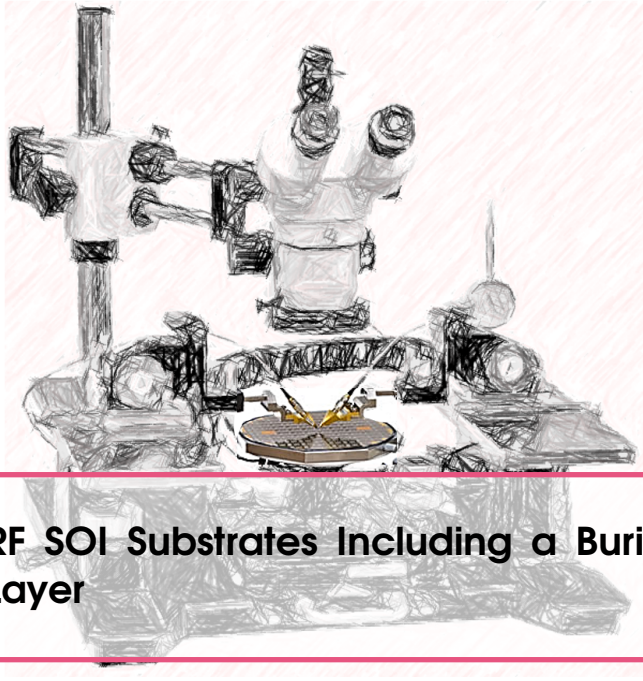
The high-low frequency capacitance method is then introduced as an alternative approach for interface trap characterization. Its application to both standard- and high-resistivity silicon MOS capacitors is examined, and the precision and limitations of the method are evaluated.

A systematic comparison between the conductance, Terman, and high-low frequency methods is provided to clarify their respective applicability and

reliability for different substrate resistivities and measurement conditions.

Finally, the extraction of the flatband voltage and fixed charge is addressed, completing the set of key MOS interface parameters. Overall, this chapter establishes a rigorous theoretical and methodological basis for the experimental analysis and TCAD simulations presented in the subsequent chapters, particularly for high-resistivity and engineered MOS structures.





## 5. RF SOI Substrates Including a Buried SiGe Layer

### 5.1 Introduction

Tensile strain is considered to be an important feature of FDSOI n-channel MOSFETs as it enhances electron mobility and thus device performance. One route to inducing such strain is a buried SiGe layer: it has been demonstrated that the edge relaxation of a buried SiGe layer, facilitated by shallow trench isolation (STI) structures, can transfer tensile strain into the overlying silicon channel [56]. This strain enhances both the saturation drain current ( $I_{\text{dsat}}$ ) and the transconductance ( $g_m$ ), leading to improved transition frequency ( $f_T$ ) and maximum oscillation frequency ( $f_{\text{max}}$ ) for RF transistors [57], [58].

However, this prior work was demonstrated on standard substrates and focused on strain transfer for digital FD-SOI performance. Two aspects relevant to RF applications remain unaddressed: the characterization of the SiGe interface as a passivation scheme on a high-resistivity (HR) silicon substrate, and RF characterization of substrate loss for this passivation approach.

This thesis addresses both gaps. The interface at  $\text{SiO}_2/\text{SiGe}$  is characterized through C-V measurements based on the equivalent circuit model developed in Section 4.3.3, from which the interface-trap distribution is extracted. The density of interface traps is promising to counter against PSC. Then it investigates the RF potential of SOI substrates featuring a buried SiGe layer on an HR silicon wafer, evaluating whether the SiGe interface can simultaneously provide

effective passivation and substrate-loss reduction. It is the first time that SiGe has been assessed as a candidate passivation technique for RF SOI substrates.

Overall, this chapter bridges the gap between strain engineering and substrate passivation in FD-SOI technologies, offering a novel integration pathway that unites performance, linearity, and manufacturability for next-generation RF applications.

## 5.2 Buried SiGe on Standard-Resistivity Si Substrates

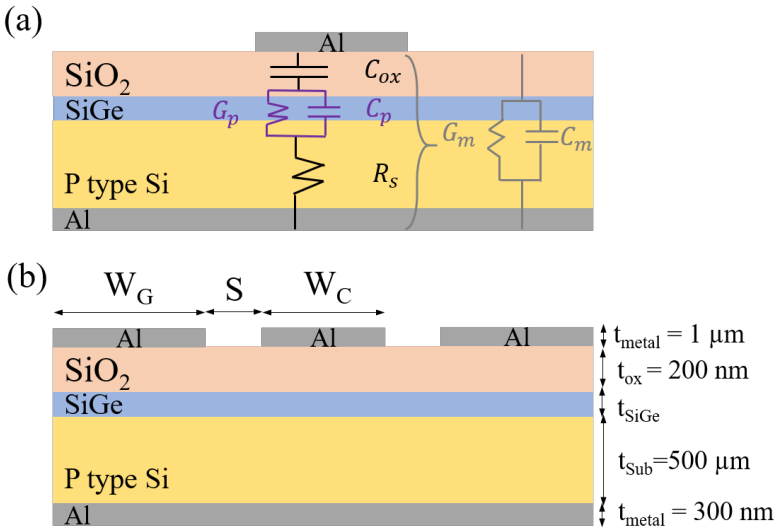
When it comes to radio-frequency (RF) applications, a Silicon-on-Insulator (SOI) substrate requires low propagation losses and harmonic distortion at microwave frequencies, and this necessitates a high effective resistivity. However, fixed charges present at the BOX/semiconductor bottom interface attract free carriers toward the interface, lowering the effective resistivity of the substrate. This is referred to as the parasitic surface conduction (PSC) that undermines the efficiency of employing a High-Resistivity (HR) substrate. One efficient way to reduce free carriers near the Si surface and conserve the high resistivity property of the substrate is to take advantage of a large density of interface traps ( $D_{it}$ ) at the  $\text{SiO}_2/\text{Si}$  interface. High interface trapping states lead to deep Fermi level pinning in the band gap, so that the concentration of free carriers remains low, ensuring a state of high resistivity. This translates into lower losses and higher linearity of the substrate [59], [60]. In our work, an epitaxial SiGe layer is inserted between the buried oxide (BOX) and the handle Si substrate. A  $\text{SiO}_2/\text{SiGe}$  interface tends to have higher  $D_{it}$  values than  $\text{SiO}_2/\text{Si}$ , attributed to the formation of Ge-O bonds at the interfacial layer [61]. Consequently, it would be valuable to investigate  $D_{it}$  and the effective resistivity ( $\rho_{\text{eff}}$ ) in different buried SiGe stressor substrates.

### 5.2.1 Sample Descriptions

**Figure 5.1** shows a SiGe buried stressor MOS capacitor (a) and a coplanar waveguide (CPW) transmission line structure on SiGe buried stressor substrate schematic cross-section (b). Here,  $R_s$  is the series resistance of the Si substrate.  $C_{\text{ox}}$  is the capacitance of the dielectric stack.  $G_p$  and  $C_p$  are the parallel equivalent conductance and capacitance, respectively, corresponding to the  $\text{SiO}_2/\text{SiGe}$  interface. The SiGe/Si is assumed to be a trap-free interface.

**Table 5.1** lists the composition of five buried SiGe stressor substrates and the related thickness of the SiGe layer. The preparation of MOS capacitors and

CPW lines on buried SiGe stressor substrate is described hereafter. 76.2 mm SOI wafers(<100>, p-type, standard resistivity) with buried SiGe under the BOX (20 nm) were fabricated by Acorn Technologies. The Si layer (260 nm) of the SOI samples was removed using 25% TMAH at 75 °C. 180 nm SiO<sub>2</sub> was then deposited by PECVD on the SOI substrates, followed by the evaporation of an aluminum layer approximately 1 μm thick and the lithography to define the electrodes of the MOS capacitors and the CPW lines. To enable measurement of the MOS capacitor characteristics (C–V–G and I–V) with the B1500, a 300 nm-thick Al layer was deposited on the wafer backside using an E-gun (Vacotec) evaporator. Prior to Al evaporation, the wafer backside were dipped in BHF to remove the native oxide and ensure good metal contact.



**Figure 5.1:** (a) The cross-section of SiGe buried stressor MOS capacitor. (b) The cross-section of a CPW line on top of SiGe buried stressor substrate.

**Table 5.1:** Composition and thickness of SiGe layers in SiGe buried stressor substrates.

| Sample number     | SiGe thickness<br>(Å) | % Ge | $D_{it}$ (eV <sup>-1</sup> cm <sup>-2</sup> )<br>(Conductance method) | $\rho_{eff}$ (Ω·cm)<br>@ 2 GHz @ 0 V |
|-------------------|-----------------------|------|-----------------------------------------------------------------------|--------------------------------------|
| 1                 | 90                    | 20   | $1.6 \times 10^{12}$                                                  | 45.7                                 |
| 2                 | 130                   | 20   | $2.2 \times 10^{12}$                                                  | 46.0                                 |
| 3                 | 700                   | 20   | $2.5 \times 10^{12}$                                                  | 46.1                                 |
| 4                 | 60                    | 40   | $4.0 \times 10^{11}$                                                  | 39.3                                 |
| 5                 | 110                   | 30   | $8.0 \times 10^{11}$                                                  | 43.6                                 |
| Standard Si       | -                     | -    | $2.5 \times 10^{11}$                                                  | 21.5                                 |
| SiGe/HR Si (TCAD) | 1100                  | 20   | $2.2 \times 10^{12}$                                                  | 5213                                 |

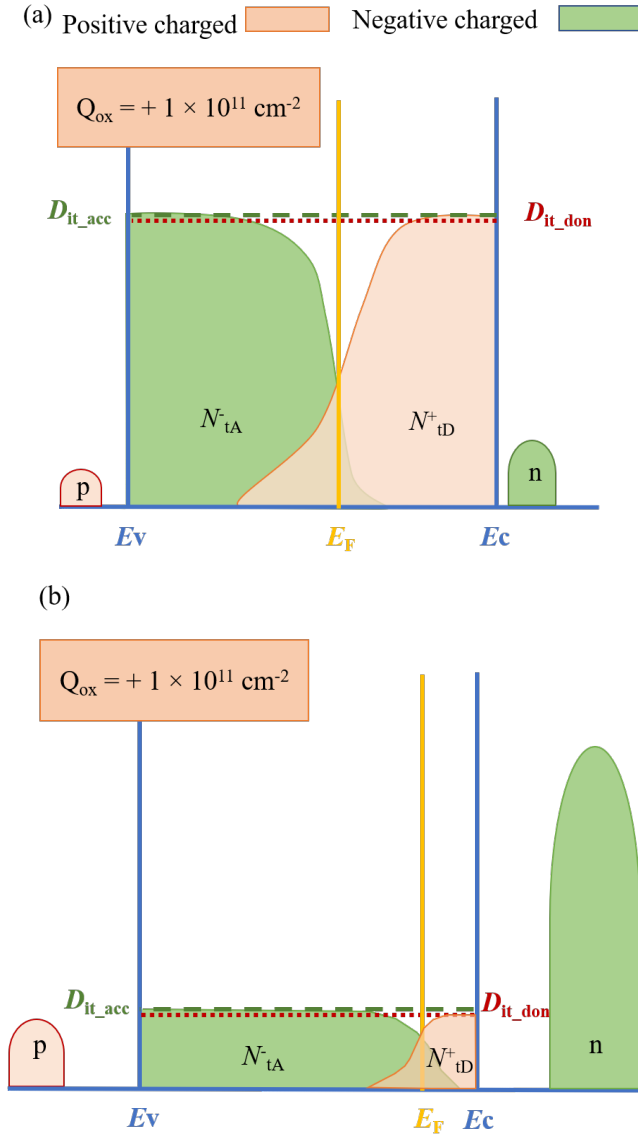
### 5.2.2 The Charge Compensation Mechanism Mitigating PSC

Summary of charge compensation mechanisms in silicon-based substrates in response to an increase in positive charge  $+\Delta Q_{Applied}$  (voltage on electrode or fixed interface charges, for example):

- $n$   $\nearrow$
  - $p$   $\searrow$
- } Dominant (only) charge compensation mechanism in HR substrates.  
Large swings in  $E_F$ .
- 
- $N_{tA}^-$   $\nearrow$
  - $N_{tD}^+$   $\searrow$
- } Dominant charge compensation mechanism in TR substrates.  
Fundamentals of Fermi level pinning.

**Figure 5.2** shows the energy band diagram of the SiO<sub>2</sub>/SiGe interface, illustrating the trap occupancy and free-carrier variation in response to a shift of the Fermi level ( $E_F$ ) at 0 V applied bias, where  $Q_{ox}$  is fixed at  $1 \times 10^{11}$  cm<sup>-2</sup>, the value typically characterized for the PECVD SiO<sub>2</sub>.  $D_{it,don}$  and  $D_{it,acc}$  are the donor and acceptor interface trap densities, respectively;  $N_{tD}^+$  and  $N_{tA}^-$  are the densities of ionized donor and acceptor traps, respectively; and  $p$  and  $n$  are the free-carrier densities of holes and electrons, respectively. The parasitic surface



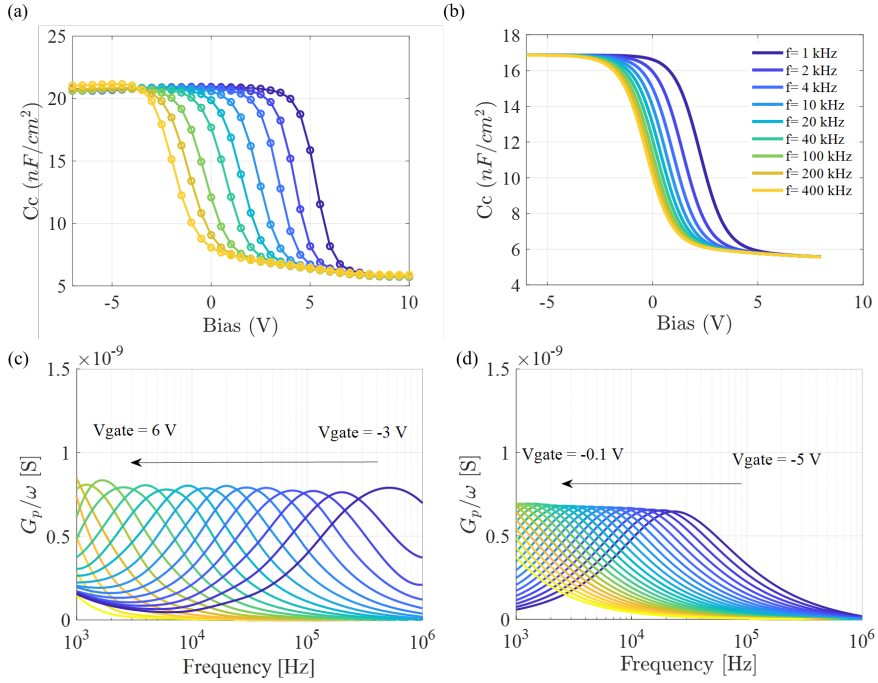


**Figure 5.2:** Graphic representations of traps occupancy and free carrier density variation in response to a shift of Fermi level  $E_F$  at 0 V applied bias at  $\text{SiO}_2/\text{SiGe}$  interface: (a) PSC induced by  $Q_{\text{ox}}$  is compensated mainly by ionized acceptor and donor interface traps ( $D_{\text{it,acc}}$  &  $D_{\text{it,don}} > 1 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ ). (b) PSC induced by  $Q_{\text{ox}}$  is compensated mainly by free carriers  $p$  and  $n$  ( $D_{\text{it,acc}}$  &  $D_{\text{it,don}} < 1 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ ).

conduction (PSC) effect arises from the presence of the fixed charge,  $Q_{\text{ox}}$  (positive at the  $\text{SiO}_2/\text{SiGe}$  interface), which triggers significant band bending of the Fermi level towards the edge of the conduction band. Consequently, this phenomenon results in an increased population of free electrons that counterbalance the positive fixed charges found at the interface and form a conductive parasitic surface conduction (PSC) sheet layer. To maintain the high resistivity of the substrate (high  $\rho_{\text{eff}}$ ), the compensating charges at the interface must be ionized interface traps instead of free carriers that contribute to the PSC. The ionized interface traps  $N_{\text{tD}}^+$  and  $N_{\text{tA}}^-$  at the  $\text{SiO}_2/\text{SiGe}$  interface, distributed in the band gap, will mainly compensate for the applied charge ( $Q_{\text{applied}} = Q_{\text{ionized}} + Q_{\text{free}}$ ) [62].

In **Figure 5.2 (a)**, when the density of ionized interface traps exceeds  $1 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ , it primarily contributes to compensation instead of free carriers (at least for usual values of  $Q_{\text{ox}}$  (i.e., in the range of  $10^{11}$ ) and/or for usual applied bias voltages (i.e., in the range of a few Volts)). This leads to the Fermi level being strongly pinned within the band gap. Conversely, in **Figure 5.2 (b)**, when the density of ionized interface traps is lower than  $1 \times 10^{12} \text{ eV}^{-1}\text{cm}^{-2}$ , the free carriers  $n$  and  $p$  dominate the compensation, causing the Fermi level to shift closer to the conduction band and the formation of a PSC layer to compensate for the  $Q_{\text{ox}}$ .

### 5.2.3 C-V and G-V Characterizations and TCAD Simulations Interface Trap Extraction



**Figure 5.3:** (a) Measured and (b) TCAD simulated corrected capacitance versus applied bias ( $C_c$  - V) from 1 kHz to 400 kHz for sample 2. (c) Measured and (d) TCAD simulated parallel equivalent conductance ( $G_p/\omega$ ) as a function of angular frequency ( $\omega$ ) at different gate voltages in the depletion regime. In simulations,  $Q_{\text{ox}} = 1 \times 10^{11} \text{ cm}^{-2}$  and  $D_{\text{it}} = 2.2 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$  are used.

The measured and simulated (with TCAD Silvaco Atlas) corrected  $C_c$ -V curves for frequencies ranging from 1 kHz to 400 kHz are shown in **Figure 5.3 (a)** and **Figure 5.3 (b)**, respectively. The measured and simulated parallel equivalent conductance ( $G_p/\omega$ ) as a function of angular frequency ( $\omega$ ) at different gate voltages in the depletion regime for sample 2 are shown in **Figure 5.3 (c)** and **Figure 5.3 (d)**, respectively.

The simulated  $C_c$ -V and  $G_p/\omega$  - f curves, along with the extracted  $D_{\text{it}}$  from the C-V measurements, exhibit similar trends. Using the series resistance correction model (SRC) proposed by Nicollian [31], as presented in **Figure 5.1 (a)**,

$C_c$  and  $G_c$  can be calculated to withdraw the effect of the series resistance in **Figure 5.3 (a)** and **Figure 5.3 (b)**. One can observe that the flatband voltages shift towards negative values with increased frequencies, preventing a conventional flatband extraction. The effective pinned Fermi level can explain this horizontal frequency-dependent shift due to high  $D_{it}$  at the  $\text{SiO}_2/\text{SiGe}$  interface [63].

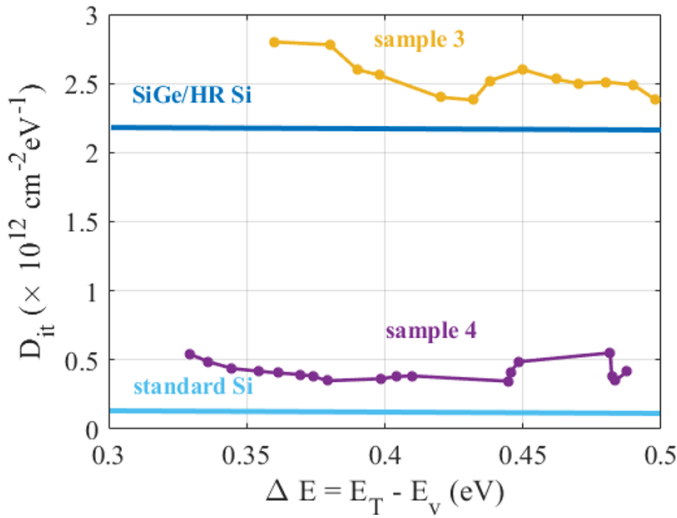
The "bump" arises within the inversion region, where the increase in capacitance under positive bias with decreasing frequency is largely mitigated. This could also be attributed to a high interface trap density, effectively stabilizing the Fermi level [64]. The extraction of average substrate p-type doping concentration,  $N_A (= 1.10 \times 10^{15} \text{ cm}^{-3})$ , is based on the slope of the linear part of the  $(1/C_c)^2$  curve versus the applied voltage in the inset, corresponding to  $14 \text{ } \Omega\cdot\text{cm}$  for all SiGe samples [39].

**Figure 5.3 (c)** and **Figure 5.3 (d)** show  $G_p/\omega - f$  curves for both measurements and simulations. The peak positions of the  $G_p/\omega (f)$  curves shift to higher voltage values with decreased frequency due to the presence of interface trap states. Therefore, we obtain the interface trap response for a gate voltage range from -3 to 6 V.

**Figure 5.4** shows the  $D_{it} (\Delta E = E_T - E_V)$  profiles of samples 3, 4, standard Si, and TCAD SiGe/HR Si at room temperature, where the trap energy states are distributed in the band from 0.3 to 0.5 eV above the valence band. For comparison, samples 3 and 4, with the highest and lowest  $D_{it}$ , respectively, are selected among all buried SiGe substrates. The  $D_{it}$  of TCAD SiGe/HR Si is based on the extracted value from sample 2. Standard Si with a  $\text{SiO}_2/\text{Si}$  interface typically exhibits the normal  $D_{it}$  around  $\sim 10^{10} \text{ cm}^{-2}\text{eV}^{-1}$ .

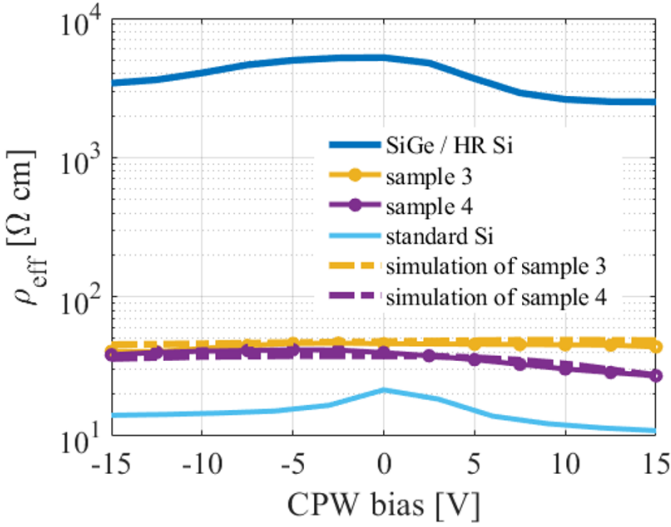
#### 5.2.4 RF Characterizations and Simulations of CPW Lines

In **Figure 5.5**, the  $\rho_{\text{eff}}$  of sample 3, which has the highest  $D_{it}$  around  $2.5 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$  among five SiGe samples, shows a relatively flat and elevated  $\rho_{\text{eff}}$  compared to sample 4 over the range of -15 to 15 V at 2 GHz. In contrast, sample 4, with the lowest  $D_{it}$  ( $4.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ ), exhibits a more bias-dependent  $\rho_{\text{eff}}$  due to reduced interface trap compensation. Unlike samples 3 and 4, standard silicon (Si) with a resistivity of  $15 \text{ } \Omega\cdot\text{cm}$  demonstrates an even lower effective resistivity ( $\rho_{\text{eff}}$ ), which also varies with gate bias. This



**Figure 5.4:**  $D_{it}$  ( $\Delta E = E_T - E_v$ ) profile showing  $D_{it}$  of samples 3, 4, standard Si, and SiGe/HR Si energy distribution in the band gap respectively.

corresponds to an interface trap density ( $D_{it}$ ) an order of magnitude lower than that of sample 4. The boost in  $\rho_{eff}$  is attributed to the larger  $D_{it}$  at the  $\text{SiO}_2/\text{SiGe}$  interface compared to that of  $\text{SiO}_2/\text{Si}$ . The simulations for samples 3 and 4 align with their experimental characterization, allowing for accurate modeling of high-resistivity buried SiGe stressor fully depleted silicon-on-insulator (FD-SOI) substrates. To explore the potential of the SiGe approach in enabling high-quality RF performance, a buried SiGe high-resistivity Si substrate ( $2 \text{ k}\Omega \cdot \text{cm}$ ) is employed in the TCAD simulation, as shown in **Table 5.1**. Based on Acorn Technologies' upcoming fabrication plan, the SiGe layer on the buried HR Si substrate is undoped and 110 nm thick. This substrate demonstrates a high and bias-independent  $\rho_{eff}$  above  $2 \text{ k}\Omega \cdot \text{cm}$ , owing to the sufficient compensation provided by the interface traps ( $2.2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ ) to counter against the PSC extracted by  $Q_f = 1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . The details will be mentioned in the next section.



**Figure 5.5:** CPW line effective resistivity of samples 3 (includes the simulation), 4 (with the simulation), standard Si, and simulated SiGe/HR Si extracted at 2 GHz as a function of applied bias from -15 to 15 V.

### 5.3 Buried SiGe on High-Resistivity Si Substrates

From the [Section 5.2](#), conductance measurements have revealed high interface trap densities ( $D_{it}$ ) at the  $\text{SiO}_2/\text{SiGe}$  interface, compared to the conventional  $\text{SiO}_2/\text{Si}$  interface, likely due to the emergence of Ge-O bonds within the interfacial region. This yielded valuable insights into optimizing substrate performance for RF applications using HR silicon, as discussed in this section. This section provided detailed information on the quantitative analysis of six different SiGeHR Si substrates under C-V, small-amplitude, and large-amplitude excitations. The impact of annealing on the RF behaviors is well quantified, which could motivate further studies to align annealing processes with current SOI process requirements.

#### 5.3.1 Sample Description

**Table 5.2** lists the compositions of six SiGe high-resistivity (HR) Si substrates and the related thickness of the SiGe layer. The preparation of the MOS capacitor and coplanar waveguide (CPW) lines on SiGe HR Si substrates is

described hereafter.

P-type HR ( $>10\text{ k}\Omega\text{cm}$ ) wafers, measured by four-probe contact characterization with buried SiGe layers, were provided by Acorn Technologies. A 200 nm  $\text{SiO}_2$  layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) on top of the SiGe as the dielectric. Three samples were annealed for one hour at high temperature ( $950^\circ\text{C}$  in pure  $\text{N}_2$ ). They are referred to as group A, while those without annealing are denoted as group NA. Finally, a 1  $\mu\text{m}$  Al layer was deposited using electron-beam physical vapor deposition and patterned to define the RF passive structures over  $\text{SiO}_2$ .

For comparison, one HR Si substrate ( $> 5\text{ k}\Omega\cdot\text{cm}$ , P-type) with the same thick oxide 200 nm and Al layers, as well as one RFeSI70 substrate provided by Soitec, are included in the RF large-signal characterizations. RFeSI<sup>TM</sup> refers to a trap-rich polysilicon substrate. RFeSI70 exhibits a low H2 distortion level at -70 dBm for a fundamental component H1 of +15 dBm at 0 V.

The CPW line used to characterize all substrates is 2.1 mm long with specific dimensions: a signal width of 26  $\mu\text{m}$ , a spacing of 12  $\mu\text{m}$  between the signal and ground tracks, and a ground width of 208  $\mu\text{m}$ .

Simulations were conducted using Silvaco TCAD, including a detailed representation of oxide charges ( $Q_{\text{ox}}$ ) within the  $\text{SiO}_2$  layer, as well as interface traps present at the  $\text{SiO}_2/\text{SiGe}$  interface. The oxide charge density was extracted as  $1 \times 10^{11}\text{ cm}^{-2}$  for all simulations. The interface trap density ( $D_{\text{it}}$ ) was simulated using Gaussian distributions for donor and acceptor-like traps, with the extracted  $D_{\text{it}}$  values obtained from C–V characterizations. The trap distribution within the energy gap was assumed to be uniform and continuous.

**Figure 5.1** shows the schematic cross-sections of a SiGe MOS capacitor (a) and a coplanar waveguide (CPW) transmission line (b). The MOS capacitor has an electrode area of  $A_{\text{pad}} = 0.0154\text{ cm}^2$ . The CPW line dimensions are: signal line width  $W_c = 26\mu\text{m}$ , ground line width  $W_G = 208\mu\text{m}$ , and gap spacing to the ground lines  $S = 12\mu\text{m}$ . Both structures have the same metal thickness  $t_{\text{metal}} = 1\mu\text{m}$  and oxide thickness  $t_{\text{ox}} = 200\text{ nm}$ . Instead of the equivalent circuit used in **Figure 5.1(a)**, we will develop a new model to analyze the impedance and extract  $D_{\text{it}}$  of SiGeHR substrates in the next section.

### 5.3.2 Capacitance-Voltage (C-V) Measurements

Capacitance-voltage (C–V) measurements were carried out in the dark using a PM8PS probe station in combination with a B1500 semiconductor parameter analyzer. The device under test was the MOS capacitor illustrated in **Figure**

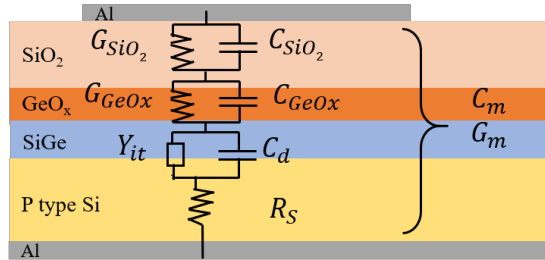
**Table 5.2:** Summary of substrate parameters.

| Sample Number                    | SiGe Thickness (Å) | % Ge | $D_{it}$<br>( $\text{cm}^{-2}\text{eV}^{-1}$ )<br>Conductance Method | $D_{it}$<br>( $\text{cm}^{-2}\text{eV}^{-1}$ )<br>Terman Method |
|----------------------------------|--------------------|------|----------------------------------------------------------------------|-----------------------------------------------------------------|
| <b>Non-Annealed Samples (NA)</b> |                    |      |                                                                      |                                                                 |
| NA20                             | 767                | 20   | $6.0 \times 10^{11}$                                                 | $5.1 \times 10^{11}$                                            |
| NA30                             | 76                 | 30   | $5.0 \times 10^{11}$                                                 | $4.0 \times 10^{11}$                                            |
| NA40                             | 157                | 40   | $6.0 \times 10^{11}$                                                 | $5.8 \times 10^{11}$                                            |
| <b>Annealed Samples (A)</b>      |                    |      |                                                                      |                                                                 |
| A20                              | 767                | 20   | $4.0 \times 10^{12}$                                                 | $2.0 \times 10^{12}$                                            |
| A30                              | 76                 | 30   | $4.8 \times 10^{12}$                                                 | $2.1 \times 10^{12}$                                            |
| A40                              | 157                | 40   | $5.0 \times 10^{12}$                                                 | $2.5 \times 10^{12}$                                            |

**5.3(a).** Measurements were performed across a frequency range from 1 kHz to 1 MHz at room temperature.

**Figure 5.6** shows the cross section and equivalent circuit of a SiGe buried high-resistivity Si substrate. We noticed that several researches concern about relatively high interface trap density at the interfacial layer/SiGe, which be attributed to the undesired  $\text{GeO}_x$  formation in this interfacial layer [65]. The out-diffused Ge from SiGe accumulates at the  $\text{SiO}_2/\text{SiGe}$  interface during the high temperature annealing ( $950^\circ\text{C}$ ), forming a lossy  $\text{GeO}_x$ . Si–O–Si or Si–O–Ge networks both exist. Because the Ge–O bond is weaker, oxygen in the Si–O–Ge structure easily dissociates, resulting in a Si–O dangling bond. This dangling bond can follow two pathways: if it bonds with an interstitial Si atom, it resolves into a fully formed  $\text{SiO}_2$  lattice; however, if no Si atom is available to complete the bond, the dangling bond traps a free electron, creating a localized negative charge state, introducing a significant amount of interface traps [66]. The Ge percentage in the SiGe plays a critical role in determining  $D_{it}$  [67]. Therefore, to precisely extract  $D_{it}$ ,  $\text{GeO}_x$  will be accounted into the equivalent circuit model. Note that the exact physical thickness of  $\text{GeO}_x$  layer was not characterized in this thesis.





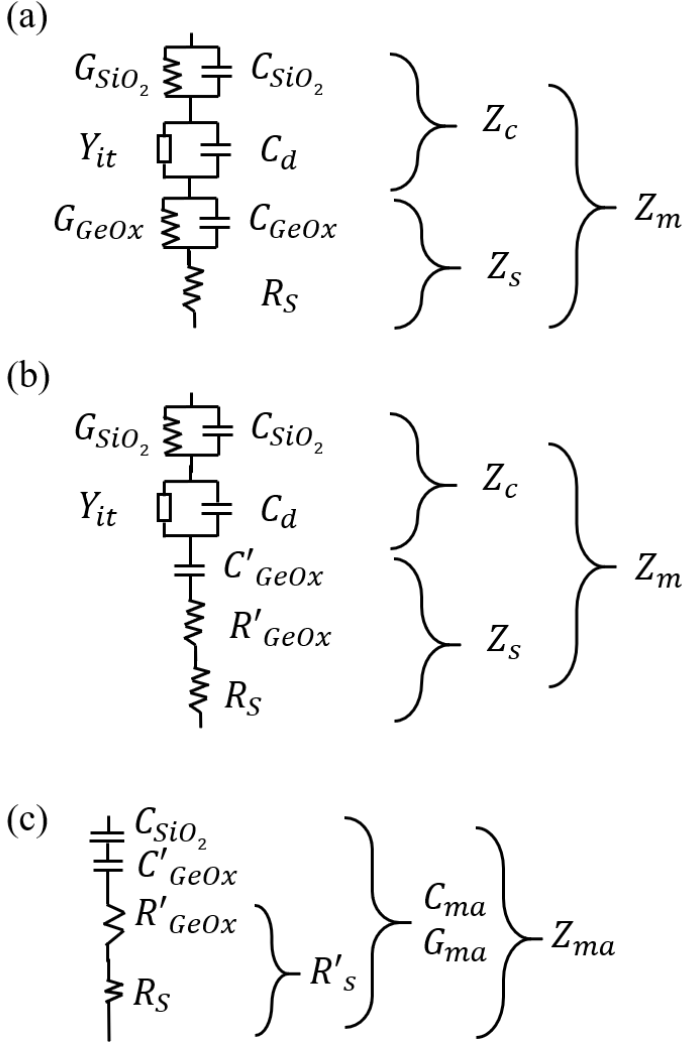
**Figure 5.6:** Cross-section with equivalent circuit of a SiGe buried high-resistivity Si substrate (layer thickness of  $\text{SiO}_2$ ,  $\text{GeO}_x$ , and SiGe are not to scale).

Extracting the interface trap density ( $D_{it}$ ) using a single technique can be affected by parasitic effects such as high series resistance—common in high-resistivity substrates—and frequency-dependent dispersion in the accumulation and depletion regions. These parasitic influences distort the measured C-V characteristics, potentially leading to erroneous interpretations of  $D_{it}$ . To mitigate these effects, we employ the series resistance and high-conductance (SRHC) correction model introduced in [68], which accounts for the series resistance ( $R_s$ ) arising from the high-resistivity Si substrate and lossy  $\text{GeO}_x$ .

**Figure 5.7 (a)** presents the equivalent circuit of the SiGe-buried MOS capacitor, where  $C_{\text{SiO}_2}$  and  $G_{\text{SiO}_2}$  denote the capacitance and conductance of the  $\text{SiO}_2$  layer, respectively;  $C_d$  represents the depletion capacitance; and  $Y_{it}$  is the admittance due to interface traps at the  $\text{SiO}_2/\text{SiGe}$  interface. The SiGe/Si interface is assumed to be free of traps. The lossy  $\text{GeO}_x$  layer is modeled by a parallel RC network ( $C_{\text{GeO}_x}$  and  $G_{\text{GeO}_x}$ )<sup>1</sup>, which is equivalently transformed into a series configuration comprising  $C'_{\text{GeO}_x}$  and  $R'_{\text{GeO}_x}$ , as illustrated in **Figure 5.7 (b)**.

In the strong accumulation regime, the equivalent circuit is illustrated in **Figure 5.7 (c)**, where the measured capacitance ( $C_{ma}$ ) and conductance ( $G_{ma}$ ) reflect the behavior of the device. Since the oxide capacitance ( $C_{\text{SiO}_2}$ ) is known from the capacitor geometry, and both depletion capacitance ( $C_d$ ) and interface trap admittance ( $Y_{it}$ ) are negligible in this regime, we derive the following

<sup>1</sup>To simplify circuit equations, the RC network of  $\text{GeO}_x$  from **Figure 5.6** has been swapped with the network comprising interface admittance  $Y_{it}$  and the depletion capacitance  $C_d$ .



**Figure 5.7:** (a) Equivalent circuit of SiGe buried high-resistivity Si substrate. Since the 200 nm SiO<sub>2</sub> layer exhibits low leakage, the conductance  $G_{\text{SiO}_2}$  can be neglected. (b) Simplified circuit of (a). (c) Simplified circuit in the strong accumulation region.

relations:

$$Z_{\text{ma}} = \frac{1}{G_{\text{ma}} + j\omega C_{\text{ma}}} = R'_s + \frac{1}{j\omega C_{\text{SiO}_2}} + \frac{1}{j\omega C'_{\text{GeOx}}} \quad (5.1)$$

Comparing the real and imaginary parts of equation **Equation 5.1**, we can extract the series resistance:

$$R'_s = R_s + R'_{\text{GeOx}} = \frac{G_{\text{ma}}}{G_{\text{ma}}^2 + \omega^2 C_{\text{ma}}^2} \quad (5.2)$$

Additionally, as  $C_{\text{SiO}_2}$  is known from the geometry of the structure, we have:

$$C'_{\text{GeOx}} = -C_{\text{SiO}_2} \cdot \frac{G_{\text{ma}}^2 + \omega^2 C_{\text{ma}}^2}{\omega^2 (C_{\text{ma}}^2 - C_{\text{ma}} C_{\text{SiO}_2}) + G_{\text{ma}}^2} \quad (5.3)$$

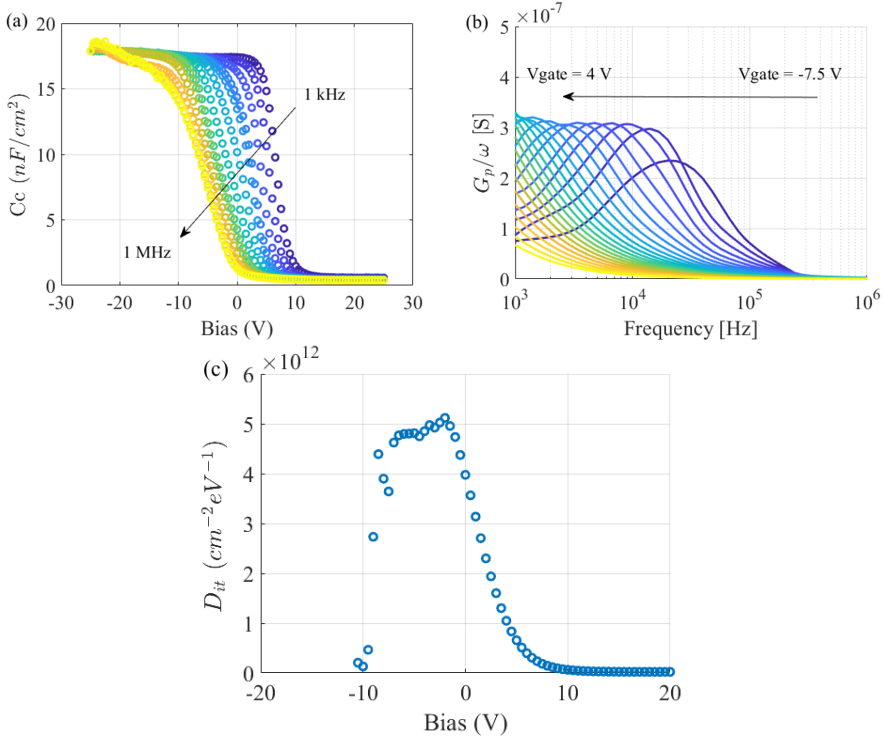
Using **Equation 5.2** and **Equation 5.3**, we extract  $R'_s$  and  $C'_{\text{GeOx}}$  directly from the measured  $C_{\text{ma}}$  and  $G_{\text{ma}}$  in strong accumulation. As a result, the impedance  $Z_s$  in **Figure 5.7 (a)** can be estimated from measurements in strong accumulation. This allows for a correction to be applied to the measured impedance  $Z_m$ , yielding the corrected impedance  $Z_c$ :

$$Z_c = \frac{1}{G_c + j\omega C_c} = Z_m - Z_s \quad (5.4)$$

$$C_c = \frac{(\omega^2 C_m C'_{\text{GeOx}} - G_m^2 - \omega^2 C_m^2)(G_m^2 + \omega^2 C_m^2) C'_{\text{GeOx}}}{(\omega^2 C_{\text{GeOx}}'^2) [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C'_{\text{GeOx}})^2} \quad (5.5)$$

$$G_c = \frac{[G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2] (G_m^2 + \omega^2 C_m^2) (\omega^2 C_{\text{GeOx}}'^2)}{(\omega^2 C_{\text{GeOx}}'^2) [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C'_{\text{GeOx}})^2} \quad (5.6)$$

Following the deembedding of the series resistance and the impedance of  $\text{GeO}_x$ , both of which may impact the  $D_{\text{it}}$  extraction, corrected  $C_c$  and  $G_c$  in **Equation 5.5** and **Equation 5.6** are provided. To assure that the extracted  $D_{\text{it}}$  values are correctly estimated, two extraction methods of interface traps are described below.



**Figure 5.8:** (a) The corrected capacitance versus applied bias ( $C_c - V$ ) from 1 kHz to 1 MHz. (b) Measured parallel equivalent conductance ( $G_p/\omega$ ) as a function of angular frequency ( $\omega$ ) at different gate voltages in the depletion regime. (c) Interface trap density extracted from the conductance method versus applied bias.

### 5.3.3 Extraction of Interface Trap Density

Two methods are used to extract the interface trap density: the conductance method and the Terman method. As an example, we examine sample A40.

#### Extraction of Interface Trap from the Conductance Method

The conductance method is used to investigate changes in the occupancy of interface trap levels within the silicon bandgap near the Fermi level, following the variation of gate voltage. The capture and emission of majority carriers by these interface traps introduce an energy loss mechanism, evident across a range of frequencies—except at very low frequencies, where no energy loss occurs, and at very high frequencies, where the interface traps do not respond. This energy loss is measured as an equivalent parallel conductance per unit area ( $G_p/\omega$ ) as a function of bias voltage and frequency.

We take sample A40 as an example. After removing  $R_s$ , **Figure 5.8 (a)** and **Figure 5.8 (b)** show the corrected  $C_c$ -V curves of A40 for frequencies ranging from 1 kHz to 1 MHz, and the parallel equivalent conductance ( $G_p/\omega$ ) as a function of angular frequency ( $\omega$ ) at different gate voltages in the depletion regime from  $-7.5$  V to 4 V.

$D_{it}$  is extracted by calculating the peak values of  $G_p/\omega$  from **Figure 5.8 (b)** using the equation below [49]:

$$D_{it} \approx \frac{2.49}{qA} \cdot \left( \frac{G_p}{\omega} \right)_{\max} \quad (5.7)$$

where  $\omega = 2\pi f$ ,  $q = 1.6 \times 10^{-19}$  C, and the electrode area  $A = 0.0154$  cm<sup>2</sup>. The extracted  $D_{it}$  is approximately  $5 \times 10^{12}$  cm<sup>-2</sup>eV<sup>-1</sup> in the depletion regime, as shown in **Figure 5.8 (c)**. For other samples, the corresponding values are reported in **Table 5.2**.

#### Extraction of Interface Trap from the Terman Method

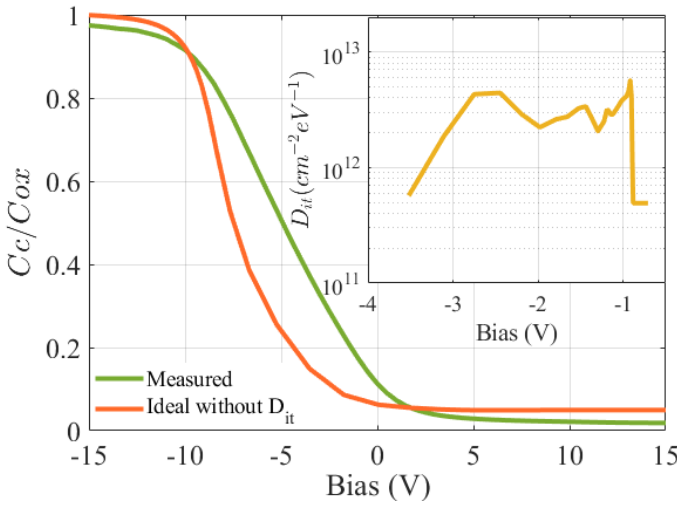
The Terman method provides a rapid evaluation of the SiO<sub>2</sub>/SiGe interface and serves as a reference for comparison with the conductance method. This technique is based on the extraction of the experimental surface potential ( $\phi_s$ ) as a function of gate bias, and a comparison with a theoretical C-V curve assuming no interface traps ( $D_{it} = 0$  cm<sup>-2</sup>eV<sup>-1</sup>), to determine the interface trap density.

The same sample, A40, was analyzed in this context. **Figure 5.9** presents the normalized C-V characteristics of sample A40 at 100 kHz, comparing the measured data with the ideal curve generated by TCAD simulation (excluding

interface traps). Both curves are normalized by the oxide capacitance ( $C_{ox}$ ) and have been corrected for  $R_s$ . The stretch-out does not produce a parallel shift of the C–V curves, as do the fixed charge and work function differences.

The stretch-out observed in the depletion region of the measured curve indicates the presence of  $D_{it}$ . This occurs because the interface traps capture and emit carriers too slowly to follow high-frequency signals and instead respond to the slowly varying DC component of the gate voltage.

The inset of **Figure 5.9** shows that the extracted  $D_{it}$ , determined using the Terman method [49], lies in the range of  $3 \times 10^{12}$  to  $4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . It is worth noting that the  $D_{it}$  values obtained from the conductance method are in good agreement with those extracted using the Terman method. Corresponding values for the other samples are summarized in **Table 5.2**.

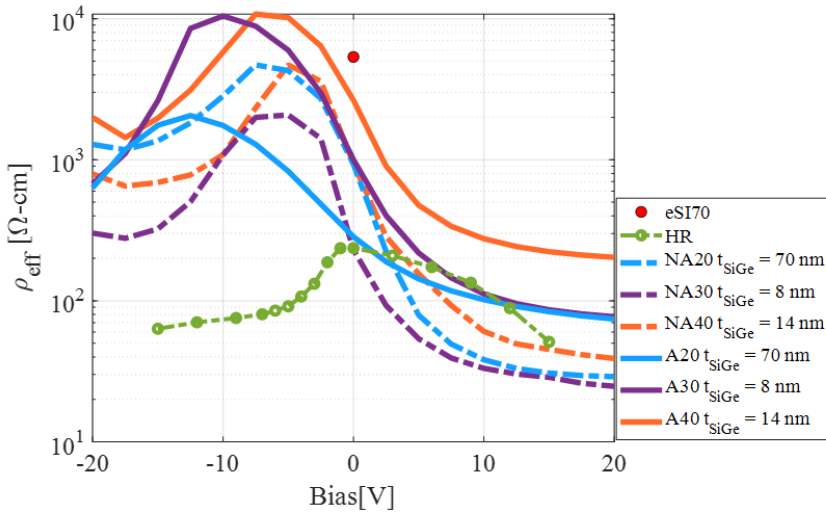


**Figure 5.9:** An ideal  $C_{HF}$  without  $D_{it}$  plot compared with an experimental  $C_{HF}$  versus bias at 100 kHz. The inset shows the  $D_{it}$  extracted from the Terman method versus the bias in the depletion region for sample A40.

#### 5.3.4 Small-Signal Measurements

The small-signal measurements of the CPW lines have been performed using an Agilent 2-port performance network analyzer (PNA) and a pair of 100- $\mu\text{m}$  pitch ground signal ground (GSG) |Z| probes. The S-parameters have been measured to extract the effective resistivity [69], [12]. The short-open-thru-load (SOTL)

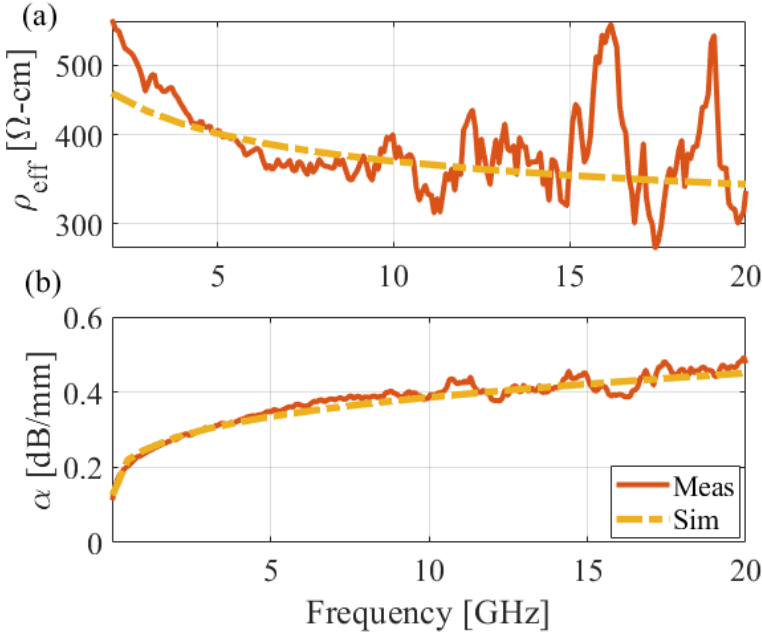
method calibrated the system at the probe tips. After measuring the open, thru, and line, the de-embedding method proposed by [62] was used to remove the pad parasitics.



**Figure 5.10:** Effective resistivity ( $\rho_{\text{eff}}$ ) as a function of DC bias at 2 GHz for two substrate groups: non-annealed substrates (dash-dot lines) and annealed substrates (solid lines) with different Ge compositions (20 %, 30 %, and 40 %), HR Si (green dash-dot line), and eSI70 (red dot) as references.

**Figure 5.10** shows the extracted effective resistivity ( $\rho_{\text{eff}}$ ) as a function of DC bias applied on the signal electrode at 2 GHz for two substrate groups: the non-annealed (NA20, NA30, NA40) and annealed group (A20, A30, A40), along with two reference cases, RFeSI70 and HR Si. At 0 V DC bias, all SiGe-passivated substrates exhibit superior  $\rho_{\text{eff}}$  compared to HR Si with sample A40 approaching  $3 \text{ k}\Omega \cdot \text{cm}$  and the  $5 \text{ k}\Omega \cdot \text{cm}$  of the reference TR SOI substrate. Further, the annealed samples A30 and A40 exhibit higher  $\rho_{\text{eff}}$  values than their non-annealed counterparts. This difference is attributed to the increased interface trap density in the annealed group, which leads to more effective PSC mitigation by Fermi level pinning and consequently results in a higher effective resistivity. In contrast, HR Si with  $D_{\text{it}}$  around  $10^{10}$  exhibits the lowest effective

resistivity, around  $100 \Omega \cdot \text{cm}$  due to the conductive PSC layer. The RFeSI70 (red dot) lies in the high-resistivity regime around  $5.4 \times 10^3 \Omega \cdot \text{cm}$  at 0 V. As expected, the trap-rich polysilicon in RFeSI70 offers high trap density, leading to a bias-independent effective resistivity  $\rho_{\text{eff}}$ .



**Figure 5.11:** Comparison between measured and TCAD simulated (a) extracted effective resistivity and (b) insertion loss of CPW line with the DC bias 0 V as a function of frequency for sample NA40.

When the DC bias is varied, all samples exhibit a bias dependence of  $\rho_{\text{eff}}$ , particularly in the positive bias region. The reduction of  $\rho_{\text{eff}}$  for  $V_{\text{DC}} > 0$  is not yet fully understood and requires further investigation. We discussed one possibility of this variation in [Section 5.3.6](#). However, for practical RF applications, the value of  $\rho_{\text{eff}}$  at or near 0 V is more critical, as it represents the condition required to maintain good effective resistivity while minimizing power consumption.



### TCAD Simulation

A TCAD simulation was conducted using Silvaco Atlas at 0 V to assess the RF performance of the SiGe structure NA40, with the identical dimensions of the CPW line shown in **Figure 5.1 (b)**. The key physical parameters used in the simulations are listed below:

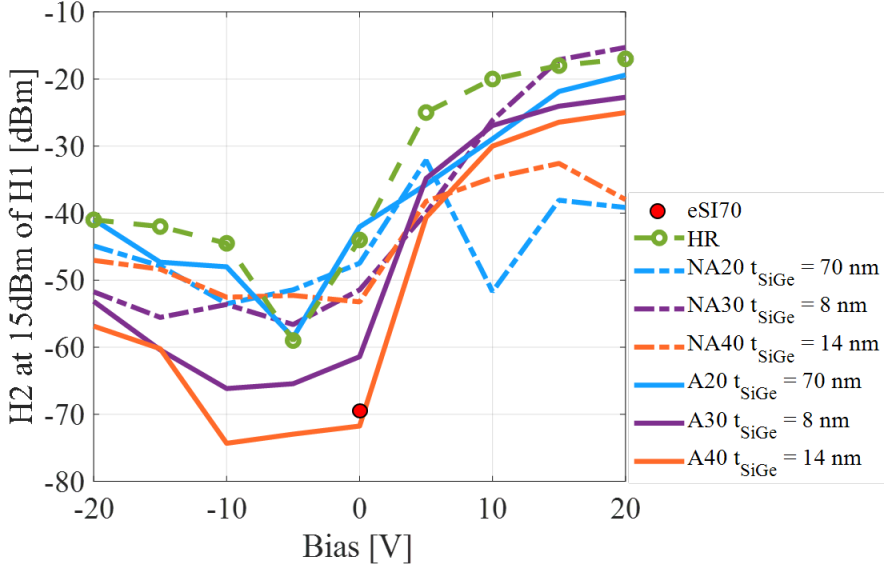
1. Metal thickness of Al contact:  $t_{\text{Al}} = 1 \mu\text{m}$ .
  - (a) Aluminum, with metal work function  $\phi_M = 4.1 \text{ eV}$ .
2. Oxide thickness:  $t_{\text{ox}} = 200 \text{ nm}$ .
  - (a) With  $N_{\text{ox}} = \frac{Q_{\text{ox}}}{q} = +1.25 \times 10^{11} \text{ cm}^{-2}$ .
3. Interface trap: using Gaussian distributions  $g_{\text{GA}}(E)$  and  $g_{\text{GD}}(E)$ .
  - (a) Characteristic decay energies:  $W_{\text{GA}} = W_{\text{GD}} = 0.1 \text{ eV}$ .
  - (b) **Interface trap density:**  $N_{\text{GA}} = N_{\text{GD}} = 6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ .
  - (c) Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution  $g_{\text{GA}}(E)$ :  $E_{\text{GA}} = 0.6 \text{ eV}$ .
  - (d) Energy position from the valence band edge of the peak of the Gaussian donor trap distribution  $g_{\text{GD}}(E)$ :  $E_{\text{GD}} = 0.3 \text{ eV}$ .
4. Silicon substrate thickness:  $t_{\text{sub}} = 700 \mu\text{m}$ .
  - (a)  $N_A = 2.8 \times 10^{12} \text{ cm}^{-3}$ , i.e.,  $\rho_{\text{nom}} = 5 \text{ k}\Omega \text{ cm}$  ( $5 \text{ k}\Omega \cdot \text{cm}$ ).

Considering parasitic surface conduction (PSC),  $Q_{\text{ox}}$  in the insulating layer was set to  $1.25 \times 10^{11} \text{ cm}^{-2}$ , as extracted from C–V measurements, and a trap model with an interface trap density of  $6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  was included. For sample NA40, the simulated results show good agreement with the measured  $\rho_{\text{eff}}$  and the insertion loss ( $\alpha$ ) at 0 V from 100 MHz to 20 GHz, as shown in **Figure 5.11**. The simulation indicates that the implemented level of interface trap density effectively passivates the parasitic surface conduction (PSC).

### 5.3.5 Large-Signal Measurements

To characterize the linearity of the CPW lines described above, a harmonic distortion (HD) measurement setup was employed as follows: a single-tone signal (H1) at 900 MHz was injected into one port of the CPW line, with its power swept from -5 dBm to 24 dBm. The fundamental (H1), second (H2), and third (H3) harmonics were measured at the second port of the CPW.

**Figure 5.12** presents the measured power levels of the second (H2) harmonic as a function of DC bias for two substrate groups: the non-annealed group (NA20, NA30, NA40) and the annealed group (A20, A30, A40), along with two reference cases: RFeSi70 and HR Si. The observed harmonic levels are inversely correlated with the substrate's effective resistivity illustrated in

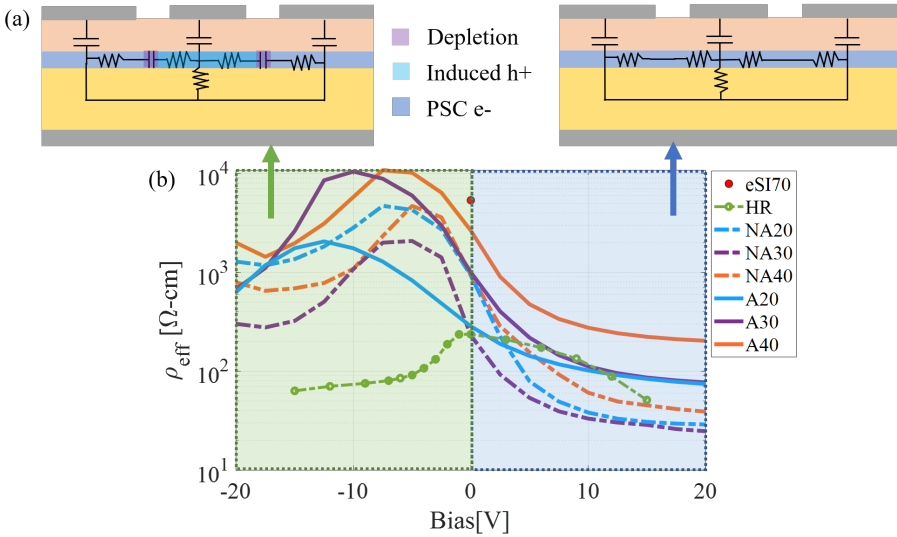


**Figure 5.12:** Measured second harmonic ( $H_2$ ) power at  $H_1 = 15$  dBm versus the applied DC bias for two substrate groups at 900 MHz: non-annealed substrates (dash-dot lines) and annealed substrates (solid lines) with different Ge compositions (20%, 30%, and 40%). The HR Si (green dash-dot line) and eSI70 (red dot) are the references for comparison.

**Figure 5.10.** The annealed samples A30 and A40, which display higher  $\rho_{\text{eff}}$  at 0 V, demonstrate  $H_2$  levels below  $-60$  dBm, even outperforming the reference TR SOI substrate at 0 V for sample A40. Among the references, HR Si exhibits higher harmonic distortion than all annealed samples and performs similarly to the non-annealed ones, likely due to its strong parasitic surface conduction (PSC). This comparison further supports the conclusion that annealing enhances the interface trap density at the  $\text{SiO}_2/\text{SiGe}$  interface, thereby minimizing PSC effects more effectively than in non-annealed substrates. Another comparison can be made with the FD-SOI-compatible PN-passivated substrate reported in [25], where  $H_2$  levels of approximately  $-70$  dBm were obtained for similar CPW dimensions and oxide thickness. These results highlight the promising linearity performance of A40, positioning it as a strong candidate for further

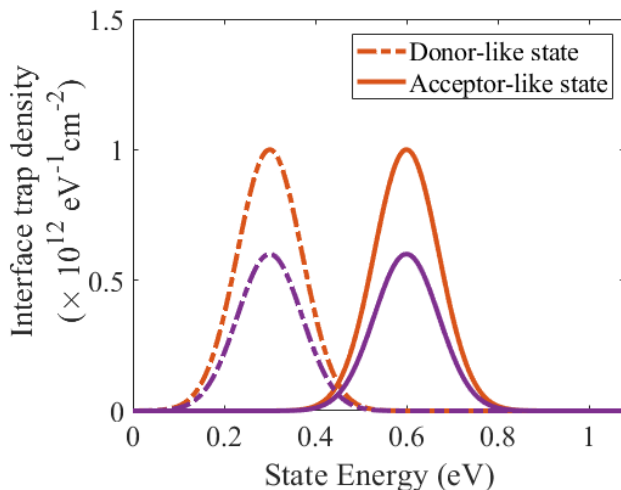
investigation, particularly in optimizing the interface trap density with respect to Ge concentration, SiGe layer thickness, and annealing conditions.

5.3.6 Discussion of Bias Dependence of the Effective Resistivity



**Figure 5.13:** (a) Resistivity cross-section profile and simplistic equivalent circuit of SiGe buried HR substrates at negative and positive applied DC bias, that correspond to states of strong accumulation and strong inversion in the substrate, respectively. (b) Effective resistivity as a function of DC bias at 2 GHz, see [Figure 5.10](#).

To help understand the trend of  $\rho_{eff}$ , a resistivity cross-section profile and a simplistic equivalent circuit of SiGe buried HR substrates with their  $\rho_{eff}$  extraction are shown in [Figure 5.13](#). Since the PSC is induced at the interface beneath the ground lines and in between the signal and ground lines of the CPW, the applied DC bias determines the carriers present below the signal line. In the negative-bias region, which corresponds to strong accumulation, holes accumulate below the signal line, and a depletion region therefore forms between this region and the adjacent electron-rich region (see [Figure 5.13 \(a\)](#)). This lateral depletion region significantly increases the path resistance and yields a high  $\rho_{eff}$ . As the bias increases, the holes beneath signal electrode are depleted, which yields highest  $\rho_{eff}$  than at large negative bias (see [Figure](#)

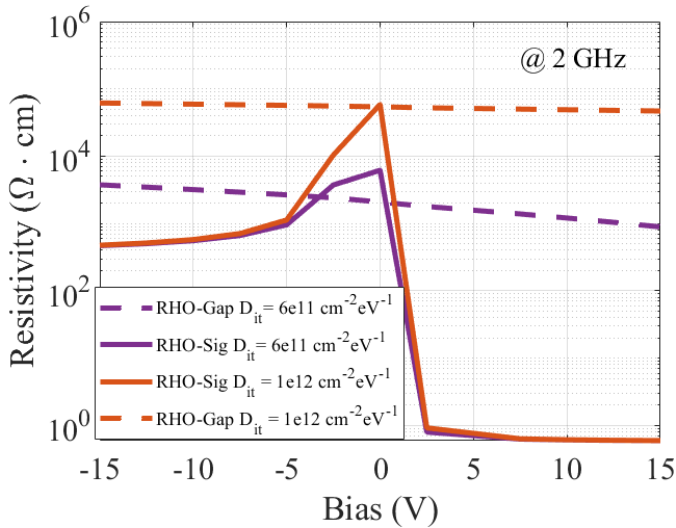


**Figure 5.14:** The distribution of interface trap density across the energy bandgap for the two simulated cases.

**5.13 (b)).** In the positive-bias region, the entire surface path at the interface fills with electrons between the signal line and ground lines of the CPW, and  $\rho_{\text{eff}}$  is therefore at a minimum. In the HR Si substrate,  $\rho_{\text{eff}}$  is dominated by what happens in the depleted gap region. Even when the region under the signal line is close to intrinsic (very high resistivity), the effective resistivity remains low, seen in [70].

The Fermi level becomes pinned and cannot approach the valence band due to a high density of traps located in the lower part of the bandgap, close to midgap. As a consequence, parasitic surface conduction by holes is effectively suppressed. In contrast, under positive gate bias, the Fermi level shifts toward the conduction band, where the density of traps in the upper half of the bandgap is low, allowing a large population of electrons to accumulate at the interface.

Two simulations were constructed using a continuously distributed interface trap profile, as shown in **Figure 5.14**, differing only in  $D_{\text{it}}$ . We probe the resistivity of the Si region under the signal line and that of the gap between the signal and ground lines, as seen below **Figure 5.15**. The resistivity of the gap is constant with bias, but the resistivity of the signal depends on the bias, the same trend as the **Figure 5.13**. With the increased  $D_{\text{it}}$ , both the resistivities of the signal and gap are increased.

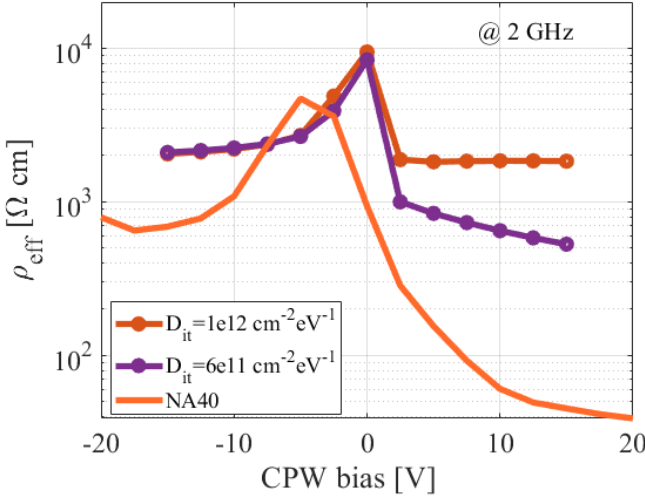


**Figure 5.15:** The resistivity as a function of DC bias at 2 GHz for two simulations (different in  $D_{it}$ , same in  $Q_{ox} = 1 \times 10^{11} \text{ cm}^{-2}$  and  $EGA = 0.6 \text{ eV}$  and  $EGD = 0.3 \text{ eV}$ ).

By examining **Figure 5.16**, it can be observed that the effective resistivity follows the same trend up to a bias of 2.5 V, after which a clear deviation appears in the positive bias region. Given the large difference between the peak value of  $\rho_{eff}$  (approximately  $10 \text{ k}\Omega \cdot \text{cm}$ ) and the minimum plateau value ( $\sim 80 \Omega \cdot \text{cm}$ ), an increase in  $D_{it}$  uniformly raises  $\rho_{eff}$  across the entire bias range rather than induce a bias-dependent variation. This deviation originates from an increase in the resistivity of the gap region. To reproduce the measured behavior of the NA40 sample, it is therefore necessary to reduce the gap resistivity while maintaining the resistivity of the signal region. One possible approach can be considered to prove the explanation: etch away the oxide above the gaps (remove  $Q_{ox}$  in the gap, no PSC) to see if the  $\rho_{eff}$  is independent of the bias.

## 5.4 Chapter Summary

This chapter presents a comprehensive study combining C–V and RF characterizations to evaluate SiGe buried on both standard-resistivity and high-resistivity (HR) Si substrates. The objective is to assess the impact of buried SiGe layers,



**Figure 5.16:** Effective resistivity ( $\rho_{\text{eff}}$ ) as a function of DC bias at 2 GHz for two simulations (different in  $D_{\text{it}}$ , same in  $Q_{\text{ox}} = 1 \times 10^{11} \text{ cm}^{-2}$  and  $\text{EGA} = 0.6 \text{ eV}$  and  $\text{EGD} = 0.3 \text{ eV}$ ) and the non-annealed 40% Ge SiGe buried HRS as a reference.

thermal processing, and interface properties on substrate resistivity, parasitic surface conduction (PSC), and RF linearity.

C–V and G–V measurements, supported by TCAD simulations, were used to analyze charge compensation mechanisms and to extract the interface trap density ( $D_{\text{it}}$ ) at the  $\text{SiO}_2/\text{SiGe}$  interface. The results show that the annealed SiGeHR Si substrates exhibit interface trap densities  $D_{\text{it}}$  at the  $\text{SiO}_2/\text{SiGe}$  interface, one order of magnitude higher compared to their non-annealed counterparts, extracted using both the conductance and Terman methods. These elevated trap densities are attributed to the thermal budget associated with high-temperature furnace annealing.

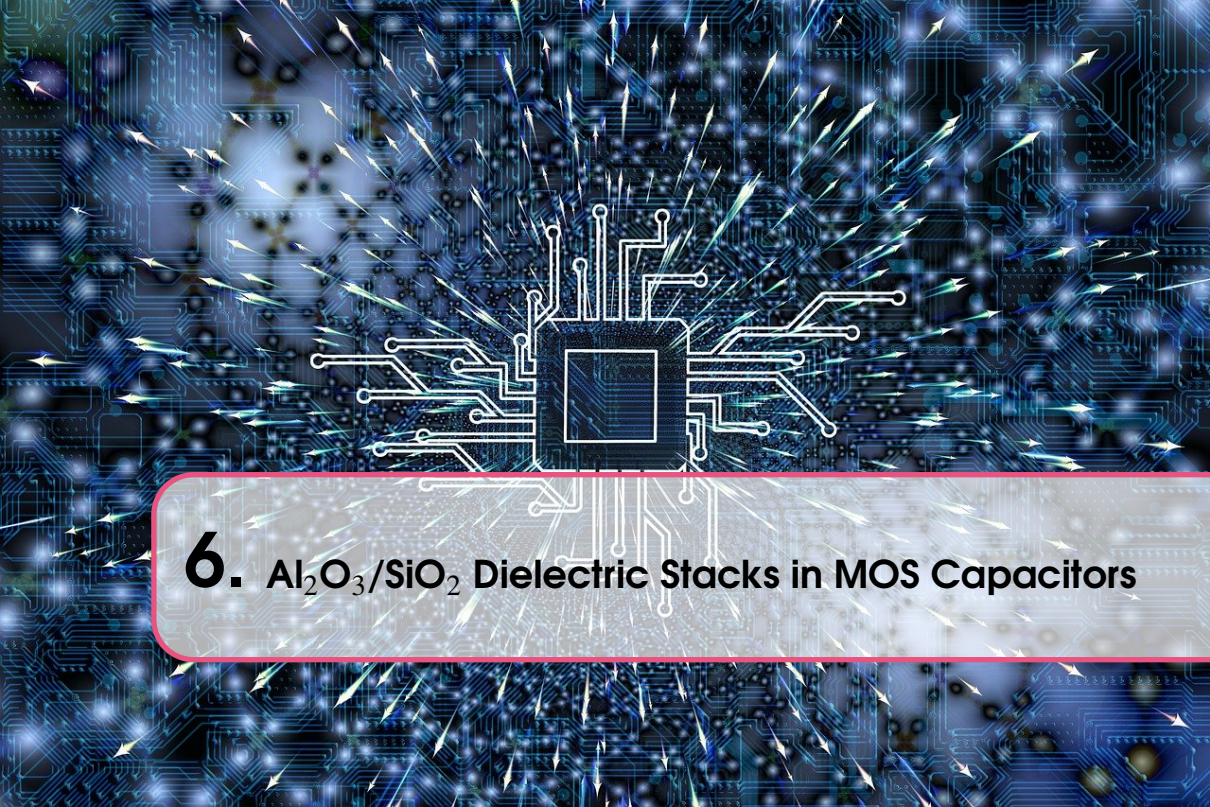
RF measurements on coplanar waveguide (CPW) lines demonstrate that a high  $D_{\text{it}}$  can effectively neutralize free carriers originating from the substrate bulk under negative gate bias, thereby mitigating the PSC effect. As a result, high effective resistivity and improved linearity are preserved near 0 V. These findings indicate that SiGe HR-Si substrates can withstand furnace annealing

up to 950°C without degradation of RF performance.

Among the investigated structures, the SiGe HR-Si substrate with a Ge content of 40% emerges as a particularly promising candidate for RF SOI integration. More generally, regardless of the Ge content, all samples show superior substrate performance after being subjected to a thermal budget comparable with CMOS processing. This chapter thus establishes buried SiGe as an effective and thermally robust solution for suppressing PSC and enabling high-linearity RF SOI technologies.







## 6. $\text{Al}_2\text{O}_3/\text{SiO}_2$ Dielectric Stacks in MOS Capacitors

### 6.1 Introduction

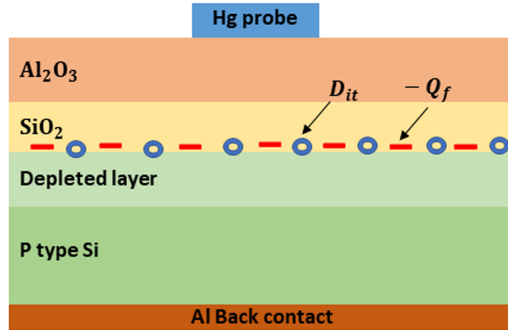
The semiconductor industry targets of high performance, high speed, low power consumption and high density of transistors on a wafer have been achieved by reducing the dimensions of the metal-oxide semiconductor field-effect transistor (MOSFET). This leads to replacing the silicon dioxide  $\text{SiO}_2$  gate dielectric by high- $k$  dielectric, considering  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$  and eventually  $\text{HfO}_2$  as the industrial reference. Suitable gate dielectric material properties must include, concurrently, (i) a high relative dielectric constant ( $k$ ) for high field-effect gate control with the same electrical thickness, (ii) a large energy bandgap for minimizing the gate leakage current, (iii) a low interface trap density ( $D_{it}$ ) for preventing Fermi level pinning and charge carrier mobility degradation, and (iv) a thermo-dynamic stability close to silicon for reliable transistor fabrication. Moreover, according to the requirement of sustainable development, we should avoid using scarce metals for high- $k$  oxides. Hf-based gate oxides have become the standard for CMOS nodes below 45 nm, i.e., for equivalent oxide thicknesses (EOT) ranging from 1.2 to 4.5 nm [71]. Aluminum oxide ( $\text{Al}_2\text{O}_3$ ) has been

considered in the past for its high  $k$  value, but too high  $D_{it}$  and interface charge scattering, thereby decreasing the channel mobility of transistors, have been reported. Kessel et al. [72] believed that this issue was related to an interfacial  $\text{SiO}_2$ -like layer  $\text{SiO}_x$  (1–2 nm) existing between  $\text{Al}_2\text{O}_3$  and Si. The reduction of  $D_{it}$  can be achieved by inserting a thermally-grown high quality  $\text{SiO}_2$  film between  $\text{Al}_2\text{O}_3$  and Si [71] to form a gate dielectric stack. Recently, high negative fixed oxide charges ( $Q_f$ ), sufficiently low  $D_{it}$ , and sustainable material usage have been investigated in Atomic layer-deposited (ALD)  $\text{Al}_2\text{O}_3$  layers for solar cells [73]. Therefore, the questions are: “Could these features be of interest and application for CMOS at the 65 nm node and beyond?” and “Could thicker high- $k$  gate oxides be used in advanced nodes for special analog or I/O (input-output) functions?” Negative  $Q_f$  indeed results in a shift of threshold voltage ( $V_{th}$ ) towards more positive values in nMOS devices. This could be exploited to decrease the doping concentration in the channel for compensating  $V_{th}$  change, simultaneously increasing channel mobility [74] and potentially decreasing variability.

These properties make the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack a promising high- $k$  candidate to extend gate-dielectric scaling at the 65 nm CMOS node and beyond, where conventional  $\text{SiO}_2$  (and its nitrided  $\text{SiON}$  variant) reaches its leakage limits, before  $\text{HfO}_2$  became the industry choice at 45 nm and below. To assess this potential, in this chapter, we fabricate and characterize MOS capacitors based on  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate dielectric stacks with a target equivalent oxide thickness (EOT) of 4.9 nm. In Section 6.2 and Section 6.3, the device fabrication and electrical characterization techniques are introduced. Section 6.4 details different extraction methodologies of series resistance ( $R_s$ ) (including an equivalent circuit model), fixed oxide charge density ( $Q_f$ ), flatband voltage ( $V_{fb}$ ), and interface trap density ( $D_{it}$ ). In Section 6.5, leakage currents and tunneling mechanisms through the different gate dielectric stacks are investigated. To evaluate the passivation quality of different dielectric stacks on the silicon surface, carrier lifetime and surface recombination characteristics were investigated in Section 6.7. Finally, optimization of dielectric stacks and conclusions are drawn from the analysis of gate-dielectric-stack MOS capacitors in Section 6.6.

## 6.2 Sample Fabrication

The cross-section of a MOS capacitor with the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate stack is illustrated in **Figure 6.1**.

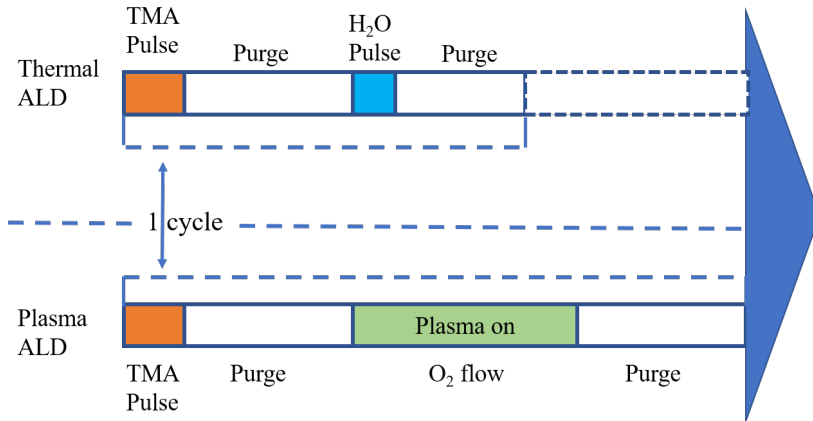


**Figure 6.1:** Cross-section of a MOS capacitor with the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate stack.

We prepare four kinds of gate dielectric stacks. Prior to the gate stack formation, 3-in. Si substrates ( $\langle 100 \rangle$ , p-type,  $10 \, \Omega\cdot\text{cm}$ , single-side polished) were cleaned by Piranha solution (3:1:  $\text{H}_2\text{SO}_4\text{:H}_2\text{O}_2$  for a duration of 20 min at  $110^\circ\text{C}$ ). After the Piranha cleaning, all the wafers were dipped in dilute HF solution (1:50: HF:Deionized water) to remove the native oxide. Then the substrates were immediately put into a Fiji F200 ALD machine or Koyo Thermalsystem for, respectively, depositing  $\text{Al}_2\text{O}_3$  or oxidizing Si to thermal  $\text{SiO}_2$ . **Table 6.1** gives an overview of the different gate stacks studied in this work. Sample 1, 3.9-nm-thick thermal  $\text{SiO}_2$  grown on Si substrate at  $900^\circ\text{C}$  in an ultra-dry oxygen atmosphere for 30 min, is used as a reference sample. For samples 2 and 3, the same fabrication process was used to grow 2-nm-thick thermal  $\text{SiO}_2$  by reducing growth time. Otherwise, for samples 4 and 5, 2-nm-thick  $\text{SiO}_2$  was deposited by plasma enhanced atomic layer deposition (PE-ALD), using tris(dimethylamino)silane and  $\text{O}_2$  radical as, respectively, Si and O sources at  $250^\circ\text{C}$ .

In **Table 6.1**, 3.5-nm-thick  $\text{Al}_2\text{O}_3$  layers were deposited by thermal atomic layer deposition (T-ALD) or PE-ALD at  $200^\circ\text{C}$ , respectively. The brief schematic view of ALD process cycle is drawn in the **Figure 6.2**. In both cases, trimethylaluminum precursor (TMA) from Sigma-Aldrich was used as the aluminum source. Deionized water pulses and oxygen flows were used for T-ALD and PE-ALD, respectively. In T-ALD, TMA and  $\text{H}_2\text{O}$  pulses duration was 0.06

s and purge time was 10 s. In PE-ALD, TMA pulse duration and purge time of, respectively, 0.06 and 10 s were used. The pulse duration and purge time of the  $\text{O}_2$  plasma were 20 s and 5 s, respectively. An  $\text{O}_2$  flow of 30 sccm and a plasma power of 300 W were used. The growth rate of  $\text{Al}_2\text{O}_3$  was 1 Å per cycle for both PE-ALD and T-ALD. After deposition, the thicknesses were mapped by ellipsometry over the wafer. In order to measure MOS capacitor characteristics (C-V, G-V) with Mercury Probe Station, a 300-nm-thick Al layer was deposited on the backside of the Si wafer using E-gun evaporation. Before the evaporation, the backside of the Si wafers was dipped in BHF to remove the native oxide for ensuring an ohmic contact. Finally, all the samples were annealed in forming gas ( $\text{N}_2:\text{H}_2 = 9:1$ ) at 432 °C for 30 min.



**Figure 6.2:** Schematic view of the ALD cycle. Firstly, TMA is pulsed and a purge time is performed to pump away the reaction products and residual TMA. Secondly, water is pulsed in case of thermal ALD. For PE-ALD, remote oxygen plasma is activated. Finally, purge time is performed for the same purpose as before.

### 6.3 Experimental Details

Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were performed using Mercury Probe Station and HP 4284A LCR meter at different frequencies from 1 kHz to 1 MHz. The use of the mercury probe allows to avoid the deposition of metal electrodes on top of the stacks, which simplifies

the fabrication process of the MOS capacitors. In order to obtain accurate and reliable measurement results, the following factors are important: (i) before starting C–V measurements, the electrical equilibrium and the initial state of the device must be ensured. For this purpose, we used sufficient hold time (5 s) and delay time (2 s) for each sweep step and each bias point, respectively; (ii) the series resistances coming from the substrate and dielectric leakage in the C-G equivalent circuit must be de-embedded; (iii) the parasitic capacitance coming from interconnect cables of instruments must be withdrawn. All the measurements were carried out at room temperature.

## 6.4 Extraction of Physical Parameters

### 6.4.1 Equivalent Oxide Thickness

Before describing the fabrication of MOS capacitors, we define the EOT of the gate dielectric stack according to the combined capacitance of the two dielectrics in series:

$$t_{\text{EOT}} = t_{\text{SiO}_2} + \left( \frac{k_{\text{SiO}_2}}{k_{\text{Al}_2\text{O}_3}} \right) t_{\text{Al}_2\text{O}_3} \quad (6.1)$$

where  $t_{\text{SiO}_2}$  and  $t_{\text{Al}_2\text{O}_3}$  are the thicknesses of the interfacial  $\text{SiO}_2$  layer and  $\text{Al}_2\text{O}_3$  layer, respectively, with relative dielectric constants  $k_{\text{SiO}_2} = 3.9$  and  $k_{\text{Al}_2\text{O}_3} = 9$ . The EOT of the stack is calculated using a two-capacitor in-series model written as below [75]:

$$\text{EOT} = \frac{\epsilon_{\text{SiO}_2} \cdot t_{\text{high-k}}}{\epsilon_{\text{high-k}}} + t_{\text{IL}} \quad (6.2)$$

where  $\epsilon_{\text{SiO}_2}$ ,  $\epsilon_{\text{IL}}$ , and  $\epsilon_{\text{high-k}}$  are the dielectric constants of  $\text{SiO}_2$ , the interfacial layer, and the high- $k$  dielectric layer, respectively, and  $t_{\text{IL}}$  and  $t_{\text{high-k}}$  are the thicknesses of the interfacial layer and the high- $k$  dielectric layer. In our work, the interfacial layer is  $\text{SiO}_2$  and the high- $k$  dielectric layer is  $\text{Al}_2\text{O}_3$ . We prepared four types of dielectric stacks as shown in **Table 6.1**.

**Table 6.1:** Summary of five gate dielectric stacks, including compositions, target, measured, and Equivalent Oxide Thicknesses (Targeted EOT = 3.9 nm).

| Sample Number | Dielectric Stack                                           | Target Thickness (nm) | Measured Thickness (nm)* | EOT (nm)** |
|---------------|------------------------------------------------------------|-----------------------|--------------------------|------------|
| 1             | Thermal $\text{SiO}_2$                                     | 3.9                   | $3.9 \pm 0.1$            | 3.9        |
| 2             | PE-ALD $\text{Al}_2\text{O}_3$ /<br>thermal $\text{SiO}_2$ | 3.5/2                 | $2.8 \pm 0.1$ / 2.5      | 4.9        |
| 3             | T-ALD $\text{Al}_2\text{O}_3$ /<br>thermal $\text{SiO}_2$  | 3.5/2                 | $3.2 \pm 0.2$ / 2.5      | 5.0        |
| 4             | PE-ALD $\text{Al}_2\text{O}_3$ /<br>PE-ALD $\text{SiO}_2$  | 3.5/2                 | $3.7 \pm 0.2$ / 2.5      | 5.8        |
| 5             | T-ALD $\text{Al}_2\text{O}_3$ /<br>PE-ALD $\text{SiO}_2$   | 3.5/2                 | $3.5 \pm 0.2$ / 2.5      | 5.6        |

\*Measured thickness is the average value of 16 points on one sample.

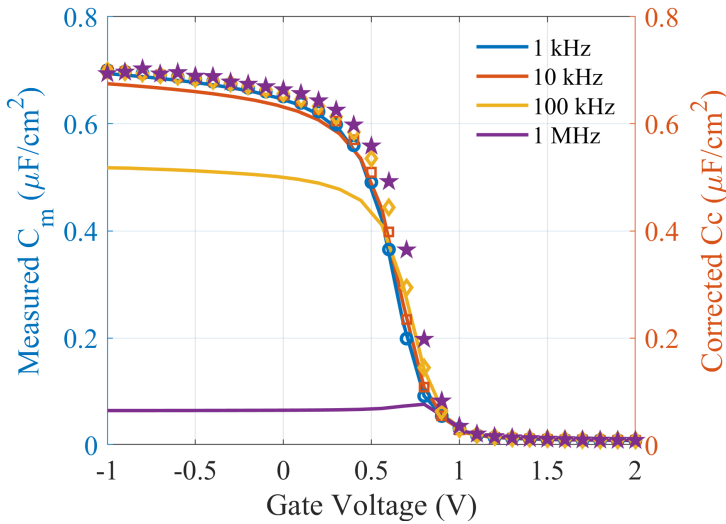
\*\*Equivalent Oxide Thickness (EOT) is calculated by:

$$t_{EOT} = t_{\text{SiO}_2} + \left( \frac{k_{\text{SiO}_2}}{k_{\text{Al}_2\text{O}_3}} \right) t_{\text{Al}_2\text{O}_3}.$$



### 6.4.2 Series Resistance Extraction

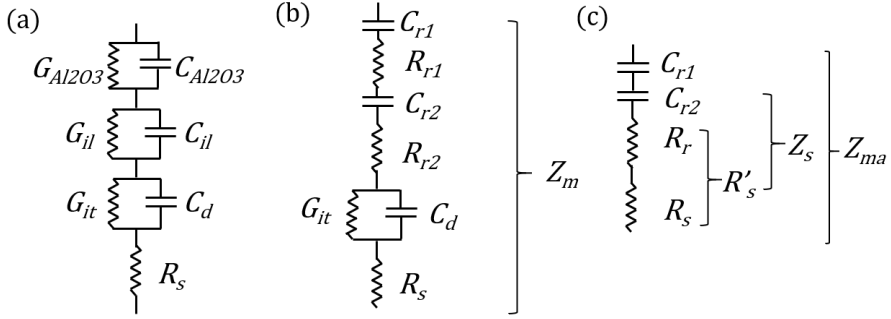
**Figure 6.3** shows an example of C–V curves measured on MOS capacitors at various frequencies. A large dispersion in the strong accumulation region is observed due to the large existing series resistance ( $R_s$ ) originating from the Si substrate. Therefore, to correctly interpret the data,  $R_s$  needs to be de-embedded from the measurement data. This requires small-signal equivalent circuit modeling of the MOS capacitor.



**Figure 6.3:** Measured capacitance (lines) versus gate voltage at different frequencies for sample 2, showing frequency dependence in accumulation. Corrected curves (symbols) after removing the effect of series resistance  $R_s$ .

In order to model the MOS capacitor with a multilayer gate dielectric stack seen in **Figure 6.1**,  $C_{\text{Al}_2\text{O}_3}$  is defined as the capacitance of  $\text{Al}_2\text{O}_3$ ,  $C_{\text{il}}$  and  $G_{\text{il}}$  are the capacitance and conductance of the interfacial layer (IL)  $\text{SiO}_2$ ,  $C_{\text{ox}}$  is the total capacitance of the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stack,  $C_d$  and  $G_{\text{it}}$  are the capacitance of the depletion layer and the conductance of interface traps between the gate dielectric stack and Si substrate, and  $R_s$  is the total series resistance. Hg probe acts as the top electrode.

**Figure 6.4** depicts the equivalent circuit of a MOS capacitor with the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate stack. As shown in **Figure 6.4 (b)**, for simplification purposes,  $G_{\text{Al}_2\text{O}_3}$  and  $C_{\text{Al}_2\text{O}_3}$  elements are replaced by  $C_{\text{r1}}$  and  $R_{\text{r1}}$  in series,  $G_{\text{il}}$  and  $C_{\text{il}}$



**Figure 6.4:** (a) Equivalent circuit of a MOS capacitor with  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate stack. (b) Simplified circuit of (a). (c) Simplified circuit in strong accumulation regime.

elements are replaced by  $C_{r2}$  and  $R_{r2}$  in series as given by:

$$C_{\text{Al}_2\text{O}_3} \approx C_{r1}, \quad G_{\text{Al}_2\text{O}_3} \approx R_{r1} \quad (6.3)$$

$$C_{\text{il}} \approx C_{r2}, \quad G_{\text{il}} \approx R_{r2} \quad (6.4)$$

$$C_{r1} = \frac{G_{\text{Al}_2\text{O}_3}^2 + \omega^2 C_{\text{Al}_2\text{O}_3}^2}{\omega^2 C_{\text{Al}_2\text{O}_3}} \quad (6.5)$$

$$G_{r1} = \frac{G_{\text{Al}_2\text{O}_3}}{G_{\text{Al}_2\text{O}_3}^2 + \omega^2 C_{\text{Al}_2\text{O}_3}^2} \quad (6.6)$$

$$C_{r2} = \frac{G_{\text{il}}^2 + \omega^2 C_{\text{il}}^2}{\omega^2 C_{\text{il}}} \quad (6.7)$$

$$G_{r2} = \frac{1}{R_{r2}} = \frac{G_{\text{il}}}{G_{\text{il}}^2 + \omega^2 C_{\text{il}}^2} \quad (6.8)$$



where  $\omega = 2\pi f$ . The total impedance of the simplified circuit in **Figure 6.4 (b)** is:

$$Z_m = \frac{1}{G_m + j\omega C_m} \quad (6.9)$$

Here,  $G_m$  and  $C_m$  denote, respectively, the conductance and capacitance values measured in the experiments. In the strong accumulation region,  $C_d$  and  $G_{it}$  can be neglected and the equivalent circuit in **Figure 6.4 (b)** is further simplified to that in **Figure 6.4 (c)**, in which  $R'_s$  is the total series resistance:

$$R'_s = R_s + R_r \quad (6.10)$$

where  $R_r = R_{r1} + R_{r2}$ . In this case, the measured accumulation impedance  $Z_{ma}$  can be expressed as:

$$Z_{ma} = \frac{1}{G_{ma} + j\omega C_{ma}} \quad (6.11)$$

or

$$Z_{ma} = R'_s - \frac{1}{j\omega C_{r1} + C_{r2}} \quad (6.12)$$

where  $C_{ma}$  and  $G_{ma}$  are the measured accumulation capacitance and conductance, respectively. Comparing the real and imaginary parts of **Equation 6.11** and **Equation 6.12**, we obtain:

$$R'_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \quad (6.13)$$

$$C_{r2} = -\frac{C_{r1}(G_{ma}^2 + \omega^2 C_{ma}^2)}{\omega^2(C_{ma}^2 - C_{ma}C_{r1}) + G_{ma}^2} \quad (6.14)$$

$$Z_c = \frac{1}{G_c + j\omega C_c} = Z_m - Z_s \quad (6.15)$$

$$Z_s = R'_s + \frac{1}{j\omega C_{r2}} \quad (6.16)$$

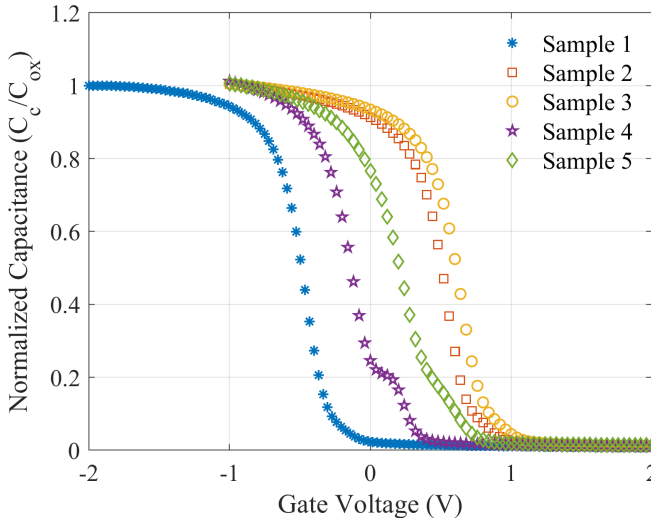
Finally,  $C_c$  and  $G_c$  are the corrected capacitance and conductance of the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stack after removal of  $R_s$ , respectively. The total stack capacitance  $C_{\text{ox}}$  is obtained from the plateau of  $C_c$  in strong accumulation. By substituting **Equation 6.9** and **Equation 6.16** into **Equation 6.15**, we obtain: The corrected  $C_c$  and  $G_c$  without frequency dispersion [76] are given by:

$$C_c = \frac{(\omega^2 C_m C_{r2} - G_m^2 - \omega^2 C_m^2)(G_m^2 + \omega^2 C_m^2)C_{r2}}{(\omega^2 C_{r2}^2) [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_{r2})^2} \quad (6.17)$$

$$G_c = \frac{[G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2](G_m^2 + \omega^2 C_m^2)(\omega^2 C_{r2}^2)}{(\omega^2 C_{r2}^2) [G_m(1 - R'_s G_m) - \omega^2 R'_s C_m^2]^2 + (G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_{r2})^2} \quad (6.18)$$

Using **Equation 6.17**, the corrected values  $C_c$  are obtained and are represented in **Figure 6.3**. One can see that after the elimination of  $R_s$ , no frequency dispersion is observed.

### 6.4.3 Fixed Oxide Charge Density ( $Q_f$ )



**Figure 6.5:** Normalized corrected  $C_c$ -V characteristics for different dielectric stacks at 1 kHz after removing series resistance.

**Figure 6.5** shows the corrected  $C_c$ -V curves for different dielectric stacks measured at 1 kHz. From the  $C_c$ -V curves, the density of  $Q_f$  can be calculated as follows:

$$Q_f = \frac{\phi_{MS} - V_{fb}}{C_{ox} \cdot q} \quad (6.19)$$

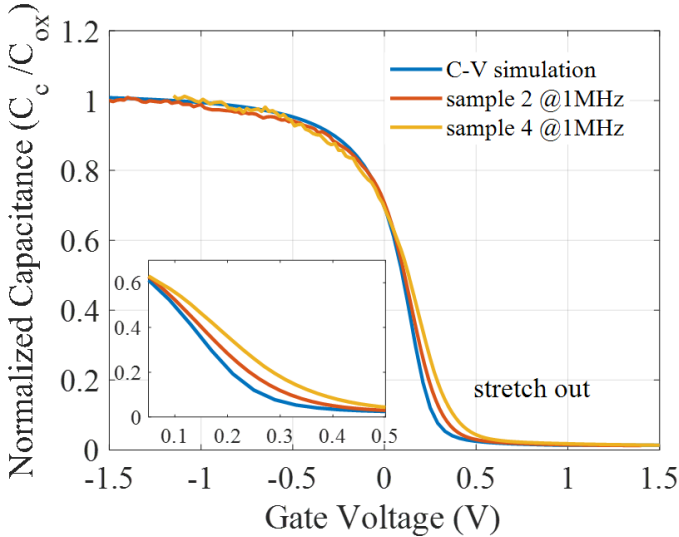
where  $\phi_{MS}$  is the work function difference between mercury and silicon (0.435 V),  $C_{ox}$  is the total gate dielectric capacitance including  $Al_2O_3$  and  $SiO_2$ ,  $V_{fb}$  is the flatband voltage, and  $q$  is the electron charge ( $1.6 \times 10^{-19}$  C).

For instance, for sample 2,  $C_{ox} = 7.0 \times 10^{-7}$  A/cm<sup>2</sup>,  $V_{fb} = +0.61$  V, calculated by the second derivative technique [55]. Therefore, we obtain a negative oxide charge ( $Q_f = -4.57 \times 10^{12}$  cm<sup>-2</sup>). **Table 6.3** summarizes  $V_{fb}$  and  $Q_f$  extracted for the four gate stacks and the reference thermal oxide sample (sample 1).

#### 6.4.4 Interface Trap Density ( $D_{\text{it}}$ ) and Energy Gap Position

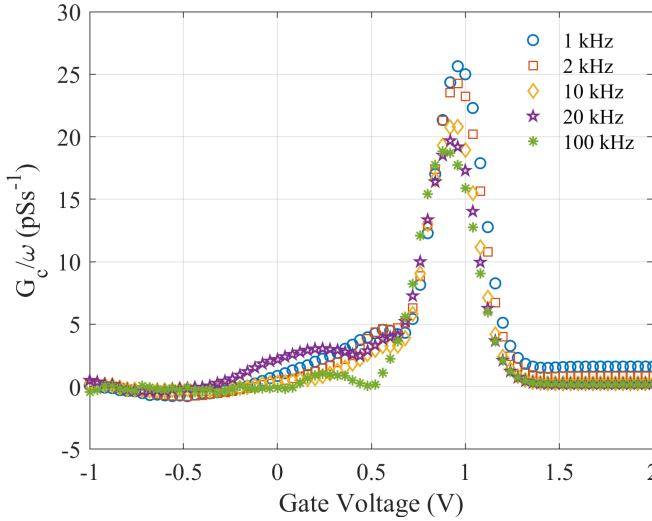
##### Interface Trap Density Extraction: Terman Method

**Figure 6.6** shows the corrected  $C_c$ -V characteristics after subtracting  $V_{\text{fb}}$  at 1 MHz for samples 2 and 4. The ideal C-V curve simulated by Silvaco software (with zero  $V_{\text{fb}}$  and  $D_{\text{it}}$ ) is also shown. A stretch-out in the depletion region is observed. This is due to the fact that carriers captured and emitted in the interface traps follow slowly varying DC voltage, rather than high-frequency excitation. Based on the Terman method [50],  $D_{\text{it}}$  are extracted to be about  $5.60 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  and  $2.82 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  by comparing the measured and simulated C-V curves for samples 2 and 4. The small and large stretch-outs imply the lowest and highest  $D_{\text{it}}$  of samples 2 and 4, respectively.



**Figure 6.6:** Corrected (red and orange) and simulated (blue)  $C_c$ -V characteristics after subtracting  $V_{\text{fb}}$  at 1 MHz for samples 2 and 4, in which the inset shows the stretch-out in the depletion region due to the existence of  $D_{\text{it}}$ .

### Interface Trap Density Extraction: Conductance Method



**Figure 6.7:** Corrected  $G_c$ -V characteristics for sample 2 at different frequencies, in which  $D_{it}$  can be extracted by using the conduction method.

The conductance method aims at probing the variation of occupancy of interface trap levels located in the Si bandgap around the Fermi level, following the variation of gate voltage. The capture and emission of majority carriers by interface traps cause an energy loss mechanism observed at all the frequencies except at the lowest frequencies (no energy loss occurs) and at the highest frequencies (no interface traps response occurs). This energy loss is measured as an equivalent parallel conductance  $G_p$  (in our work) as a function of frequency.  $G_c$  can be extracted from  $G_c$  and calculated as follows [49]:

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_c}{G_c^2 + \omega^2 (C_{ox} + C_c)^2} \quad (6.20)$$

An approximate expression giving the interface trap density in terms of the measured maximum conductance is [49], [50]:

$$D_{it} \approx \frac{2.49}{qA} \cdot \left( \frac{G_p}{\omega} \right)_{\max} \quad (6.21)$$

where  $\omega = 2\pi f$ ,  $q = 1.6 \times 10^{-19} \text{ C}$ , and the mercury probe contact area  $A = 0.0065 \text{ cm}^2$ . **Figure 6.7** represents corrected  $G_c/\omega$  as a function of gate voltage using the conductance method for sample 2 measured at different frequencies. According to the highest peak of  $G_p/\omega$  as a function of  $\omega$ , we can calculate  $D_{it}$  by **Equation 6.21**. The derivation of the constant value 2.49 can be found in **Appendices Section A**.

For sample 2,  $D_{it}$  being equal to  $5.2 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  indicates a low interface trap density ( $C_{it} = qD_{it} \ll C_{ox}$ ) [77]. For other samples, values are reported in **Table 6.3**. It is worth pointing out that the values extracted by the conductance method agree well with the values extracted by the Terman method.

### Time Constant and Energy Gap Position

The energy distribution of the interface traps in the bandgap  $D_{it}$  ( $\Delta E = E_T - E_V$ ) profile is an important input for calibrating TCAD simulation. The first step in obtaining this profile is to quantitatively extract the interface trap response on the DUT, which  $D_{it}$  approximates via **Equation 6.21**.

The second step is to determine the energy position of the interface traps. The accessible trap energy can be calculated for any temperature and frequency according to Shockley-Read-Hall statistics of the capture and emission rate [51]:

$$\tau = \frac{1}{\omega} = \frac{\exp\left(\frac{\Delta E}{kT}\right)}{\sigma v_t N_V} \quad (6.22)$$

where  $\tau$  is the time constant of the interface trap,  $v_t$  is the average thermal velocity,  $\sigma$  is the capture cross-section,  $N_V$  is the density of states in the valence band,  $k$  is the Boltzmann constant, and  $\Delta E$  ( $\Delta E = E_T - E_V$ ) is the energy difference between the trap energy level ( $E_T$ ) and the top of the Si valence band ( $E_V$ ) in p-type Si.  $\Delta E$  can be calculated using **Equation 6.22** from the angular frequency  $\omega$  corresponding to the peak of the  $G_p/\omega$  vs.  $\omega$  curve.

**Table 6.2:** Summary of thermal velocity and density of states at different temperatures.

| Temperature (°C) | $v_t$ (cm/s)       | $N_v$ (cm <sup>3</sup> ) |
|------------------|--------------------|--------------------------|
| 25               | $1.95 \times 10^7$ | $3.10 \times 10^{19}$    |
| 50               | $2.02 \times 10^7$ | $3.59 \times 10^{19}$    |
| 75               | $2.10 \times 10^7$ | $4.13 \times 10^{19}$    |
| 100              | $2.17 \times 10^7$ | $4.69 \times 10^{19}$    |
| 125              | $2.24 \times 10^7$ | $5.30 \times 10^{19}$    |
| 150              | $2.31 \times 10^7$ | $6.02 \times 10^{19}$    |

**Table 6.2** summarizes the thermal velocity and density of states at different temperatures. The thermal velocity,  $v_t$ , is given by:

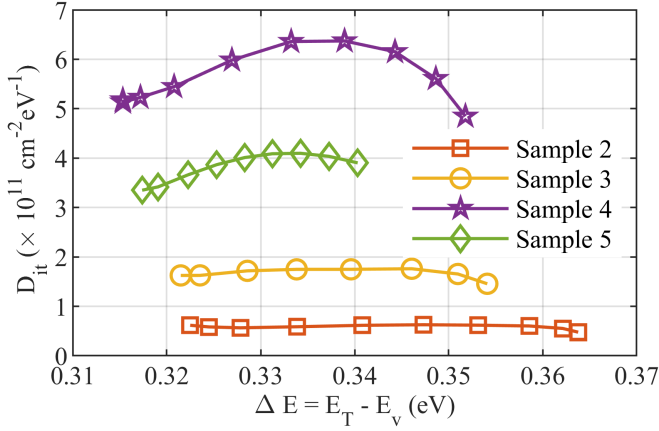
$$v_t = \sqrt{\frac{3kT}{m^*}}, \quad (6.23)$$

where  $m^*$  ( $0.36 m_0$ ) is the transport effective mass for holes. The density of states,  $N_v$ , is given by:

$$N_v = 2 \left( \frac{2\pi m_{dv}^* kT}{h^2} \right)^{3/2}, \quad (6.24)$$

where  $m_{dv}^*$  is the density-of-states effective mass in the valence bands in silicon [52]. **Table 6.2** presents the average thermal velocity,  $v_t$ , and density of states,  $N_v$ , for the calculation of trap response time  $\tau$  under different temperatures.

**$D_{it}$  ( $\Delta E = E_T - E_V$ ) At Room Temperature**



**Figure 6.8:** The  $D_{it}$  ( $\Delta E = E_T - E_v$ ) profile of four dielectric stacks was calculated by combining Equation 6.21 and Equation 6.22 in the text, showing that  $D_{it}$  is distributed in the energy band of the Si.

By combining Equation 6.21 and Equation 6.22, we obtain the  $D_{it}(\Delta E = E_T - E_v)$  profile for DUT as shown in Figure 6.8. Figure 6.8 show the  $D_{it}$  as a function of the silicon bandgap energy with respect to the valence band edge at room temperature for four dielectric stacks. At room temperature, the trap energy states distribute in the band from 0.315 eV to 0.364 eV above the top of the Si valence band for four stacks. Moreover, the maximal trap densities of  $6.37 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  and  $4.09 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  for samples 4 and 5, respectively, appear at the energy levels of 0.339 eV and 0.334 eV.

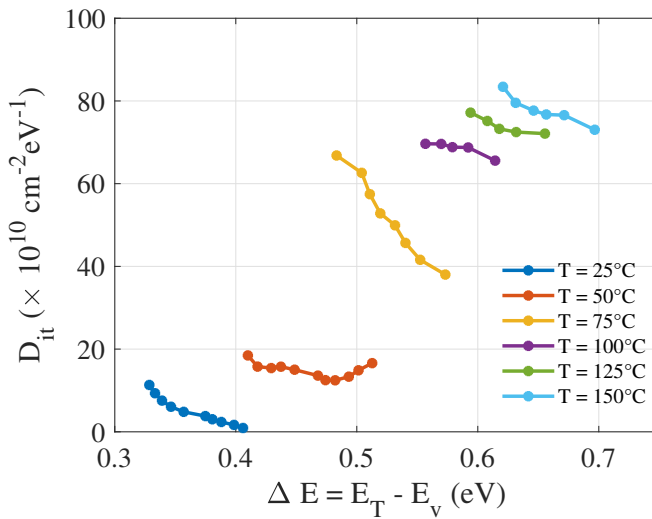
In order to reduce the interface trap density, the difference of the interface trap properties at the interface between the gate stack  $\text{Al}_2\text{O}_3/\text{SiO}_2$  and  $\text{SiO}_2/\text{Si}$  was compared according to the fabrication methods. In the case of  $\text{Al}_2\text{O}_3$  directly deposited on Si, the lattice mismatch causes interface traps, and thus an interfacial  $\text{SiO}_2$  layer is introduced to reduce the mismatch and improve the interface characteristics. We compared two kinds of technologies for forming the ultrathin  $\text{SiO}_2$  layer sandwiched between the  $\text{Al}_2\text{O}_3$  and the Si substrate. One is thermal oxidation and the other is plasma-enhanced atomic layer deposition (PE-ALD). For samples 2 and 3 in Table 6.3, the Si wafers were placed into a Koyo thermal system to form a thermal  $\text{SiO}_2$  layer of 2 nm at 900 °C in an ultra-dry oxygen atmosphere. These are attributed to a low  $D_{it}$  value. Indeed, in Table 6.3, samples 2 and 3 have  $D_{it}$  values of about  $5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ , which



are an order of magnitude lower than those of samples 4 and 5. The results of **Figure 6.8** are consistent with **Table 6.3**. They suggest that in the case of PE-ALD  $\text{SiO}_2$  (as in samples 4 and 5) the surfaces of the Si wafers may be damaged by the plasma in the pretreatment step of PE-ALD. Conversely, in the case of thermal  $\text{SiO}_2$  (as in samples 2 and 3), the  $D_{it}$  value is low thanks to the good bonding properties of the thermal  $\text{SiO}_2$  formed by oxidizing the Si substrate.

#### $D_{it}(\Delta E = E_T - E_V)$ At Different Temperatures

By combining **Equation 6.21** and **Equation 6.22**, we obtain the  $D_{it}(\Delta E = E_T - E_V)$  profile for DUT as shown in **Figure 6.9**. **Figure 6.9** show the  $D_{it}$  as a function of the silicon bandgap energy with respect to the valence band edge at different temperatures. At room temperature, the trap energy states can only be measured in the narrow range of energy bandgap from 0.32 to 0.50 eV above the top of the Si valence band. To probe  $D_{it}$  across a larger energy range in the Si bandgap, temperatures from 25 to 150 °C were considered. The conductance method is used at each temperature to draw a  $D_{it}(E)$  profile.



**Figure 6.9:**  $D_{it}(\Delta E = E_T - E_V)$  profile under elevated temperature on DUT showing the temperature dependence of  $D_{it}$  energy distribution.

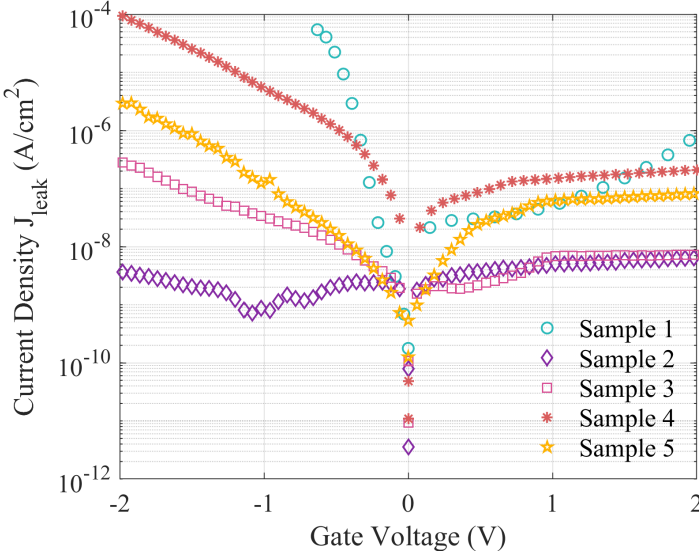
$D_{it}(\Delta E = E_T - E_V)$  distributions of DUT extracted for 25, 50, 75, 100, 125,

and 150 °C at 1 kHz cover the silicon bandgap from 0.32 to 0.73 eV, as shown in **Figure 6.9**. The increasing trend of  $D_{it}$  with elevated temperatures shows that the higher temperature increases the capture/emission rate ( $= 1/\tau$ ) of interface traps corresponding to AC frequency. There are more traps responding at high temperatures, thus the total  $D_{it}$  appears increased. The latter effect drives hole capture and determines higher energy loss—the peak of  $G_p$  as a function of frequency  $(G_p/\omega)_{\max}$  is related to  $D_{it}$  [49].

**Table 6.3:** Comparison of High-*k* Candidates and Conventional SiO<sub>2</sub>

| Sample Number | Materials                                                           | $C_{\text{ox}}$<br>(F/cm <sup>2</sup> ) | $V_{\text{fb}}$<br>(V) | $Q_{\text{f}}$<br>(cm <sup>-2</sup> ) | $D_{\text{it}}$ (cm <sup>-2</sup> eV <sup>-1</sup> )<br>(Terman method) | $D_{\text{it}}$ (cm <sup>-2</sup> eV <sup>-1</sup> )<br>(Conductance method) |
|---------------|---------------------------------------------------------------------|-----------------------------------------|------------------------|---------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|
| 1             | SiO <sub>2</sub>                                                    | $1.0 \times 10^{-6}$                    | -0.72                  | $+1.89 \times 10^{12}$                | $2.31 \times 10^{10}$                                                   | $2.00 \times 10^{10}$                                                        |
| 2             | PE-ALD Al <sub>2</sub> O <sub>3</sub> /<br>thermal SiO <sub>2</sub> | $7.0 \times 10^{-7}$                    | +0.61                  | $-4.57 \times 10^{12}$                | $5.60 \times 10^{10}$                                                   | $5.20 \times 10^{10}$                                                        |
| 3             | T-ALD Al <sub>2</sub> O <sub>3</sub> /<br>thermal SiO <sub>2</sub>  | $6.9 \times 10^{-7}$                    | +0.69                  | $-4.92 \times 10^{12}$                | $6.86 \times 10^{10}$                                                   | $6.21 \times 10^{10}$                                                        |
| 4             | PE-ALD Al <sub>2</sub> O <sub>3</sub> /<br>PE-ALD SiO <sub>2</sub>  | $6.0 \times 10^{-7}$                    | -0.06                  | $-1.45 \times 10^{12}$                | $2.82 \times 10^{11}$                                                   | $2.61 \times 10^{11}$                                                        |
| 5             | T-ALD Al <sub>2</sub> O <sub>3</sub> /<br>PE-ALD SiO <sub>2</sub>   | $6.2 \times 10^{-7}$                    | +0.31                  | $-2.79 \times 10^{12}$                | $1.95 \times 10^{11}$                                                   | $1.88 \times 10^{11}$                                                        |

## 6.5 Current-Voltage Characterizations



**Figure 6.10:** Leakage current density vs gate voltage for four dielectric stacks and a single-layer  $\text{SiO}_2$  dielectric (sample 1) with the similar EOT.

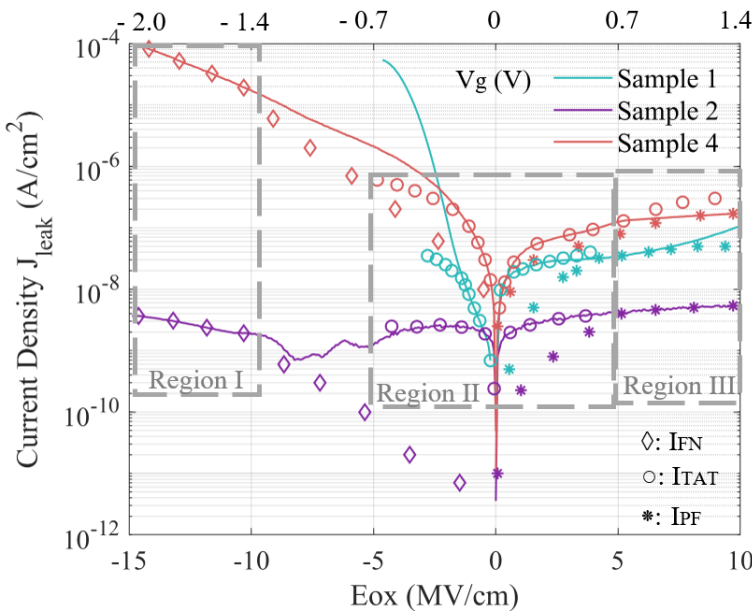
**Figure 6.10** presents the leakage current density ( $J_{\text{leak}}$ ) through the gate stack as a function of gate voltage for the different dielectric stacks and single-layer  $\text{SiO}_2$  counterpart dielectric, measured at room temperature. It can be seen that  $J_{\text{leak}}$  of the dielectric stacks is several orders of magnitude lower than that through the single-layer  $\text{SiO}_2$  dielectric with similar EOT. Particularly, the PE-ALD  $\text{Al}_2\text{O}_3/\text{thermal SiO}_2$  stack (sample 2) has the lowest leakage current.

As shown in the figure,  $J_{\text{leak}}$  is not symmetric for positive and negative  $V_g$ . This phenomenon is caused by different transport mechanisms for the type and number of carriers. The leakage current through the dielectrics may be caused by different mechanisms [78]. **Table 6.4** lists the main mechanisms in our case, namely Poole-Frenkel (PF) emission, trap-assisted tunneling (TAT), and Fowler-Nordheim tunneling (FN).

In **Table 6.4**,  $J$  is the current density,  $E_{\text{ox}}$  is the electric field calculated as follows:

$$E_{\text{ox}} = \frac{V_g - V_{\text{fb}}}{t_{\text{SiO}_2}} \left( \frac{\epsilon_{\text{SiO}_2} t_{\text{Al}_2\text{O}_3}}{\epsilon_{\text{Al}_2\text{O}_3} t_{\text{SiO}_2}} + 1 \right)^{-1} \quad (6.25)$$

$\beta$  is the Poole-Frenkel constant ( $\beta/kT = 0.01486$ ),  $A_{\text{PF}}$  is a proportionality constant varying from  $1.3 \times 10^{13}$  to  $4 \times 10^{13}$  [79],  $A_{\text{TAT}}$  is a technology constant from  $1 \times 10^6$  to  $1 \times 10^5$  in agreement with experimental data.  $m_{\text{ox}}$  is the electron effective mass in  $\text{Al}_2\text{O}_3$  ( $0.28m_0$ ) [80],  $q\phi_T$  is the energy position of the electron traps with respect to the conduction band edge of the dielectric in the range of 1.2–3 eV,  $\phi_B$  is the barrier height from 3.85 to 4.6 eV between the dielectric and silicon [81],  $k$  is Boltzmann's constant,  $T$  is the absolute temperature, and  $h$  is Planck's constant.



**Figure 6.11:** Different components of the total leakage current (lines for measurements and symbols for FN, TAT and PF models) as a function of  $E_{\text{ox}}$  (bottom axis) and  $V_g$  (top axis) for samples 1, 2 and 4. Samples 3 and 5 are not plotted as they show similar trends to samples 2 and 4, resp.

**Figure 6.11** shows different current components (as a function of  $E_{\text{ox}}$  and  $V_g$ ) contributing to the total leakage current  $J_{\text{leak}}$  for the MOS capacitors of

samples 1, 2, and 4. As shown in **Figure 6.10**, the curves of samples 2 and 3 show similar trends, whereas samples 4 and 5 behave differently. To make the plot clear, we do not plot the current of samples 3 and 5 here. The leakage mechanisms in different regions are analyzed hereafter.

**Region I (Fowler-Nordheim tunneling):** The leakage is observed to increase rapidly with increased bias. It is suggested that FN tunneling is prominent in the higher voltage range of  $-2\text{ V} < V_g < -1.4\text{ V}$  for samples 2, 3, 4, and 5. Sample 1 featured very high currents already at  $-0.7\text{ V}$ , so that compliance was triggered, and we could not analyze this sample at very negative biases. FN mechanism is a one-step process: when a higher negative voltage is applied to the metal with respect to the substrate, electrons directly tunnel from the interface of metal and dielectric into the conduction band of silicon, through an approximately triangular potential barrier.

**Region II (Trap-assisted tunneling):** TAT current dominates the measured data in the range of  $-0.7\text{ V} < V_g < 0.7\text{ V}$  for all samples. Instead of one-step FN tunneling through the potential barrier directly, the electron transport process of TAT tunneling considers that electrons first tunnel into the traps in the dielectric from silicon or metal, and subsequently tunnel into metal or silicon under a low bias. The presence of traps inside the dielectric splits the energy barrier in several parts, thus allowing the consecutive tunneling through thinner energy barriers, thereby increasing the tunneling probability.

**Region III (Poole-Frenkel emission):** The PF current yields a fair agreement with the measurement data for the region of  $0.7\text{ V} < V_g < 1.4\text{ V}$ . It is shown that the leakage mechanism follows PF emission in this region for all samples. Therefore, the PF transport process considers that electrons are emitted from traps into the conduction band of the dielectric stack by the PF mechanism and flow from the dielectric across the metal-dielectric interface into the metal with a higher bias than TAT. The three leakage currents appear in all  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks. The results indicate that the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks are less leaky than the single-layer  $\text{SiO}_2$ , and that the deposition conditions of the thin  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks are important. As long as the deposition process is well

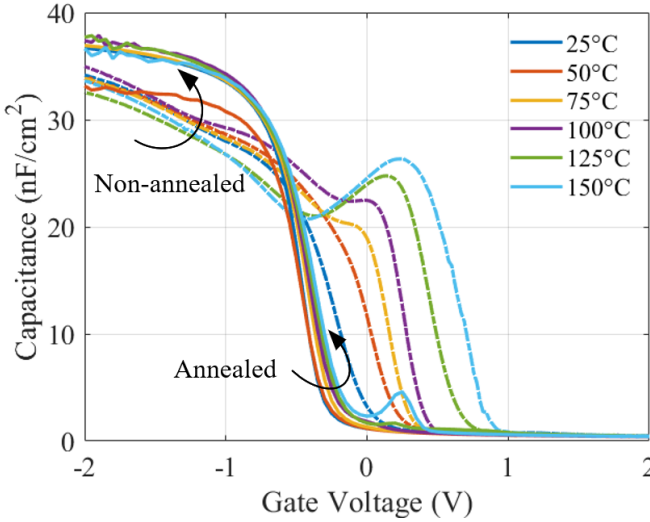
optimized, the Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stack could be a good candidate to replace SiO<sub>2</sub> in CMOS applications beyond the 65 nm node.

**Table 6.4:** Summary of Leakage Current Mechanisms and Their Expressions

| Mechanism                      | Expression                                                                                                    | E-field Dependence                               |
|--------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------|
| Poole-Frenkel [35], [77], [79] | $J = A_{PF} E_{ox} \exp \left( \frac{q \phi_T}{\beta \sqrt{E_{ox}} 2kT} \right)$                              | $\ln \left( \frac{J}{E} \right) \propto E^{1/2}$ |
| Trap-assisted tunneling [79]   | $J = A_{TAT} \exp \left( \frac{8\pi \sqrt{2q m_{ox}}}{3h E_{ox}} \phi_T^{3/2} \right)$                        | $\ln(J) \propto E$                               |
| Fowler-Nordheim [82]           | $J = \frac{q^3}{8\pi h \phi_B} E_{ox}^2 \exp \left( -\frac{8\sqrt{2m_{ox}}}{3hq E_{ox}} \phi_B^{3/2} \right)$ | $\ln \left( \frac{J}{E^2} \right) \propto E$     |

## 6.6 Optimization of Dielectric Stacks

### 6.6.1 Influence of $\text{N}_2$ and $\text{H}_2$ Anneal



**Figure 6.12:** Corrected capacitance versus gate voltage at 1 kHz under different temperatures (from 25 °C to 150 °C) for non-annealed (in dotted lines) and forming gas annealed (in solid lines) sample with dielectric stack PE-ALD  $\text{Al}_2\text{O}_3$ /PE-ALD  $\text{SiO}_2$  (sample 3 in Table 6.3).

Figure 6.12 shows the temperature effect on dispersions due to interface traps, especially observed on non-annealed (NA) sample with dielectric stack PE-ALD  $\text{Al}_2\text{O}_3$ /PE-ALD  $\text{SiO}_2$  (sample 3 in Table 6.3). Without the annealing treatment, the humps on C-V curves caused by interface traps largely increase at higher temperatures. Besides, a shift of the C-V curves towards positive bias is clearly shown on the lower part of the C-V curves close to the mid-gap voltage on NA sample 3. This is due to oxide traps, including higher electron trapping induced by elevated temperatures and negative fixed charges [68]. It is ascribed to post-annealing that the interface traps hump disappears for the C-V curves of forming gas annealing (FGA) sample 3 and the lateral shift towards positive bias decreases. This means that FGA can significantly reduce  $D_{it}$  in addition to the reduction of effective negative charge trapping in the dielectric stacks.



### 6.6.2 The Comparison and Optimization

**Table 6.3** summarizes the  $V_{fb}$ ,  $Q_f$ ,  $D_{it}$  and  $J_{leak}$  for the four  $Al_2O_3/SiO_2$  samples and  $SiO_2$  reference sample. The PE-ALD  $Al_2O_3$ /thermal  $SiO_2$  and T-ALD  $Al_2O_3$ /thermal  $SiO_2$  samples show higher negative fixed oxide charge density, compared with the PE-ALD  $Al_2O_3$ /PE-ALD  $SiO_2$  and T-ALD  $Al_2O_3$ /PE-ALD  $SiO_2$  samples. The high negative  $Q_f$  would cause a positive shift of the  $V_{th}$  in an n-MOSFET as follows [83]:

$$V_{th} = \phi_{ms} - \frac{Q_f}{C_{ox}} + V_{it} + 2\phi_F + \sqrt{\frac{4q\epsilon_{si}N_a\phi_F}{C_{ox}}} \quad (6.26)$$

$V_{th}$  can then be tuned to its desired (or target) value by changing the channel doping concentration  $N_a$ . When  $Q_f$  is negative,  $V_{th}$  increases. Lowering  $N_a$  can compensate for the increase of  $V_{th}$ . Simultaneously, low  $N_a$  is beneficial for the enhancement of the electron mobility [84] and reduction of the variability.

Next to that, we can see that the  $D_{it}$  values calculated by Terman and Conductance methods are rather similar. This confirms the reliability of our extracted results. Moreover, the  $D_{it}$  values in the PE-ALD  $Al_2O_3$ /thermal  $SiO_2$  and T-ALD  $Al_2O_3$ /thermal  $SiO_2$  samples are 2 to 3 times lower than in the PE-ALD  $Al_2O_3$ /PE-ALD  $SiO_2$  and T-ALD  $Al_2O_3$ /PE-ALD  $SiO_2$  samples. This indicates that the thermal  $SiO_2$  is required as the interfacial layer for improving the interface quality of the gate stack. The reason may be due to the fact that plasma slightly damages the silicon surface, which creates more interface traps. It was reported [71] that the  $D_{it}$  ideal value is  $\sim 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  for advanced MOSFETs, but a value of  $\sim 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , giving the interface trap capacitance  $C_{it} = qD_{it}$ , to be much lower than  $C_{ox}$  is acceptable for thin oxides. In our case, the  $C_{it}$  of all dielectric stacks is one to two orders of magnitude lower than  $C_{ox}$ . When the  $D_{it}$  value becomes much larger than this value, the subthreshold slope and the mobility of the channel carriers degrade. In this case, the high- $k$  dielectric materials will lose their benefits.

The ALD  $Al_2O_3$ /thermal  $SiO_2$  samples present low leakage current of  $5 - 7 \times 10^{-9} \text{ A/cm}^2$  (at  $V_g = 1 \text{ V}$ ), about an order of magnitude lower than the  $SiO_2$  reference sample, while the PE-ALD  $SiO_2$  samples lie above the ALD  $Al_2O_3$ /thermal  $SiO_2$  ones (but still lower than reference  $SiO_2$ ). This correlates with our conclusion on the best stack from the interface quality point of view and appears related to the interface traps that play a crucial role in the leakage current (PF and TAT) of the stacks. The improvement of the leakage current

can then be achieved by proper choice of deposition methods or post-annealing of the dielectric stack to reduce the interface trap density [85].

According to the literature survey, we summarize in **Table 6.5** the published important parameters of conventional  $\text{SiO}_2$  layer and high- $k$  dielectric stacks we could find with an EOT close to 3 nm. To ease the comparison, our best sample is also cited in the table. Among all the stacks in the table, our stack (PE-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$ ) presents the lowest  $D_{\text{it}}$ , highest negative  $Q_{\text{f}}$ , and lowest leakage current density at 1 V. Low  $D_{\text{it}}$  value does not only decrease the trap-assisted tunneling current but also prevents the degradation of the carrier mobility and subthreshold slope as well as reliability issues in MOSFETs. A high negative  $Q_{\text{f}}$  value allows a lower doping concentration of channel to increase the carrier mobility and reduce variability at constant  $V_{\text{th}}$ . The low  $J_{\text{leak}}$  assures a good insulator property and lower power consumption. Although the dielectric constant of  $\text{Al}_2\text{O}_3$  is lower than  $\text{HfO}_2$  and  $\text{ZrO}_2$  and similar to  $\text{SiO}_x\text{N}_y$ , the stack of PE-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  shows overall better dielectric properties than the other stacks for our targeted thickness. Our result reveals that the ultra-thin, high-quality  $\text{SiO}_2$  interfacial layer plays a crucial role in the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack. Therefore,  $\text{Al}_2\text{O}_3$  could be a trade-off between  $\text{SiO}_2$  and the high- $k$  dielectric materials with relative dielectric constants larger than 10 (larger band gap) [84].

Table 6.5: Comparison of SiO<sub>2</sub>, SiO<sub>x</sub>N<sub>y</sub>, and high-*k* dielectric stacks

| Materials                                                   | T <sub>ox</sub> (nm) | Dielectric Constant <i>k</i> | Q <sub>T</sub> (cm <sup>-2</sup> ) | D <sub>it</sub> (cm <sup>-2</sup> eV <sup>-1</sup> ) | J <sub>leak</sub> (A/cm <sup>2</sup> ) | Technology Node | References             |
|-------------------------------------------------------------|----------------------|------------------------------|------------------------------------|------------------------------------------------------|----------------------------------------|-----------------|------------------------|
| SiO <sub>2</sub>                                            | 2.9                  | 3.9                          | + 1.00 × 10 <sup>12</sup>          | 2.00 × 10 <sup>10</sup>                              | 10 <sup>-5</sup> @ 1 V                 | 180 nm          | [75]                   |
| SiO <sub>x</sub> N <sub>y</sub> /SiO <sub>2</sub>           | 2.0                  | 7.0                          | + 6.21 × 10 <sup>11</sup>          | 7.00 × 10 <sup>11</sup>                              | 10 <sup>-6</sup> @ 1 V                 | >45 nm          | [71], [86]             |
| HfO <sub>2</sub> /SiO <sub>2</sub>                          | 1.7                  | 20                           | - 1.80 × 10 <sup>12</sup>          | 5.21 × 10 <sup>12</sup>                              | 8.95 × 10 <sup>-7</sup> @ 1 V          | < 28 nm         | [78], [87], [88], [89] |
| ZrO <sub>2</sub> /SiO <sub>2</sub>                          | 1.3                  | 25.0                         | - 2.51 × 10 <sup>12</sup>          | 3.00 × 10 <sup>11</sup>                              | 1.00 × 10 <sup>-5</sup> @ -1 V         | < 20 nm (DRAM)  | [75], [90], [91], [92] |
| Al <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> (sample 2) | 4.9                  | 9                            | - 4.57 × 10 <sup>12</sup>          | 5.20 × 10 <sup>10</sup>                              | 5.06 × 10 <sup>-9</sup> @ 1 V          | ≥ 65 nm         | This work              |

## 6.7 Carrier Lifetime

$\text{Al}_2\text{O}_3$  material has been explored for many applications, including surface passivation in photovoltaics and photodetectors, gate dielectric in downscaling MOSFETs, etc.  $\text{Al}_2\text{O}_3$  provides good passivation qualities for silicon. The negative fixed charges in  $\text{Al}_2\text{O}_3$  induce an accumulation layer at the Si interface for p-type Si solar cells, shielding surface recombination and thereby increasing efficiency [73]. Recent works [93] have also demonstrated that  $\text{Al}_2\text{O}_3$  is well suited for the field-effect passivation of n-type silicon substrate. It was proven [94] that an  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack shows better performance than each material used individually. Particularly, the interfacial defect density was shown to be lower in the stack than in the  $\text{SiO}_2/\text{Si}$  case. The  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks produce very low surface recombination velocities (SRV) of less than 2 cm/s, and the fixed charge density can be tuned with the  $\text{SiO}_2$  layer thickness.

In the field of photodetectors, the surface recombination velocity and fixed charge density dominate the reverse leakage behavior of the photodiode [84]. Passivation of device surfaces is very important to achieve high performance in photodiodes.  $\text{Al}_2\text{O}_3$  also has interesting antireflection properties. The  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack should then be one of the considered candidates, especially for lateral photodiodes.

$\text{SiO}_2$  is commonly used as the gate dielectric material in MOSFETs. With the scaling of the gate dielectric thickness down to the 1–2 nm range, a single layer of  $\text{SiO}_2$  faces many issues such as high gate leakage current, standby power consumption, and gate oxide reliability [95]. The quality of the dielectric/Si substrate interface plays an important role in the nano-scaled device behavior and final performance. The carrier lifetime and surface recombination velocity are the main parameters to assess the intrinsic interface and dielectric quality.

$\text{Al}_2\text{O}_3$  appears to be more attractive than other high- $k$  replacements for  $\text{SiO}_2$  due to its abundance, low cost, and compatibility with CMOS technology. However, high trap density formed at the  $\text{Al}_2\text{O}_3/\text{Si}$  substrate increases the interface charge scattering, thereby decreasing the carrier mobility in the transistors' channel [96].

In this section, we investigate the carrier lifetime and surface recombination velocity of the ultra-thin  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks on silicon and compare them with the  $\text{SiO}_2/\text{Si}$  counterpart. To this end, the ultra-thin  $\text{Al}_2\text{O}_3$  was deposited by plasma-enhanced atomic layer deposition (PE-ALD) or thermal atomic layer deposition (T-ALD) on either thermally grown high-quality  $\text{SiO}_2$  films (Samples 1 and 2, see Table 6.6) or PE-ALD  $\text{SiO}_2$  thin films (Samples 3 and 4).

The photoconductance decay (PCD) technique [97] allows for a fast determination of the carrier lifetime without any electrical contact. It includes two operating modes: transient mode and quasi-steady-state mode. The former, with a quick flash of light, is especially suitable for long carrier lifetime cases, while the latter, with a slow decay illumination, is for short carrier lifetimes. In this work, the PCD technique was used to measure the effective carrier lifetimes for the different fabricated dielectric stacks.

**Table 6.6:** Targeted and measured thickness of samples (EOT = 3 nm).

| Sample number    | Dielectric stack                                                   | Targeted<br>thickness (nm) | Measured<br>thickness (nm) |
|------------------|--------------------------------------------------------------------|----------------------------|----------------------------|
| Reference sample | Thermal SiO <sub>2</sub>                                           | 3.0                        | 3.9                        |
| Sample 1         | PE-ALD Al <sub>2</sub> O <sub>3</sub><br>/thermal SiO <sub>2</sub> | 3.0/2.0                    | 2.8/2.5                    |
| Sample 2         | T-ALD Al <sub>2</sub> O <sub>3</sub><br>/thermal SiO <sub>2</sub>  | 3.0/2.0                    | 3.2/2.5                    |
| Sample 3         | PE-ALD Al <sub>2</sub> O <sub>3</sub><br>/PE-ALD SiO <sub>2</sub>  | 3.0/2.0                    | 3.2/2.5                    |
| Sample 4         | T-ALD Al <sub>2</sub> O <sub>3</sub><br>/PE-ALD SiO <sub>2</sub>   | 3.0/2.0                    | 3.5/2.5                    |

\*Measured thickness in nm is the average value of 16 points on one sample.

Sample Description

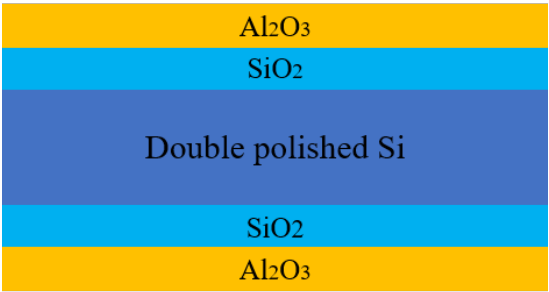
Double side polished silicon wafers (FZ, n-type,  $\langle 100 \rangle$ ,  $1\ \Omega \cdot \text{cm} - 10\ \Omega \cdot \text{cm}$ ) were used as the starting substrates. After the standard RCA cleaning procedures, different dielectric stacks with the same equivalent oxide thickness (EOT) of 3 nm were symmetrically deposited on both sides of silicon wafers.

**Experimental Details**

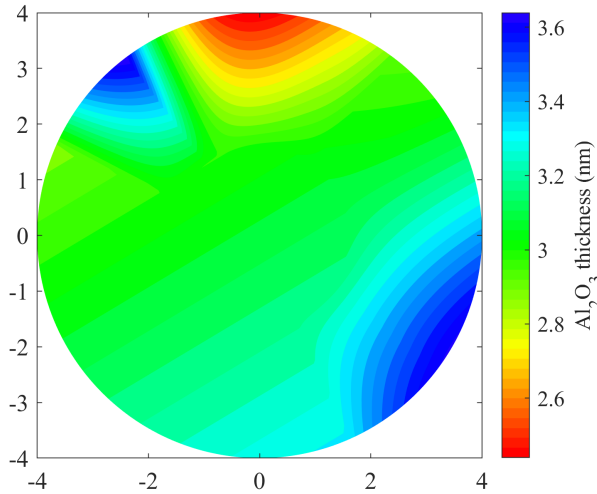
We prepared four types of dielectric stacks as shown in **Table 6.7**. The reference sample with a 3-nm-thick  $\text{SiO}_2$  layer was prepared for comparison purposes. The thermal  $\text{SiO}_2$  thin films were grown at  $900\ ^\circ\text{C}$  in the Koyo thermal system (Reference sample, Samples 1 and 2). The plasma enhanced atomic layer deposition (PE-ALD)  $\text{SiO}_2$  thin films were obtained at  $250\ ^\circ\text{C}$  in Fiji F200 ALD system (Samples 3 and 4). The  $\text{Al}_2\text{O}_3$  thin films were grown either by plasma enhanced atomic layer deposition (PE-ALD) at  $200\ ^\circ\text{C}$  (Samples 1 and 3) or by thermal atomic layer deposition (T-ALD) at  $200\ ^\circ\text{C}$  (Samples 2 and 4). In both cases, Trimethylaluminum (TMA) precursor was used as aluminum source. Oxygen flow and water pulse were used as oxygen sources for PE-ALD and T-ALD, respectively. The growth rate was  $1\ \text{\AA}$  per cycle for both of them. The carrier lifetime measurements were performed by Sinton WCT-120 instrument. We used a white light illumination (the wavelength ranges from 400 to 700 nm), which can totally penetrate the dielectric stacks.

In our measurements of the effective carrier lifetime, both the QSS and transient modes were used. The measurement results obtained from both modes are similar.

**Thickness Uniformity of Ultra-Thin Dielectrics**



**Figure 6.13:** Cross-section of a dielectric stack.

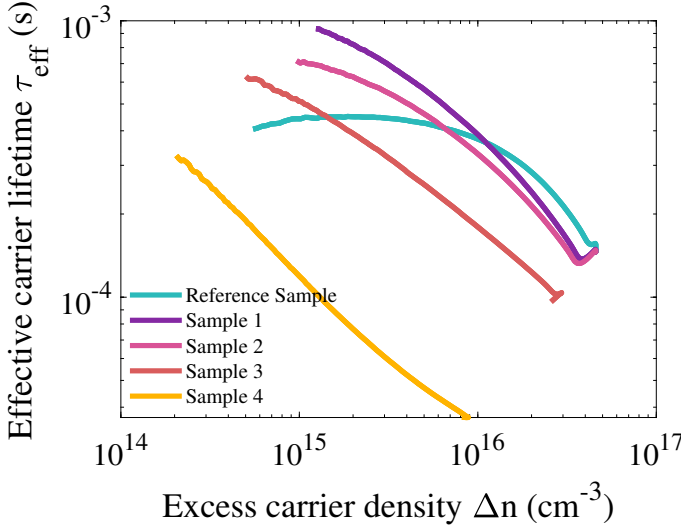


**Figure 6.14:** Thickness distribution of a PE-ALD  $\text{Al}_2\text{O}_3$  layer over a thermal  $\text{SiO}_2$  layer, mapped cyclically by Ellipsometry.

**Figure 6.13** plots the schematic cross-section of an  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack. One of the key issues for depositing the ultra-thin dielectric stacks on silicon is to achieve a reproducible thickness, which guarantees uniformity of device characteristics. In order to examine the thickness uniformity of the dielectric stacks, a 3-inch silicon wafer was mapped cyclically by Ellipsometry. **Figure 6.14** shows the typical thickness distribution of a PE-ALD  $\text{Al}_2\text{O}_3$  layer. The targeted thickness of the  $\text{Al}_2\text{O}_3$  layer is 3 nm, while the measured average thickness is  $2.8 \pm 0.7$  nm. If the edge region of the wafer is ignored, the standard deviation will be reduced. The thickness deviation may be due to the original roughness of the silicon wafer or to edge effects on wafer sides. It is worth noting that the thermal  $\text{SiO}_2$  layer under  $\text{Al}_2\text{O}_3$  is very uniform.

### Measurement of Effective Carrier Lifetime

Nagel et al. [36] developed a generalized model to analyze the relationship between the effective carrier lifetime ( $\tau_{\text{eff}}$ ) and the excess carrier density ( $\Delta n$ )



**Figure 6.15:** Effective carrier lifetime vs. excess carrier density for the silicon samples with the different dielectric stacks of **Table 6.6**, measured by using QSS mode.

by illumination:

$$\tau_{\text{eff}}(\Delta n) = \frac{\Delta n}{G_{\text{bulk}} - \frac{\partial \Delta n}{\partial t}} \quad (6.27)$$

Here  $G_{\text{bulk}}$  is the charge carrier generation rate. In the quasi-steady-state (QSS) case,  $\frac{\partial \Delta n}{\partial t} \approx 0$ , this gives

$$\tau_{\text{eff,QSS}}(\Delta n) = \frac{\Delta n}{G_{\text{bulk}}} \quad (6.28)$$

By considering  $G_{\text{bulk}} = 0$  in the transient (trans) case, **Equation 6.27** can be rewritten as:

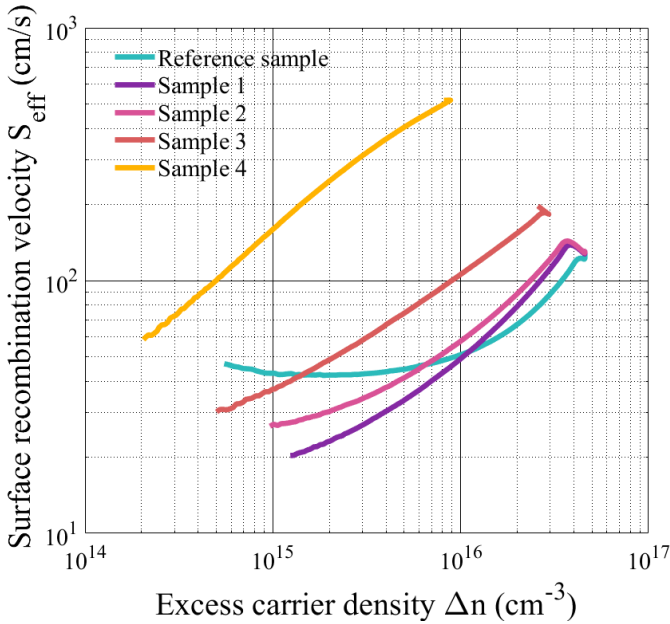
$$\tau_{\text{eff,trans}}(\Delta n) = -\frac{\Delta n}{\frac{\partial \Delta n}{\partial t}} \quad (6.29)$$

The effective carrier lifetime measurements presented below were performed in QSS mode. **Figure 6.15** illustrates the effective carrier lifetime as a function of



the excess carrier density for four samples with different dielectric stacks and the reference sample with only a single SiO<sub>2</sub> layer. **Table 6.7** summarizes the  $\tau_{\text{eff}}$  values of the five cases for the excess carrier density of  $5 \times 10^{15} \text{ cm}^{-3}$ .

### Surface Recombination Velocity



**Figure 6.16:** Calculated effective surface recombination velocity vs. excess carrier density for the silicon samples with different dielectric stacks and the reference sample with only SiO<sub>2</sub> by using QSS mode.

When the effective carrier lifetime ( $\tau_{\text{eff}}$ ) is obtained by the measurement as mentioned above, surface recombination velocity,  $S_{\text{eff}}$  can be calculated using the following equation [37]:

$$S_{\text{eff}} = \frac{W}{2} \left( \frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{bulk}}} \right) \quad (6.30)$$

where  $W$  is the silicon wafer thickness ( $W = 380 \mu\text{m}$  in this work).  $\tau_{\text{bulk}}$  is the bulk carrier lifetime and it can be neglected due to the high quality of the FZ wafer. In this case, **Equation 6.30** can be approximated to:

**Table 6.7:** Effective carrier lifetime ( $\tau_{\text{eff}}$ ) and calculated effective surface recombination ( $S_{\text{eff}}$ ) for different samples, the values from lifetime measurements are taken at  $\Delta n = 5 \times 10^{15} \text{ cm}^{-3}$ .

| Sample number    | Dielectric stack               | $\tau_{\text{eff}} (\mu\text{s})$ for         | $S_{\text{eff}} (\text{cm.s}^{-1})$ |
|------------------|--------------------------------|-----------------------------------------------|-------------------------------------|
|                  |                                | $\Delta n = 5 \times 10^{15} \text{ cm}^{-3}$ |                                     |
| Reference sample | Thermal $\text{SiO}_2$         | 426                                           | 45                                  |
| Sample 1         | PE-ALD $\text{Al}_2\text{O}_3$ | 561                                           | 34                                  |
|                  | /thermal $\text{SiO}_2$        |                                               |                                     |
| Sample 2         | T-ALD $\text{Al}_2\text{O}_3$  | 460                                           | 41                                  |
|                  | /thermal $\text{SiO}_2$        |                                               |                                     |
| Sample 3         | PE-ALD $\text{Al}_2\text{O}_3$ | 254                                           | 75                                  |
|                  | /PE-ALD $\text{SiO}_2$         |                                               |                                     |
| Sample 4         | T-ALD $\text{Al}_2\text{O}_3$  | 47                                            | 402                                 |
|                  | /PE-ALD $\text{SiO}_2$         |                                               |                                     |

$$S_{\text{eff}} \approx \frac{W}{2\tau_{\text{eff}}} \quad (6.31)$$

One should note that as the sample structure is symmetrical (i.e., the dielectric stack was deposited on both sides of the double side polished silicon wafer), the surface recombination velocity is identical for the front and back surfaces ( $S_{\text{front}} = S_{\text{back}} = S_{\text{eff}}$ ). Therefore, hereafter  $S_{\text{eff}}$  refers to the effective surface recombination velocity. **Figure 6.16** plots the  $S_{\text{eff}}$  as a function of  $\tau_{\text{eff}}$  curves for the samples with different dielectric stacks and the reference sample. The  $S_{\text{eff}}$

values are calculated using **Equation 6.31** with the measured  $\tau_{\text{eff}}$  values shown in **Figure 6.15** provides the typical  $S_{\text{eff}}$  values taken at  $\Delta n = 5 \times 10^{15} \text{ cm}^{-3}$ .

In comparison to the PE-ALD  $\text{Al}_2\text{O}_3$ /PE-ALD  $\text{SiO}_2$  and T-ALD  $\text{Al}_2\text{O}_3$ /PE-ALD  $\text{SiO}_2$  samples, the PE-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  and T-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  samples feature lower effective surface recombination velocity and higher effective carrier lifetimes. This could be explained by the fact that plasma makes the silicon surface rough during the PE-ALD  $\text{SiO}_2$  process [98]. In other words, the thermal  $\text{SiO}_2$  layer can protect the silicon surface from damage. Therefore, the deposition method of the ultra-thin interfacial layer  $\text{SiO}_2$  is crucial for the stack fabrication.

From **Figure 6.15** and **Figure 6.16**, we can also see that when  $\Delta n < 1 \times 10^{16} \text{ cm}^{-3}$ , the effective surface recombination velocity is lower in the PE-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  and T-ALD  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  samples than in the reference sample. This indicates that the ultra-thin stack of ALD- $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  shows better field-effect passivation for silicon compared with a single thin  $\text{SiO}_2$  layer. Dingemans et al.[99] fabricated two stacks with different thicknesses of ALD- $\text{Al}_2\text{O}_3$  and thermal  $\text{SiO}_2$ . Stack 1 and Stack 2 were composed of  $\text{Al}_2\text{O}_3/\text{SiO}_2$  (30/1 nm) and  $\text{Al}_2\text{O}_3/\text{SiO}_2$  (5/10 nm), respectively. With injection levels ( $\Delta n$ ) of  $5 \times 10^{14}$  and  $1 \times 10^{14} \text{ cm}^{-3}$ , the surface recombination velocities ( $S_{\text{eff}}$ ) were measured to be about 17 and 3 cm/s for Stack 1 and Stack 2, respectively. Their  $S_{\text{eff}}$  values depend on the choice of the injection level ( $\Delta n$ ). As shown in **Figure 6.16**, if the injection level was extended into  $\Delta n = 1 \times 10^{14} \text{ cm}^{-3}$ , our  $S_{\text{eff}}$  values approach Dingemans's results.

To further increase the effective carrier lifetime and decrease the  $S_{\text{eff}}$  value, we could activate the negative fixed charges in the stacks at an optimized temperature in forming gas or ozone. We also can adjust the  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  thickness. However, the other performance of the ultra-thin stack, such as interface trap state density and leakage current should be further investigated in the future.

## 6.8 Negative Bias Temperature Instability (NBTI) Characterization

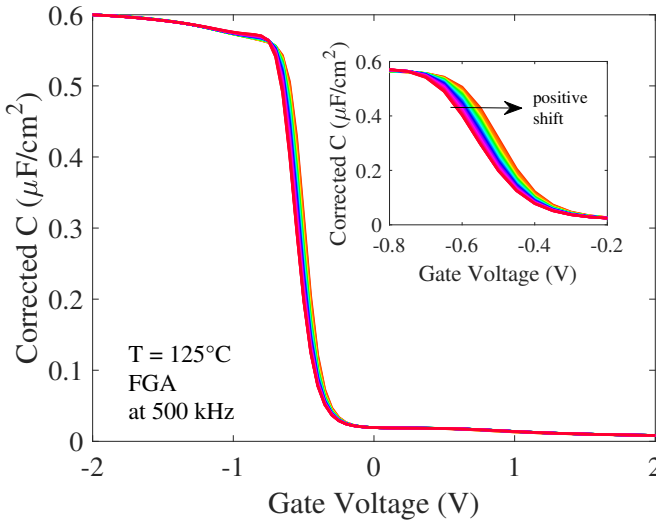
In our previous sections, the investigation of the interface between different thin dielectric  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks and silicon substrates was focused on the interface trap density ( $D_{it}$ ) and energy level distribution in a narrow part of the Si bandgap at room temperature [100].

In this section, p-substrate MOS capacitor with PE-ALD  $\text{Al}_2\text{O}_3$ / thermally-grown  $\text{SiO}_2$  dielectric stack (with a target equivalent oxide thickness of 4.2 nm), named sample 1 in **Table 6.3**, is investigated by means of the conductance method in a temperature range from 25 °C to 150 °C. The trap state density and energy level distribution in the silicon bandgap are extracted over the bandgap. Furthermore, negative bias temperature instability is analyzed by two-point C-V characterization to evaluate the electrical stability and dielectric reliability of the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack. The two main causes of NBTI in  $\text{SiO}_2$  are known to be the generation of Si/ $\text{SiO}_2$  interface traps and the generation of hole traps in the bulk of the oxide. Both of these hole traps contribute to screening of the gate bias from the channel as well as the trapping of minority charge carriers available for conduction in the inversion layer of the channel. The contributions from interface and oxide trap generations will be investigated in the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stack. To get deeper insight into the robustness of the  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stack, we extend to p-substrate, a NBTI measurement method based on MOS capacitor C-V characterization named two-point capacitance–voltage (TPCV) [101]. The details of the procedure can also be found in **Section 3.5**.

### Interface Traps Effect Under High Temperature on $\text{Al}_2\text{O}_3/\text{SiO}_2$

#### NBTI Effect on $\text{Al}_2\text{O}_3/\text{SiO}_2$ Stacks

**Figure 6.17** shows the C-V evolution with stress time obtained on the DUT, under NBTI stress ( $E_{ox} = 4.9$  MV/cm and  $T = 125^\circ\text{C}$ ) at 500 kHz. The C-V curves under stress show a limited positive shift of the flat-band voltage and a stretch-out of the curve. This could be related to the combination of two phenomena: the generation of new defects and the activation of pre-existing defects [102].



**Figure 6.17:** C-V curve shift and stretch-out under NBTI stress at 500 kHz and 125 °C for DUT. The inset represents positive shifts of C-V curves in the depletion regime.

Under stress, electrons injected from the gate electrode, trapping in pre-existing defects of  $\text{Al}_2\text{O}_3$ , may create active defects responsible for the time-dependent drift of electrical characteristics. These are then related to additional apparent oxide charges. The C-V curves become more stretched out over time due to the generation of more interface traps.

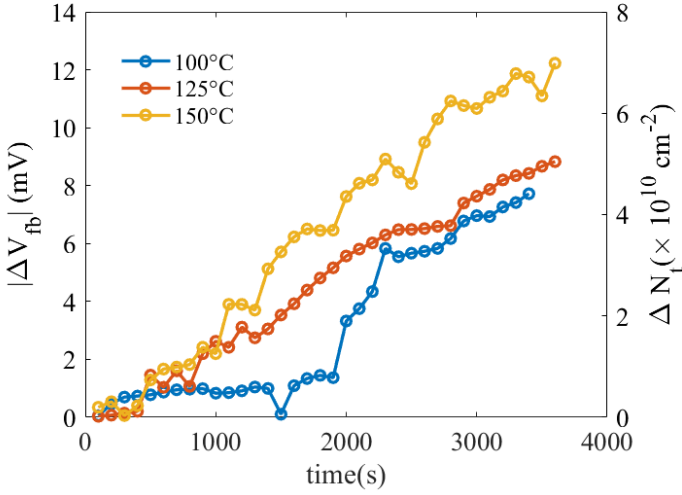
The voltage shift of a MOS capacitor curve can be expressed as the sum of two components induced by the creation of interface traps ( $Q_{it}$ ) and oxide charges ( $Q_{ot}$ ) [103]:

$$\Delta V_{fb} = \Delta V_{ot} + \Delta V_{it}, \quad (6.32)$$

where  $\Delta V_{ot}$  and  $\Delta V_{it}$  relate to the apparent oxide charges and interface traps, respectively, and can be obtained from the TPCV method.  $\Delta V_{ot}$  is calculated as the mid-gap voltage shift ( $\Delta V_{mg}$ ) when the Fermi level is at mid-gap and both acceptor- and donor-like interface traps are neutral. The mid-gap voltage is determined from full capacitance–voltage curves corresponding to the mid-gap capacitance  $C_{mg}$ , given by:

$$C_{\text{mg}} = \frac{C_{\text{dep}}C_{\text{ox}}}{C_{\text{ox}} + C_{\text{dep}}}, \quad (6.33)$$

where  $C_{\text{ox}}$  and  $C_{\text{dep}}$  are the oxide capacitance and the measured capacitance in depletion, respectively.



**Figure 6.18:** Time evolution of  $\Delta V_{\text{fb}}$  in absolute value and trap density  $\Delta N_t$  for different temperatures from 100 to 150 °C at 2 V ( $E_{\text{ox}} = 4.9$  MV/cm) on DUT.

**Figure 6.18** illustrates that the obtained  $\Delta V_{\text{fb}}$  in absolute value and the trap density ( $\Delta N_t$ ) increase as a function of stress time at applied stress  $E_{\text{ox}}$  (4.9 MV/cm) for elevated temperatures from 100 to 150 °C. The increased value of  $\Delta V_{\text{fb}}$  with time indicates the generation of traps at the interface and in the oxide induced by NBTI degradation.

To give insight into the generation and evolution of  $\Delta N_t$  ( $\text{cm}^{-2}$ ), two relations for the p-substrate are used below:

$$\Delta V_{\text{fb}} = \frac{q(\Delta N_{\text{it}} + \Delta N_{\text{ot}})}{C_{\text{ox}}}, \quad (6.34)$$

$$\Delta N_t = \Delta N_{\text{it}} + \Delta N_{\text{ot}}, \quad (6.35)$$

where  $C_{\text{ox}}$  (F/cm<sup>2</sup>) is the gate capacitance per unit area,  $q$  (C) is the electron charge,  $\Delta N_{\text{it}}$  (cm<sup>-2</sup>) is the interface trap density, and  $\Delta N_{\text{ot}}$  (cm<sup>-2</sup>) is the oxide trap density. The increased  $\Delta N_{\text{it}}$  is caused by the generation of interface traps at the SiO<sub>2</sub>/Si interface. Two possible reasons led to the generation of new oxide traps associated with an increased  $\Delta N_{\text{ot}}$  during the stressing of dielectric stacks.

Compared with single SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> in the stack produced by plasma ALD exhibits efficient negative charge trapping resulting from pre-existing oxide traps [104]. Another potential reason could be the occurrence of Al vacancies in the Al<sub>2</sub>O<sub>3</sub> film [72]. To enhance reliability, we need to optimize the thermal budget for ALD deposition [105] and the diffusion of the metal gate electrode to decrease charge trapping.

According to the literature survey, we summarize in Table 6.8, the published important parameters for the conventional SiO<sub>2</sub>, SiO<sub>x</sub>N<sub>y</sub>/SiO<sub>2</sub>, HfO<sub>2</sub>/SiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>/SiO<sub>2</sub> stacks with an EOT close to 4.2 nm. The stress bias we found is close to 2 V at which RS behaviors of RRAM-based RF switches can be observed for further application purpose. Among the stacks compared in the table, our stack (PE-ALD Al<sub>2</sub>O<sub>3</sub>/thermal SiO<sub>2</sub>) presents the lowest  $D_{\text{it}}$ , high  $Q_{\text{f}}$ , lowest leakage current density  $J_{\text{leak}}$  at 1 V, and comparable  $\Delta V_{\text{th}}$  at 125 °C under stress with sustainable material usage. Low  $D_{\text{it}}$  prevents the degradation of channel mobility, subthreshold slope as well as reliability (low  $D_{\text{it}}$  initially) in MOSFETs. A high negative  $Q_{\text{f}}$  value allows a low channel doping concentration at constant  $V_{\text{th}}$  and a reduced oxide electrical field, leading to an improved reliability [106]. The low  $J_{\text{leak}}$  confirms a good insulator property. The  $\Delta V_{\text{th}}$  at a comparable level to other dielectric stacks indicates a sufficient gate stack reliability. The generation of EOT ( $\sim 4.2$  nm) used in our work allows high operating voltage, maintains the reliability and lowers the leakage current. Although the dielectric constant of Al<sub>2</sub>O<sub>3</sub> is lower than HfO<sub>2</sub> and similar to SiO<sub>x</sub>N<sub>y</sub>, the stack shows overall better dielectric properties than the other stacks.

Table 6.8: Comparison of SiO<sub>2</sub>, SiO<sub>x</sub>N<sub>y</sub> and high-*k* dielectric stacks.

| Materials                                              | <i>T</i> <sub>ox</sub> (nm) | Dielectric constant <i>k</i> | Δ <i>V</i> <sub>th</sub> (mV)@125 °C | <i>D</i> <sub>it</sub> (cm <sup>-2</sup> eV <sup>-1</sup> ) | <i>Q</i> <sub>f</sub> (cm <sup>-2</sup> ) | <i>J</i> <sub>leak</sub> (A/cm <sup>2</sup> ) | References         |
|--------------------------------------------------------|-----------------------------|------------------------------|--------------------------------------|-------------------------------------------------------------|-------------------------------------------|-----------------------------------------------|--------------------|
| SiO <sub>2</sub>                                       | 2.2                         | 3.9                          | ~100 (@ -2.5 V)                      | 2.00 × 10 <sup>10</sup>                                     | +1.00 × 10 <sup>12</sup>                  | 10 <sup>-5</sup> @ 1 V                        | [107], [108]       |
| SiO <sub>x</sub> N <sub>y</sub> /SiO <sub>2</sub>      | 2.5                         | 5.0                          | ~100 (@ -2.5 V)                      | 7.00 × 10 <sup>11</sup>                                     | +6.21 × 10 <sup>11</sup>                  | 10 <sup>-6</sup> @ 1 V                        | [108], [109]       |
| HfO <sub>2</sub> /SiO <sub>2</sub>                     | 2.4                         | 20.0                         | ~100 (@ -2.0 V)                      | 5.21 × 10 <sup>12</sup>                                     | -1.80 × 10 <sup>12</sup>                  | 8.95 × 10 <sup>-7</sup> @ 1 V                 | [89], [110]        |
| Al <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub>       | 4.0                         | 9.0                          | ~200 (@ -2.0 V)                      | 1.00 × 10 <sup>11</sup>                                     | -5.00 × 10 <sup>12</sup>                  | 3.88 × 10 <sup>-6</sup> @ 1 V                 | [72], [111], [112] |
| Al <sub>2</sub> O <sub>3</sub> /SiO <sub>2</sub> (DUT) | 4.2                         | 9.0                          | ~10.0 (@ -2.0 V)                     | 5.20 × 10 <sup>10</sup>                                     | -4.57 × 10 <sup>12</sup>                  | 5.06 × 10 <sup>-9</sup> @ 1 V                 | This work, [68]    |



## 6.9 Chapter Summary

This chapter investigated  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stacks in MOS capacitors, aiming to evaluate their suitability for advanced CMOS gate-stack applications. Different fabrication methods were compared to assess the influence of the deposition method and interfacial layer quality on electrical performance.

Electrical characterization was performed using C–V, G–V, and I–V measurements. Key parameters, including equivalent oxide thickness (EOT), series resistance, fixed oxide charge density ( $Q_f$ ), and interface trap density ( $D_{it}$ ), were extracted using established methodologies. The good agreement between the Terman and conductance methods confirms the reliability of the extracted  $D_{it}$  values.

The results demonstrate that stacks with a thermal  $\text{SiO}_2$  interfacial layer exhibit improved interface quality, with  $D_{it}$  reduced by a factor of two to three compared to stacks using plasma-deposited  $\text{SiO}_2$ . Furthermore,  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  stacks exhibit a high negative fixed charge density, which enables threshold voltage tuning while allowing lower channel doping concentrations, thereby improving carrier mobility and reducing variability. In addition, these stacks show low leakage current densities, approximately one order of magnitude lower than the  $\text{SiO}_2$  reference, reflecting the strong impact of interface traps on leakage mechanisms.

Comparison with literature data indicates that the optimized  $\text{Al}_2\text{O}_3$ /thermal  $\text{SiO}_2$  stack offers a favorable trade-off between interface quality, fixed charge, and leakage current at an EOT of about 3 nm. Overall, this chapter highlights the critical role of a high-quality  $\text{SiO}_2$  interfacial layer and identifies  $\text{Al}_2\text{O}_3/\text{SiO}_2$  as a competitive gate-stack solution for advanced MOS technologies.





## 7. Conclusion and Perspectives

### Conclusion

#### *Summary*

This thesis investigated interface traps in MOS capacitors with a particular focus on their characterization, physical role, and technological impact in both CMOS and RF-SOI contexts. While interface traps are traditionally regarded as detrimental to device performance, this work demonstrates that their effects strongly depend on the targeted application and substrate architecture. In particular, interface traps can be either harmful or deliberately exploited, depending on whether MOSFET or RF-SOI is prioritized.

A framework based on admittance methods was established to characterize interface traps in MOS capacitors fabricated on standard and high-resistivity Si-based substrates. Capacitance–voltage, conductance, and current–voltage measurements were combined with TCAD simulations to assess the applicability, sensitivity, and limitations of three extraction methods. Although the high-low frequency capacitance method was experimentally implemented due to laboratory constraints, three methods were shown to provide consistent results on standard-resistivity silicon-based substrates, while their interpretation on high-resistivity silicon-based substrates requires careful consideration of substrate impedance during de-embedding to ensure the reliability of the

extraction.

For RF-SOI substrates, this thesis provides the first detailed experimental study combining C–V characterization and RF measurements on SiGe-buried high-resistivity silicon. The results demonstrate that high interface trap densities at the  $\text{SiO}_2/\text{SiGe}$  interface can effectively compensate free carriers in the substrate, suppress parasitic surface conduction, and preserve high effective resistivity and linearity under bias. Furthermore, SiGe-buried high-resistivity substrates were shown to withstand CMOS-compatible thermal budgets, with a Ge content of 40% emerging as a promising solution for RF-SOI integration.

In parallel, interface trap characterization was applied to  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stacks on MOS capacitors relevant to CMOS scaling. The results demonstrate the critical role of an ultra-thin thermal  $\text{SiO}_2$  interfacial layer in achieving low interface trap densities, while  $\text{Al}_2\text{O}_3/\text{SiO}_2$  stacks also enable low leakage current and a favorable negative fixed charge providing effective field-effect passivation. The consistency of the extracted interface trap density between different extraction methods confirms the robustness of the conductance and Terman methods, and reinforces the importance of interface engineering in advanced gate stacks.

Overall, this thesis establishes a strong link between material engineering and electrical characterization. It demonstrates that admittance-based methods, when carefully adapted, remain powerful tools for probing interface traps even in challenging high-resistivity RF-SOI substrates. At the same time, SiGe buried substrates emerge as a promising engineering lever in RF-SOI technologies, offering a pathway to combine the mobility enhancement provided by SiGe strain with improved RF substrate performance.

### ***RF Power Switch Benchmarking***

To assess the impact of the buried-SiGe FD-SOI with  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate dielectric platform on power switches, we focus on two transistor-level figures of merit (FoM), one for small-signal and one for large-signal operation:

1. **Small-signal (SS):**  $R_{\text{on}}C_{\text{off}}$
2. **Large-signal (LS):** drain breakdown voltage

These FoMs serve as proxies for the circuit-level performance achievable with a given FET. By using buried SiGe booster in FD-SOI and replacing the gate dielectric with  $\text{Al}_2\text{O}_3/\text{SiO}_2$  ( $\text{EOT} = 5 \text{ nm}$ ), we can then predict how our technology would perform if implemented on a commercial FD-SOI process.

$R_{\text{on}}C_{\text{off}}$  quantifies how well a given FET performs as an RF switch at the small-signal level. In an RF switch, the FET operates in one of two modes: ON-mode, where it behaves as a source–drain resistance  $R_{\text{on}}$ , or OFF-mode, where it behaves as a source–drain capacitor  $C_{\text{off}}$ . The FoM is the product of these two quantities, and it should be as low as possible for a good switch. The reason is intuitive if the transistor is viewed as a simple switch: a low  $R_{\text{on}}$  acts like a short circuit, presenting a low-impedance path for the signal, while a low  $C_{\text{off}}$  presents a high impedance that isolates source from drain and blocks signal. When both parameters are small, their product  $R_{\text{on}}C_{\text{off}}$  is small, capturing the device’s ability to provide a low-impedance path and a high-impedance isolation simultaneously.

A key advantage of  $R_{\text{on}}C_{\text{off}}$  is its independence from device dimensions, which makes it ideal for fair comparison between devices of different sizes. For example, doubling the FET width doubles the total capacitance (two capacitors in parallel) while simultaneously halving the resistance (two resistors in parallel), so the product  $R_{\text{on}}C_{\text{off}}$  is unchanged. A single  $R_{\text{on}}C_{\text{off}}$  value therefore requires no normalization by device dimensions.

### Improvement of $R_{\text{on}}C_{\text{off}}$

Let’s assume that the mobility is boosted by 20 %. As  $R_{\text{on}}$  (i.e.  $1/g_d$ ) is directly proportional to mobility, it should be boosted by the same amount.

On the other hand,  $C_{\text{off}}$  does not depend on carrier mobility, but a modified dielectric alters the permittivity of the gate capacitance. However, its impact on the source-drain capacitance is expected to be minimal and will be neglected here. Increasing mobility therefore improves  $R_{\text{on}}$  directly without changing  $C_{\text{off}}$ , lowering the overall  $R_{\text{on}}C_{\text{off}}$ . In the ideal limit, a 20 % increase in mobility translates into roughly a 20 % decrease in  $R_{\text{on}}C_{\text{off}}$ .

For the case of an SLVT FET in 22FDX, simulated through the PDK with a normalized mobility increase of  $1 \rightarrow 1.2$  (+20 %) gives:

- $R_{\text{on}}$ :  $4.79 \Omega \rightarrow 4.51 \Omega$
- $C_{\text{off}}$ : unchanged at 21.61 fF
- $R_{\text{on}} \times C_{\text{off}}$ : reduced by 5.8 % (at  $\mu = 1.2$ )

The smaller simulated reduction of 5.8 % is due to the access resistances up to metal M1 that is not impacted by the mobility boost. It is therefore expected that the real gain in a practical switch implementation with full metalization would be even smaller than this.

A final consideration about the alternative  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate oxide. It enables

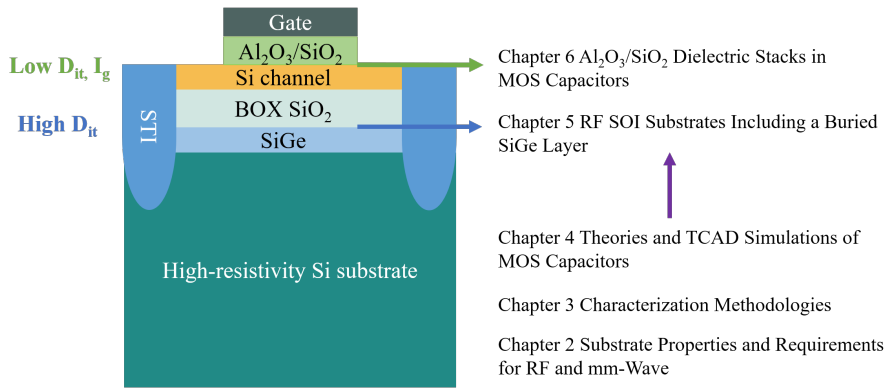
a higher gate breakdown voltage and thus allows a higher gate voltage to be applied. FD-SOI technologies such as 22FDX offer thicker-gate-oxide devices—for example, EG-SLVT FETs operating at 1.8 V instead of the 0.9 V of thinner SLVT FETs. This  $\text{Al}_2\text{O}_3/\text{SiO}_2$  gate oxide ( $\text{EOT} = 5 \text{ nm}$ ) allows the gate voltage to be raised, further improving  $R_{\text{on}}$ , reaching a gate breakdown voltage of 6 V. This solution shown in **Figure 7.1** therefore appears to provide significant improvements to the small-signal characteristics of RF switches.

Large-Signal / High-Power Behaviour

Drain breakdown voltage is equally important, as it reflects the FET’s ability to withstand high voltages—a crucial characteristic for high-power switches. For high-power operation, the benefit of  $\text{Al}_2\text{O}_3/\text{SiO}_2$  is less clear. A higher breakdown is achieved for the gate voltage, but in power switches, the OFF-state transistor is subject to *drain* breakdown rather than gate breakdown. Drain breakdown voltage was not studied in this work, but it would likely remain similar to that of conventional FDSOI.

The Feasibility of Fabrication

Our architecture described here is easily ported to a foundry process, as it requires the epitaxial stressor layer SiGe under the BOX, which is implemented in the starting wafer, and a high- $\kappa$  dielectric stack  $\text{Al}_2\text{O}_3/\text{SiO}_2$  that is compatible with existing gate-first or gate-last flows. Therefore, there are no additional process steps in the IC manufacturing flow.



**Figure 7.1:** The cross-sectional schematic of RF power switch.

## Perspectives

Several promising directions for future work emerge from the discussions presented in this thesis.

### *Applications*

#### —— Low temperature for interface trap characterizations

Conventional capacitance–voltage (C–V) characterization techniques and their associated interpretation methods are employed to evaluate the interface trap density ( $D_{it}$ ) in MOS capacitors fabricated on silicon substrates with different resistivities. Among the available extraction techniques, the Terman method and the conductance method are the most commonly used approaches for assessing interface quality.

The conductance method is generally regarded as the most reliable and widely adopted technique for  $D_{it}$  extraction, owing to its high sensitivity to interface states and its direct physical interpretation. Despite its simplicity, this method provides accurate quantitative information on interface passivation and can be readily extended to low temperature measurements, such as 4K. Such extensions can observe interface traps located near the band edges at the dielectric/Si interface, therefore offering deeper insight into interface passivation relevant for cryogenic and low-temperature device applications.

#### —— RFSOI integration of SiGe buried HRS ——

The physical understanding and modeling of SiGe-based buried high-resistivity silicon provide valuable guidance for developing buried-SiGe FDSOI solutions on RF substrates. This thesis shows that a buried SiGe layer can act as an effective trap-rich passivation scheme for HR substrates in RF-SOI technology: at the same time, it highlights the need to clarify the bias-dependent behavior observed in both small and large-signal characterizations.

Further investigations are required to determine the impact of Ge concentration on interface trap density and to identify an optimal FDSOI thermal budget that preserves RF performance without degrading the strain transferred from the SiGe layer to the channel. Ultimately, these insights will enable the design

and evaluation of millimeter-wave circuits, such as low-noise amplifiers (LNAs) and power amplifiers (PAs), based on field-effect transistors fabricated on this alternative substrate platform.

### — Conductive bridging-based memristive RF switch

The memristive RF switch offers several key advantages, including a large switching ratio, high cutoff frequency, and nonvolatile behavior, consistent with the hysteretic current–voltage characteristics of a memristor. Due to its nonvolatile nature, the memristive switch is able to maintain its ON and OFF states without continuous biasing, thereby achieving very low static power consumption. Furthermore, these devices are compatible with back-end-of-line (BEOL) CMOS integration, which minimizes the routing of signals between the top metal layers and the transistor layer, leading to reduced power dissipation. Together, these features position memristive RF switches as a promising candidate for next-generation intelligent RF systems.

The RF switch investigated in this work is based on conductive-bridge RAM (CBRAM) technology and employs an  $\text{Al}_2\text{O}_3/\text{SiO}_2$  dielectric stack integrated on a trap-rich substrate. This device consists of a pair of electrochemically asymmetric metal electrodes—namely, an active electrode and an inert electrode—separated by a 1  $\mu\text{m}$  gap. The switching mechanism is governed by a redox process in which a metallic filament is formed or ruptured between the two electrodes as a result of ion migration and Joule heating. When an external electric field is applied, metal ions (Ag) originating from the active electrode migrate toward the inert electrode (Au), leading to the growth of a conductive filament. Reversing the polarity of the electric field induces filament dissolution, whereby metal ions are released from the filament and migrate back toward the active electrode, recombining with the bulk metal.

At the current stage of development, the device can be reliably switched ON (low resistive state) and OFF (high resistive state) for more than 100 cycles using a set voltage of 3 V and a reset voltage of 2 V. The filament-forming voltage is approximately 10 V and is strongly dependent on the gap between the left and right electrodes. At 67 GHz, the measured insertion loss ranges from 2 to 4 dB, while the isolation varies between 20 and 25 dB. However, long-term switching repeatability affects the development of this new RF switch. Since the



filament formation is intrinsically a stochastic process, the RF performance is prone to exhibiting cycle-to-cycle variations. Besides, the filament overgrowth due to the large compliance current and forming voltage can result in reset failure. These issues may be mitigated through process optimization, including improvements in electrode selection and insulator layer engineering. In addition, characterization conditions, such as operating temperature, can significantly influence filament formation and growth.





## 8. Appendices

### A Derivation of the Conductance Method Relation for $D_{it}$

#### A.1 Single-level interface trap

Interface traps exchange charge with the semiconductor majority-carrier band by capture and emission. The loss associated with this process appears, in the small-signal admittance, as a frequency-dependent parallel conductance. For a *single* trap level characterized by one time constant  $\tau$ , the equivalent parallel conductance normalized to frequency is

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau} \ln[1 + (\omega\tau)^2], \quad (8.1)$$

where  $q$  is the elementary charge and  $\tau = [\sigma v_{th} n_s]^{-1}$  is the trap response time, set by the capture cross section  $\sigma$ , the thermal velocity  $v_{th}$  and the surface carrier concentration  $n_s$ .

#### A.2 Location of the peak

The quantity  $G_p/\omega$  in **Equation 8.1** exhibits a maximum when swept against  $\omega\tau$ . Introducing the dimensionless variable  $x \equiv \omega\tau$ , the bracketed function is

$$f(x) = \frac{\ln(1+x^2)}{2x}. \quad (8.2)$$

The extremum is found from  $df/dx = 0$ , which yields the transcendental condition

$$\frac{2x^2}{1+x^2} = \ln(1+x^2). \quad (8.3)$$

The non-trivial root of **Equation 8.3** is

$$x_{\max} = (\omega\tau)_{\max} \approx 1.98. \quad (8.4)$$

Substituting  $x_{\max} \approx 1.98$  back into **Equation 8.2** gives

$$f(x_{\max}) = \frac{\ln(1+1.98^2)}{2 \times 1.98} \approx 0.402, \quad (8.5)$$

so that the peak value of the normalized conductance is

$$\left(\frac{G_p}{\omega}\right)_{\max} \approx 0.402 qA D_{it}. \quad (8.6)$$

Inverting **Equation 8.6** and noting that  $1/0.402 \approx 2.49$  recovers the single-level extraction relation

$$D_{it} \approx \frac{1}{0.402} \frac{1}{qA} \left(\frac{G_p}{\omega}\right)_{\max} \approx 2.49 \frac{1}{qA} \left(\frac{G_p}{\omega}\right)_{\max}. \quad (8.7)$$

The constant is frequently rounded to 2.5; because  $f(x)$  is very flat near its maximum, the extracted  $D_{it}$  is insensitive to small errors in locating the peak. Evaluating **Equation 8.2** at  $x = 2.5$ , for instance, gives  $f \approx 0.396$  and hence a prefactor of  $\approx 2.52$ , a change of only about 1%.

## B Derivation of the Second Extraction Method of Flatband Voltage Based on Flatband Capacitance

The flatband capacitance follows from the series combination of the oxide and semiconductor capacitances at flatband,

$$\frac{C_{FB}}{C_{ox}} = \frac{1}{1 + C_{ox}/C_S}, \quad (8.8)$$

with

$$C_S = \frac{K_s \epsilon_0}{L_D}, \quad C_{ox} = \frac{K_{ox} \epsilon_0}{t_{ox}}, \quad (8.9)$$

so that

$$\frac{C_{\text{ox}}}{C_{\text{S}}} = \frac{K_{\text{ox}}}{K_{\text{S}}} \frac{L_D}{t_{\text{ox}}}. \quad (8.10)$$

Inserting the Debye length  $L_D = \sqrt{kTK_s\epsilon_0/(q^2N_A)}$  and simplifying gives

$$\frac{C_{\text{ox}}}{C_{\text{S}}} = \frac{K_{\text{ox}}}{t_{\text{ox}}\sqrt{N_A}} \sqrt{\frac{kT\epsilon_0}{q^2K_s}}. \quad (8.11)$$

Writing  $\sqrt{T} = \sqrt{300} \sqrt{T/300}$  allows all physical constants to be collected into a single prefactor,

$$\frac{C_{\text{ox}}}{C_{\text{S}}} = K_{\text{ox}} \underbrace{\sqrt{\frac{k\epsilon_0 \cdot 300}{q^2K_s}}}_{\approx 136} \frac{\sqrt{T/300}}{t_{\text{ox}}\sqrt{N_A}}. \quad (8.12)$$

Evaluating the prefactor for the  $\text{SiO}_2$ –Si system ( $K_{\text{ox}} = 3.9$ ,  $K_{\text{S}} = 11.7$ ,  $\epsilon_0 = 8.854 \times 10^{-14}$  F/cm,  $k = 1.381 \times 10^{-23}$  J/K,  $q = 1.602 \times 10^{-19}$  C) yields

$$K_{\text{ox}} \sqrt{\frac{k\epsilon_0 \cdot 300}{q^2K_s}} = 3.9 \sqrt{\frac{(1.381 \times 10^{-23})(300)(8.854 \times 10^{-14})}{(1.602 \times 10^{-19})^2(11.7)}} \approx 136, \quad (8.13)$$

so that, with  $t_{\text{ox}}$  in cm and  $N_A$  in  $\text{cm}^{-3}$ ,

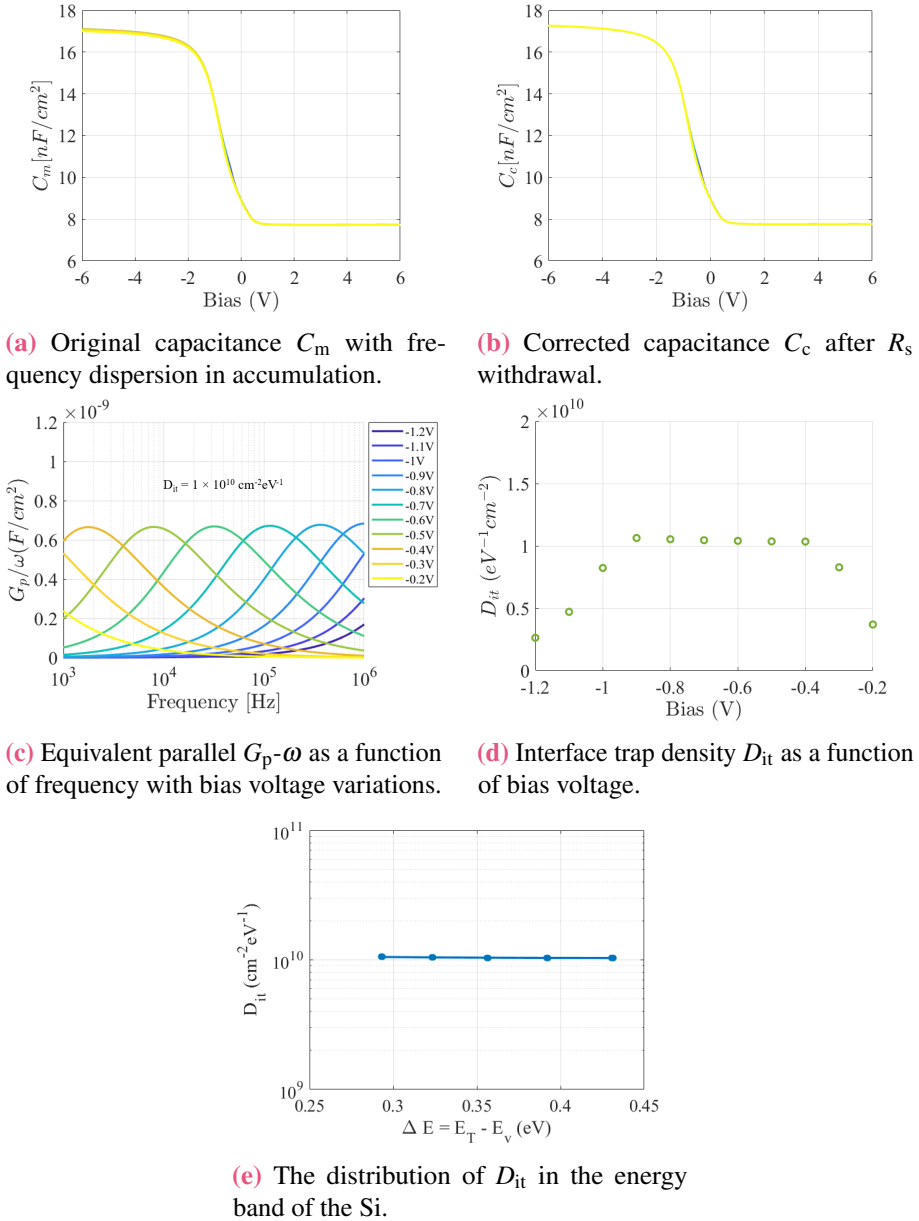
$$\frac{C_{\text{FB}}}{C_{\text{ox}}} = \left( 1 + \frac{136\sqrt{T/300}}{t_{\text{ox}}\sqrt{N_A}} \right)^{-1}. \quad (8.14)$$

The coefficient 136 is therefore not a fundamental constant but simply the grouped material and physical constants of the  $\text{SiO}_2$ –Si system.



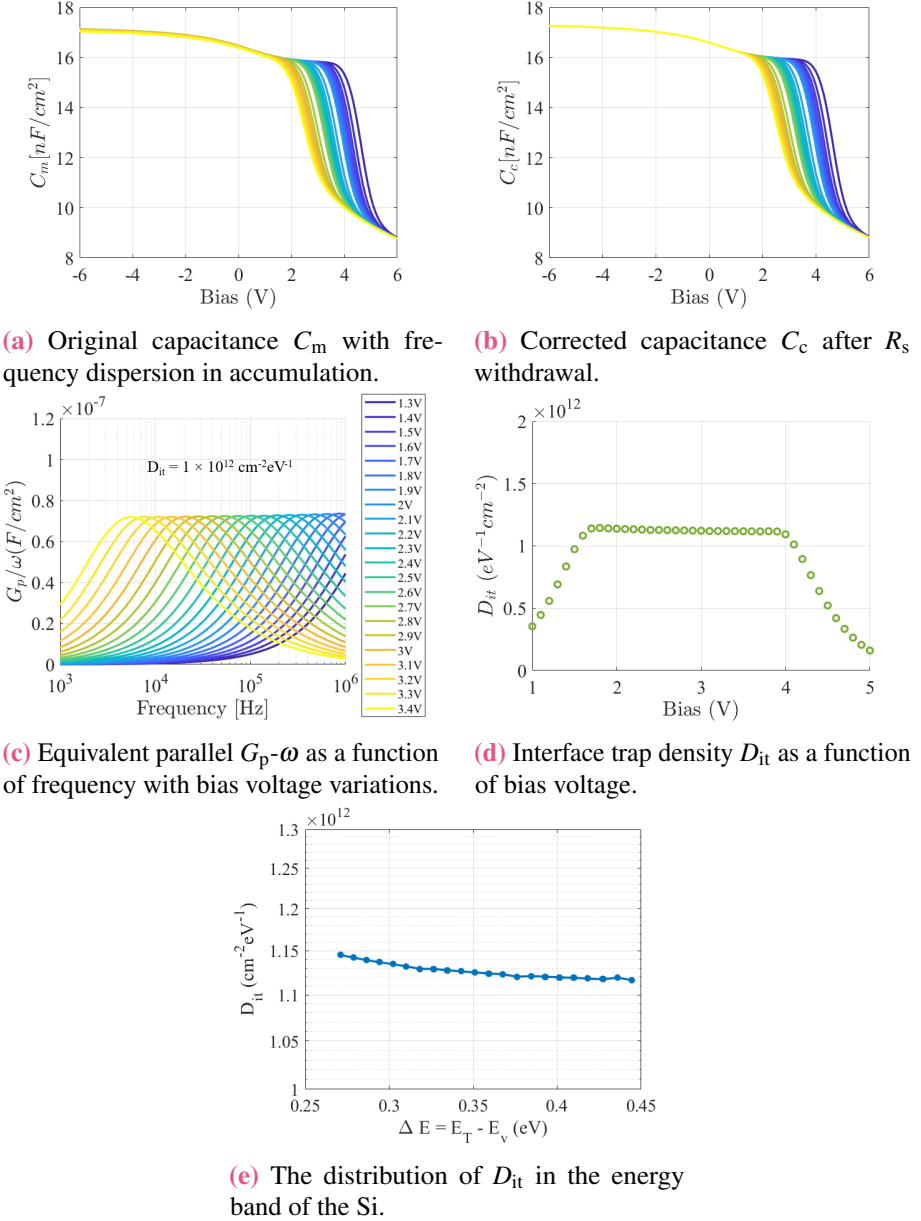
### C The Influence of $D_{it}$ Variation on the conductance method

MOS capacitor on STD with  $D_{it} = 1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$



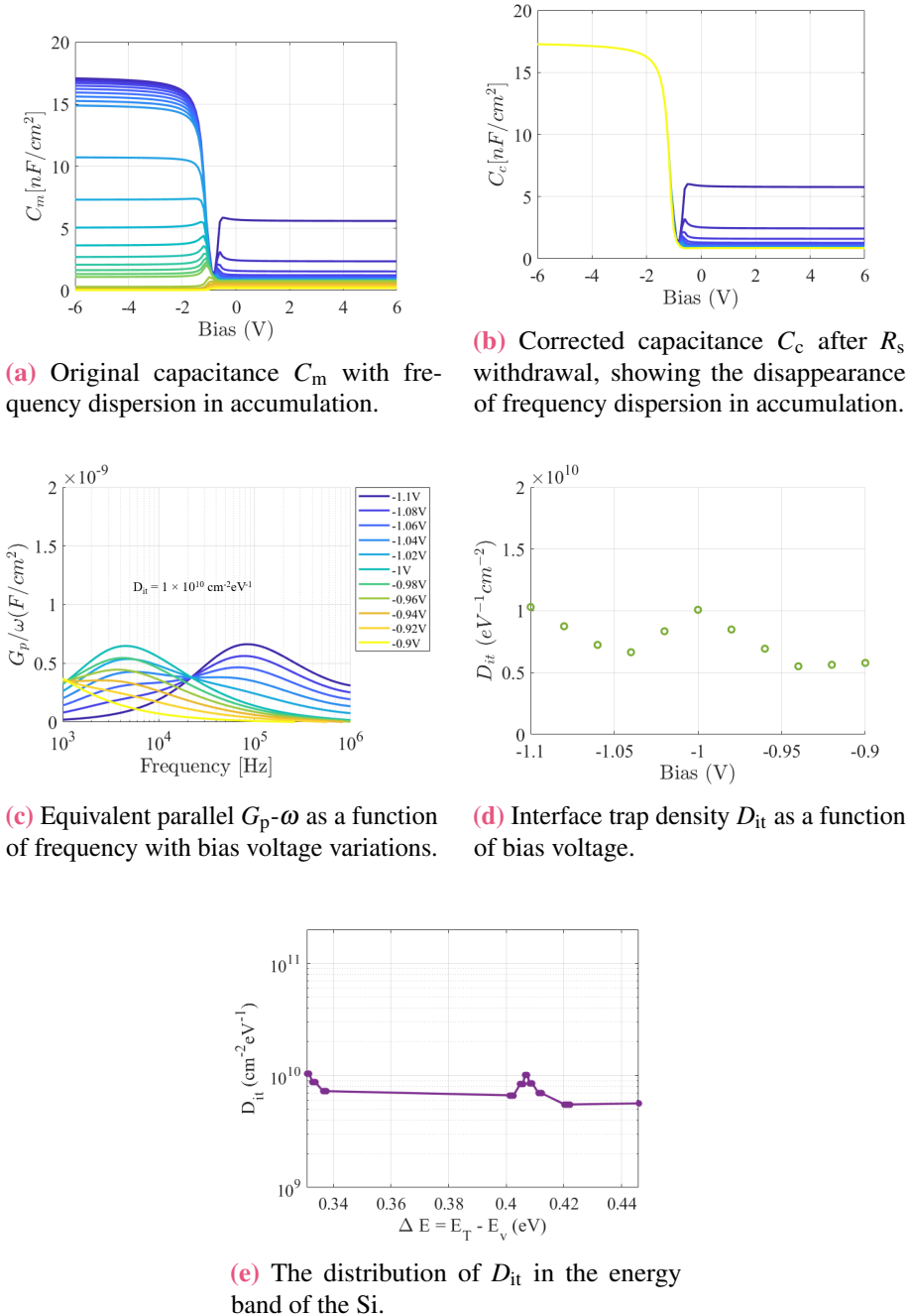
**Figure 8.1:** Illustrations of the conductance method applied to MOS capacitor based on standard Si (resistivity around  $30 \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.

### MOS capacitor on STD with $D_{it} = 1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$



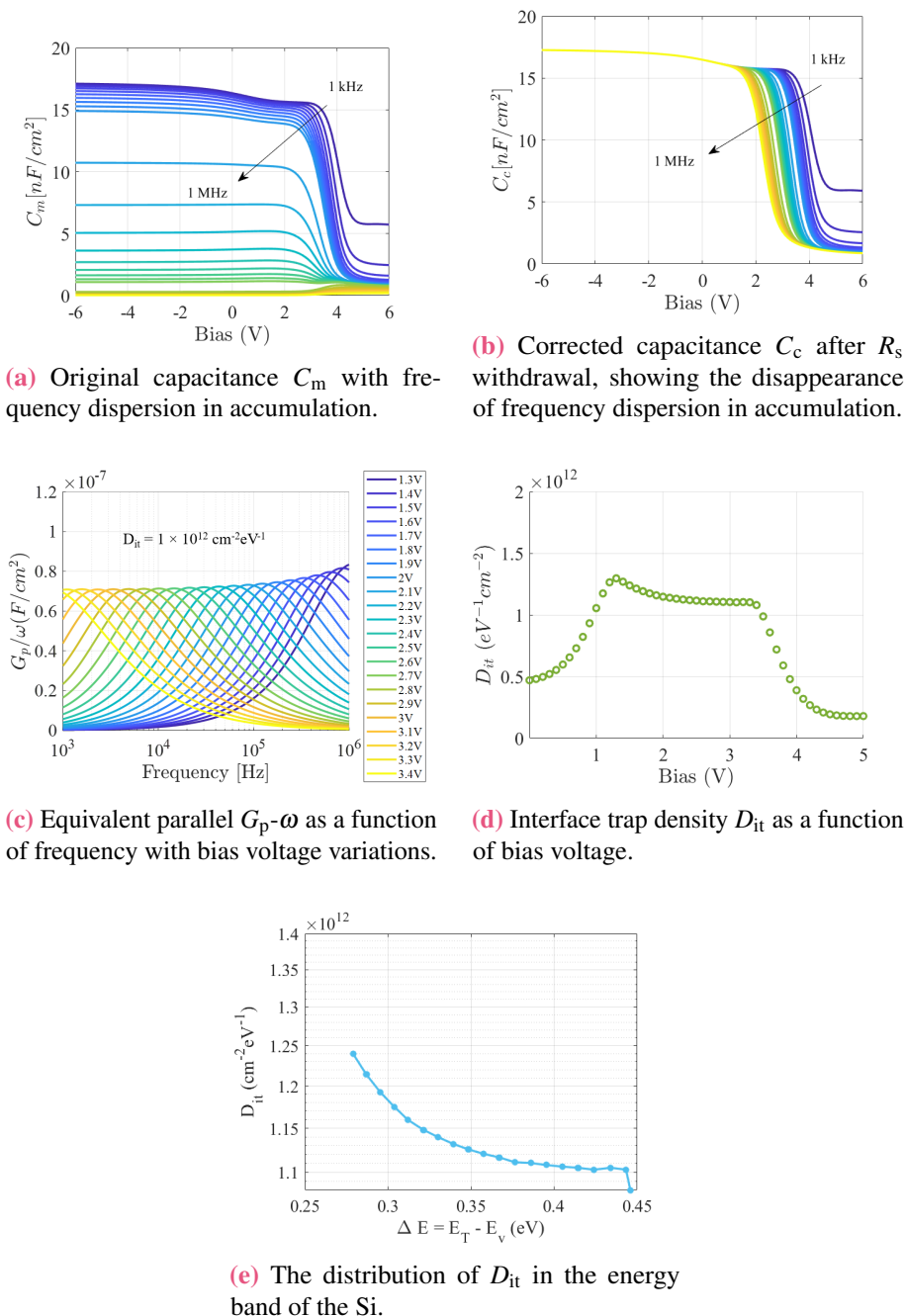
**Figure 8.2:** Illustrations of the conductance method applied to MOS capacitor based on standard Si (resistivity around  $30 \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.



**MOS capacitor on HRS with  $D_{it} = 1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$** 

**Figure 8.3:** Illustrations of the conductance method applied to MOS capacitor based on HR Si (resistivity around  $5 \text{ k } \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.

### MOS capacitor on HRS with $D_{it} = 1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$

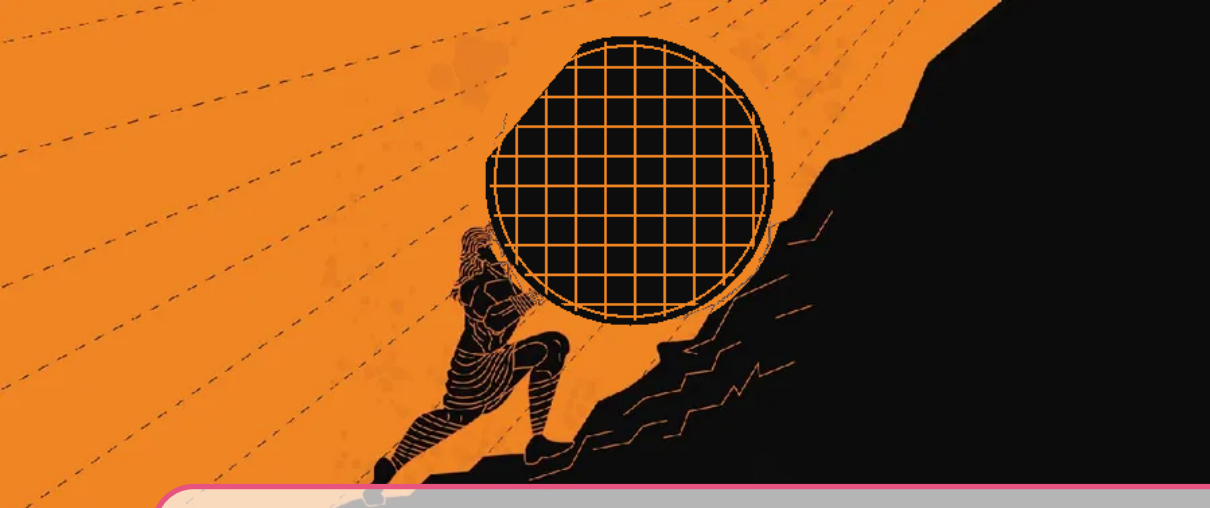


**Figure 8.4:** Illustrations of the conductance method applied to MOS capacitor based on HR Si (resistivity around  $5k \Omega \cdot \text{cm}$ ) with acceptor-like interface trap density equal to  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  widely distributed in the energy bandgap.

### C.1 Discussion

In **Figure 8.1**, **Figure 8.2**, **Figure 8.3**, and **Figure 8.4**, the interface trap density,  $D_{it}$ , was assigned values of  $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  and  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$  to cover the range of  $D_{it}$  values considered in **Section 4.2.5**. The objective of this section is to evaluate the lower detection limit of the conductance method with respect to  $D_{it}$ .

When the imposed interface trap density is  $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ , the extracted  $D_{it}$  values for both the STD and HRS substrates agree well with the values specified in the TCAD simulations. In contrast, when  $D_{it}$  is reduced to  $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ , the extraction for the STD substrate remains consistent with the imposed value, whereas the extraction for the HRS substrate becomes less accurate. This degradation is attributed to the smearing of the hole response, which makes the conductance peak less distinct and therefore limits the accuracy of the  $D_{it}$  extraction.



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