Bottom-Up Life-Cycle Assessment of MEMS Piezoresistive Pressure Sensors

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***Abstract*—The manufacturing of modern silicon-based MEMS requires highly energy- and resource-intensive processes. Understanding and gathering objective data of the impacts of silicon manufacturing is crucial to select design strategies reducing the environmental impacts. In this work, we present a bottom-up assessment of the embodied energy and carbon footprint of two piezoresistive pressure sensors, by adapting previously published LCA data set to model the sensors process sheets. Then we use these models as generic models of pressure sensors processes to discuss their environmental impacts regarding their performances. Our results highlight that using Silicon-on-Insulator (SOI) substrates and deep reactive ion etching (DRIE) as release process could lead to a 50-fold reduction of the environmental impacts of MEMS pressure sensors regarding to their specifications.**

***Index Terms*—life-cycle assessment, pressure sensor, semiconductor, microfabrication.**

I. Introduction

Silicon-based MEMS are a growing technology. They are now widely used in automotive, medical, avionics, industrial and consumer electronics, and their market growth rate seems continuously increasing [1]. Since silicon manufacturing is extremely energy and resources intensive, this growth could lead to a high environmental impact in a few years [2]. It is so becoming a real interest to consider early environmental assessments of MEMS manufacturing.

Life Cycle Assessment (LCA), a methodology to evaluate the environmental impact of products or services over its whole life cycle (from material sourcing to end-of-life), has become a standard used extensively in different disciplines.

LCA interest lies in highlighting the hotspots, i.e. the main responsible of the environmental costs resulting from the product fabrication, use and disposal. In the electronics sector, major parts of the impacts (carbon emission, energy and water consumption) are caused in the production phase by the sourcing (extraction, refinement) of the precious raw materials (silicon wafer, cobalt, tungsten, etc), by the fab high electricity consumption (to run the cleanrooms), the gas emissions of the complex semiconductor manufacturing processes and from the very low material efficiency in the fab leading to exhausts and local pollution.

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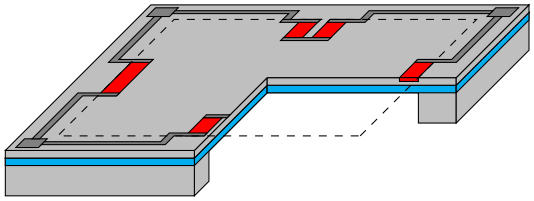

Fig. 1: Cross-section view of a typical SOI piezoresistive pressure sensor: silicon (Si) in ligth-gray, buried silicon dioxide ($Si0_2$) is in blue, heavily-doped silicon (h-d-Si) contacts are in pink, lightly-doped silicon (l-d-Si) resistors are in pink, silicon nitride (Si_3N_4) is in green, aluminum (Al) conductive lines are in gray, dashed lines highlight the perimeter of the membrane. [6]

Therefore, quantification of the Cumulated primary Energy Demand (CED), Global Warming Potential (GWP) and water consumption indicators for the fabrication of electronic devices is of particular importance. However, many other impacts could be considered, especially for electronics: ecotoxicity and resource depletion are also crucial, among others. LCA, as a multi-indicator assessment tool, could be extended to the quantification of such indicators.

Seminal LCA evaluations have already been carried out for CMOS processes by [3]–[5], but much remains to be studied for other semiconductor devices, e.g., MEMS devices.

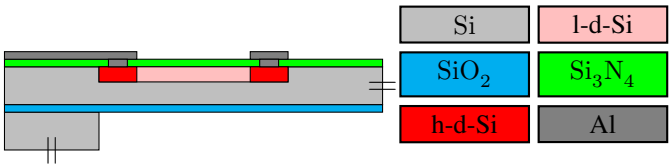

Fig. 2: Typical structure of a SOI piezoresistive pressure sensor membrane, with monocrystaline silicon resistors: silicon in ligth-gray, buried silicon dioxide is in blue, heavily-doped silicon contact areas are in red, lightly-doped silicon piezoresistor is in pink, silicon nitride is in green and aluminum conductive lines are in gray, small dashes indicats continuing geometries.

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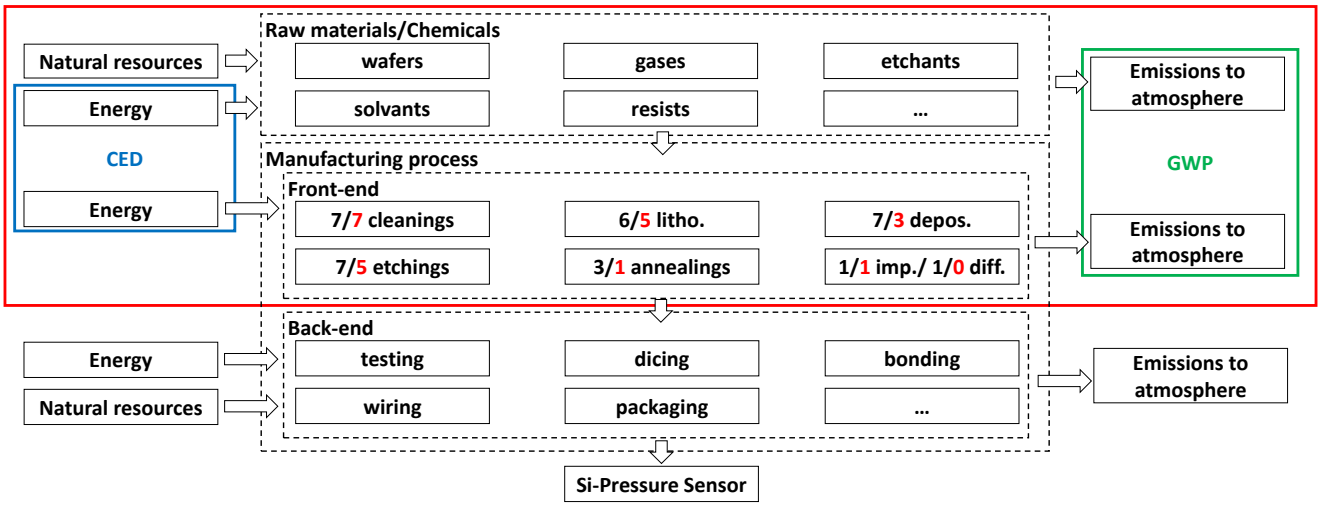

Fig. 3: Silicon pressure sensor manufacturing process from Kumar *et al.* [8] (black numbers) and Li *et al.* [9] (red numbers). The red box defines the perimeter of the LCA.

In this work, we assess the environmental footprint of silicon-based piezoresistive pressure sensors that were the biggest share in the MEMS market for many years [1]. Even if their design seems simple, as presented for Silicon-on-Insulator (SOI) pressure sensor on Fig. 1, their structure is complex and composed by multiple layers, as seen in Fig. 2; their fabrication can include up to 30 process steps, or more, and requires precious raw materials and natural resources. In particular, silicon-based piezoresistive pressure sensors require to manufacture a thin silicon membrane, which acts as a transducer. Here, we propose a quantification of (1) the CED, (2) the GWP and (3) the ultra-pure water (UPW) consumption indicators for two typical process flows, with a focus on the membrane release and the most impacting steps of those two sensors. Then, we discuss sensor performance aspects with regard to the environmental assessment to support the development of new research practices and design guidelines and offer the most appropriate solutions in terms of environmental cost, design and functionalities.

II. Methodology

MEMS devices are fabricated starting with SOI substrates that are 300 mm in diameter, and we choose 1 cm^2 of manufactured wafer as a functional unit.

The methodology adopted in this work is based on the use of a previously generated life-cycle inventory database for CMOS processes, also intended to model and evaluate multiple semiconductor devices and to serve as a basis for quantifying environmental implications of other applications that use nano-fabrication [4]. This approach has already been applied to water quality sensors [7]. We evaluated the CED, GWP and UPW consumption based on the process flows, by respectively computing the tools energy requirement and time, average input and output gas flows for each tool (including the usage factor, i.e. material efficiency), corrected by an abatement factor, and the UPW use for each process step [5].

Fig. 3 shows process flows of the two sensors and this study perimeter, i.e., the CED and GWP of the front-end manufacturing processes as well as the embodied CED and GWP of all raw materials (e.g. electronic-grade silicon wafer production), UPW, chemicals, gases and natural resources used. Back-end manufacturing and facility contributions (CED, GWP and UPW) are not included. The process from Kumar *et al.* [8] presents the larger number of wafer manufacturing steps and the membrane release is obtained through wet etching (KOH). On the opposite, Li *et al.* [9] process involves several dry reactive ion etching (RIE) steps to etch the wafer back side in order to form a thin membrane.

III. Results

A. Cumulated Energy Demand

The energy consumption (CED) is similar for the two process flows: 0.69 kWh/cm^2 for Li *et al.* and 0.71 kWh/cm^2 for Kumar *et al.* (Fig. 4). The energy demand is mainly driven by the silicon wafer production. The high embedded energy of the final product (about 2 127 kWh/kg of crystalline silicon wafer) is due not only to the energy intensity of the processes for electronics-grade silicon wafer production (99.9999999% purity), including refining silica, crystallisation of polysilicon to ingots and sawing, but also a cumulative low yield caused by the losses at each step [3]. The SOI fabrication was estimated to contribute to about 0.12 kWh/cm^2. Regarding the manufacturing processes, the major contributors to CED are the standard photolithography, dry etching and CVD utilities (Fig. 5).

B. Global Warming Potential

As for CED, a significant part of the GWP is caused by the silicon-wafer production, about 190 g.CO_2eq/cm^2 (equivalent

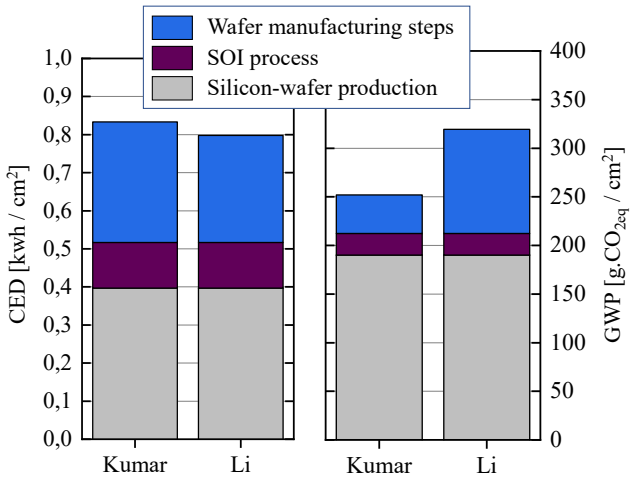

Fig. 4: Total CED and GWP per cm^2 for Kumar *et al.* and Li *et al.* pressure sensor full process flows (300 mm wafer= 706 cm^2), including silicon-wafer production, SOI process and wafer manufacturing steps. Energy and GWP are mainly deriving for silicon-wafer production (processing quartz into metallurgical grade Si, purification of Si into ingots and then into wafers [3]). Facility energy is excluded from the process flow. The details about the manufacturing step impacts are shown in the Figs. 6 and 5. Although these values represent the impacts of two specific process flows, we will consider these processes as reference values to model generic pressure sensors and discuss the impact of technology choice on performances in Section IV.

CO_2 emissions related to the energy-intensive process), and by the SOI process, about 22 $g.CO_2eq/cm^2$ (Fig. 4). Most differences between the two processes occur in the wafer manufacturing steps (Fig. 6). Our analysis shows a significant increase in GWP/cm^2 of manufactured wafer for the process of Li *et al.* (about 107 $g.CO_2eq/cm^2$), as compared to the one of Kumar *et al.* (about 39 $g.CO_2eq/cm^2$). In particular, we see that greenhouse gas (GHGs) emissions, including fluorinated compounds (SF_6, C_4F_8 and NF_3) used in dry etch and LPCVD process steps are the major contributors to $g.CO_2eq$ due to their high GWP. The high carbon footprint of Li et al process can thus be attributed to the use of long-lasting Deep-RIE (DRIE) process steps to release the membrane. We see that wafer manufacturing GWP of Kumar *et al.* process flow is significantly lower thanks to the use of wet etch steps (KOH and BHF) that help reducing the GHGs by replacing some long dry etching steps.

For the sake of comparison and perspectives on these results, we compared the $g.CO_2eq$ emissions obtained for Kumar and Li's processes with the carbon emissions of a MEMS device fabricated at the ST-Microelectronics (ST-M) foundries [10]. They claim a total impact of about 147 $g.CO_2eq$ emissions for the MEMS device, with 90% of all the impacts that can be attributed to the raw materials and the ST-M production facilities. The $g.CO_2eq$ emissions therefore lie in the same order of magnitude as compared with the piezoresistive sensors, although the exact dimensions and composition of the ST-M MEMS device remains unclear (the packaged device stays in the cm^2-range size). We also looked at the carbon emissions of the manufacturing process of a microcontroller, which involves logic technologies. The processing of logic technologies includes more than 10 times processing steps than the studied piezoresistive sensors [5]. ST-M reports a footprint of about 390 $g.CO_2eq$ for its manufactured microcontroller [11]. Despite the high complexity of the microcontroller fabrication process compared to MEMS devices, Li *et al.* process flow has relatively quite significant impacts compared to the microcontroller. This could be explained as the two devices do not require the same technical specificities: the release of the membrane from the silicon wafer through long dry etching steps is very particular to the pressure sensor and highly contribute to its high embodied carbon, which are not needed for the microcontroller functionalities. We therefore conclude that the impact of microelectronic devices cannot be only attributed to process complexity, but also strongly depends on the specific functionalities required and the specificity of the resulting process steps.

C. Ultra-Pure Water Consumption

UPW consumption is mainly driven by the wafer cleaning steps, where UPW is used to rinse the wafer in wet benches. Both processes share the same UPW consumption, about 0.84 L/cm^2 of processed wafer, as the two processes present the same number of wet wafer cleaning steps. As UPW is contaminated after use and purification systems are cost and energy intensive, recycling is challenging [5]. However, some UPW can be reinjected towards cooling system of the facility. UPW production also uses chemicals and energy and about twice its volume of water. Process cooling water, mainly coming from industrial city water sources, was not taken into account. For instance, the UPW consumption of 28 nm technologies was estimated at about 6 L/cm^2 for full process flow for 300 mm wafers, though including much more wet steps [5].

The environmental assessment results seem to point out that design strategies reducing the number of DRIE process steps while keeping the sensor functionalities should be preferred, and that different indicators should be studied to highlight variations in impacts between different processes.

IV. Discussion

A point of attention is that due to the different sizes and thicknesses of membranes, it is difficult to have a fair comparison of sensors impacts since they have different absolute performances. In this discussion section we are proposing a way to compare the different fabrication processes, according to the sensors performances they are enabling.

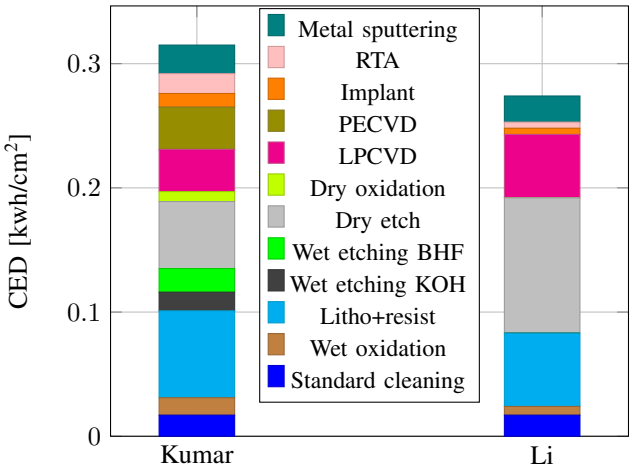

Fig. 5: Cumulated primary Energy Demand (CED) for the different wafer manufacturing process steps. Kumar *et al.*'s process shows a higher CED because of its larger number of process steps. Facility energy is excluded from the process flow.

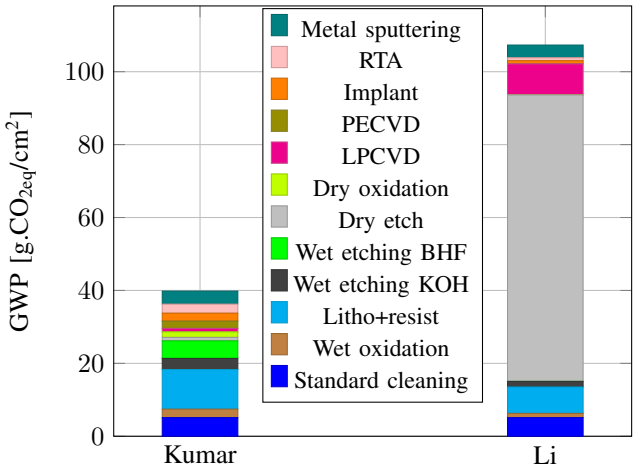

Fig. 6: Global Warming Potential (GWP) by process step assuming abatement factor of 90% for GHGs [5]. Li *et al.* process flow includes two time-consuming deep RIE (DRIE) steps that involve consequent quantities of high GWP SF_6 and C_4F_8 gases, while the chemicals engaged in Kumar *et al.* wet etch steps do not contribute significantly.

A. Mechanical Figure of Merit

We use the Mechanical Figure of Merit (S_A) that we defined in [6] as the ratio between the normalized sensitivity and the area of the membrane, expressed in $\mu V/V/Pa/mm^2$. Thanks to the presented State of the Art in [6], we highlight in Fig.7 that the use of SOI wafer allows for reaching thinner membranes, down to 3 μm, while using DRIE allows for enhancing S_A thanks to membrane patterning from back-side. Moreover, we draw to experimental trends: Dashed line is following the best S_A reachable without membrane patterning and solid line is showing the best S_A with membrane patterning. At 10 μm membrane thickness, we can observe that membrane patterning allows for increasing S_A by a factor of 6.

B. Normalized Performances

Using the experimental lines defined in the last section, we normalized the S_A by the reachable membrane thickness depending on the substrate, i.e., $10\mu m$ for bulk silicon and 3 μm for SOI. This allows us to have an estimation of the best S_A that is achievable depending on the process and the substrate used.

Since the CED and GWP are related to the sensor die area, we have to estimate the die area needed to reach a specified sensitivity, A_s, to establish a fair comparison between sensitivity and impacts. With anisotropic wet etching, side walls have a 54.7° slope: this means that, considering a 300 μm thick substrate, a 220 μm wide area has to be added on each side of the membrane. With DRIE, vertical side walls are almost achievable, meaning no additional area is needed for the membrane release. So, in addition to the extra sensitivity DRIE is enabling, it is also requiring less extra area due to the side wall slope. In both cases, a 300 μm wide area is added all around, for connection pads and packaging purpose.

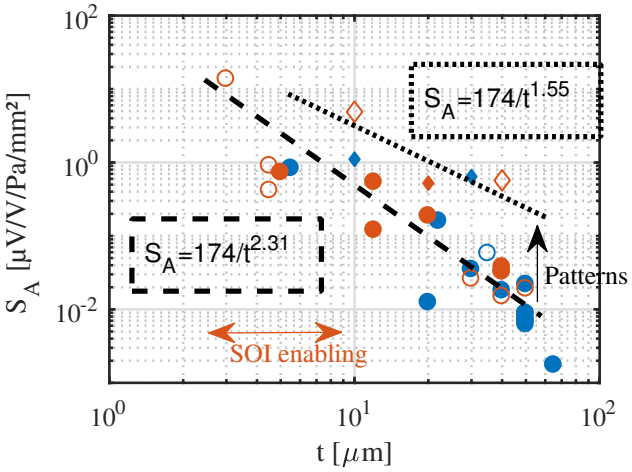

Fig. 7: Mechanical Figure of Merit regarding membrane thickness (t) from [6]. Colors represent substrate types, respectively, blue and orange for bulk-silicon and SOI. Symbols represent release membrane techniques, respectively, filled and empty for anisotropic wet etching and DRIE. Symbols shapes represent membranes topology, respectively, circle and diamond for flat or patterned membranes.

Results are shown on Fig. 8, highlighting the strong benefit of using SOI-wafers and DRIE for membrane patterning.

C. CED and GWP versus sensitivity requirements

Thanks to the results of the last sections and by using the generic steps presented in fig. 4, we can finally estimate the absolute CED and the GWP required to produce a sensor capable to achieve a desired sensitivity.

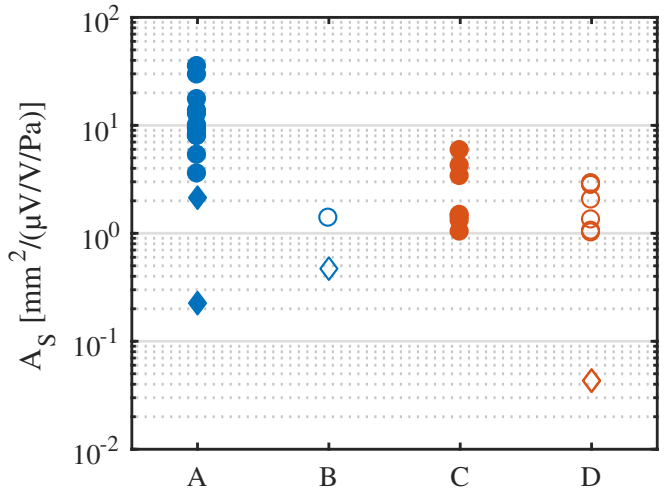

Fig. 8: Estimated area needed to reach a specified sensitivity (A_s) regarding the sensors technology. Colors represent substrate types, respectively, blue and orange for bulk-silicon and SOI. Symbols represent release membrane techniques, respectively, filled and empty for anisotropic wet etching and DRIE. Symbols shapes represent membranes topology, respectively, circle and diamond for flat or patterned membranes.

We computed four typical scenarios of CED and GWP, mixing bulk and SOI substrates, and wet and dry etching techniques. Then we expressed the ratio between these GWP and CED and the corresponding results of the normalized S_A, leading to the costs of sensors related to a sensitivity specification. Resuslts are shown in Figs. 9-10. We observe that if SOI technology is used to reduce the membrane thickness and DRIE is used to pattern effectively the membrane, gain in S_A is more than sufficient to overcome the respective increase in CED and GWP, going respectively from 25.10^{-3} kWh/(μV/V/Pa) and 8 g.CO_{2eq}/(μV/V/Pa) for flat-membrane, wet-etch, bulk pressure sensors, down to 350.10^{-6} kWh/(μV/V/Pa) and 150.10^{-3}g.CO_{2eq}/(μV/V/Pa) for patterned-membrane, dry-etch, SOI pressure sensors.

This leads us to the interesting result that for reaching desired specifications, current advanced MEMS technologies allow for reducing sensors A_s, but also CED_s and GWP_s. However, we have to take these results carefully as these advanced techniques are a big part of the total CED and GWP of the process. When using new techniques, it is essential to check that the increase in sensitivity per area overcomes the increase of CED and GWP to keep a global reduction of the impacts.

Substrate having the biggest proportion of the CED and GWP, further investigations should define the sweet spot between wafer impact reduction and yield reduction by decreasing the wafer thickness.

V. Conclusion

In this paper, we presented a LCA of two piezoresistive differential pressure sensors, based on different technologies, highlighting their CED and GWP. We used these two LCA as basis for evaluating the impact of technological choices, as using SOI or bulk silicon, releasing membrane thanks to wet or dry etch, using membrane patterning or not. These

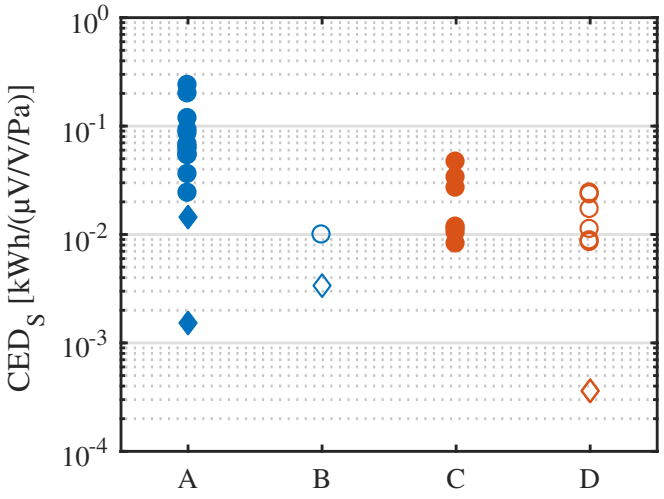

Fig. 9: Estimated CED needed to reach a specified sensitivity (CED_s) regarding the sensors technology. Colors represent substrate types, respectively, blue and orange for bulk-silicon and SOI. Symbols represent release membrane techniques, respectively, filled and empty for anisotropic wet etching and DRIE. Symbols shapes represent membranes topology, respectively, circle and diamond for flat or patterned membranes.

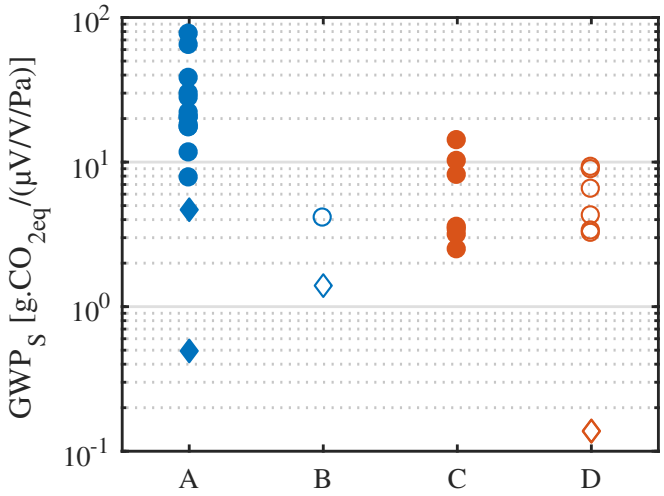

Fig. 10: Estimated GWP produced to reach a specified sensitivity (GWP_s) regarding the sensors technology. Colors represent substrate types, respectively, blue and orange for bulk-silicon and SOI. Symbols represent release membrane techniques, respectively, filled and empty for anisotropic wet etching and DRIE. Symbols shapes represent membranes topology, respectively, circle and diamond for flat or patterned membranes.

LCA showed that wafer production and the membrane release step are the two majors contributors of CED and GWP, leading to more than 70% of the CED/GWP. Then, combining these LCA with a sensitivity to pressure analysis, we observe that even if SOI-wafer and dry etch choices have a bigger CED and GWP per area than bulk and wet etch choices, these technologies can allow a sufficient increase of their S_A, leading to a high reduction of CED and GWP at same sensitivity requirements, down to 150.10^{-3}g.CO_{2eq}/(μV/V/Pa) and 350.10^{-6} kWh/(μV/V/Pa), respectively.

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