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Field-Effect Passivation of Lossy Interfaces in High-Resistivity RF Silicon Substrates

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***Abstract*—In this paper, a novel method for increasing effective resistivity in low-doped silicon substrates is presented. The parasitic surface conduction effect is known to be the dominant cause of RF substrate losses in high-resistivity silicon materials, and the proposed approach passivates the Si/SiO$_2$ interface through the field-effect. The technique is applied below CPW lines in the 45RFSOI node from GLOBALFOUNDRIES on alternate high-resistivity silicon substrates. Small-signal measurement results reveal a strong increase in substrate effective resistivity as a function of the applied bias to the passivation structures, and therefore an appreciable decrease in line loss α. Large-signal measurements performed at 900 MHz further reveal a strong increase in substrate linearity, of approximately 20 dB, achieved through the passivation technique. Finally, a TCAD-based simulation approach enables the investigation into alternate biasing-based passivation structures and the achievable RF substrate figures of merit.**

Keywords- Substrate losses, substrate linearity, effective resistivity, parasitic surface conduction, interface passivation.

I. INTRODUCTION

Nowadays, advanced silicon CMOS are offering competitive radio-frequency (RF) figures of merit [1]. In RF Integrated circuits electrical signals propagate in a conductive metal layer atop an insulator-semiconductor stack. A coplanar waveguide (CPW) is depicted in Fig. 1a atop such a stack of materials (half of the CPW is depicted). To avoid losses in such lines, and also to mitigate coupling between them, it is important for the underlying substrate to have a high *effective resistivity*. Furthermore, it is required that the substrate be as linear as possible to minimize distortion of the line signals. Low-doped silicon is then favoured with high nominal resistivity (ρ_{nom}) above 1 kΩcm. However, the effective resistivity (ρ_{eff}), which is sensed by the overlying planar circuits, can differ strongly from the nominal resistivity ρ_{nom}. This is usually due to the presence of parasitic fixed oxide charges present at semiconductor interface. Then, a highly conductive channel-like layer is induced beneath the insulator, as depicted in Fig. 1a. These charges are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This in turn lowers the sensed effective resistivity by a factor of 10 to 10^4, to values as low as 1 Ωcm. This is referred to as the *parasitic surface conduction (PSC) effect* that renders the use of a high-resistivity (HR) substrate ineffective for improving the performance of overlying ICs as compared to standard-doped Si (ρ_{nom} ~10 Ωcm) [1]. A breakthrough was made in the early 2000s with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide (BOX) in SOI technology [2, 3]. This layer effectively mitigates the PSC effect by pinning the Fermi-level near mid-gap at the interface [4] in a highly resistive state, enabling ρ_{eff} of over 1 kΩcm.

In this paper, a novel concept for combatting the PSC effect is presented, which relies on locally depleting the interface, making it highly resistive. This is achieved by biasing dedicated polysilicon or metal shapes implemented below RF passive devices. Thanks to this *field-effect passivation scheme*, significantly improved linearity and reduced substrate losses are demonstrated.

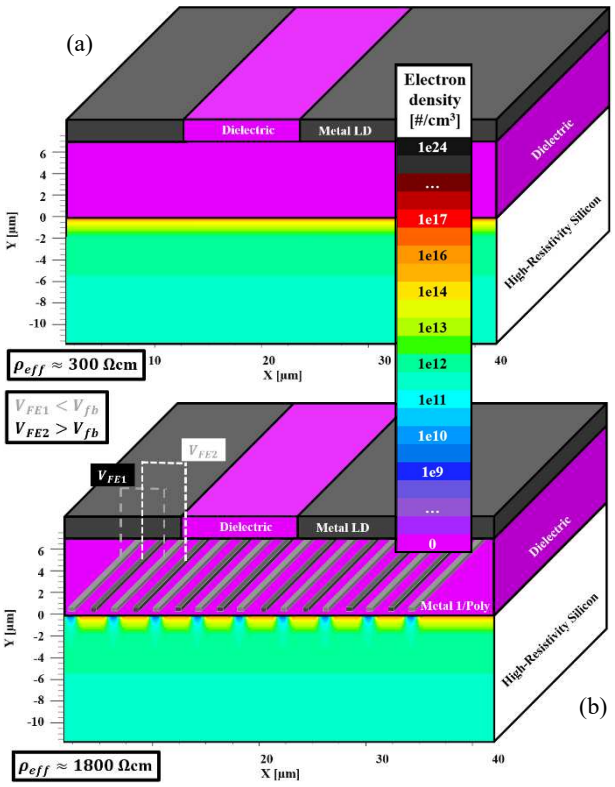

Figure 1. Carrier profile in a HR substrate (with PSC) with (a) and without (b) the FE passivation scheme, below a CPW line in "Metal LD", roughly 13 µm above the Si/SiO2 interface).

This approach is not entirely dissimilar to the PN-implant passivation scheme, which also serves to interrupt the PSC interface layer in HR substrates [5].

In this work, the highly improved quality of CPW lines is demonstrated through the extraction of the ρ_{eff} and linearity metrics by implementing the concept in GLOBALFOUNDRIES' 45RFSOI node.

It should be noted that a similar concept was patented in [6] independently of this research.

For these trials, 45RFSOI was run on HR substrates. Enabling RF performances close to those of TR wafers, this method is compatible with bulk, SOI and FD-SOI technologies.

Finally, a simulation section is included in this work, allowing us to explore potential RF performance results based on the field-effect substrate passivation scheme associated to various biased structures.

II. FIELD-EFFECT PASSIVATION FOR RF

A. Concept: Field-Effect Passivation of PSC

One concept of this passivation is depicted in Fig. 1b, based on an array of adjacent parallel lines implemented in a polysilicon layer, with various bias points applied to the lines. One line in two is biased with V_{FE1}, and the others with V_{FE2}, as illustrated. All lines are biased through large on-chip resistors and are therefore RF-floating nodes (in fact, the poly shapes used to implement them are the core of high-valued RF resistor elements). Through the filed-effect, the applied V_{FE} biases modulate the interface channel (PSC) and can be tuned to interrupt and counter its conductive and lossy nature.

This type of array was implemented physically in GLOBALFOUNDRIES' 45RFSOI technology on HR beneath CPW lines implemented in the topmost metal layer (LD), which is 2.9 µm-thick aluminium at a distance of roughly 13 µm from the Si/SiO_2 interface. The fabricated CPW lines are characterized by a signal-line width of W_c of 35 µm, a gap between signal and ground lines S of 25 µm, and a length L of 2.2 mm.

The field-effect passivation structure is an array of parallel lines of width 0.6 µm, separated by 0.5 µm, and implemented in the polysilicon/M1 layer.

B. RF Measurement Results

These CPWs were measured on-wafer using GSG probes. After pad de-embedding, ρ_{eff} is extracted from the small-signal (S-parameter) data according to [7, 8]. Large-signal measurements performed at 900 MHz enable substrate linearity evaluation, by extracting the power level of the second generated harmonic (at 1.8 GHz) at a DUT fundamental power of +15 dBm.

The measurement results pertaining to the passivated device are plotted in Fig. 2, which illustrates that a fourfold increase in substrate ρ_{eff} (from 420 Ωcm to 1800 Ωcm) is achieved by appropriately biasing the passivation structures to increase substrate impedance by combatting the PSC interface layer.

Linearity is strongly increased simultaneously with ρ_{eff} (expected correlation [9]), as a function of the applied V_{FE} biases, and Fig. 2b demonstrates a 25-30 dB reduction in the device's generated H2 power level by passivating (depleting) the interface through the field-effect scheme.

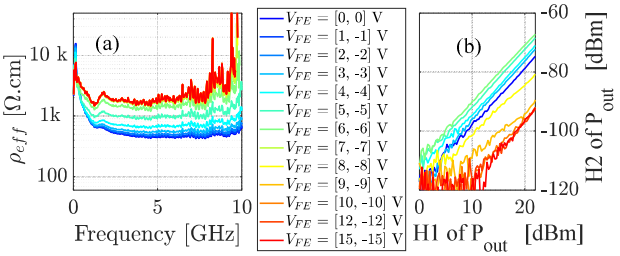

Figure 2. (a) Extracted ρ_{eff} from CPW S-parameter data. (b) Measured second harmonic power (1.8 GHz) vs. fundamental power (900 MHz) at the output of a 2.2 mm-long CPW line.

To highlight these improvements further, Fig. 3 plots the substrate small- and large-signal figures of merit (FoM) as a function of the applied V_{FE}.

When $V_{FE1} = -V_{FE2}$ are large-valued (either significantly higher or lower than the flatband voltage $V_{fb} \approx -5$ V), electron-rich and hole-rich regions are induced below the adjacent passivation line structures, as illustrated in Fig. 1b. Then, depletion regions are created between these regions of opposite polarity, and serve to substantially increase the resistance of the path along the interface. The PSC effect is then effectively countered, and high values of ρ_{eff} –in the range of 2 kΩcm– and low values of H2 –in the range of -107 dBm– are achieved. Fig. 3 shows these results to be competitive with respect to the state-of-the-art trap-rich SOI RF substrate solution.

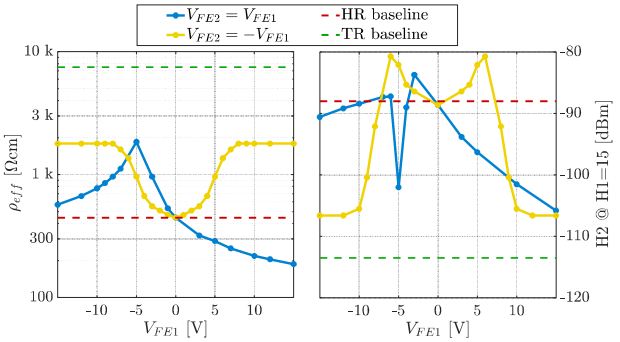

Figure 3. Measured ρ_{eff} (at 5 GHz) and H2 (at H1 = 15 dBm) as a function of the DC bias applied to the passivation structures.

C. Simulation Study

Substrate RF performance on such field-passivated substrates can be evaluated using TCAD tools. By simulating a 2D cross-section of a CPW line on a substrate material stack, the lineic capacitance C and conductance G terms between the central signal electrode and the coplanar ground electrodes of the CPW are obtained. These metrics are the converted into the effective substrate material parameters ρ_{eff} and ε_{eff} [7, 8].

Fig. 4 plots the simulated effective resistivity curves over frequency obtained for several types of field-effect

passivation schemes using lower-level electrode layers (DC biased and RF floating).

In the simulations, these lower-level electrodes are implemented using 100 nm-thick polysilicon that has a resistivity of 50 Ωcm (unless explicitly stated otherwise). The poly layer is situated 200 nm from the Si/SiO_2 interface, and the CPWs (W_c = 26 µm and S = 12 µm) are defined in a 1 µm-thick aluminum layer that is situated 5 µm from the Si/SiO_2 interface.

By applying strong negative/positive biases to an array of poly-Si shapes (each 500 nm wide, with a spacing to each neighboring shape of 1.5 µm), effective passivation is demonstrated. Indeed, ρ_{eff} values in the range of a few kΩcm are achieved, compared to only a few hundred Ωcm when the applied biases are $V_{FE1} = V_{FE2} = 0$ V. These values are in good agreement with the measured data presented in Section II-B.

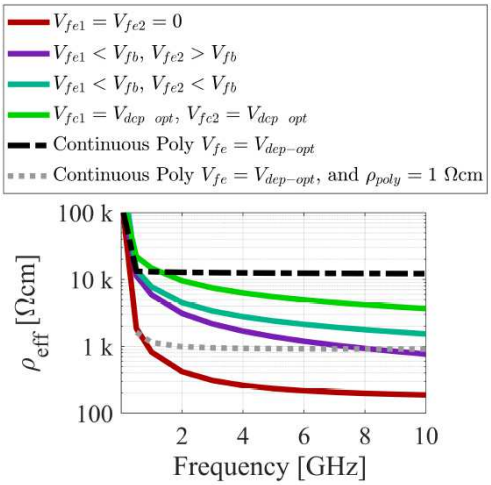

Figure 4. Extracted $\rho_{eff}(f)$ from TCAD-simulated CPW data. Poly-Si thickness is 100 nm, and resistivity is 50 Ωcm.

Fig. 5a presents the electronic configuration in the substrate when an optimal depletion-voltage is applied to the same poly-Si passivation layers. This voltage is defined as the precise condition to apply in order to induce a state of strong depletion at the Si/SiO_2 interface beneath these structures. Fig. 4 demonstrates that in that case ($V_{FE1} = V_{FE2} = V_{dep,opt}$) the ρ_{eff} sensed by the CPW line is higher still, as the TCAD results present values in the 5-10 kΩcm-range over the simulated frequencies.

This concept of accurate interface depletion can be pushed further still, by biasing to $V_{dep,opt}$ a continuous-plane of poly-Si. This is illustrated in Fig. 5b, and the simulated ρ_{eff} curve corresponding to this passivation solution is plotted as the black dashed-line in Fig. 4, which demonstrates that values above 10 kΩcm are achievable under these conditions. In this case of a continuous-plane poly-Si when the interface is in strong depletion, the dominating contributing term to the CPW's lineic G term (and hence to ρ_{eff}) is actually the conductance associated to the poly-Si plane itself. The black dashed curve of Fig. 4 illustrates that a 100 nm-thick layer of 50 Ωcm resistivity contributes only to negligible CPW loss (since ρ_{eff} > 10 kΩcm), however ρ_{eff} would be lower if the layer's thickness is increased or its resistivity decreased. This is illustrated by the dashed gray curve of Fig. 4, obtained from a simulation in which the continuous poly-Si plane's resistivity was set instead to 1 Ωcm. This plane becomes somewhat lossy, as an RF voltage drop occurs over its finite associated resistance value, explaining the 10-fold reduction in overall ρ_{eff} sensed by the overlying CPW.

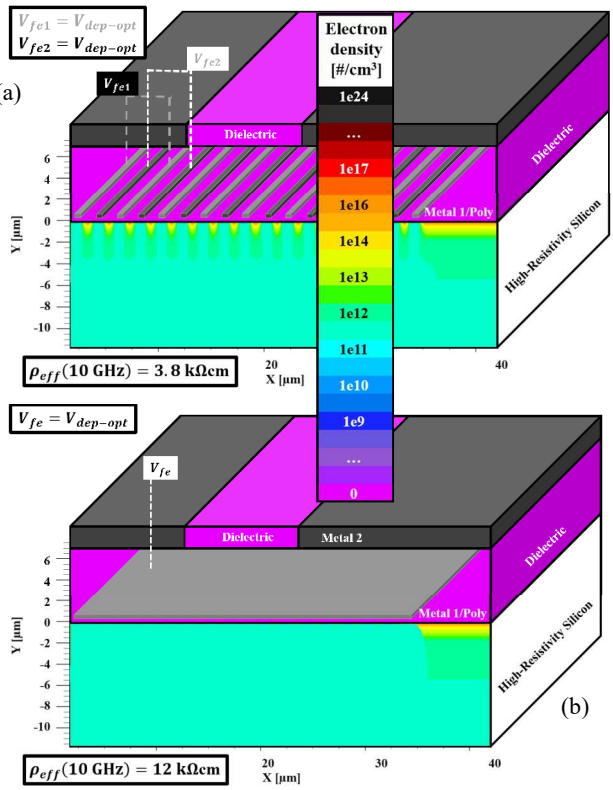

Figure 5. Carrier profile in a HR substrate with (a) the same FE passivation scheme as presented in Fig. 1b but biased to $V_{dep,opt}$ and (b) with a continuous-plane FE passivation structure, also biased to $V_{dep,opt}$.

Practical considerations for implementing such FE-passivation schemes on-chip are discussed in Appendix A.

III. Conclusion

In this paper, a novel interface passivation scheme is presented for enabling high-resistivity RF substrate solutions. It employs low-level metal or polysilicon structures to which DC potentials are applied in order to control the interface impedance. Through this passivation technique, measurements of fabricated CPW lines on such passivated substrates achieved an effective resistivity metric of 2 kΩcm, along with a linearity metric of -107 dBm of H2 generated for +15 dBm of fundamental power at 900 MHz. These competitive RF substrate results offer a new path for the passivation of the PSC effect that dominates the quality of low-doped silicon substrates. This technique is compatible with all types of CMOS technologies (Bulk, SOI, FD-SOI, etc.) and does not require any particular substrate engineering, and is directly implementable at the foundry level.

ACKNOWLEDGMENT

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IV. APPENDIX A: DISCUSSION ON PRACTICAL IMPLEMENTATION

A. Applying $V_{dep,opt}$ in practice

The best results are achieved in terms of ρ_{eff} if an optimized depletion voltage $V_{dep,opt}$ can be applied.

- An idea is to implement a voltage-regulation scheme in order to achieve a depletion condition, regardless of PVT variations.
- However, the $V_{dep,opt}$ to be applied to attain high substrate FoMs may be within quite a narrow range, which may be impractical. This range depends on the distance from the FE layer to the Si/SiO_2 interface, but also depends on the value of the parasitic interfacial oxide charge density N_{ox}. It would then be necessary for the IC designer wanting to implement such a $V_{dep,opt}$ biasing scheme to have an estimate value of N_{ox}. Depending on these parameters, it is to be understood that a $V_{dep,opt}$ value beyond a few volts may be impractical.
- In the simulations pertaining to the continuous-plane depletion-inducing arrangement at 200 nm from the Si interface (results of Fig. 4), simulations revealed that there is approximately a 200 mV bias range that allows for the CPW to sense a ρ_{eff} of at least 1 kΩcm.

If the field-effect layer to be biased is closer to the interface, for example 20 nm (which could arise in practice using an SOI film in a UTBB FD-SOI node) then the aforementioned 200 mV range is reduced to only 20 mV.

If the layer is moved further away from the Si interface, the acceptable biasing range to achieve decent ρ_{eff} increases, but so too does the absolute value of $V_{dep,opt}$ (close to the flatband voltage).

We note that $V_{dep,opt}$ may be multi-valued if the fixed oxide charge density is non-uniform over the Si/SiO_2 interface. Such consideration may be a source of a lack of robustness of exact $V_{dep,opt}$ -based approaches.

B. Continuous-plane solution vs. array-like solution

While applying $V_{dep,opt}$ (necessary for the continuous-plane solution) may require an accurate control of the applied bias, this condition can be lifted if alternate array-like P and N type regions are defined at the interface through the field-effect (see Fig. 1b).

The continuous-plane solution remains very attractive from a designer's point of view, as it alleviates the co-design between the passivation shapes and the RF device.

It is possible to design a viable array-like solution implemented using metallic layers as the filed-effect arrangements with little effect on the CPW's line parameters, while, for the continuous-plane solution, a layer of significantly higher resistivity must be used (details in the next point below).

C. On the resistivity and thickness of the FE passivation layer when implementing a continuous-plane solution

We have seen that decent results are achievable for a 100 nm thick layer of 50 Ωcm resistivity.

- We point out that if the layer was only 10 nm-thick, then similar RF FoM results would have been achieved using 5 Ωcm resistivity, as both implementations would contribute similarly to the line's absolute G parameter.

Using a 100 nm thick layer of 1 Ωcm significantly deteriorated the RF results (see Fig. 4).

Decreasing the resistivity further will continue to lower the ρ_{eff} parameter, until the slow-wave mode is brought about. Then, an RF equipotential sets up in the layer, and there is no longer any V^2/R type loss within it. The field distributions are significantly changed, and the line becomes highly capacitive, and its characteristic impedance and propagation constant are highly modified. If the plane becomes close to being of metallic properties, inductive coupling (Eddy currents) to the plane will further impact on the line's characteristics (not an accountable-for effect using a semiconductor TCAD tool.