On Noise-Induced Transient Bit Flips in Subthreshold SRAM

Léopold Van Brandt*, Fernando Silveira†, Jean-Charles Delvenne* and Denis Flandre*
* ICTEAM Institute, UCLouvain, Louvain-la-Neuve, Belgium
leopold.vanbrandt@uclouvain.be
† Electrical Engineering Department, Universidad de la República, Uruguay

***Abstract*—We propose a rigorous SPICE simulation framework, compatible with industrial process design kits, to observe transient bit flips in CMOS SRAM due to the intrinsic transistor noise. The methodology is illustrated in 28 nm FD-SOI technology. We study the combined effects of the random telegraph noise, flicker and thermal noise sources, for the first time to our knowledge. The extracted mean times to failure are compared to those reported in the literature in extreme voltage, temperature and variability conditions.**

I. Introduction

Subthreshold SRAM bitcells, with supply voltage (V_{DD}) lowered below the transistor threshold voltages or even below 200 mV [1], [2], are highly sensitive to uncertainties [3], notably process *variability*. In [4], we proposed a methodology to predict the variability-induced *failure probability* of subthreshold SRAM cells in retention mode.

The impact of the intrinsic *noise* of the MOS transistors on the functionality of digital logic circuits [5] and CMOS latches [6] operating in ultimate V_{DD} and extreme process and temperature conditions that degrade the noise margins has been addressed in a lesser extent. This concern is reinforced by experimental measurement of large *random telegraph noise* (RTN), e.g. current variations of 30 % [7].

The analytical prediction of the *mean time to failure* ($MTTF$) is still in its infancy [5], [8], [9], while the need for accelerated transient noise simulations has been addressed by [6]. In this work, we propose a rigorous simulation framework, relying on industrial SPICE tools and process design kits (PDK), to observe noise-induced transient bit flips. We exploit the notion of static noise margin to insightfully compare and explain the different results.

II. Methodology

Most subthreshold SRAM bitcells use a cross-coupled inverter pair (i.e. latch, Figure 1(a)) for data retention [2]. A cell is functional as long as it is able to retain the stored state. A noise-induced *bit* or *state flip* is a transient fault that we aim at detecting. The $MTTF$, extracted from simulations, is a metric to quantify SRAM reliability [6].

A. Transient Noise Simulations

Noise simulations are traditionally performed in the frequency domain, while observing noise-induced bit flips requires transient simulations [10] offered in industrial SPICE simulators such as Eldo®. Individual Gaussian noise sources are generated in the time domain according the compact model of the devices. Simulated and measured signals being sampled in time, the noise is generated within a finite *bandwidth*, f_{max}, constraining the (maximum) time step (dt) to be used: $dt = 1/(2\,f_{max})$. There is a CPU-time tradeoff between dt and the total duration of the simulation (to be maximized to record enough bit-flip events). Furthermore, to take into account all contributing noise components, we use $f_{max} \approx 10 \cdot f_p$, where f_p is the circuit bandwidth (here the inverter of Figure 1(a)) estimated from an `AC` (spectral) simulation.

The work has been partially supported by the Research Project "Thermodynamics of Circuits for Computation" of the National Fund for Scientific Research (FNRS) of Belgium.

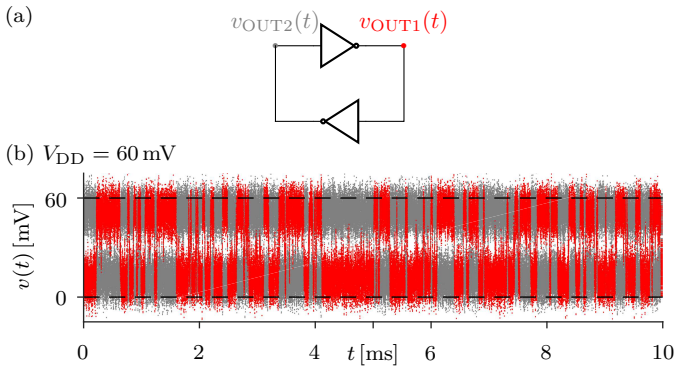

Figure 1. (a) SRAM bitcell in retention mode (b) Transient noise simulation at $V_{DD} = 60$ mV.
Illustrated case: 28 nm FD-SOI RVT inverter of minimal transistor dimensions $L_n = L_p = 30$ nm and $W_n = W_p = 80$ nm, symmetrized, at room T, by a back-gate bias $V_{SB} = 1.6$ V applied to the pMOS.
Bandwidth of the generated noise: $f_{max} = 10$ MHz.

1) Ultimate V_{DD} Lowering: We firstly reduce V_{DD} to the extreme in order to capture several bit flips in accessible computation time (at worse a few days) and to estimate the MTTF for symmetrical latches, at room temperature (T) with only thermal and $1/f$ noise sources embedded in the model. For $V_{DD} = 60$ mV (Figure 1(b)), 70 mV and 80 mV (not reproduced), $MTTF \approx 96$ µs, 8 ms and 18 s.

2) Random Telegraph Noise: To our best knowledge, no widespread PDK incorporates a compact model of the RTN yet. We here introduce it within the Eldo® `NOISETRAN` simulation framework as a series-voltage source $\delta V(t)$ (shown in Figure 2(a)), whose amplitude δV_0 and the mean time constants $\overline{\tau}_c$ and $\overline{\tau}_e$ are approximated independent of the transistor biases in this first trial. The generator is however faithful to the physics of the Markov process [7]. A bit flip occurs at 13.38 ms (Figure 2(b)): when an RTN jump is high and long enough, the low logic state is weakened, so that a peak of Gaussian noise, sufficient both in amplitude and duration, causes the voltage signals to flip.

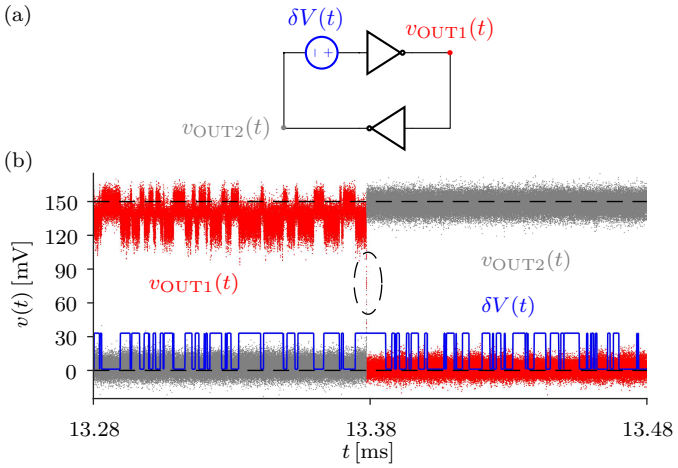

Figure 2. Combined transient RTN and intrinsic Gaussian noise (Eldo® `NOISETRAN`) simulation of the latch (a), where the RTN is modelled as a series-voltage noise applied at the input of one inverter. The RTN parameters are $\delta V_0 = 32\,\text{mV}$, $\overline{\tau}_e = \overline{\tau}_c = 2\,\mu\text{s}$ [7]. Illustrated case: 28 nm FD-SOI Single-P-Well inverter (RVT nMOS and LVT pMOS); $V_B = 0$; $V_{DD} = 150\,\text{mV}$; $T = 120\,°\text{C}$. Bandwidth of the generated Gaussian noise: $f_{max} = 500\,\text{MHz}$.

B. Static Noise Margin and Gaussian Noise RMS Value

The root mean square (RMS) value of the Gaussian voltage noise, denoted σ, estimated empirically from the transient simulations of Figures 1(b) and 2(b), weights about 6 mV for all the presented cases. The relative impact of the Gaussian noise on the stability of the cell can be assessed by the worst-case static noise margin (SNM) [5], whose extraction procedure can be found for example in [3], [4]. The SNM severely reduces with V_{DD} lowering, T increase and variability [3]–[5]. For the SRAM bitcell of Figure 1, the SNM was extracted as 10, 6 and 3 mV at V_{DD} = 80, 70 and 60 mV. In Figure 2(b) where the V_{DD} is 150 mV, the large RTN dynamically reduces the SNM from 29 mV (nominal value) to 15 mV and thereby endangers the noise immunity of the latch.

III. Results and Discussion

To observe transient bit flips due to the thermal and flicker noise sources, former works have combined extreme conditions [5], [6]: sub-200 mV V_{DD}, high T and asymmetric corner (Fast/Slow, resulting in imbalanced inverters). The purpose is to sufficiently reduce the SNM so as to lower the $MTTF$ to the order of a second or less (Figure 3); rarer events are accessible to [6]'s accelerated simulator. For a symmetrical SRAM bitcell, in typical (TT) corner at room T and without additional variability, bit flips can only be recorded provided that V_{DD} gets further lowered (Figure 1). Our results confirm the trend $\log MTTF \propto V_{DD}^2$ suggested by theoretical works [8], [9] (indicated by a dashed line in Figure 3).

In Figure 2, we have simulated a worst-case scenario at the inverter level where nMOS and pMOS transistors are adversely affected by a strong RTN, yielding $\delta V_0 = 32\,\text{mV}$. As highlighted in Figure 3, the $MTTF$ becomes less than

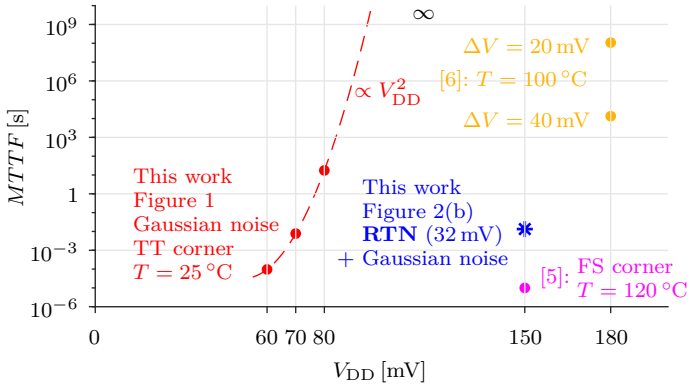

Figure 3. $MTTF$ extracted from simulations in different technologies and various extreme voltage, temperature and variability conditions. [5, Fig. 10]: 32 nm node; $T = 120\,°\text{C}$; Fast/Slow (FS) corner. [6, Fig. 6]: 7 nm predictive PDK; $T = 100\,°\text{C}$; the $\Delta V = \Delta|V_{th,p}| - \Delta V_{th,n} > 0$ is an asymmetric mismatch between nMOS and pMOS transistors applied to each inverter (FS corner).

a second at $V_{DD} = 150\,\text{mV}$. The RTN acts as an additional source of variability reducing the noise margins.

The SNM is always less than 3σ of Gaussian noise for the presented cases. Although instantaneous peaks of 3σ are frequent for a randomly time-fluctuating Gaussian process, there is also a significant requirement on the duration of the transient noise peak to cause a bit flip [11]. This explains why the state-flip events remain *rare*.

IV. Conclusion

Computational intensive noise transient simulations, available in industrial SPICE tools, are required to observe and analyse bit flips in SRAM bitcells. Previous works focused on the worst process and temperature corner cases. In 28 nm FD-SOI, we have shown that Gaussian noise-induced bidirectional bit flips can probabilistically occur in typical conditions when V_{DD} is reduced below 100 mV. We have further studied the combined effects of RTN, flicker and thermal noise at 150 mV. We claim that, whereas process variability remains a major concern, strong RTN that are likely in the smallest transistors lower the $MTTF$ by orders of magnitude and will thus need to be considered for subthreshold SRAM reliability assessment.

References

[1] M. Alioto, *IEEE TCASI*, vol. 59, no. 1, pp. 3–29, 2012.
[2] J. P. Kulkarni *et al.*, *IEEE JSSC*, vol. 42, no. 10, pp. 2303–2313, 2007.
[3] D. Bol *et al.*, *IEEE Trans. on VLSI Systems*, vol. 17, no. 10, pp. 1508–1519, 2009.
[4] L. Van Brandt *et al.*, *IEEE TCASI*, vol. 69, no. 7, pp. 2767–2780, 2022.
[5] F. Veirano *et al.*, *J. of Low Power Electronics*, vol. 12, no. 1, pp. 74–81, 2016.
[6] E. Rezaei *et al.*, *IEEE Trans. on Device and Materials Reliability*, vol. 20, no. 3, pp. 488–497, 2020.
[7] L. Van Brandt *et al.*, in *EUROSOI-ULIS*, 2019.
[8] L. B. Kish, *Physics Letters A*, vol. 305, no. 3-4, pp. 144–149, 2002.
[9] N. Freitas *et al.*, *APS PRE*, vol. 105, no. 3, p. 034107, 2022.
[10] P. Bolcato and R. Poujois, in *IEEE ISCAS*, vol. 2, 1992, pp. 887–890.
[11] J. Lohstroh, *IEEE JSSC*, vol. 14, no. 3, pp. 591–598, 1979.