VO_2-based energy-efficient artificial spiking sensor emulating human-skin-like high-precision temperature perception

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Bioinspired neuromorphic spiking sensors hold great promise for energy-efficient and architecturally simplified neuromorphic networks. Here, an energy-efficient artificial spiking sensor based on a patterned polycrystalline vanadium dioxide (VO_2) memristor grown by direct-current (dc) reactive magnetron sputtering was developed to achieve high sensitivity and low-energy consumption simultaneously. The memristor demonstrates high endurance in both static and dynamic electrical measurements with low cycle-to-cycle variations and excellent spiking performance when integrated into a 1R (memristor)-1T (transistor) spiking circuit. By optimizing the memristor current and output capacitor, the circuit achieves tunable output frequencies of 181–784 kHz under a 5-V supply voltage and an estimated intrinsic capacitance of approximately 0.51 nF. In-sensor temperature encoding is also achieved under a memristor current of 0.1478 mA without an additional external capacitor, exhibiting an excellent sensitivity of 2.98–13.62 kHz/°C, a low total energy consumption of 2.73–5.63 nJ/spike and a signal-to-noise and distortion ratio (SNDR) of 30.95–41.21 dB from 30 to 50 °C, as well as a high resolution of 0.18 °C at 47.5 °C. Compared with conventional CMOS readout integrated circuits, the energy consumption can be further reduced by lowering the supply voltage and minimizing the intrinsic capacitance through full circuit integration, while the SNDR can be enhanced by mitigating the stochasticity of VO_2 and reducing circuit noise, which will require further optimizations of material characteristics and device geometry.

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I. INTRODUCTION

Among the diverse smart sensing nodes used in Internet-of-Things (IoT) networks, accurate temperature detection near the human physiological range (approximately 37 °C) is critically significant for hazard detection related to objects, environments, buildings, and transportation systems, as well as for on-body detection of skin temperature and electronic-skin applications [1–3]. Notably, the human survival wet-bulb temperature threshold is approximately 35°C, while pain perception in human skin begins just above 43°C and burn injuries occur above 44°C [4–6].

Resistive sensors are widely used to measure diverse environmental stimuli owing to their robustness, low cost, high sensitivity and resolution, and ease of integration into miniaturized systems [7,8]. To process these sensory data, energy-efficient and real-time readout integrated circuits (ROICs) have been developed based on complementary metal-oxide-semiconductor (CMOS) technology. These ROICs typically rely on analog-to-digital converters (ADCs) to convert the sensor resistance directly into a voltage amplitude [9–11] or on voltage-controlled oscillators (VCOs) [8,12,13] and relaxation oscillators [9,14–17] to generate time-domain outputs whose period or frequency is proportional to the sensor resistance. However, these sensing systems rely on sophisticated and separate sensing and computing von Neumann architectures, resulting in processing delays and higher energy consumption [18–21].

Beyond the limitations of the von Neumann implementation and conventional silicon technology, spiking neural networks (SNNs) using neuromorphic computing to record dynamic real-time changes in the environment offer a promising approach for scalable and energy-efficient intelligence [22,23]. Bioinspired neuromorphic sensors that emulate neuronal functionalities by transducing physical stimuli directly into spiking signals have recently been developed using Mott memristors with tunable temperature-dependent metal-insulator transitions [24,25]. Vanadium dioxide (VO_2), a representative phase-change material, is widely utilized in the fabrication of memristive neurons for SNNs, thanks to its scalability, stability, high endurance, energy efficiency, CMOS compatibility, and ultrafast transition dynamics near room temperature [26,27]. Either thermally or electrically triggered, VO_2 undergoes a reversible phase transition from a low-temperature monoclinic insulating phase to a high-temperature rutile metallic phase

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near 68 °C [28]. Various physical stimuli, including temperature [3,18,29,30], strain [31–33], light [34–36], and electromagnetic waves [37] can be detected either by the naturally sensitive VO_2 memristor itself or via external sensors coupled to it. Notably, the VO_2 memristor exhibits a sensing temperature close to that of human skin, indicating its potential application in real-time physiological temperature monitoring [3]. To encode the physical stimuli, the VO_2 memristor is implemented in different spiking circuits that control the bias current via a resistor [3,18,30] or a transistor [29,34,37–39]. The latter 1R (memristor)-1T (transistor) configuration is preferred since the transistor provides a stable and constant current supply to the memristor [29]. Capacitors are normally introduced into the spiking circuit [3,18,29] to limit the spiking frequency. In Ref. [30], the external capacitor is removed from the spiking circuit, but a high intrinsic capacitance of 5.5 nF is still observed. When used simultaneously as temperature sensors and oscillators, unpatterned VO_2 spiking sensors have exhibited limited sensitivity below 2 kHz/°C and relatively high energy consumption, while their oscillation and sensing characteristics have not been fully explored [3,29,30].

This work presents the fabrication and comprehensive characterization of a patterned VO_2 spiking sensor capable of energy-efficient and high-precision temperature encoding through high-frequency spiking signals from 30 to 50 °C. The material properties of VO_2 and the static cycle-to-cycle electrical characteristics of the memristor are first investigated. Subsequently, the VO_2 memristor is integrated into a 1R-1T spiking circuit to thoroughly explore the effects of intrinsic or external capacitance as well as the memristor current on the spiking output signals. By utilizing only the intrinsic capacitance, the memristor successfully encodes varying temperature stimuli into distinct spiking signals. In parallel, a dynamic circuit model is adapted to fit the spiking behavior under different operating conditions, and the jitter induced by cycle-to-cycle variations in the spiking outputs is analyzed comprehensively. Finally, by incorporating well-established CMOS figures of merit, the performance of the VO_2 1R-1T spiking circuit is benchmarked against state-of-the-art CMOS ROICs for the first time to our best knowledge, offering valuable guidance for the optimization of future VO_2 memristor architectures.

II. RESULTS AND DISCUSSION

A. Device Structure and static electrical measurements

The schematic of the fabricated VO_2 memristor is shown in Fig. 1(a). A two-terminal VO_2 planar structure is shown in the top-viewed SEM image in Fig. 1(b). The region within the white rectangle represents patterned VO_2 with an area of $50 \times 20\ \mu m^2$ on a SiO_2 (510 nm thick)/Si substrate. Au/Ti (200/10 nm thick) top electrodes were subsequently deposited to define a VO_2 channel with a length of 0.8 μm and a width of 20 μm. Figure 1(c) shows the top and cross-sectional morphologies of the polycrystalline VO_2 layer on a CMOS-compatible Si/SiO_2 substrate with well-defined distinct interfaces. The fabrication and measurement methods and material characterization of VO_2 are shown in Fig. S1 of Supplemental Material [40].

The VO_2 memristor demonstrates stable volatile resistive switching over 1000 cycles, as observed in the voltage-driven *I-V* curves [dark curves in Fig. 1(d)]. A current compliance of 2 mA was applied to prevent overheating and damage to the VO_2 crystalline structure in the metallic state. These measurements were conducted at 40°C under an N_2 flow ambient to minimize the impact of environmental temperature fluctuations. In Fig. 1(d), the insulating resistance (R_{ins}) is defined as the local differential resistance of the *I-V* curves in the insulating state, while $R_{ins,0}$ is extracted by linear regression near zero bias. The metallic resistance (R_{met}) is approximated from linear regression of the *I-V* curves in the metallic state. Insulator-to-metal transition (IMT) is triggered at a transition voltage (V_{IMT}) of 1.288 V, where enhanced Joule heating with increased applied voltage leads to the formation of a metallic filament in the VO_2 channel [41]. This filament further expands until reaching the current compliance, resulting in an abrupt current increase at V_{IMT}. When the applied voltage is reduced, the filament cools down and breaks, driving the VO_2 back to the insulating state once the voltage goes below a metal-to-insulator transition voltage (V_{MIT}) of 0.39 V. The VO_2 memristor retains memory of the previous threshold firing events from one cycle to another, as the prior metallic filament serves as a preferable nucleation site for subsequent cycles [42]. Nevertheless, filament formation in VO_2 still exhibits stochastic relaxation dynamics [43].

Cycle-to-cycle variations are hence observed in the *I-V* characteristics, specifically in V_{IMT}, V_{MIT}, $R_{ins,0}$ and R_{met} [e.g., stochastic distribution of V_{IMT} in Fig. 1(d)]. The scatter plots and histograms of measured V_{IMT} and V_{MIT} over 1000 cycles are extracted in Figs. 1(e) and 1(f), respectively, both demonstrating nearly Gaussian distributions after a slight drift correction (approximately 25 μV, i.e., approximately 0.0019%/cycle for V_{IMT}, approximately 7.5 μV, i.e., approximately 0.0019%/cycle for V_{MIT}). During the measurement, a small voltage step of 1 mV was applied, with each *I-V* cycle lasting approximately 26 s, resulting in prolonged Joule heating, particularly in the metallic state of VO_2, potential device degradation, and slight drifts in the static *I-V* characteristics. Finally, the mean values (μ)/standard deviations (σ) of V_{IMT} and V_{MIT} are determined to be 1.288 V/9.57 mV and 0.39 V/1.42 mV, corresponding to normalized standard deviations (σ/μ) of 0.74% and 0.36%, respectively. Extracted in the insulating state close to zero bias and in the metallic state close to the compliance current, the mean

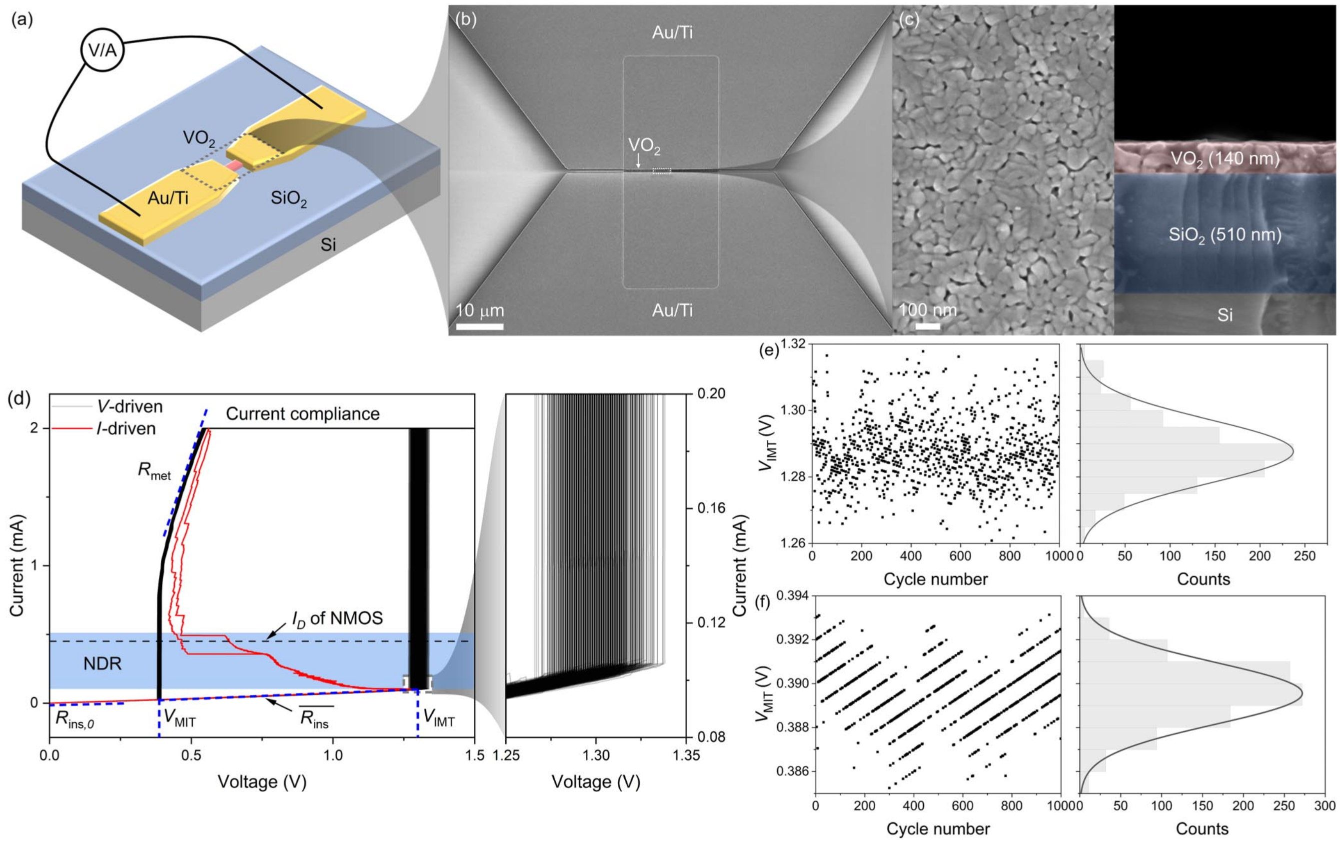

FIG. 1. (a) Schematic diagram (pink, yellow, blue, and gray areas depict VO_2, Au/Ti, SiO_2 and Si layers, respectively) and (b) top-viewed scanning electron microscopy (SEM) image of the measured VO_2 memristor with a $0.8 \times 20\ \mu m^2$ channel. (c) Close-up top and cross-sectional SEM views of the as-deposited VO_2 layer on the SiO_2/Si substrate. (d) Voltage-driven (black curves, 1000 consecutive cycles, each lasting approximately 26 s) and current-driven (red curve, one cycle) current-voltage characteristics of the VO_2 memristor at 40°C, under a current compliance of 2 mA, and a close-up view of the cycle-to-cycle variations of V_{IMT}. (e),(f) Scatter plots and histograms of V_{IMT} and V_{MIT} over 1000 voltage-driven cycles, with 1-mV voltage steps (which limits the resolution on V_{MIT} extraction).

$R_{ins,0}$ and R_{met} are 15461.15 Ω ($\sigma = 124.22$ Ω) and 177.39 Ω ($\sigma = 5.26$ Ω), respectively.

B. Spiking modulation by circuit parameters

In the current-driven *I-V* curve [red curve in Fig. 1(d)], the VO_2 memristor initially exhibits positive differential resistance at low voltage, followed by a sharp cusplike transition into a substantial negative differential resistance (NDR) regime (approximately 0.1–0.5 mA). Biasing the VO_2 memristor within the NDR regime in a spiking circuit triggers self-oscillations between the insulating and metallic states, whereas increasing the current beyond the NDR regime drives VO_2 fully into the metallic state and consequently ceases the oscillation [29]. In this work, a 1R-1T spiking circuit was implemented on a printed circuit board (PCB) [Fig. 2(a)]. An n-type metal-oxide-semiconductor field-effect transistor (NMOSFET, ALD1106), controlled by a constant gate voltage (V_G) and operated in the saturation regime, serves as a constant direct-current (dc) bias current source (I_D) for the VO_2 spiking oscillator. The output characteristics of the NMOSFET are shown in Fig. S2 of Supplemental Material [40]. Two bypass capacitors of 100 μF and 100 nF are connected in parallel to the supply voltage (V_{dd}) and V_G, respectively, to filter high-frequency noise in the circuit. To investigate the impact of output capacitance on spiking behavior, an external capacitor (C_{ex}) can be added to the intrinsic parasitic capacitor (C_{in}) in this work.

To reproduce the experimentally observed spiking behavior at frequencies well below the theoretical thermal limit [44], a compact circuit-level *RC* model is introduced. According to Kirchhoff's current law, the time-dependent equation describing the circuit dynamics can be expressed as

$$C\frac{dV_{out}}{dt} = I_{VO_2} - I_D \quad (1)$$

where the left term represents the current through the total load capacitor ($C = C_{in} + C_{ex}$), and I_{VO_2} is the current through the memristor. Considering VO_2 in its metallic state

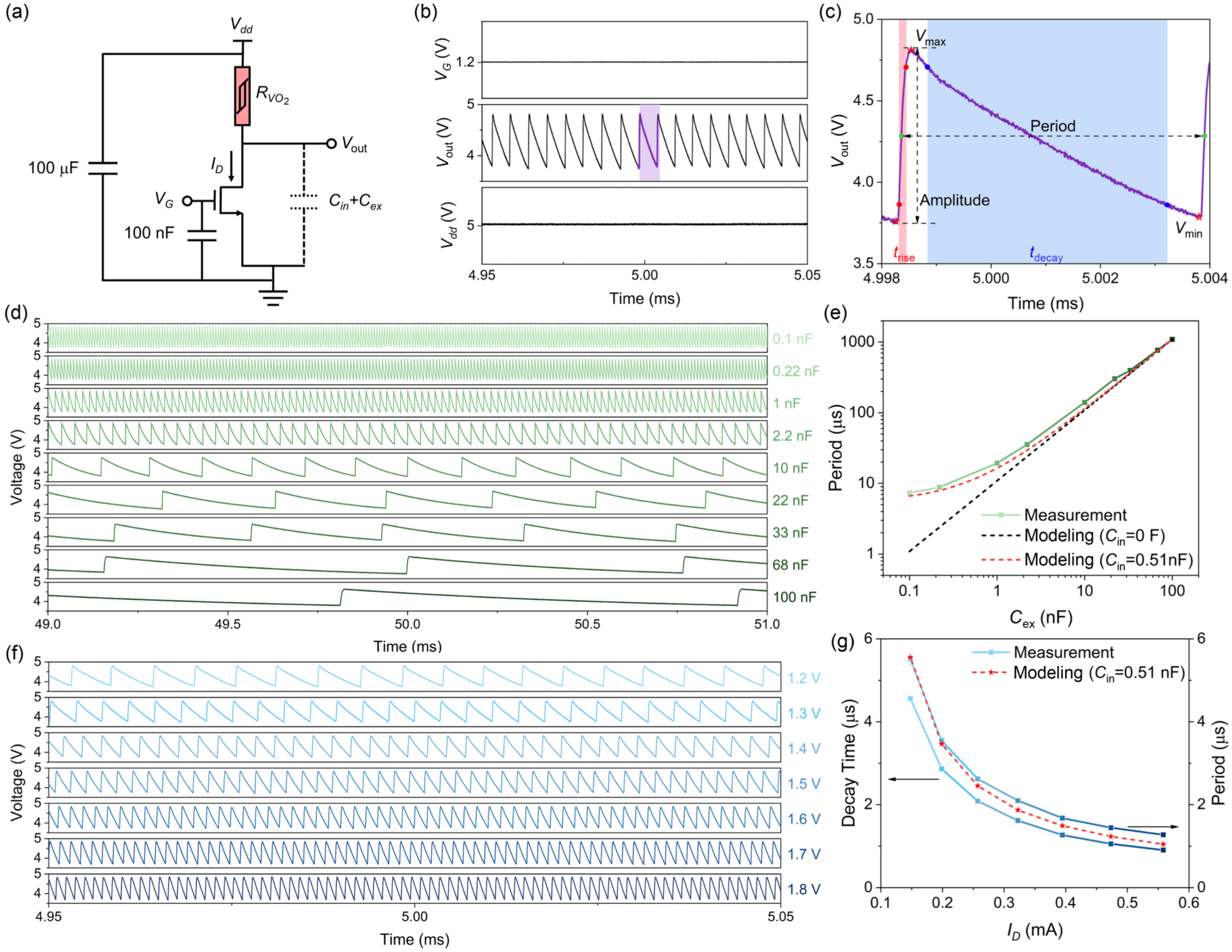

FIG. 2. (a) Circuit schematic of the VO_2 spiking oscillator. Reference spiking waveforms at 40°C, shown over (b) 0.1 ms and (c) one oscillation period within a total measurement time of 10 ms, with V_{dd} of 5 V, V_G of 1.2 V ($I_D = 0.1478$ mA), and no external capacitance. (d) Output spiking waveforms under varying external capacitance from 0.1 to 100 nF, shown over 2 ms within a total measurement time of 100 ms, with V_{dd} of 5 V and V_G of 1.2 V. (e) Period versus $C_{\rm ex}$ from 0.1 to 100 nF, compared with the fits using the dynamic circuit model [Eqs. (2)–(6), black dashed line: $C_{\rm in} = 0$ F, red dashed line: $C_{\rm in} = 0.51$ nF]. (f) Output spiking waveforms under varying V_G from 1.2 to 1.8 V, shown over 0.1 ms within a total measurement time of 10 ms, with V_{dd} of 5 V and without $C_{\rm ex}$. (g) Period and decay time versus I_D varied from 0.1478 to 0.5582 mA, corresponding to V_G from 1.2 to 1.8 V, compared with the period fitted using the dynamic circuit model [Eqs. (2)–(6)] assuming $C_{\rm in} = 0.51$ nF.

(i.e., rapid charging phase of C) or in its insulating state (i.e., slow discharging phase of C), the modeled rise time ($\tau_{\rm rise}$) and decay time ($\tau_{\rm decay}$) are estimated using 0%–100% amplitude thresholds by [34]:

$$\tau_{\rm rise} = R_{\rm met} C \cdot \ln \frac{V_{\rm IMT} - R_{\rm met} I_D}{V_{\rm MIT} - R_{\rm met} I_D} \tag{2}$$

$$\tau_{\rm decay} = \overline{R_{\rm ins}} C \cdot \ln \frac{V_{\rm MIT} - \overline{R_{\rm ins}} I_D}{V_{\rm IMT} - \overline{R_{\rm ins}} I_D} \tag{3}$$

Here, to properly fit the spiking behaviors, we introduce the equivalent insulating resistance ($\overline{R_{\rm ins}} = \overline{V_{\rm ins}}/\overline{I_{\rm ins}}$) calculated using the mean insulating-state voltage ($\overline{V_{\rm ins}}$) and current ($\overline{I_{\rm ins}}$) from $V_{\rm MIT}$ to $V_{\rm IMT}$, according to the mean value theorem for integrals:

$$\overline{V_{\rm ins}} = \frac{V_{\rm IMT} + V_{\rm MIT}}{2} \tag{4}$$

$$\overline{V_{\rm ins}} = \frac{\int_{V_{\rm MIT}}^{V_{\rm IMT}} I_{\rm ins}(V) dV}{V_{\rm IMT} - V_{\rm MIT}} \tag{5}$$

In the previous work [34], $\overline{R_{\text{ins}}}$ was extracted from a linear regression of R_{ins} from 0 to V_{IMT}, which suppresses the nonlinear *I*-*V* behavior and includes the low-voltage range below V_{MIT} that is irrelevant to the spiking dynamics. Here, $\overline{R_{\text{ins}}}$ is instead modeled to capture the overall evolution of R_{ins} from V_{MIT} to V_{IMT}, thereby inherently incorporating both the electrical behavior and the thermal evolution of the VO_2 memristor in the insulating phase during the slow ramp-up of the voltage drop across the device. Furthermore, the oscillation period (τ) and frequency (f) of the oscillator can be expressed as

$$f = \frac{1}{\tau} = \frac{1}{\tau_{\text{rise}} + \tau_{\text{decay}}} \tag{6}$$

Typical reference output waveforms with a duration of 0.1 ms within a total measurement time of 10 ms (1814 cycles) are shown in Fig. 2(b), where V_{dd}, V_G, and V_{out} are monitored using a Tektronix MSO56 oscilloscope. A typical spiking waveform of V_{out} over one oscillation period is shown in Fig. 2(c), illustrating all important figures of merit. When I_D increases into the NDR regime, the memristor first undergoes an abrupt IMT at V_{min}. As highlighted in the red region of Fig. 2(c), a large current flows through the memristor in its metallic state, rapidly charging C and increasing V_{out}. Once V_{max} is reached, the memristor experiences an MIT, reentering its insulating state, as highlighted in the blue region of Fig. 2(c). In this regime, I_D of the transistor slowly discharges C, reducing V_{out} and driving the oscillator back to the IMT threshold to resume oscillation. The experimental rise time (t_{rise}) and decay time (t_{decay}) are extracted using 10%–90% thresholds of the amplitude to avoid fluctuations. The dynamic cycle-to-cycle variations of the parameters extracted from the reference spiking waveform are shown in Fig. S3 of Supplemental Material [40]. No apparent drift is observed in the extracted parameters, which is attributed to the ultrashort t_{rise} of nanoseconds in the metallic state, thereby preventing excessive heating and degradation of VO_2. Compared with static *I*-*V* measurements, the σ/μ values of dynamic V_{IMT} (i.e., $V_{dd} - V_{\text{min}}$) and V_{MIT} (i.e., $V_{dd} - V_{\text{max}}$) are significantly reduced to 0.48% and 0.098%, respectively.

Substituting the figures of merit obtained from the static *I*-*V* measurements in Fig. 1(d) into Eqs. (2)–(6), C_{in} is estimated to be approximately 0.51 nF to fit the measured mean spiking period of 5.51 μs when no C_{ex} is added in Fig. 2(c). Because the rise time (i.e., metallic phase) is very short (approximately 140 ns), the oscillation period is dominated by the decay time (i.e., insulating phase), during which the estimated thermal time constant (< 1 μs [44]) is much smaller than the dominant electrical time constant. Thus, the thermal response can be treated as a fast internal process whose second-order influence is absorbed into the fitted effective *RC* parameters, rather than being introduced as an independent state variable.

In the spiking circuit, the load capacitance and the memristor current controlled by the gate voltage of the transistor are the two most critical circuit parameters for tuning the spiking behavior of the VO_2 oscillator. Various external capacitors are then added in parallel to the NMOSFET, rather than relying only on the intrinsic capacitance. Figure 2(d) gives the output spiking waveforms measured under varying external capacitances (0.1–100 nF) with a duration of 2 ms, within a total measurement time of 100 ms, biased by V_{dd} of 5 V and V_G of 1.2 V. The dynamic cycle-to-cycle variations of period are shown in Fig. S4 of Supplemental Material [40]. Increasing the external capacitance extends the mean spiking period from 7.37 μs ($\sigma = 0.21$ μs) to 1093.08 μs ($\sigma = 56.85$ μs) [green curve in Fig. 2(e)]. To fit the measured spiking period, its variation with capacitance is modeled using the dynamic circuit model [Eqs. (2)–(6)]. Ideally, in the absence of intrinsic capacitance from the oscillator and the measurement system, the spiking period is linearly proportional to the external capacitance, as represented by the black dashed line in Fig. 2(e). This linear trend agrees well with the measured period at large C_{ex}, where the external electrical capacitance dominates the total capacitance. Nevertheless, a tail appears in the measured spiking period when C_{ex} is small and comparable to C_{in}. To reproduce the tail, the previously empirically estimated C_{in} of approximately 0.51 nF is incorporated into the model, yielding close agreement between the measured and modeled spiking period. In the following analysis, to enhance the spiking frequency, no external capacitor is connected in parallel to the transistor, and the frequency is instead determined only by the intrinsic capacitance.

Next, the current flowing through the VO_2 spiking oscillator, controlled by the gate voltage, is investigated to modulate its spiking behavior. Since the transistor is biased in the saturation region, the memristor current remains nearly constant during each spiking cycle. Figure 2(f) shows the output spiking waveforms measured under increasing V_G (1.2 to 1.8 V, i.e., $I_D =$ 0.1478–0.5582 mA) with a duration of 0.1 ms, within a total sampling time of 10 ms, biased by V_{dd} of 5 V and using only the intrinsic capacitance. The dynamic cycle-to-cycle variations of period and decay time are shown in Fig. S5 of Supplemental Material [40]. The mean decay time decreases from 4.561 μs ($\sigma = 42.12$ ns) to 0.906 μs ($\sigma = 7.72$ ns), while the rise time remains nearly constant with increasing I_D. Similarly, the mean spiking period decreases with I_D from 5.51 μs ($\sigma = 146.16$ ns) to 1.276 μs ($\sigma = 19.93$ ns). The oscillation period is also fitted using the dynamic circuit model [Eqs. (2)–(6)], considering an intrinsic capacitance of 0.51 nF and a varying I_D from 0.1478 to 0.5582 mA. Consequently, the modeled period behavior shown in the red curve of

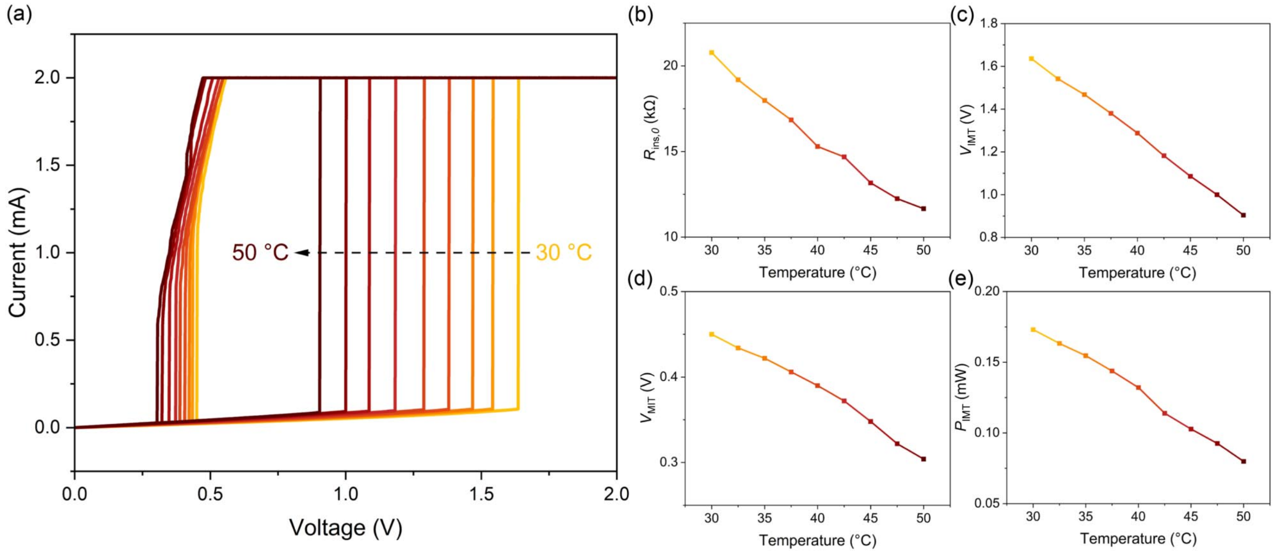

FIG. 3. (a) Voltage-driven current-voltage characteristics of the VO_2 spiking oscillator from 30 to 50 °C by a step of 2.5 °C, with a current compliance of 2 mA. Temperature dependencies of (b) $R_{ins,0}$, (c) V_{IMT}, (d) V_{MIT}, and (e) P_{IMT} from 30 to 50 °C.

Fig. 2(g) demonstrates excellent agreement with the measured behavior.

C. Temperature encoding

To perform temperature encoding in the VO_2 spiking sensor, its intrinsic temperature-dependent phase transition properties are first investigated. As shown in Fig. 3(a), the spiking behavior is modulated by the voltage-driven *I-V* characteristics under increasing temperatures from 30 to 50 °C, with a current compliance of 2 mA. As the temperature rises, $R_{ins,0}$ [Fig. 3(b)] near zero bias decreases from 20.78 to 11.66 kΩ, allowing the memristor to reach a lower V_{IMT} of 1.636 to 0.904 V [Fig. 3(c)] at an insulator-to-metal transition current (I_{IMT}) reduced from 0.1058 to 0.0883 mA. Physically speaking, $R_{ins,0}$, V_{IMT}, and I_{IMT} are jointly modulated by Joule heating and field-assisted carrier generation (e.g., Poole-Frenkel effect) [45,46]. The quasilinear temperature dependence of V_{IMT} indicates that the IMT is dominated by the Joule heating. In contrast, exponentially decreasing behavior ($V_{IMT} \propto \exp(-T/T_0)$) would be observed if the Poole-Frenkel effect dominated [47,48].

During the reverse transition back to the insulating state, V_{MIT} [Fig. 3(d)] decreases from 0.45 to 0.304 V with increasing temperature and decreasing R_{met}, which is attributed to Newton's law of cooling [3,45]. Consequently, the temperature-dependent hysteresis window $V_{IMT} - V_{MIT}$ is gradually narrowed, enabling the VO_2 spiking sensor to simultaneously perform thermal sensing and spike encoding for efficient temperature detection. $P_{IMT}(= V_{IMT}I_{IMT})$, the power required to trigger the IMT transition, is reduced linearly from 0.173 to 0.0798 mW with increasing temperature, as shown in Fig. 3(e). The linear regression of P_{IMT} similarly indicates that the IMT transition is dominated by Joule heating [49].

Inspired by biological sensory neurons, the VO_2 spiking sensor can be employed to detect and encode stimulus information (here, temperature) into spiking neuronal signals by using the spiking circuit in Fig. 2(a). The real-time temperature-dependent output spiking waveforms with a duration of 0.1 ms within a total measurement time of 10 ms are obtained in Fig. 4(a) from 30 to 50°C with a temperature step of 2.5°C, biased by V_{dd} of 5 V and V_G of 1.2 V ($I_D = 0.1478$ mA), without an external capacitor. The sensor exhibits highly stable and repeatable temperature encoding behavior over a wide temperature range. The output spiking behavior is modulated by the parameter variations discussed in Fig. 3, leading to reductions in resistance and voltage amplitude, thereby enhancing the spiking frequency. The scatter plots and histograms of the spiking amplitude and frequency are presented in Figs. 4(b) and 4(d), respectively. As the temperature increases, 1436–2806 cycles are recorded in 10 ms from the VO_2 spiking sensor, without clear drift observed throughout the measurements. The mean amplitude extracted in Fig. 4(c) decreases from 1.336 V ($\sigma = 19.28$ mV, $\sigma/\mu = 1.44\%$) to 0.609 V ($\sigma = 8.14$ mV, $\sigma/\mu = 1.34\%$), primarily thanks to the increased mean V_{min} (associated with a lower V_{IMT}) from 3.391 to 4.125 V. As shown in Fig. 4(e), the mean frequency increases from 143.71 kHz ($\sigma = 3.128$ kHz, $\sigma/\mu = 2.18\%$) to 280.7 kHz ($\sigma = 3.355$ kHz, $\sigma/\mu = 1.2\%$) as the temperature rises from 30 to 50 °C. Once the temperature exceeds 50 °C, the sensor stops oscillating owing to the gradual extinction of the NDR. The exponential frequency increase with temperature is attributed to the decrease in decay time, which is dominated by the reduction of V_{IMT} and $R_{ins,0}$. Using the

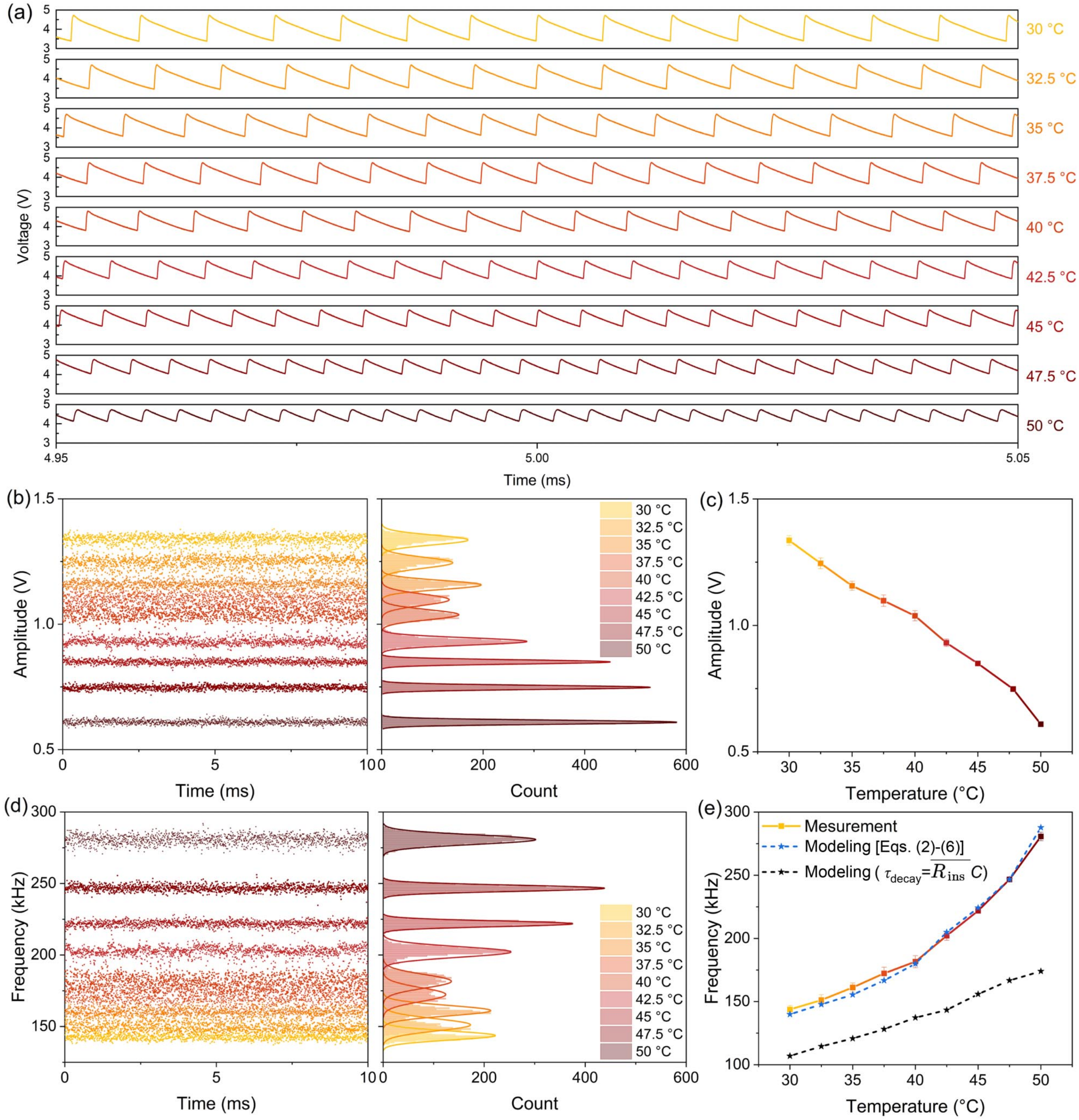

FIG. 4. (a) Temperature encoding of the VO_2 spiking sensor from 30 to 50 °C, shown over 0.1 ms within a total measurement time of 10 ms, with V_{dd} of 5 V, V_G of 1.2 V, and without external C. Scatter plots and histograms of (b) amplitude and (d) frequency from 30 to 50 °C measured over 10 ms. (c) Amplitude and (e) frequency versus temperature diagrams from 30 to 50 °C, compared with the fitted frequency using only the first factor of τ_{decay} and the full expression of the dynamic circuit model [Eqs. (2)–(6)].

parameters extracted from the temperature-dependent static I-V curves in Fig. 3 and assuming an intrinsic capacitance of 0.51 nF, the spiking frequencies calculated with only the first factor of τ_{decay} [i.e., $\overline{R_{\text{ins}}}C$ in Eq. (3)] and with the full expression are modeled in Fig. 4(e) by Eqs. (2)–(6). At lower temperatures, the relative increase in frequency is dominated by the quasilinear behavior of $\overline{R_{\text{ins}}}$. At higher temperatures, the reduction in V_{IMT} contributes more significantly to the relative increase in frequency, leading to a superlinear tendency. Consequently, the dynamic circuit model reproduces the exponential tendency and shows excellent agreement with the measured frequency behavior.

To better evaluate the temperature response, the temperature sensitivity (S_f) is defined as the change in frequency (Δf) with respect to the change in temperature (ΔT):

$$S_f = \Delta f/\Delta T \tag{7}$$

where S_f increases from 2.98 to 13.62 kHz/°C from 30 to 50 °C, calculated based on successive frequency points in Fig. 4(e). The measured temperature can be accurately evaluated from the temperature sensitivity, but the spiking frequency jitter originating mostly from the cycle-to-cycle variations in the sensor behavior [29] introduces uncertainty in the temperature encoding. Resolution (δT) is defined as the ratio of the frequency standard deviation (σ_f) to the temperature sensitivity [50]:

$$\delta T = \frac{\sigma_f}{S_f} \tag{8}$$

At 47.5 °C, δT reaches 0.182 °C ($\sigma_f = 2145.52$ Hz), while S_f is approximately 11.77 kHz/°C, derived from a linear fit of the frequency response between 45 and 50 °C in Fig. 4(e).

D. Benchmarking and performance comparison

Energy-efficient and versatile resistive sensor readout integrated circuits (ROICs) based on CMOS technology are widely used in smart sensing applications in the IoT era to process diverse environment stimuli. Therefore, it is essential to benchmark our 1R-1T spiking circuit against state-of-the-art CMOS ROICs using their well-established figures of merits (FOMs), including energy per conversion (EPC), signal-to-noise and distortion ratio (SNDR), and Walden's figure of merit (FOM_W).

EPC_{VO_2}, the energy required to generate a single spike in one period (τ) of the VO_2 spiking oscillator, can be divided into static and dynamic components:

$$EPC_{VO_2} = E_{stat} + E_{dyn} = V_{dd} I_{dd} \tau + \frac{CA^2}{2} \tag{9}$$

where E_{stat} is the static energy to trigger oscillation and E_{dyn} is the dynamic energy required to charge the load capacitance during the spike rise time, thereby changing the output voltage by the spike amplitude (A). However, for CMOS ROICs, E_{dyn} is generally neglected since the load capacitance is only a few picofarads. Therefore, the energy required to convert one analog value into its digital or frequency representation [16,17] is divided into the static energy (EPC_{ROIC}) consumed by the sensor and the ROIC:

$$EPC_{ROIC} = \tau_c \cdot (P_{sens} + P_{ROIC}) \tag{10}$$

where τ_c is the conversion time, and P_{sens} and P_{ROIC} represent the power consumed by the sensor and the ROIC, respectively. For ROICs based on relaxation oscillators or VO_2 oscillators, τ_c corresponds to the period of an oscillation cycle, whereas for ADC- or VCO-based ROICs, multiple digital conversions or oscillation cycles are considered within one conversion time. Therefore, ADC- or VCO-based ROICs are not directly comparable with VO_2 oscillators.

Furthermore, SNDR, defined as 10 times the logarithm of the ratio between the signal power and the noise power, is calculated from the ratio of the period or frequency to its jitter [18]:

$$\mathrm{SNDR} = 10 \log_{10} \frac{\mu_\tau^2}{\sigma_\tau^2} = 10 \log_{10} \frac{\mu_f^2}{\sigma_f^2}. \tag{11}$$

When comparing ROICs with different structures, SNDR and EPC can be combined into a single Walden figure of merit (FOM_W), which relates the energy consumption to the conversion rate and its uncertainty [51]:

$$\mathrm{FOM}_W = \frac{\mathrm{EPC}}{2^{\mathrm{ENOB}}}, \tag{12}$$

where the effective number of bits (ENOB) is derived from the measured SNDR by [51]:

$$\mathrm{ENOB} = (\mathrm{SNDR} - 1.76)/6.02. \tag{13}$$

Significantly higher temperature sensitivity and lower energy consumption are achieved for the VO_2 spiking sensor presented in this work compared with other reported VO_2 spiking sensors, as summarized in Table I. Removing the external capacitors significantly enhances the temperature sensitivity and reduces the energy consumption compared with Refs. [3] and [29], where the external capacitors reduce the circuit dynamics. Furthermore, the intrinsic capacitance is reduced by a factor of 10, leading to up to 8 times higher sensitivity than in Ref. [30]. Although integrating a commercial temperature sensor in the VO_2 spiking circuit can extend the temperature range [18], its temperature sensitivity remains much lower than that in this work, due to the naturally higher temperature sensitivity of VO_2. As the temperature increases from 30 to 50 °C, E_{stat} and E_{dyn} of the sensor decrease from 5.14 and 0.49 nJ/spike to 2.63 and 0.1 nJ/spike, respectively. The total EPC_{VO_2} of 2.73–5.63 nJ/spike achieved in this work is much lower than 90–154 nJ/spike reported for a sensor driven by a similar circuit architecture in Ref. [29] and is comparable to state-of-the-art VO_2 spiking sensors implemented with standard *RC* circuits [18,30]. Meanwhile, the sensor in this work achieves a better temperature resolution than that reported in Ref. [29] and a higher SNDR than those reported in Refs. [18,29].

Next, Fig. 5 compares the static EPC and SNDR of the VO_2 spiking circuits with those of CMOS ROICs based on relaxation oscillators, considering a conversion time of one period. The detailed parameters for this comparison are shown in Table SI of Supplemental Material [40]. The

TABLE I. Comparison with reported VO_2 spiking sensors for temperature encoding.

	Temperature (°C)	C (nF)	V_{dd} (V)	I (mA)	f (kHz)	E_{stat}[a] (nJ/spike)	E_{dyn}[a] (nJ/spike)	S_f (kHz/°C)	δT (°C)	SNDR (dB)
[18][b]	30–100	2	5	…	100–300	2.9		2.8	…	29.92
[3]	21–42	10	5	…	17–35[c]	50		~0.9[c]	…	…
[29]	41–47	33	2.55	1	17.3–29.3	87–147[c]	2.8–7[c]	1.7	0.26[d]	33.3[d]
[30]	20–40	Intrinsic, 5.5	…	0.11	16.8–60.2	3		1.7	…	…
This work	30–50	Intrinsic, 0.51	5	0.1478	144–280	2.63–5.14	0.1–0.49	2.98–13.62	0.18[e]	30.95–41.21

[a]Digitization energy to obtain a digital representation of frequency is not considered.
[b]Temperature detected by an external sensor instead of VO_2 memristor.
[c]Not explicitly mentioned by the authors but estimated from the graphs or other numerical values.
[d]δT and SNDR extracted at 43 °C.
[e]δT extracted at 47.5 °C.

static EPC values of the ROICs used for benchmarking do not include the digitization and sensor energy consumption but focus on the energy consumption required to convert one analog value into its frequency representation. The ROICs are capable of processing analog signals from a wide range of resistive sensors, rather than from a specific application. Compared with ADC or VCO-based ROICs, ROICs based on relaxation oscillators offer the capability to simultaneously achieve ultralow power consumption, a wide input resistance range, and high SNDR above 55 dB [14,16,17]. In comparison, the VO_2 spiking circuit demonstrates close performance in terms of EPC, although there remains room for further improvement in both the resistive sensor and the oscillation circuit, notably in terms of SNDR.

a) In conventional temperature sensing, external sensors such as Pt100 and Pt1000 with a positive temperature coefficient (TC) of 0.385%/°C [52] or silicon thermistors with a TC of > 0.7%/°C can be connected to the ROIC on a PCB. These CMOS ROICs [14–17] typically occupy an on-chip area of 0.1–0.3 mm^2, but large external sensors significantly increase the overall PCB area and reduce the integration density. To reduce the chip area below 0.01 mm^2, advanced CMOS technology nodes enable monolithic integration of the temperature sensor and ROIC on a single chip [53–56]. However, the TCs of integrated polysilicon resistors (approximately 0.3%/°C) [53,54] and wire-metal resistors (0.1%–0.2%/°C) used in, e.g., sub-28-nm processes [55,56] are lower than those of external sensors.

Using VO_2 spiking sensors enables a significantly higher TC with a very compact 1R-1T circuit implementation that could require a very small area after optimization. As calculated from Fig. 3(b), the insulating resistance of VO_2 exhibits an average measured negative TC of −2.19%/°C from 30 to 50°C, exceeding previously reported values for undoped VO_2 (−1.12%/°C [57], −1.65%/°C [58]). Moreover, employing the VO_2 oscillator for temperature sensing leads to a relative increase in output frequency of 2.1%/°C (30–32.5 °C) to 5.5%/°C (47.5–50 °C), owing to the additional contribution from the temperature-induced reduction in V_{IMT} as discussed in

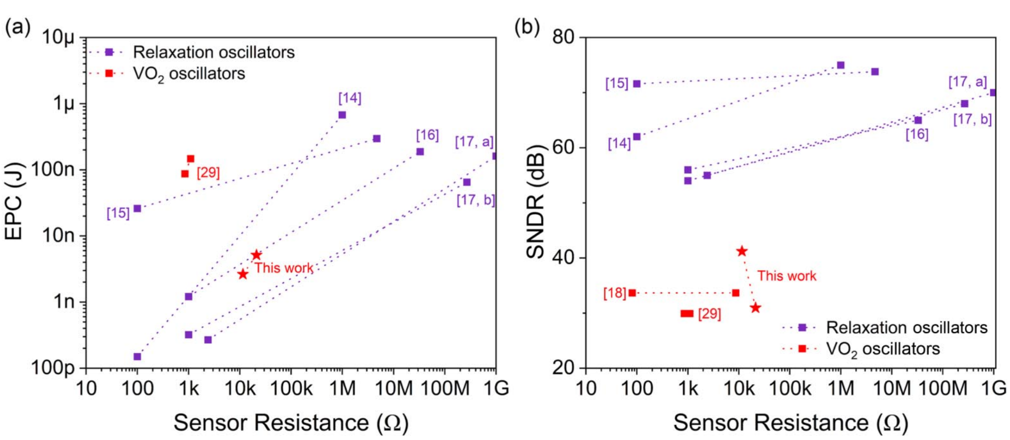

FIG. 5. (a) Static EPC and (b) SNDR of VO_2 spiking oscillators compared with CMOS ROICs based on relaxation oscillators, considering a single oscillation cycle.

Fig. 4(e). Meanwhile, the VO_2 1R-1T spiking circuit could potentially be scaled down to an area of only a few hundred μm^2 in future combined integrations, considering a VO_2 channel size of 0.8×20 μm^2 and, for example, a standard 180-nm CMOS process for bias transistor integration.

b) Operating as a temperature-sensitive oscillator, the VO_2 spiking circuit demonstrates low static EPC, comparable to that of CMOS ROICs [14–17], and could be further improved by lowering V_{dd} and I_D as well as minimizing the intrinsic capacitance. Specifically, E_{stat} can be decreased to approximately 2.57–1.32 nJ by lowering V_{dd} to approximately 2.5 V, as long as $V_{\min}$ remains above ~1 V to keep the transistor in its saturation region, or by lowering the hysteresis window of the memristor (i.e., $V_{\mathrm{IMT}} - V_{\mathrm{MIT}}$). I_D could be lowered by decreasing the channel dimension and the VO_2 thickness [59,60]. The integration capacitance of advanced CMOS ROICs is generally only a few picofarads [14,16,17], whereas the intrinsic capacitance in the present VO_2 spiking circuit still reaches 0.51 nF. This high capacitance originates primarily from PCB, probe station, and wire connections. To achieve a capacitance of only a few picofarads, the 1R-1T circuit must be fully integrated onto a single chip in the future.

As shown in Table SI of Supplemental Material [40], although the FOM_W of the temperature-sensitive VO_2 spiking circuit is comparable to those of CMOS ROICs [14–17], a lower *SNDR* of 30.95–41.21 dB is achieved for the VO_2 spiking circuit in this work, compared with the typically higher values exceeding 55 dB for CMOS ROICs [14–17]. The *SNDR* of the VO_2 spiking circuit can be further improved by reducing the stochasticity of the VO_2 oscillators, by tuning the material geometry [60] or using other structures like VO_2 nanowires [61], and by minimizing the noise within the 1R-1T circuit.

III. CONCLUSIONS

In conclusion, this work presents an in-depth investigation of the static and dynamic electrical characteristics, as well as the temperature-encoding properties, of an artificial spiking sensor based on a polycrystalline vanadium dioxide (VO_2) memristor grown by dc reactive magnetron sputtering. The fabricated VO_2 memristor demonstrates high endurance at 40 °C over 1000 cycles of static electrical measurements, with low cycle-to-cycle variations of 0.74% and 0.36% for V_{IMT} and V_{MIT}, respectively. By implementing the memristor in a 1R-1T spiking circuit, the stochasticity is further reduced to 0.48% and 0.098%, for dynamic V_{IMT} and V_{MIT}. Introducing external capacitors from 0.1 to 100 nF, the spiking period increases nonlinearly from 7.37 μs to 1093.56 μs due to an intrinsic parasitic capacitance of approximately ~0.51 nF from the VO_2 oscillator and the measurement setup. Increasing the memristor current from 0.1478 to 0.5582 mA and removing the external capacitor expands the output frequency to 181–784 kHz. By combining the high negative TC of $R_{\mathrm{ins},0}$ (−2.19%/°C) with the lowered V_{IMT}, the VO_2 spiking sensor exhibits efficient in-sensor temperature encoding from 30 to 50°C, achieving an excellent sensitivity (2.98–13.62 kHz/°C) and a high resolution (0.18 °C at 47.5 °C) without an additional external capacitor. Meanwhile, a low static EPC (2.63–5.14 nJ) comparable to most CMOS ROICs is obtained, although the SNDR (30.95–41.21 dB) remains lower than that of CMOS ROICs (> 55 dB). To further reduce the energy consumption and enhance the SNDR, full circuit integration and VO_2 optimization will be essential to minimize the supply voltage, intrinsic capacitance, chip area, circuit noise, and material stochasticity. Overall, the VO_2 spiking sensor integrated in a simple 1R-1T circuit exhibits great potential as an energy-efficient and low-noise alternative to sophisticated CMOS ROICs, providing a promising route toward high-performance sensory systems with strong potential for integration into neuromorphic computing and edge AI platforms.

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DATA AVAILABILITY

The data that support the findings of this article are not publicly available upon publication because it is not technically feasible and/or the cost of preparing, depositing, and hosting the data would be prohibitive within the terms of this research project. The data are available from the authors upon reasonable request.

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