A Compact 120 GHz LNA in 22 nm FD-SOI with Back-Gate Controllable Variable-Gain

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***Abstract*—This paper describes the design and implementation of a 113.5-127 GHz D-band LNA using GlobalFoundries' 22 nm FD-SOI technology. The proposed design achieves 6.6 dB of minimal noise-figure in-band for a peak gain of 17.5 dB at its nominal bias for a 27.5 mW power-consumption using a low supply voltage of 0.75 V, and can achieve an NF down to 6.1 dB and gain up to 19.1 dB in a high-performance state. On top of that, the LNA can be configured as a variable-gain device by making use of the unique back-gate bias node of the 22FDX® technology. In that case, a 9.7 dB gain-control is achieved over a 2 V bias range at the back-gates. The design achieves a low area of 0.039 mm² thanks to its layout based on compact transformers.**

***Keywords*—LNA, variable gain, beyond 5G, mm-wave, sub-THz, D-band, FD-SOI, transformer, noise-figure (NF).**

I. Introduction

The 60 GHz of continuous spectrum that it offers makes D-band (110-170 GHz) of particularly high interest for next generations of communication standards (such as 6G) targeting data rates up to 100 Gbit/s, as well as being an appealing band for high-accuracy radar systems [1].

Today, commercially available technologies such as sub-30 nm fully-depleted silicon-on-insulator (FD-SOI) nodes offer transit- (f_t) and maximum oscillation- (f_{max}) frequencies up to 350 GHz [2], along with low noise performance and low power consumption, making such nodes strong candidates for mm-wave and sub-THz front-end modules (FEM). On top of those RF performances, silicon-based technologies have the advantage of offering state-of-the art digital and baseband circuitry alongside FEMs, supporting an efficient monolithic single-chip integration of a full communications system.

In this paper, the design and measurements of a differential 113.5 to 127 GHz low-noise amplifier (LNA) with 9.7 dB variable-gain in GlobalFoundries' 22 nm FD-SOI node are presented. Overall, the highly compact design achieves 17.5 dB of peak gain for 6.6 dB of minimum noise figure under its nominal bias condition (0.75 V supply for 27.5 mW).

II. Circuit Design

The LNA design includes four stages based on common-source differential-pair cores with cross-coupled neutralization capacitors for stabilization, as illustrated in Fig. 1a.

The interstage matching circuits are based on compact transformer cells, that include center-tap connections that provide the biasing for the amplifier cores.

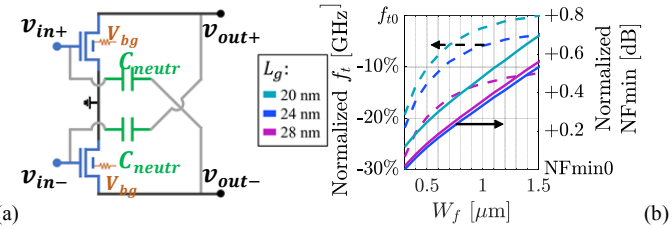
At the input and output, the matching circuits are also based on transformer elements, and those passive networks are implemented to function simultaneously as baluns to drive the differential circuit in a balanced manner. It is worth noting that this design choice based on transformer elements inherently comes with the benefit of electrostatic discharge (ESD) protection from the interfacing input/output pads.

The overall schematic along with the core layout of the 4-stage LNA is presented in Fig. 2.

A. Transistor Dimensions

The choice of the transistor finger width (W_f) dictates the gate resistance of the device and also affects strongly the NFmin value. Shorter W_f values are then preferred for LNA designs, though this comes at the price of increased fringing capacitances at the finger tips and therefore to a lower f_t, as can be seen from the simulation-based data of Fig. 1b.

The length L_g of each transistor was relaxed from the nominal 20 nm to 24 nm to reduce noise contribution from the gate accesses. This trade-off is highlighted in Fig. 1b. Relaxing L_g to 24 nm comes with a little sacrifice in f_t (and therefore available gain of the stage) but for improved noise figure (NF). It is also shown that relaxing L_g further to 28 nm only degrades f_t without any significant change in NF. For these reasons, the gate lengths were set to 24 nm.



(a) (b)

Fig. 1. (a) Core amplification stage based on a common-source differential pair with neutralization feedback capacitors. (b) Simulated normalized ft and NFmin as a function of transistor finger width for a mm-wave SLVT-NFET device biased to Vg = 0.4 V, Vbg = 2 V, Vd = 0.75 V.

In this work, W_f was set to 0.5 µm, prioritising NFmin performance while suffering an acceptable degradation in f_t. Each transistor was sized using 33 fingers, separated into 3 parallel transistors of 11 fingers each.

The bias point was set to V_g = 0.4 V, V_{bg} = 2 V, and V_d = 0.75 V to perform the nominal design. This point was chosen in order to implement a flexible design, capable of reducing its performance metrics (gain and NF) by decreasing the overdrive voltage on the devices through the lowering of the high-valued V_{bg} from the nominal 2 V down to 0 V. This approach leads to an LNA design that can efficiently trade-off power for performance and targeting around 10 dB of gain control through the V_{bg} tuning of the four stages.

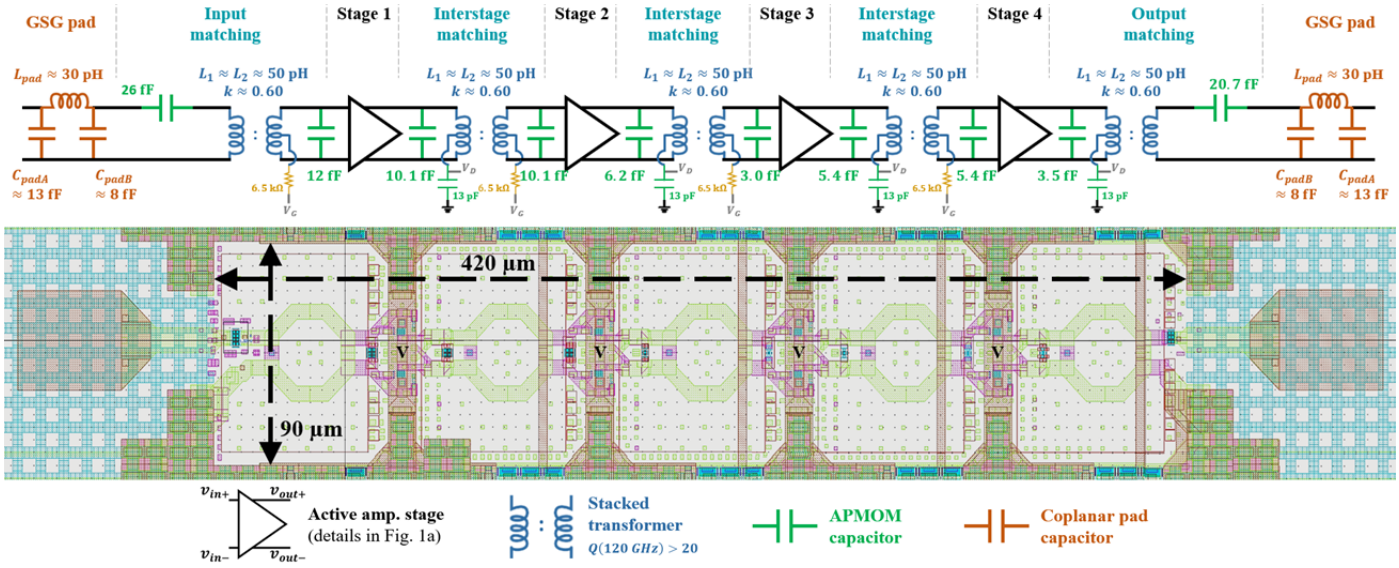


Fig. 2. Schematic diagram of the 4-stage LNA design and associated layout view.

The cross-coupled neutralization capacitors were sized to be approximately 5.5 fF, compensating for the device's C_{gd} feedback capacitor and unconditionally stabilizing the differential amplification stages over a wide band.

B. Stage Matching

The first stages of the LNA are sourced-matched close to Γ_{opt} in order to achieve close to minimal noise-figure performance, while the last stages are closer to achieving conjugate matching at their sources to maximize the gain.

These slight variations in source impedances seen from each stage are implemented in practice through the tuning of the MOM capacitors present in parallel with each coil of the transformers, as shown in Fig. 2. Perfect conjugate matching is applied at slightly different frequencies for the four stages in order to broaden and flatten-out the overall gain response targeting close to 15 GHz of 3 dB-gain bandwidth.

C. Parasitic and EM Simulations

FETs with reference planes up to metal 8 (metallization optimized for low electro-migration) were chosen for this design, in order to rely on the accurate PDK models as heavily as possible and avoid any potential mis-estimation of parasitic elements from low-level interconnects at high frequencies.

At such high-frequencies, all metallic parasitics must be carefully controlled as even small values of parasitic inductors or capacitors impact strongly the node impedances.

During the design process, three major parts of the circuit were simulated as standalone sub-layouts using EM simulators, and mainly take advantage of the topmost metal alu-cap layer (LB) and the two topmost 3 µm-thick copper layers (QA / QB):

1) GSG Probe Pads

Being compatible for 100 µm-pitch GSG probes, the central signal pads in the topmost metal layer (LB) have a dimension of 40 µm height for 50 µm length. After which comes a transition to the QB layer which runs in total over approximately 20 µm of length.

Overall, this pad contributes to approximately 21 fF of shunt capacitance towards the surrounding ground plane and to around 30 pH of series inductance (depicted in Fig. 2).

2) Transformers

All five transformers are implemented having their two inductors as single-turn stacked coils in the QA and QB layers. Using a width of 6 µm and an inner diameter of 27 µm, the two coupled inductors have self-inductance values of approximately 50 pH and a coupling factor k of 0.6. Those values were determined through optimizations by dedicated EM simulations, enabling Q-factors of approximately 22 at 120 GHz to be achieved (thanks to the high-quality "option 19" back-end of line tailored for mm-wave applications [3]).

3) Interconnects Around Differential Pair

The feedback paths for the neutralization capacitors (paths in grey in Fig. 1a) contribute to non-negligible series inductance. Through careful layout optimization based on EM simulations, the total series inductance in those paths was reduced from 35 pH to 20 pH. Considering their series combination with 5 fF neutralization capacitor at 120 GHz, this optimization reduces their impact on the total imaginary part of the feedback impedance from 11% to 7%.

The common-sources of the differential pair transistors are connected to the overall metallic RF ground plane of the device through LB to M1 vias. Their location is noted by the "V" symbols in Fig. 2. Again, the overlying LB connections were carefully tailored to avoid coupling to the adjacent transformers in the compact design, while still providing a good connection from the ground-plane to the device sources.

Once the individual EM simulations have been optimized to provide the desired response from those different circuit sub-blocks for the desired LNA performance, a full-layout EM-solve was run for a more accurate simulation. In that case, all parts of the layout are connected together into a *single* EM simulation layout that takes into account all coupling, interactions and feedbacks present in the final layout design.

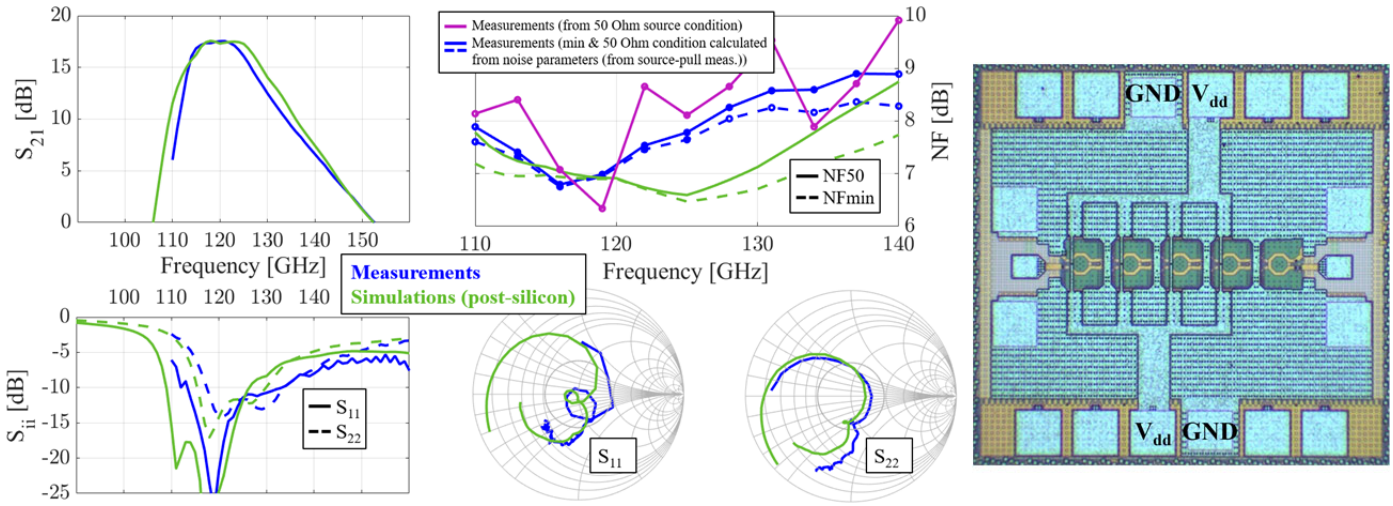


Fig. 3. (a) Measured and simulated performance of the final design at nominal bias (Vg = 0.4 V, Vbg = 2 V and Vdd = 0.75 V). (b) Microphotograph of the LNA.

Some discrepancies were observed between the full-layout EM simulation and the partitioned-layout EM simulation due to some proximity interactions in the compact layout. The slight change in the LNA behaviour was compensated for by tailoring the MOM capacitors influencing the different interstage matching circuits to achieve again an optimal response. All values of the implemented MOM capacitors are given in Fig. 2, corresponding to those included in the most accurate full-layout final design simulation (and fabrication).

III. Measurement Results

A. Setup

The fabricated LNA was measured on-wafer using a tuner-based D-band noise measurement setup from Focus Microwave capable of simultaneously measuring the device's S-parameters. In this setup, the noise figure can be measured directly under 50-Ohm environment or calculated from the extracted noise parameters by using source-pull techniques [4].

The LNA was biased using two 6-pin DC probes placed in the north and south configuration at 90° to the RF probes through the pads depicted in the microphotograph of Fig. 3b. These probes include decoupling capacitors that, along-side on-chip integrated decoupling elements, serve to enforce a wideband decoupling between the V_{dd} pins and the GND pins of the LNA (see associated label in Fig. 3b), and in this configuration, all stages of the LNA are unconditionally stable over a wideband (verified from DC to 200 GHz).

B. Performance

The S-parameter and noise-figure measurement results are plotted in blue in Fig. 3a. Under the nominal bias condition of V_g of 0.4 V, V_{bg} of 2.0 V, and V_{dd} of 0.75 V. At this bias the 4-stage LNA draws a DC power of 27.5 mW and achieves a peak gain of 17.5 dB at 120 GHz, with its 3 dB-bandwidth spanning approximately 13.5 GHz, from 113.5 to 127 GHz.

The amplifier is well matched in that band, with the measured S_{11} being below -10 dB from 112 to 134 GHz. S_{22} is below -10 dB from 117 to 134 GHz.

The measured noise figure from the two techniques agree well, and the amplifier achieves a minimum noise figure value of 6.6 dB at 117 GHz. Furthermore, the NFmin curve (extracted from the full "noise parameter" technique using source-pulling) demonstrates that optimal noise-figure matching has been achieved at the input of the first stage.

C. Model-Hardware Correlation

Fig. 3a also plots simulation results for the LNA at nominal bias.

The correlation is excellent in terms of the S-parameter data, with in particular the two in-band resonant behaviours of S_{11} and S_{22} close to the center of the smith chart being well captured. The gain S_{21} is also well modelled, in terms of in-band peak value, general shape, and out-of-band roll-off.

The minimum simulated NF point occurs at 125 GHz instead of at 117 GHz, but overall the trend and values of the NF data correlate well, with at most 1 dB discrepancy to the measurements.

D. Operation Modes: Power vs. Performance Trade-Off

The LNA's V_{dd} bias can be tuned to trade-off performance (Gain and NF) for DC power consumption.

Measurement results pertaining to those states are plotted in Fig. 4a. It includes the nominal supply-bias of V_{dd} = 0.75 V along with a higher V_{dd} point of 0.9 V and two lower V_{dd} points down to 0.5 V.

At V_{dd} = 0.9 V, the *high-performance mode* is achieved, with a peak gain of 19.1 dB and a minimum NF of 6.1 dB, at the price of an increased power consumption of 34.8 mW.

At V_{dd} = 0.5 V, the *low-power mode* is achieved, consuming only 17.5 mW for a peak gain of 15.5 dB and a minimum NF of 7.2 dB.

E. Operation Modes: Variable Gain Control

As mentioned in Section II.A, the nominal back-gate was chosen as 2 V so that the overdrive voltages on the gates of the LNA stage-cores could be reduced by lowering V_{bg}, providing less gain per stage towards variable-gain control.

Table 1. Performance Benchmarking Against State-of-the-Art CMOS D-Band LNAs.

Reference		Technology	Topology	Gain (peak) [dB]	Bandwidth [GHz]	NF (min.) [dB]	P_{DC} [mW]	Area [10^{-3} mm²]
[5]	TMTT18	28 nm FD-SOI	4-sage CS single-ended, slow-wave coupled CPWs	15.7	143-166	8.5	32	340*
[6]	RFIC20	45 nm RF-SOI	3-stage CS differential, transformers	17.2	137-151	6.4	30	250*
[7]	RFIC21	22 nm FD-SOI	4-stage CS differential, transformers	20	133-146£	9.2$	20	60*$, 32*%
[8]	EuMIC22	22 nm FD-SOI	4-stage CS differential, transmission lines	17	117.6-142.4	8	60	133*
[9]	RFIT22	40 nm CMOS	4-stage CS differential^, transforms. & T-lines	8.7-21.2&	146-151&	8.1µ	34-46&	240*
[10]	IMS22	22 nm FD-SOI	4-stage CS differential, transmission lines	9.0-18.0&	146.6-157.4&	7.5-9.3&	17.5-27.5&	90*
This work	Low-Power	22 nm FD-SOI	4-stage CS differential, transformers	15.5	113-127	7.2	17.5	39*
	Nominal			17.5	113.5-127	6.6	27.5	
	High-perf.			19.1	113.5-127	6.1	34.8	
	Var.-Gain			8.1-17.8&	116.5-127&	6.6-8.9&	8.0-38.1&	

* without pads (core) & variable gain (VG) % without T/R switch $ with T/R switch ^ with cascoded output µ at max. setting (46 mW)

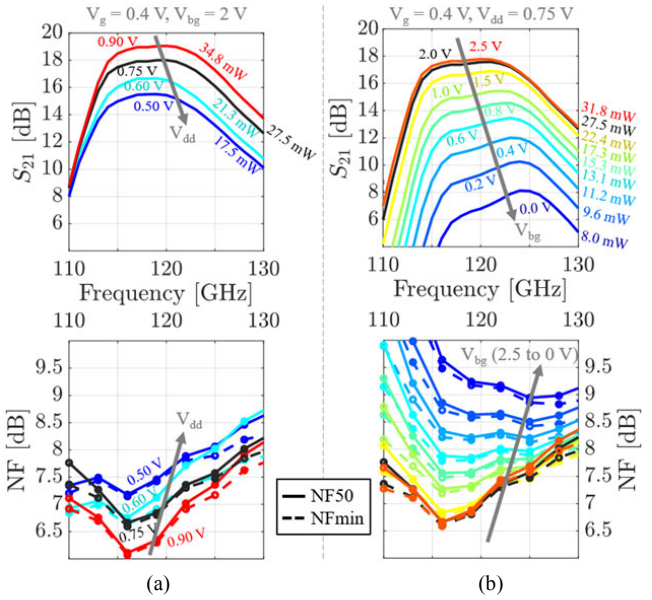


Fig. 4. Gain and NF: (a) vs. decreasing Vdd, and (b) vs. decreasing Vbg.

Fig. 4b plots the gain and NF at the nominal bias with a sweep on the V_{bg} value of all stages, from 2.5 V down to 0 V.

The variable gain functionality is well achieved, with a control range of 9.7 dB in the peak gain as a function of V_{bg}. The DC power consumption improves down to below 10 mW for the lowest gain settings, while the NF degrades to a value of up to 8.9 dB (up from 6.6 dB). This NF values remains acceptable for a D-band LNA. The input matching remains similar to that of the nominal bias condition (see Fig. 3).

The performance results of the presented LNA are recapped in Table 1 in all operation modes and compared to the state-of-the art CMOS D-band LNAs from the published scientific literature.

IV. Conclusion

This paper described the design and implementation of a 113.5-127 GHz D-band LNA using GlobalFoundries' 22 nm FD-SOI technology. The proposed design achieves 6.6 dB of minimal noise-figure in-band for a peak gain of 17.5 dB at its nominal bias for a 27.5 mW power-consumption using a low supply voltage of 0.75 V, and can achieve an NF down to 6.1 dB and gain up to 19.1 dB in a "high-performance state" using an 0.9 V supply for 34.8 mW consumption.

On top of that, the LNA can be configured as a variable-gain device by making use of the unique back-gate bias node of the 22FDX® technology. In that case, a 9.7 dB gain control (from 17.8 to 8.1 dB) is achieved over a 2 V bias range at the back-gates, while maintaining a good NF value (6.6 to 8.9 dB).

Overall, the proposed design achieves excellent results with respect to the state of the art (see Table 1), reporting low NF and low power, along with low area (0.039 mm²) thanks to its compact layout based on small-sized transformer elements.

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