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Probe-Dependent Residual Error Analysis for Accurate On-Wafer MOSFET Measurements up to 110 GHz

L. Nyssens, *Graduate Student Member, IEEE*, S. Ma, M. Rack, *Member, IEEE*, D. Lederer, *Member, IEEE* and J.-P. Raskin, *Fellow, IEEE*

***Abstract*—Advances in CMOS technology have enabled MOSFET with cutoff and maximum oscillation frequencies (f_t and f_{max}) in the 400 GHz range, thus opening the path to CMOS-based applications at millimeter-wave (mm-wave) and sub-THz frequencies. Accurate compact models and therefore on-wafer MOSFET measurements at mm-wave frequencies and beyond become crucial for IC design at such high frequencies. However, accurate on-wafer measurement at these frequencies is a complex task requiring dedicating special care to calibration kit (calkit) design and characterization. This paper presents a complete and detailed parasitic correction procedure approach that demonstrates accurate corrected MOSFET measurements up to 110 GHz. It describes the custom calkit designed to perform 'in-situ' multiline Thru-Reflect-Line (mTRL) calibration. In this work, we compare different methods to evaluate the transmission line standards characteristic impedance and identify the best one by comparing the extracted series resistances of a MOSFET. The best method features frequency variations as low as <5% and <20% in source-drain and gate resistances, respectively, up to 110 GHz. Finally, by applying the most suited correction procedure to measurements of different RF probe technologies and comparing them to compact model simulations, we demonstrated high-accuracy FET measurements up to 110 GHz, thanks to an excellent agreement between the probe data and simulations, even in presence of probe-dependent residual errors.**

***Index Terms*— calibration, characteristic impedance, FD-SOI, fmax, millimeter-wave, multiline TRL, MOSFET characterization, on-wafer, RF probes, transmission line.**

I. INTRODUCTION

THE advances in semiconductor technology have opened the path to applications operating at millimeter-wave (mm-wave) and sub-THz frequencies. CMOS technology with its low-cost integration of digital and analog circuitry coupled with its high RF performance has become a serious contender of III-V technologies in the RF and mm-wave domain. Fully-depleted silicon-on-insulator (FD-SOI) technology notably exhibits the best-in-class RF performance among CMOS, described by the cutoff and maximum oscillation frequencies (f_t and f_{max}, respectively) that are as high as 365 GHz and 413 GHz for the same device [1].

To enable circuit design at mm-wave frequencies and beyond, compact models of high accuracy including very high frequency effects such as non-quasi-static (NQS) effects are essential. To construct these models, accurate transistor measurements in the high mm-wave spectrum range and beyond is needed.

However, on-wafer measurement becomes a complex task above a few tens of GHz. Special care to the de-embedding strategy [2], structures design and floorplan [3] are needed for high-frequency measurements and modeling. Indeed, it is now commonly accepted that the best high-frequency measurements are obtained when the calibration reference plane is placed as close as possible to the device, via an *'in-situ' calibration* [2], [4], i.e. when the calibration standards measurement and the device-under-test (dut) measurements are performed with a similar on-wafer environment.

Furthermore, the in-situ calibration method used is another essential choice to make. Multiline Thru-Reflect-Line (mTRL) [5] has the strong advantage of not relying on any electrical model for its standards, and therefore, its accuracy is not degraded when the actual standard behavior deviates from its model (either due to standard inaccurate characterization, incomplete model or fabrication tolerances), contrarily to lumped-based calibrations. For that reason, mTRL is usually preferred for on-wafer high-frequency measurements.

However, while the propagation constant (γ) of the transmission line (TL) standards is accurately extracted with the mTRL algorithm, the characteristic impedance (Z_c) is not and is rather tricky to evaluate. Its knowledge is required to transform the measurements reference impedance from Z_c to 50 Ω.

For CPW lines on low-loss substrates (such as commercial calibration substrates), Z_c is commonly evaluated from the extracted γ and the TL per-unit-length capacitance (C) as $Z_c = \gamma/j\omega C$ [6], while C is usually evaluated with the load method [7]. This Z_c evaluation method assumes the TL per-unit-length conductance (G) is negligible and C is frequency-independent. We shall refer to this method [6]-[7] as Marks' method in the following. Marks' method is often referred to as the benchmark method, as it was demonstrated to be valid (at least up to 40 GHz) for CPW lines on low-loss substrates [8], however, it

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Lucas Nyssens, Shiqi Ma, Martin Rack, Dimitri Lederer and Jean-Pierre Raskin are with the Institute of Information and Communication Technologies, Electronics and Applied Mathematics, Université catholique de Louvain, Louvain-la-Neuve, Belgium, (phone: +3210478386; e-mail: lucas.nyssens@uclouvain.be).

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is not applicable to dispersive lines or CPW lines on lossy substrates.

The other main technique is called the calibration comparison technique [9], in which a first-tier calibration is performed with its reference plane at the probe tips (usually on a commercial calibration substrate), then a second-tier calibration is realized on the transmission lines to be characterized. The Z_c of the TL is finally extracted from the error box terms describing the change between the two calibrations [10]. While it is commonly used to characterize a wide variety of transmission lines (as it does not make any assumption on the type or behavior of transmission line), its accuracy is limited in general at high frequencies [11].

In [11] another method is proposed to improve the accuracy of the calibration comparison technique at higher frequencies. Although it was used to extract a TL model in the sub-THz range, *it has never been used for on-wafer calibration toward FET measurement and characterization* to the best of the authors' knowledge. Its operation will be further described in the text.

Aiming accurate MOSFET measurements up to 110 GHz, this paper extends [12] in which the accuracy of different calibration and de-embedding approaches were evaluated on the extraction of extrinsic series resistances of a MOSFET on the 22FDX® technology. It was found for the designed calibration kit (calkit) that the in-situ mTRL calibration followed by a classic Open-Short de-embedding also show the best accuracy. However, measurements with three different RF probe technologies demonstrated significant uncorrected probe-dependent bumps that are mainly visible in the extracted gate resistance and f_{max} curves.

In this work, we first extend [12] by improving the calibration method accuracy using the Z_c extraction method described in [11]. Secondly, measurements with a different probe technology are presented and its effect compared to the other ones. Thirdly, we analyze the probe-dependent residual error effect on a larger set of corrected MOSFET measurements with reference plane in M1, which include extrinsic and intrinsic parameters effect: gate capacitance, transconductance, f_t, etc.

So, this paper is organized as follow. Section II presents the designed calkit and its standards characterization. First, the standards' layouts are described. Then, the transmission line γ and Z_c are extracted for different probe measurements and with different methods. The probe-dependent errors observed in γ and Z_c are discussed via the measurements of different Open de-embedding structures. Then, Section III compares the effect of different Z_c extraction techniques on the evaluation of a MOSFET series resistances. Finally, Section IV presents the impact of probe-dependent residual errors on the MOSFET measurements in high RF performance conditions.

II. Calkit Presentation and Characterization

To move the calibration reference plane as close as possible to the dut (MOSFET) and perform in-situ calibration, i.e. with an on-wafer environment similar as the situation when the dut is measured, a dedicated calkit is designed in the same chip. This section first introduces, then presents the characterization results of the designed calkit and de-embedding structures.

A. Calkit structures and dut presentation

The designed calkit consists of a multiline TRL calkit, along with additional standards (such as a Load) and de-embedding structures (Probe-Short, Short-M1, Open-M1). A super-low-threshold voltage (SLVT) nMOSFET from 22FDX® technology featuring a 20 nm gate length and total width of 64 µm is used as dut in this work. The FET is measured in common-source configuration with port 1 and 2 connected to the gate and drain, respectively. A back-gate bias of 0 V is used in this paper.

The 22FDX® stack option used in this work has a backend-of-line (BEOL) with 11 metal layers (labeled from M1 to M7 and thicker layers M8 to M11). Fig. 1 shows a sketch of the transmission line cross-section. The transmission line signal is designed in a 9 µm-wide thick M10 layer. The ground plane is made of several thin metal layers and one thick metal layer for a combined thickness of >1 µm (M1-M8). Ground sidewalls are also present at 12.7 µm from the signal line in order to comply to the minimum density design rules without needing to add any dummy fills. Due to the relatively short distance between the signal line and ground sidewalls, the transmission line is effectively a grounded coplanar waveguide (G-CPW) line. The dimensions are selected to achieve a 50 Ω characteristic impedance (Z_c). Lines of multiple lengths (67 µm, 207 µm, 625 µm, 1648 µm) are fabricated, along with dedicated Open and Short to enable wideband mTRL calibration. The Open (Short) shares the same footprint and probe to probe distance (of ~188 µm) as the Thru to ease the measurements, thus with an 18 µm long opening (shorted section).

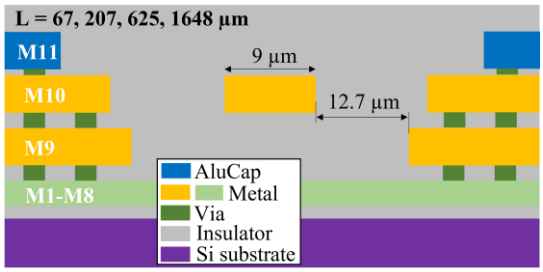


Fig. 1. Sketch of in-situ calkit transmission line, with dimensions.

The RF signal pad in M11 is 60 µm long, 40 µm wide and 15 µm away from the ground pads. A ground shield beneath the signal pad is designed to prevent the electric field to enter in the lossy Si substrate by stacking only the 5 thin bottom-most metal layers (M1-M5) for a reduced pad capacitance. The Open structure measurement yields a 15 fF shunt capacitance for the Open structure. A sketch of the Open is given in Fig. 2(a). The nMOSFET (dut) is designed in a separate structure with the same pads and accesses as the in-situ calkit, with the same footprint (and probe to probe distance) as the Thru, Open and Short structures. It lies inside an opening in the TL's ground plane. In addition, Short and Open structures with all

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the FET access parasitics down to M1 are included (called Short-M1 and Open-M1) for a complete measurement correction down to M1.

The chip floor management is designed to present similar first neighboring structures on the left and right side of each measured structure: in-situ calkit standards, FET and its Open-M1 and Short-M1 de-embeddings. The top and bottom structures share the same ground plane, which saves some area with a limited impact on probe coupling, since their coupling is stronger in the horizontal (x) direction [13]. The structures are separated by 105 µm in the x-direction and their ground planes are tied together by a uniform ground plane using the 7 thin bottommost metal layers (M1-M7), as proposed in [3], [14] in order to present a neighbor environment that is as close as possible for all structures (cf. Fig. 2(b)) and to eliminate the possibility of slot modes between grounds of adjacent structures.

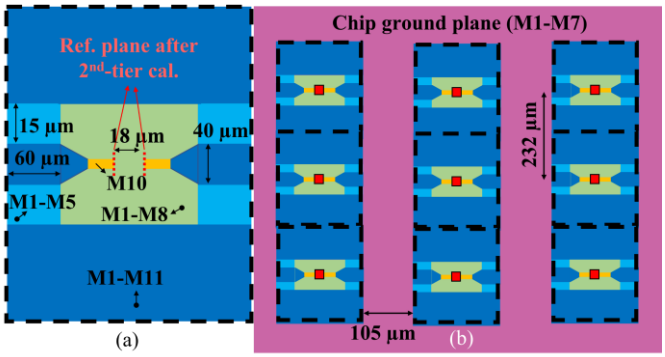


Fig. 2. Sketch of Open calkit standard (a) and floorplan (b).

B. Standards characterization

Measurements of the calkit standards, dut and de-embedding structures have been performed with FormFactor Infinity I67 probes ('I67') from 0.1 to 67 GHz and with 110 GHz Picoprobe GGB ('GGB'), MPI TITAN™ ('TITAN') and FormFactor Infinity I110 ('I110') probes from 0.2 to 110 GHz. All probes have a 100 µm pitch. First-tier calibrations are performed on the commercial calibration substrate specific to each probe technology (101-190C for I67, CS15 for GGB, AC-2 for TITAN and 104-783A for I110). LRRM calibration with WinCal XE is used as first-tier calibration for all probes. The second-tier calibration is performed on the in-situ standards described above.

The first step is to characterize the transmission line standards. They are fully described by the propagation constant (γ) and characteristic impedance (Z_c). γ is accurately extracted with the mTRL algorithm, while Z_c is obtained with the calibration comparison technique [10]. The extracted Z_c and γ are shown in Fig. 3, along with full-wave (3D electromagnetic) simulations of the TL standards.

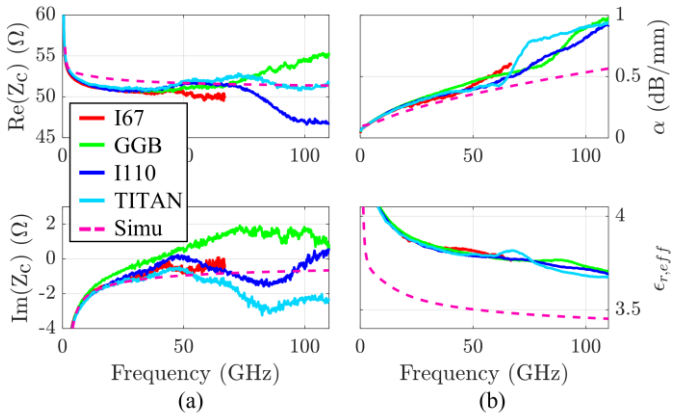


Fig. 3. Extracted characteristic impedance (a) and propagation constant (b) extractions from transmission line standards measurements. $\alpha \equiv \mathrm{Re}(\gamma)$, $\varepsilon_{r,eff} \equiv -(\mathrm{Im}(\gamma)/\omega)^2/(\varepsilon_0\mu_0)$.

We see some strong bumps in measurements of the propagation constant (around 40 GHz for I67, 60-90 GHz for GGB, 40-70 GHz for I110, 50-90 GHz for TITAN) that are not expected from the intrinsic transmission lines (smooth behavior of full-wave simulations). The mTRL algorithm extracts γ as part of the self-calibration process [5], [15], and γ does therefore *not depend on the first-tier calibration*, contrarily to Z_c. As these bumps vary according to the probes, they are attributed to probe coupling with the nearby on-wafer environment. We will further discuss about the probe-dependent bumps later on. There is an overall satisfying agreement between the simulations and the measured γ and Z_c. A small ~7% discrepancy in $\varepsilon_{r,eff}$ remains, which might be explained by fabricated structures with material parameters that slightly deviate from their typical values that are used in the simulation (different metal conductivity or dielectric permittivity values). Better agreement could be achieved by accounting for potential fabrication corners variation, fewer layout simplification, etc., but an exact agreement is out of scope of the paper.

The extracted Z_c also varies significantly from probe to probe. Contrarily to γ, Z_c does depend on the first-tier calibration. So, the probe-to-probe variations can be partially explained by significant systematic deviations coming from the first-tier calibration performed on different calibration substrates. Then, there are still some bumps that seem correlated (similar frequency ranges) to the observed bumps in γ.

As mentioned in Section I, there are other methods to extract Z_c, in particular the benchmark Marks' method used for CPW lines on low-loss substrates [6]-[7]. In this method, Z_c is extracted from the propagation constant measurement, assuming the per-unit-length C is constant and G = 0 (per-unit-length *RLGC* elements of a TL).

Let us apply it here to the I110 probes measurements as it features the smoother γ. Fig. 4 shows the extracted Z_c, per-unit-length C and G terms from the transmission line using different methods. As we clearly see in Fig. 4(c)-(d), C *is not constant with frequency* and G *is clearly positive*, thus invalidating the two assumptions used in the benchmark method to

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evaluate Z_c. So, using this method to evaluate the Z_c of these lines should induce a significant error in extraction.

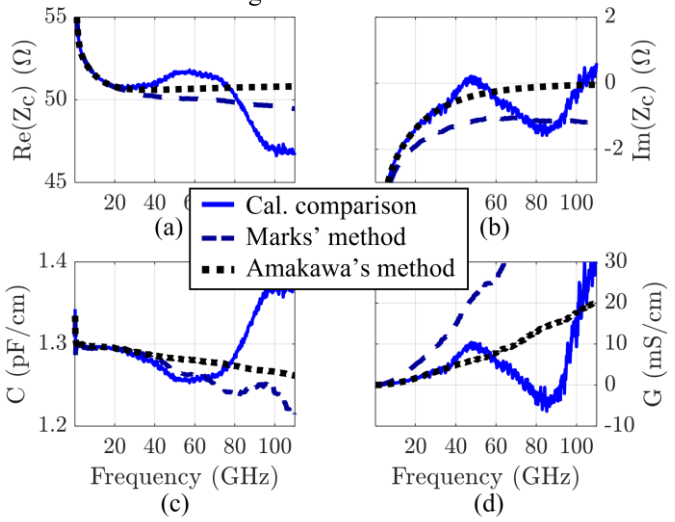


Fig. 4. Extracted Z_c (a, b), per-unit-length C (c) and G (d) terms, with the calibration comparison (solid lines) [10], load or Marks' method (dashed lines) [6]-[7], Amakawa's method (black dotted lines) [11], from I110 measurements.

Instead, an interesting method recently proposed by Amakawa *et al.* [11] assumes that the first-tier calibration and the calibration comparison technique yield meaningful Z_c at 'low frequencies'. This 'low-frequency' data is used to fit a shunt admittance network that is extrapolated to obtain G(f) and C(f) curves over the whole frequency range. Finally, Z_c is extracted as $Z_c = \gamma/(G(f) + j\omega C(f))$. By synthesizing a meaningful shunt admittance network (shown in Fig. 5), this method yields a *causal* Z_c. Amakawa's technique can be seen as a *'correction' method* in which we use the 'reliable' low-frequency data to fit a meaningful electrical model and extrapolate it to 'correct' the higher frequency data.

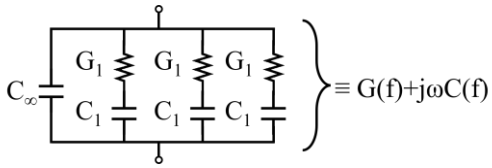


Fig. 5. Shunt admittance network used to fit 'low-frequency' (< 35 GHz) measurements and extrapolated to higher frequencies (up to 110 GHz) in Amakawa's Z_c extraction method [11].

The third order network shown in Fig. 5 has been used to fit measurement data up to 35 GHz, where no bump in γ or Z_c is observed for any probes. This method is applied to the I110 probe data shown in Fig. 4 (black dotted lines), and we observe a much smoother behavior in Z_c that is behaving above 40 GHz in a much better way than the Z_c uniquely extracted from the calibration comparison technique (especially in its real part above 80 GHz).

C. Open-M1 characterization

As we have seen from the measured γ, there are some significant probe-dependent effects in the measurements of the calibration standards that will be propagated in corrected measurements of other structures. To help identifying the origin of these effects, let us analyze Open-type structures. Reflection coefficient measurements with reference plane at the probe tips (so after 1st-tier calibration correction) of the Open-M1 de-embedding structure are shown in Fig. 6(a).

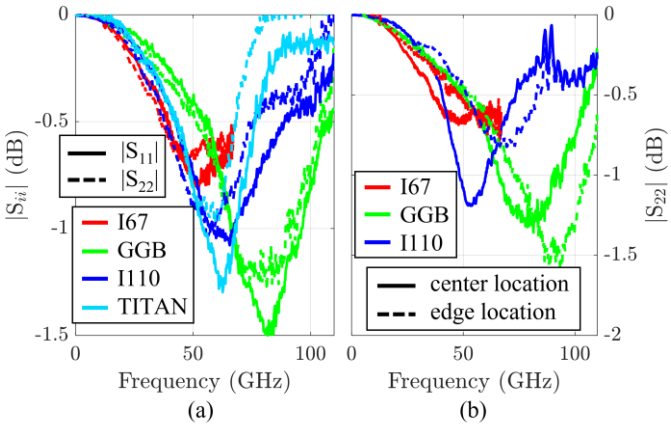


Fig. 6. $|S_{ii}|$ of Open-type de-embedding structures. Measurements with different probes corrected after first-tier calibration only (reference plane at probe tips). (a) Open-M1 de-embedding structure. (b) $|S_{22}|$ of two similar Open-type de-embedding structures, one at the center of the chip (solid lines), the other close to the right edge (dashed lines): see Fig. 7.

A strong resonance is systematically observed in the magnitude of the reflection coefficients. Furthermore, the resonance is different for the left and right probes. The frequency at which these resonances occur, and their magnitude vary according to the probe technology, and *absolute position of the structure on the chip*. Indeed, this is clearly observed by comparing the $|S_{22}|$ at Fig. 6(b) of two Open de-embedding structures at different locations on the chip. One of them is toward the center of the chip, while the second one is closer to the right edge. A sketch representing the two measurement situations is shown in Fig. 7.

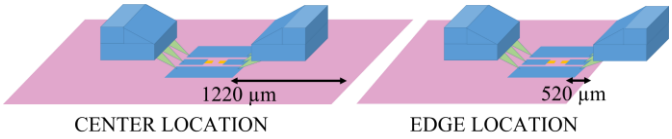


Fig. 7. Sketch of the two Open-type de-embedding structures measurements (Fig. 6(b)): chip center location (left) and chip edge location (right).

Furthermore, we observe that the $|S_{22}|$ of the *I110* measurement is even *more sensitive to the on-wafer environment*, as the variation is stronger than for the other I67 and GGB probes (such measurement is not available for the TITAN probe). The GGB probe measurements also exhibit a strong resonance, but (i) at higher frequency, and (ii) the curves for the two measurements are in good agreement up to 50-60 GHz (whereas deviation in the two $|S_{22}|$ is already observed around 20-30 GHz for the two Infinity probes).

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These trends with GGB and I110 probes have recently been observed and explained in [16] in terms of the nature of probe coupling. Fregonese *et al.* show via 3D EM simulations reproducing the measurements conditions (including a probe model and calkit structures) that the trends in I110 measurements are mainly explained by a strong and localized coupling between the I110 probe and the on-wafer test structures due to the presence of a solder joint in the probe that is ~500 µm away from the probe tips and ~176 µm above the substrate. The probe to on-wafer environment is more distributed for the GGB probe. Indeed, it is less sensitive to the test structure environment (as seen in Fig. 6(b)), as there is not such strong and localized coupling happening that far away from the probe tips. However, it still suffers from larger probe-to-probe crosstalk than I110 probes, which degrades measurement accuracy at higher frequencies.

Such a detailed EM analysis of 110 GHz TITAN probes (or Allistron: previous model on which it is based) coupling with on-wafer test structures on Si-based technology has not yet been reported to the best of the authors' knowledge. However, we will see in the following that TITAN probe measurements exhibit a 'wavy'-like behavior with frequency, like I110 probes, but with some differences in behavior, mainly in the upper frequency range.

Anyway, with the effort of reproducing a similar environment for each measured structure, one could hope that some of these undesired effects are corrected (or at least attenuated) with a second-tier, in-situ calibration. The 'Open-M1' de-embedding measurements corrected with the mTRL second-tier calibration (with Z_c determined using Amakawa's method [11]) are shown in Fig. 8, together with process design kit (PDK) parasitic extraction (PEX, up to M10) simulations. The reference plane after the 2nd-tier in-situ mTRL calibration is in M10, as illustrated in Fig. 2(a). The measured capacitances from the π-equivalent model are also shown. They are computed from the Y-parameter measurements as

$$C_{12} \equiv -\frac{\mathrm{Im}(Y_{12})}{\omega}, \quad C_{11} \equiv \frac{\mathrm{Im}(Y_{11}+Y_{12})}{\omega}, \quad C_{22} \equiv \frac{\mathrm{Im}(Y_{22}+Y_{12})}{\omega}. \tag{1}$$

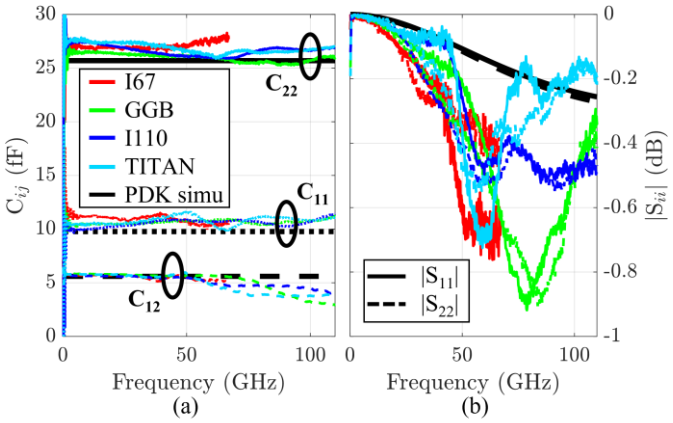


Fig. 8. Open-M1 measurements with different probes, corrected by in-situ second-tier calibration. Reference plane in M10. Capacitance measurements (a) and reflection coefficient magnitude (b).

The PDK parasitic extractions agree well, mostly in terms of capacitance, with roughly frequency-independent C_{11} and C_{22}. C_{12} deviates at similar frequencies as the resonances in $|S_{ii}|$, which is explained by probe coupling too [16].

This non-ideal correction could have been expected as mTRL is based on an 8-term error box and does not account for crosstalk terms. So, it is unlikely to accurately correct probe-to-probe crosstalk. In addition, mTRL assumes there is only one mode propagating inside the transmission line, while the resonances in measured γ (cf. Fig. 3) indicate the existence of several modes propagating on-wafer, thus degrading the accuracy of mTRL calibration. Finally, due to the distributed nature of the crosstalk (mainly for GGB probe), even SOLT algorithm (with two crosstalk terms) fails to correct well these parasitic behaviors [16].

There is a final de-embedding step in transistor measurements, which should (hopefully) reduce the parasitic effects from the resonances and bumps. This is evaluated in the next section.

III. Analysis of Different In-Situ Calibration Methods

The effect of de-embedding strategies on the test structures studied in this paper has already been analyzed in [12] and confirmed -in agreement with other studies [2], [14]- that the in-situ multiline TRL calibration (followed by a classic Open-M1-Short-M1 de-embedding) yields the most accurate and consistent extraction results.

Nevertheless, the calibration comparison technique was used to obtain Z_c of the Lines standards in [12] and Marks' method in [2], [6], [16]. Yet, as we have seen above, both methods are prone to error. For Marks' method, it highly depends on the calkit design and on the validity of the assumptions of constant C and G = 0. Even without such assumptions, the calibration comparison method yields Z_c with unexpected deviations at higher frequencies. The interesting correction method proposed in [11] provides a better-behaved Z_c at higher frequencies as shown above. So, we will assess the validity of these different Z_c extraction methods via extrinsic FET se-

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ries resistances measurements as it was done in [12]. All FET measurements shown in the following are corrected such that the reference plane is in M1.

Bracale's method [17] to extract FET series resistances uses measurements in cold FET (V_{ds} = 0 V) and strong inversion regime (V_{gs} >> V_{th}, where V_{th} is the threshold voltage). The measurements under such conditions (port 1 connected to the gate, port 2 to the drain) yield the following expressions:

$$\mathrm{Re}(Z_{11} - Z_{12}) = R_g - \frac{1}{4g_d}\,, \qquad (2)$$

$$\mathrm{Re}(Z_{22}) = R_{sd} + \frac{1}{2g_d}\,, \qquad (3)$$

where R_g is the extrinsic gate resistance, R_{sd} is the sum of the series source and drain resistances, g_d is the output conductance. g_d is proportional to the overdrive voltage (V_{gs}-V_{th}), such that its contribution to the above expressions becomes smaller with larger gate voltage. The goal being to compare measurement and extraction accuracy in this section, we only present (2) and (3) versus frequency at the highest possible V_{gs} bias of the technology (to minimize the $1/g_d$ terms), instead of extracting the actual series resistances values (R_g and R_{sd}). Nevertheless, (2) and (3) are expected to be constant with frequency (above a few GHz for (1)). Indeed, complete expressions for (2) and (3) in terms of the FET small-signal equivalent circuit parameters can be found in [18]. Any frequency-dependent deviation is attributed to inaccuracies in measurement extraction.

Fig. 9 shows (2) and (3) for different probes measurements corrected by the 2nd-tier mTRL calibration using different Z_c evaluation techniques: calibration comparison, Amakawa's correction method and Marks' method (only shown for I110 to avoid overloading the graphs).

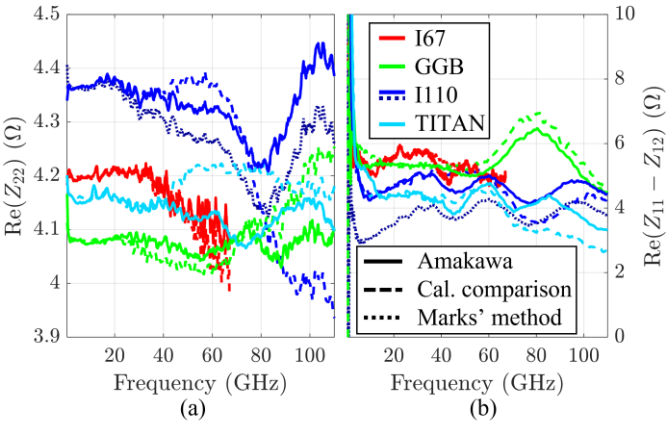


Fig. 9. Re(Z_{22}) (a) and Re(Z_{11}-Z_{12}) (b) from cold FET measurement biased in strong inversion. Data corrected by 2-tier calibration with Open-M1-Short-M1 de-embedding. Comparison between different Z_c extraction methods [10] (dashed lines), [11] (solid lines) and [6] (dark dotted lines), for different probe measurements.

As expected, the data corrected using Marks' method shows strong deviations, mostly in Re(Z_{11}-Z_{12}), and it shall no longer be discussed in the following. Apart from that, there are two types of observations from Fig. 9, i.e. probe-related and Z_c-extraction-related. Let us first start with the latter.

In Re(Z_{22}), we observe that Amakawa's method enables the correction of residual non-ideal behaviors (mostly for the I110 probe measurements) and an excellent consistency up to 110 GHz is achieved, with *frequency-dependent variations up to 5% in all curves*. As for Re(Z_{11}-Z_{12}), the bumps still present are dampened and the high-frequency roll-offs (in TITAN and I110) are decreased. With the exception of the I67 probes (where there is almost no change), Amakawa's method does a good job at correcting unexpected measured behaviors thanks to a more meaningful high-frequency Z_c extraction.

Concerning the probe-to-probe variations, there is little deviation (ΔRe(Z_{22}) < 8% and ΔRe(Z_{11}-Z_{12}) < 24% at 20 GHz) among the measurements with different probes. It means that all elements (FET, de-embedding and calibration structures) have been measured with high quality and repeatable contact, and that there is little die-to-die process variation. Furthermore, Fig. 9(b) shows the same typical probe trends observed above: (i) steady behavior up to ~50-60 GHz then strong deviation for GGB, (ii) 'wavy' curves for I110 (and TITAN) already around 20-40 GHz but with smaller bump amplitude than GGB.

R_g (expressed as Re(Z_{11}-Z_{12}) in cold FET, high inversion regime) is not commonly used to evaluate the extraction accuracy. Instead, the two curves $f_t(f)$ and $f_{max}(f)$ are rather used, defined as

$$f_t(f) \equiv f|H_{21}|\,, \quad f_{max}(f) \equiv f\sqrt{|U|}\,, \qquad (4)$$

where H_{21} is the short-circuited-output current gain and U the (Mason) unilateral power gain. However, $f_t(f)$ is not so sensitive to measurement errors, and the extrinsic FET behavior only features a frequency-independent $f_{max}(f)$ above ~20 GHz. These two statements are demonstrated in the following section. On the other side, R_g (as Re(Z_{11}-Z_{12})) is just as *sensitive* to measurement errors as $f_{max}(f)$ *and should feature a frequency-independent behavior* (already above 5-10 GHz), which makes it a pertinent figure of merit (FoM) to evaluate the extracted results accuracy.

As a last step, let us analyze the probes' effect and their related residual errors on the FET measurements in high RF performance conditions.

IV. MOSFET Measurements up to 110 GHz in High RF Performance Bias

The measurements in this section are corrected with the mTRL 2nd-tier calibration using Amakawa's method to determine Z_c, then de-embedded with the classic Open-M1-Short-M1. Transistor measurements (and simulations) biased in saturation (nominal V_{ds} = 0.8 V) and at peak f_t (corresponding to V_{gs} = 0.6 V) are shown in the following (with reference plane in M1). The measured parameters displayed in Fig. 10 are defined as (4) and

$$g_{21} \equiv \mathrm{Re}(Y_{21})\,, \quad g_{22} \equiv \mathrm{Re}(Y_{22})\,, \quad C_{22} \equiv \frac{\mathrm{Im}(Y_{22} + Y_{12})}{\omega}\,, \qquad (5)$$

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$$C_1 \equiv C_{11} + C_{12} \equiv \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} - \frac{\mathrm{Im}(Y_{12})}{\omega}. \quad (6)$$

Port 1 and 2 are connected to the gate and drain terminals, respectively. Note that the parameters defined above include the effect of intrinsic and extrinsic MOSFET elements. These parameters depend only weakly on frequency, and they are often used as metrics to evaluate the ability of a calibration to measure MOSFET parameters [1]-[2], [4], [8]. Since we are mostly interested in their variation with frequency, they have been normalized to values given in the caption of Fig. 10.

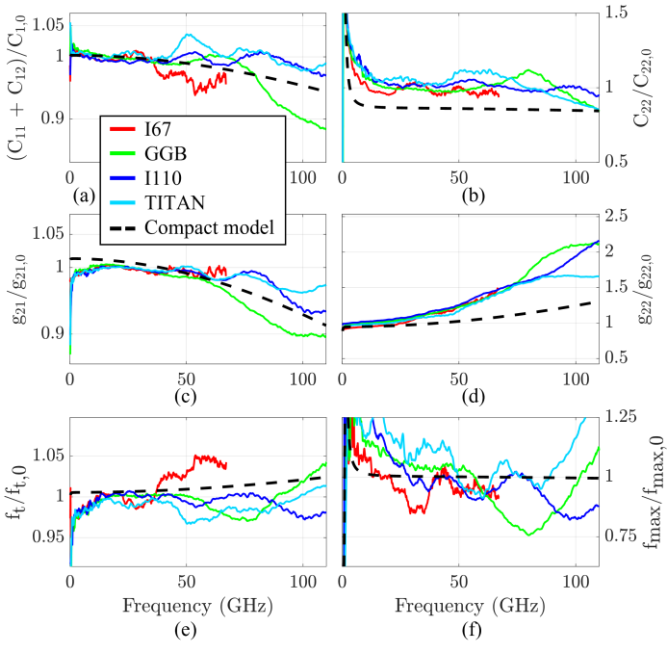


Fig. 10. FET parameters C_1 (a), C_{22} (b), g_{21} (c), g_{22} (d), f_t (e) and f_{max} (f), measurements (solid lines) for different probe technologies and compact model (from PDK) simulations (black dashed lines), biased at V_{ds} = 0.8 V, V_{gs} = 0.6 V. All graphs are normalized with respect to $C_{1,0}$ = 54.2 fF, $C_{22,0}$ = 18.4 fF, $g_{21,0}$ = 111.1 mS, $g_{22,0}$ = 7.1 mS, $f_{t,0}$ = 328 GHz, $f_{max,0}$ = 400 GHz from (a) to (f), respectively.

Except for a larger spread in $f_{max}(f)$ (being a very sensitive parameter), all probe measurements agree very well with each other up to ~70 GHz. Beyond 70 GHz, each probe data show distinct deviations. These almost overlapping curves give great confidence in measurement accuracy up to ~70 GHz and their deviations beyond 70 GHz seem to provide an interval within which should lie the actual FET electrical behavior.

The $f_{max}(f)$ curves exhibit larger variations from probe to probe *and* across frequency. It is a very sensitive parameter that is difficult to accurately extract [16], [19], [20], in particular for technologies featuring high f_{max} values (such as this one). Even though it features impressively large bumps (up to ~100 GHz deviation), it is in the same order of relative variations (up to ~25%) as R_g observed above. However, its measured behavior is not so constant with frequency as observed from the steady decreasing trend in measurements above 10 GHz (as opposed to R_g), which makes R_g an interesting sensitive alternative to evaluate residual measurement error.

Equivalently, the measured S-parameters are shown in Fig. 11. Excellent measurement consistency from different probe data is achieved with almost overlapping curves. PDK compact model simulations are also shown in Fig. 10 and Fig. ***11*** and agree very well in general with measurements.

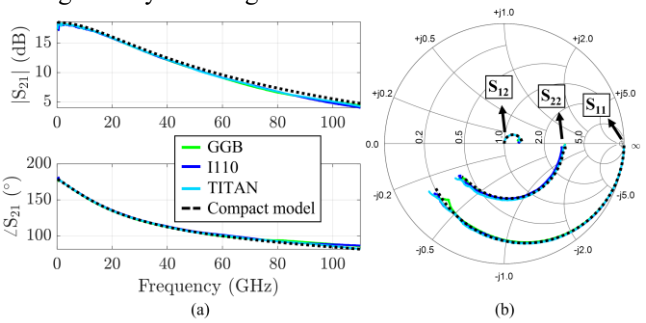


Fig. 11. FET S-parameters S_{21} (a) and S_{11}, S_{12}, S_{22} (b), measurements (solid lines) for different probe technologies and compact model (from PDK) simulations (black dotted lines), biased at V_{ds} = 0.8 V, V_{gs} = 0.6 V.

Nevertheless, some small discrepancies between the compact model simulations and measurements are observed, mostly visible in Fig. 10: (i) offset in C_{22} value and low-frequency discrepancy in g_{21} curve, (ii) high-frequency deviation in g_{22} (above ~20-30 GHz). The good agreement between measurements of different probes and the excellent consistency obtained in Fig. 9(a) indicate that some physical phenomena are likely not well modeled by the PDK compact model. The discrepancies in C_{22} and g_{21} might be associated to an incomplete low-frequency modeling of back-gate and substrate networks as already reported in [21], while the g_{22} discrepancy could be a high-frequency drain-to-substrate coupling not well modeled as recently shown in [22] for heterogenous bipolar transistors. Further investigation is needed to confirm the origin of these discrepancies.

Finally, the very good agreement obtained in general with the PDK's compact model simulations further confirms that despite the residual probe-dependent errors, a high measurement accuracy up to 110 GHz is achieved with the selected measurement correction procedure.

V. Conclusion

Targeting accurate measurements of high-performance FD-SOI MOSFETs at mm-wave frequencies, we have studied different ways to correct measurements from on-wafer parasitics up to 110 GHz. It is well acknowledged in the literature that in-situ calibration is a must for high-frequency on-wafer measurements. mTRL calibration is usually preferred as it does not rely on standards that must be well characterized. However, mTRL requires the transmission line Z_c knowledge, which is a tricky parameter to extract, for S-parameter renormalization to 50 Ω.

A specially designed in-situ mTRL calkit is first characterized with different RF probe technologies. The extracted transmission line parameters (γ and Z_c) feature some undesired probe-dependent bumps (that are identified as coming from

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strong probe coupling to adjacent environment), which also deteriorate the FET measurement accuracy.

So, different extraction methods for Z_c are tested: calibration comparison, load method and Amakawa's method. For the first time, to the best of the authors' knowledge, it is shown that *Amakawa's method* applied to in-situ calibration provides an interesting correction *reducing probe-dependent errors* (of various probe technologies) *in MOSFET measurements*. Indeed, measured *source and drain resistances* of the tested transistor geometry *varying by less than 5% up to 110 GHz* is obtained for all tested probes. Whereas the *bumps in R_g are dampened* with this method, and its roll-off at higher frequencies is reduced, achieving variations up to ~20% in the worst case.

Finally, additional measurements in high RF performance conditions (shown in terms of S-parameters, capacitances, f_t, f_{max}, etc.) are corrected applying this method and compared to the PDK's compact model. Even though each probe data still suffer from probe-dependent residual errors that are more visible beyond 70 GHz, we have achieved *high-accuracy FET measurements up to 110 GHz*, which is demonstrated by: (i) *almost overlapping curves* below 70 GHz for each parameter (with a wider spread in f_{max} though) that (ii) *consistently follow the PDK's compact model up to 110 GHz* with marginal deviation. The results shown here are promising for high-frequency transistor characterization, even though more work is needed to verify the achieved accuracy for FETs of different geometries and dimensions.

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