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Comparison of Heat Sinks in Back-End of Line to reduce Self-Heating in 22FDX® MOSFETs

Arka Halder *, Lucas Nyssens, Dimitri Lederer, Valeriya Kilchytska, Jean-Pierre Raskin

Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium

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ABSTRACT

This work compares the effect of different heat sink dimensions in the back-end of line (BEOL) on the self-heating (SH) parameters. To assess the self-heating (SH) parameters, the RF characterization technique is employed, which involves measuring S-parameters across a broad frequency spectrum. In addition to the standard device without a sink, two sinks of different dimensions, both connected to the gate, are considered: one smaller and one bigger in size. We experimentally demonstrate lower self-heating as the sink size increases. By using a smaller and a larger sink, a mean reduction of 4.7% and 8.9% in thermal resistance is observed, showing greater SH reduction with increasing sink size, which is also verified from comparison with previous works. The impact of the sinks on RF figures-of-merit (FoMs), namely the cutoff frequency f_T and maximum oscillation frequency f_{max} is investigated. f_T is seen to degrade stronger due to increased gate capacitance whereas f_{max} degradation is limited because of reduced gate resistance.

1. Introduction

Despite enhanced device performance and minimized manufacturing expenses, the aggressive scaling of CMOS technology has led to higher current and power densities, potentially increasing concerns associated with self-heating (SH) effect [1]. The undesirable effects resulting from self-heating, such as reduced mobility, threshold voltage shift, lower output current, and reduced reliability [2], can be mitigated by facilitating the dissipation of the heat generated in the channel. Amongst the various possible heat evacuation paths like substrate, source and drain regions, this work focuses on the back-end of line (BEOL) path located above the MOSFET for removing the heat generated in the channel.

The underestimation of SH due to cooling through the gate contacts was demonstrated in [3], establishing the possibility of heat evacuation through the BEOL. In order to limit this cooling effect through the gate contacts, two gate contacts instead of four are used to measure self-heating using the gate resistance thermometry method in [4]. The prospect of utilizing thermal shunts in the BEOL to suppress SH was validated through simulations in [5]. Previously, our work experimentally demonstrated the impact of SH reduction by using a heat sink in the BEOL [67]. Our work here follows up on that by addressing heat evacuation through the BEOL using different heat sink sizes by experimental analysis. In this paper, a comparison of sinks of different dimensions in the back-end of line (BEOL) is carried out experimentally using dedicated heat sinks for the devices. The devices are implemented in the 22 nm FDSOI technology from GlobalFoundries. With this technology being one of the most advanced nodes catering to various mobile and RF applications (5G, IoT, wearable electronics etc.), the devices studied act as excellent state-of-the-art demonstrators. Given the rich 11-metal layer BEOL in 22FDX®, there is ample scope to realize heat sinks which offer different thermal resistances and see their impact on aiding heat evacuation of the device. Starting from the proof of concept done in our earlier works [67], we now move to a more compact device and sink area with the target of still demonstrating thermal resistance reduction. The quantitative impact of the area of the sink used on helping heat evacuation through the BEOL path is experimentally explored.

2. Experimental Details and Approach

The devices used in this study originate from the 22 nm FDSOI technology from GlobalFoundries [8]. The device gate length is 20 nm, total width is 30 μm for each of these devices composed by 60 fingers of 0.5 μm finger width. As SH is more pronounced in shorter devices, a small device length of 20 nm is chosen to see the impact of the sink. In

* Corresponding author.
E-mail address: arka.halder@uclouvain.be (A. Halder).

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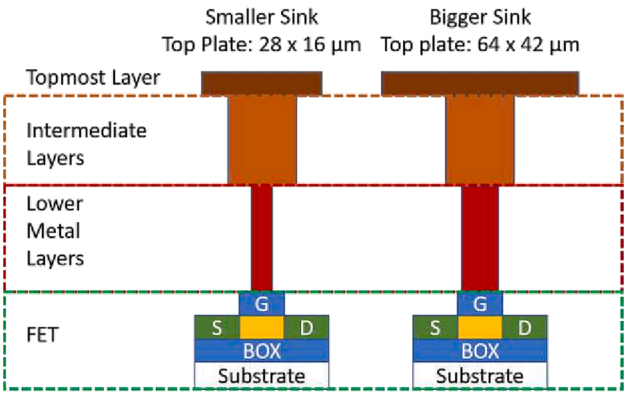

Fig. 1. Cross-sectional schematic of the sink device in BEOL.

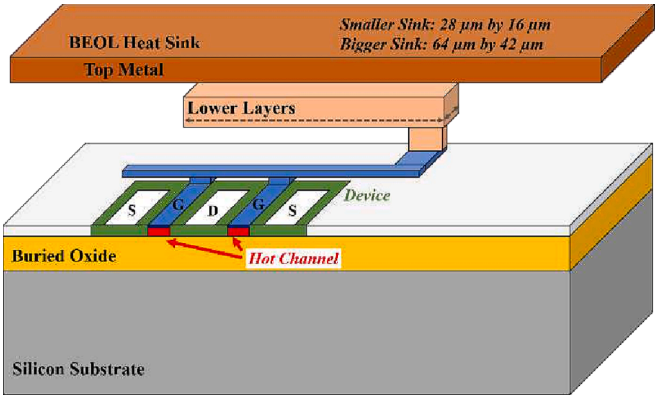

Fig. 2. Schematic for 3D sink configuration [7].

this work, three devices based on the same core FET above are considered. Apart from a standard device without any heat sink, two other devices with sink in the BEOL are designed: one with a smaller sink and the other with a larger sink dimension. With the thermal resistance expected to decrease with increasing cross-sectional area of the sink, the larger sink is expected to ease heat evacuation further through the BEOL.

Fig. 1 and Fig. 2 illustrate the sink configurations with just the area of the metal plate and connections being bigger for the bigger sink. The heat sink consists of a metallic pad right above the FET over which the passivation layer is removed. This top metal plate is connected down to the FET using metallic connections in the intermediate and lower metal layers below and eventually connected by vias to the gate above the gate access on the side of the FET as seen in Fig. 2. The dimension of this plate on the top metal is 28 µm by 16 µm for the smaller sink device and 64 µm by 42 µm for the bigger sink device respectively. The heat sink itself is similar in configuration but much smaller than in our last work (234 µm by 114 µm) in [7] to not introduce additional parasitics while having a more compact device.

In order to estimate self-heating features, the RF characterization technique, a frequency domain method is used here. The RF technique was recently shown to be the most suitable for SH characterization in the most advanced deeply down-sized state-of-the-art devices [9], because frequencies up to gigahertz range need to be reached to attain dynamic self-heating-free conditions in these devices. For the RF characterization of SH, S-parameters are measured in a frequency range from 100 kHz to 1 GHz, de-embedded and converted to Y parameters. Two Ground-Signal-Ground RF |Z| probes of 100 µm-pitch are used for these measurements. The probes are compatible with high temperature measurements up to the necessary temperature value of 125 °C. The output conductance (g_d) is computed as the real part of Y_{dd}, transconductance (g_m) is the real part of Y_{dg}. The g_d versus frequency curve and the drain

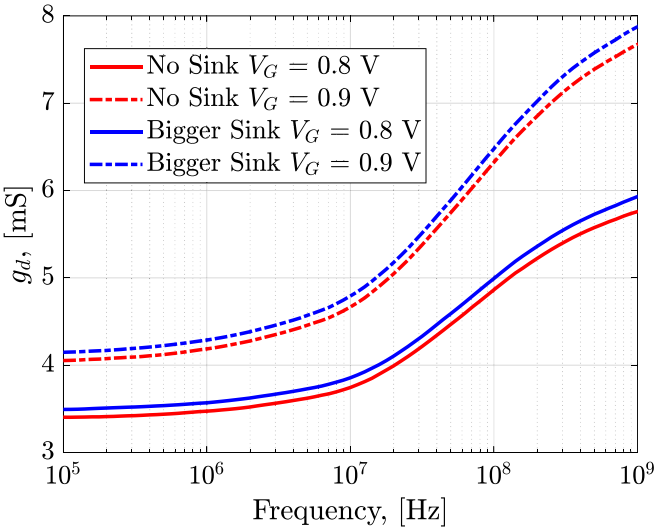

Fig. 3. Output conductance g_d vs frequency for no sink and bigger sink cases at $V_d = 0.8$ V and V_g 0.8 and 0.9 V.

capacitance C_{dd} versus frequency curve show transition due to SH, which allows assessment of SH-related features (e.g. R_{th} and C_{th}). The transition in g_d with frequency is caused not only due to SH but also due to substrate and back-gate network [1011]. In this context, the importance of the zero-temperature coefficient (ZTC) point, where dynamic SH vanishes becomes of interest. The transition due to the substrate network is removed by considering the transition in g_d at the zero-temperature coefficient (ZTC) point at which there is no transition due to SH. R_{th} and capacitance C_{th} is then extracted using (1) and (2) given below [7]:

$$R_{th} = \frac{\Delta g_d}{(I_d + V_d g_{d,LF})\partial I_d/\partial T} \tag{1}$$

$$C_{th} = \frac{\Delta C_{dd}}{R_{Th}^2 (I_d + V_d g_{d,LF})\partial I_d/\partial T} \tag{2}$$

where Δg_d is the difference between g_d at low and high frequencies of 100 kHz and 1 GHz, ΔC_{dd} the corresponding difference for drain capacitance C_{dd}, I_d is the DC drain current, $g_{d,LF}$ is the output conductance g_d at low frequency (100 kHz) and $\partial I_d/\partial T$ is the slope of the I_d

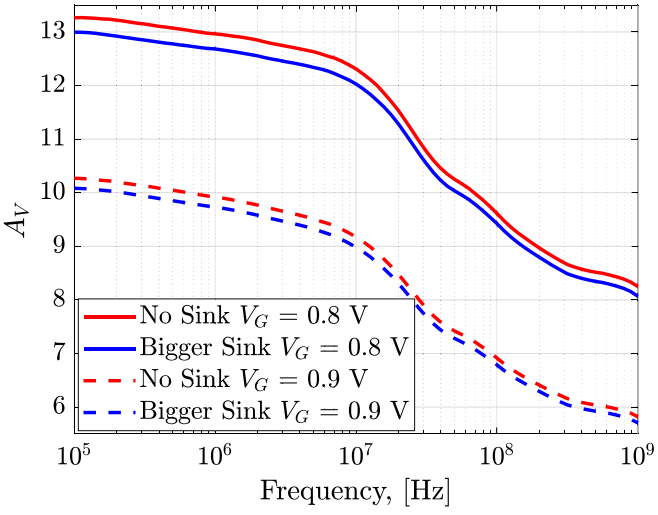

Fig. 4. Gain A_V vs frequency for the no sink and bigger sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.

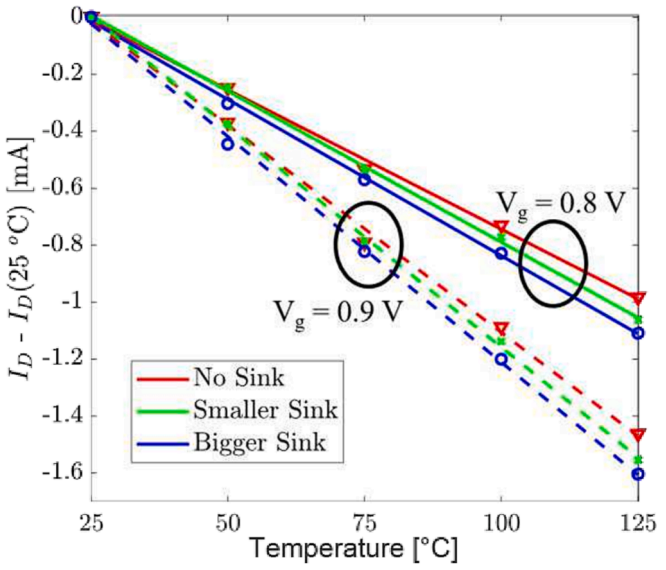

Fig. 5. Drain current I_d vs temperature for the different sink cases at $V_d = 0.8$ V and at V_g of 0.8 and 0.9 V.

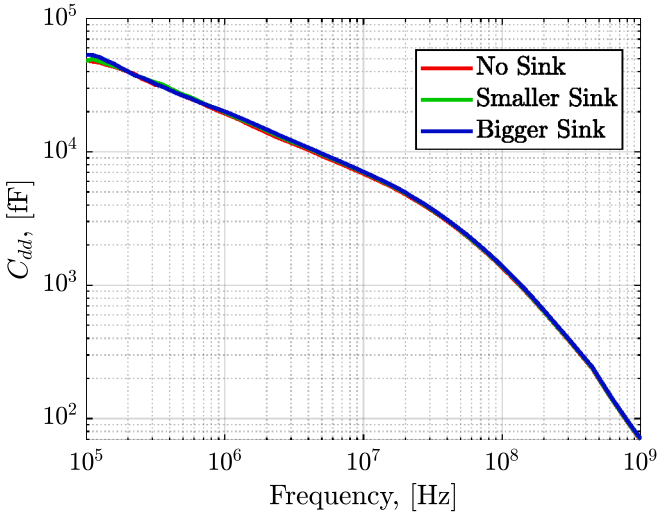

Fig. 6. Drain capacitance C_{dd} vs frequency for the different sink cases at $V_d = V_g = 0.8$ V.

versus temperature plot extracted from I_d-V_g curves measured in a temperature range from 25 up to 125 °C. The DC measurements in temperature are made at 25, 50, 75, 100 and 125 °C respectively. In order to have a steady temperature value while measuring, the whole system was let to steady for at least half an hour to ensure temperature stability. The extractions have been made in saturation at a V_d of 0.8 V. The back gate was grounded ($V_{bg} = 0$ V).

3. Results and Discussion

It is verified that the DC performances of the devices are similar, ensuring a fair comparison between the devices. Fig. 3 shows the variation of output conductance g_d with frequency for the no sink and bigger sink device at $V_d = 0.8$ V and two different V_g biases of 0.8 and 0.9 V. Higher value of g_d obtained for the bigger sink for two different biases demonstrate the fact that it is less affected by SH compared to the other sinks.(See Fig 4.).

In Fig. 5, the variation of drain current I_d normalized with respect to the value at 25 °C with temperature is shown. The bigger sink has the highest I_d versus temperature slope (having a steeper slope), demonstrating the lowest SH is observed in its case. The reason for the above can be seen in [7] as dI_d/dT is higher at higher temperatures representative of higher SH computed from I_d versus temperature. For a V_d of 0.8 V, two different bias conditions in V_g in 0.8 V and 0.9 V are considered and the aforementioned trends are verified for both cases. At V_g 0.9 V, a higher dI_d/dT is seen as this bias point is further away from the ZTC than the V_g 0.8 V case.

Table 1
Self-Heating Parameters. Vg=Vd=0.8 V.

Sink Type	$g_{d,LF}$(mS)	Δg_d(mS)	$\partial I_d/\partial T$ (μA/K)	R_{th} Normalized (Kμm/mW)	C_{th}(pJ/K)
No Sink	3.4	1.81	-10.54	201.5	4.52
Smaller Sink	3.35	1.82	-11.12	192.5	4.7
Bigger Sink	3.49	1.87	-11.88	182.2	4.84

Table 2
Thermal Resistance Reduction Comparison with Sink Size.

	Smaller Sink (This work)	Bigger Sink(This Work)	Sink in previous work [7]
Sink Top Plate Size	28 μm x 16 μm	64 μm x 42 μm	234 μm x 114 μm
Area Ratio w.r.t [7]	1/60	1/10	1
% R_{Th} Reduction	4.7%	8.9%	~ 20%

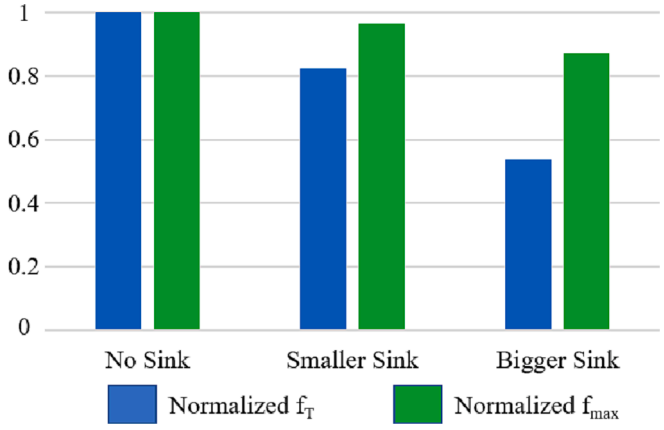

Fig. 7. Reduction in peak cutoff frequency f_T at $V_g = 0.6$ V (corresponding to $g_{m,max}$) and $V_d = 0.8$ V. f_T-f_{max} are normalized with respect to no sink case.

The SH-related variation in drain capacitance C_{dd} is observed to be around three orders of magnitude in Fig. 6 similar to observations in previous work in [7].

Table 1 summarizes the comparison of the devices from an SH perspective. The absolute value of $\partial I_d/\partial T$ is found to be highest for the bigger sink and lowest for the no sink device confirming the weakest and the strongest SH in their cases respectively. A combination of the above parameters results in the lowest value of R_{th} for the bigger sink. An average R_{Th} reduction of 4.7% and 8.9% on using the smaller and bigger sink respectively is observed over multiple dies. The C_{Th} values observed are similar to the values reported in [7], slightly lower owing to lower R_{th} observed here possibly from the substrate network impact correction. Table 2 clearly demonstrates the impact of sink size on SH reduction including comparisons with our previous work [7]. Compared to the sink in [7], shrinking sink area by a factor of 60 (bigger sink) and 10 (smaller sink) makes the percentage R_{Th} reduction go down from 20% in

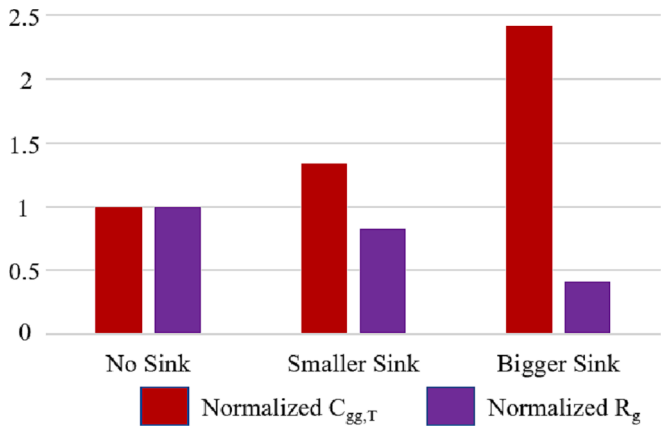

Fig. 8. Variation in total gate capacitance $C_{gg,T}$ and gate resistance R_g, normalized with respect to no sink case.

[7] to 8.9% and 4.7% for bigger and smaller sink.

The impact of the sink on the RF performance is investigated next. In Fig. 7, the impact of the sink on the RF FoM cutoff frequency f_T and f_{max} is demonstrated. The peak f_T and f_{max} are computed from current gain H_{21} and unilateral power gain U at V_g corresponding to $g_{m,max}$ (0.6 V in this case). f_T is seen to degrade around 17.5% and 46% whereas fmax degrades around 3.4% and 12.8% for the smaller sink and bigger sink respectively. Analytically, as observed in (3) and (4), f_T is inversely proportional to $C_{gg,T}$ whereas f_{max} has a more complicated dependence on multiple parameters (like source resistance R_s, gate to drain capacitance $C_{gd,T}$) including gate resistance R_g which is of interest here. In order to understand the variation in f_T-f_{max}, the trends on total gate capacitance $C_{gg,T}$ and gate resistance R_g in Fig. 8.

$$f_T \approx \frac{g_{m,e}}{2\pi C_{gg,T}}, \tag{3}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{2\pi f_T R_g C_{gd,T} + (R_s + R_g) g_{d,e}}} \tag{4}$$

The degradation in f_T is mainly owing to increased $C_{gg,T}$ which affects f_T inversely. It is expected that due to the additional parasitics that are brought in by the sink, there would be a degradation of the RF performance which is seen. However, the f_{max} degradation is much lesser because of a reduction in gate resistance R_g which has an inverse proportionality with f_{max}. As the sink connection is parallel to the standard gate access path, a lower R_g is expected and this is verified from the experimental results. A tradeoff between using the sink to improve SH performance while not degrading RF performance is therefore established. The importance of the sink still comes into play for analog and certain RF applications as the f_T-f_{max} offered by the technology is high enough to provide for them despite the degradation in RF performance owing to the sink.

4. Conclusion

The thermal resistance of a device using gate-connected heat sinks is observed to reduce with increasing sink size. A mean reduction of 4.7% and 8.9% in R_{th} compared to a standard no sink device is observed with the connection of a smaller and larger sink respectively, with the trends being verified over multiple dies with limited impact on C_{th}. The impact of the sink of the RF FoMs is investigated and it is observed that the cutoff frequency f_T degrades 17.5% and 46% mainly due to increased gate capacitance. The degradation on f_{max} is limited to around 3.4% and 12.8% on using the smaller and the bigger sink respectively owing to reduced gate resistance with the connection of the sink creating a parallel network to the usual gate connection. While this work considered a small device length of 20 nm, future work would include investigation of the sink on devices of greater lengths.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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