High-Resistivity Trap-Rich Silicon Substrate Advantages for Large Integrated MIM Capacitors

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***Abstract*— Metal-insulator-metal (MIM) capacitors are critical passive components in integrated circuits (ICs) and are widely used in analog, mixed-signal, and radio frequency (RF) applications. This study investigates the advantages of high-resistivity (HR) silicon substrate incorporating a trap-rich (TR) layer (HR-Si+TR) on the performance of large MIM capacitors, compared with conventional silicon substrate, through experimental measurements and electromagnetic simulations. A lumped-element π-model is validated to extract and interpret key performance metrics of the MIM structures, accounting for dielectric leakage, substrate coupling, and resistive losses. A substantial improvement in the quality factor is observed, reaching 65 at 170 MHz compared to 13.5 for the standard Std-Si reference at the same frequency, alongside a slight increase in the resonance frequency. This enhancement originates from the HR-Si+TR substrate transition to dielectric-like behavior at frequencies below the operational RF range, which substantially reduces substrate losses and parasitic coupling. Consequently, minimized parasitic capacitances (ground coupling and fringing effects) allow for a higher quality factor and resonant frequency.**

***Index Terms*— High-resistivity (HR) substrate, inflection frequency, metal-insulator-metal (MIM) capacitor, quality factor, self-resonance frequency, substrate losses, trap-rich (TR) layer.**

I. Introduction

INTEGRATED passive device (IPD) design techniques are evolving in various aspects to meet the growing demands for higher performance, miniaturization, and cost efficiency in radio frequency (RF) and microwave applications [1]. These advancements aim to achieve monolithic and complete integration of circuits with passive components, including resistors, microstrip lines, inductors, and capacitors, onto semiconductor substrates. As a result, IPDs performance does not only depend on their circuit design but also on the properties of the used materials (conductors, dielectrics, and substrates), along with the associated fabrication techniques [1]. In particular, planar metal–insulator-metal (MIM) capacitors incorporating thick dielectric layers are essential components in power integrated circuits (ICs) and high-voltage circuits that require high breakdown voltage, low leakage current, minimized parasitic substrate coupling, and a high-quality factor (Q), while maintaining robust performance at high frequency [2], [3], [4]. These requirements are common in many capacitor-based RF/microwave circuits, such as switched-capacitor power amplifiers [5], resonant tanks [6], and impedance-matching networks [7], as well as in high-voltage power management systems, including power converters [8] and digital isolators [5]. In such applications, dielectric materials (e.g., SiO_2) can reach significant thicknesses as large as 10 μm to ensure adequate insulation and stability [5].

Improving the performance of MIM structures has been pursued through various approaches, such as optimizing capacitor dimensions and geometry [6], modifying dielectric materials [7], incorporating stacked dielectric configurations [8], or improving substrate properties [1], [2], [9], [10]. The latter is particularly critical for silicon-based MIM capacitors, since the Q-factor and the self-resonant frequency (SRF) are primarily limited by substrate losses at high frequencies. This underscores the importance of minimizing substrate parasitics to improve overall device performance [10], [11]. While alternative substrates such as glass [12] or GaAs [1] can mitigate these issues, they are often costly or incompatible with standard CMOS fabrication processes. On standard silicon (Std-Si) substrates, a ground shield can be used beneath the MIM capacitor to reduce substrate losses, although this adds complexity through additional metal layers and increased parasitic capacitance [2]. High-resistivity (HR) Si substrates have also been proposed as a solution [13], but they can suffer from parasitic surface conduction effects (PSC) that degrade performance by offsetting the benefits of the HR [14]. Another strategy involves creating a suspended structure by etching away the underlying silicon [9], a method that has demonstrated considerable improvements in MIM capacitor

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performance. For instance, the Q-factor of a 3.3 pF suspended MIM capacitor at 2 GHz is approximately 79% larger than its counterpart on substrate, along with an increase in the frequency of maximum Q-factor from 0.35 to 0.65 GHz. Despite these benefits, the method remains impractical for large-scale production due to the need for micromachining steps and concerns over mechanical robustness and assembly reliability.

An alternative approach involves incorporating a trap-rich (TR) polysilicon layer between the buried oxide (BOX) and the HR-Si substrate (HR-Si+TR), a stacking that has previously been proven to suppress PSC effects and improve coplanar waveguide (CPW) lines behavior and inductor performance [14]. This substrate is especially relevant to on-chip MIM capacitors because their planar electrodes produce strong fringing fields that penetrate into the silicon and, on low-resistivity substrates, induce conduction losses that degrade the Q-factor, alter the effective capacitance, and lower the SRF [15]. These substrate-related limitations become particularly severe for small footprints and thin interelectrode dielectrics. In this work we investigate, for the first time, the impact of this HR-Si+TR structure on the performance of a large MIM capacitor with a thick dielectric layer by converting measurements into a lumped-element π-model to extract key device characteristics. Our study combines experimental measurements on a capacitor fabricated on an HR-Si+TR substrate with electromagnetic simulations carried out using advanced design system (ADS) software. The analysis focuses on extracting and analyzing critical performance metrics, including intrinsic capacitance, Q-factor, and SRF. To isolate and evaluate the influence of the used substrate, all results are systematically compared with those obtained from a reference MIM capacitor fabricated on a Std-Si substrate.

This article is organized as follows. Section II outlines the microfabrication and measurement procedures. Section III presents the lumped-element π-model derived from both measurements and simulations. Section IV provides a comprehensive analysis of MIM capacitor characteristics on Std-Si and HR-Si+TR substrates, including evaluation of effective capacitance, substrate leakage, Q-factor, and SRF. And finally, Section V concludes with a comparison to state-of-the-art technologies.

II. Design, Microfabrication, and Measurements

The large on-chip MIM capacitor [320 × 320 μm, Fig. 1(a) and (b)] is fabricated on two types of substrates [Fig. 1(c)]: 1) a 600 μm -thick HR-Si substrate with a resistivity of 5 kΩ·cm, with an additional 500 nm thick undoped TR top polysilicon layer having a resistivity of about 8 kΩ·cm [16], insulated by a 500 nm thick PECVD SiO_2 layer and 2) a 380 μm thick Std-Si substrate with a resistivity of about 16 Ω·cm, insulated by a 500 nm thick SiO_2 layer (ε_r = 4) thermally grown in a humid atmosphere at 1000 °C, used as a reference. The combination of a HR substrate and a TR polysilicon layer is a proven specialized technique used to mitigate substrate-related losses, noise coupling, and parasitic effects. Atop the substrates, the microfabrication process involves three photolithographic steps. First, a 1.5 μm thick aluminum layer (with measured

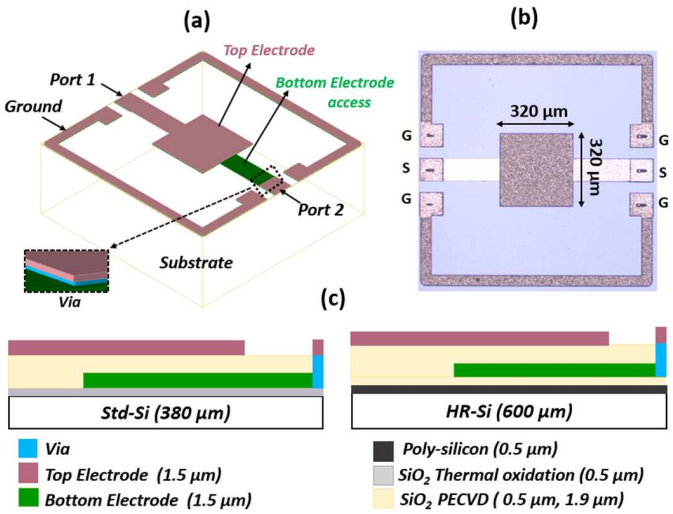

Fig. 1. On-chip MIM capacitor. (a) Perspective view showing the two electrodes (port 1 on top and port 2 on the bottom layer), (b) top view of the fabricated capacitor taken with an optical microscope, and (c) cross-sectional views of the layer stack on the two different substrates (the Std-Si and the HR-Si+TR).

TABLE I
Material Properties Used in ADS Simulation

Material	*Characteristics*	*Value*
Al	σ (10^7 S/m)	1.7
Std-Si	ρ (Ω.cm)	16
	ε_r	11.9
HR-Si	ρ (kΩ.cm)	5
	ε_r	11.9
Poly-Si	ρ (kΩ.cm)	8
	ε_r	11.8
PECVD SiO_2	ε_r	5
Thermal SiO_2	ε_r	4

conductivity σ = 1.7 10^7 S/m) is deposited by e-beam and then patterned to form the bottom MIM electrode. Next, a 1.9 μm thick PECVD SiO_2 insulating layer (with a measured dielectric relative permittivity ε_r = 5 and leakage current of less than 0.6 nA at 100 V) is deposited in an Oxford Plasmalab System 100 at 300 °C, 1 torr pressure, 30 W RF power at 13.56 MHz, and a N_2O/SiH_4 gas ratio of 7. After lithography this layer is patterned and etched with buffered hydrofluoric acid (BHF) to create vias that contact the bottom electrode to the second metallization level. Finally, a second 1.5 μm thick Al layer is deposited by e-beam and patterned to form the second electrode, the RF ground-signal-ground (GSG) access pads, and the surrounding ground planes. The two Al layers are precisely etched in the Corial system using a mixture of BCl_3 (boron trichloride) and Cl_2 (chlorine) gases.

The two-port S-parameters of the device under test (DUT) structure are measured using a Keysight N5242B PNA-X 26.5 GHz vector network analyzer, using on-wafer RF probes in GSG configuration. The short-open-load-thru (SOLT) procedure is used to calibrate the test setup over a frequency range from 20 MHz to 10 GHz. The characteristic impedance of the test system is 50 Ω. Besides the on-chip measurement, ADS software is used to simulate both structures (DUT and Open dummy) through the physical properties of the materials given in Table I. The measured and simulated S-parameters of the DUT and Open structures are first converted into

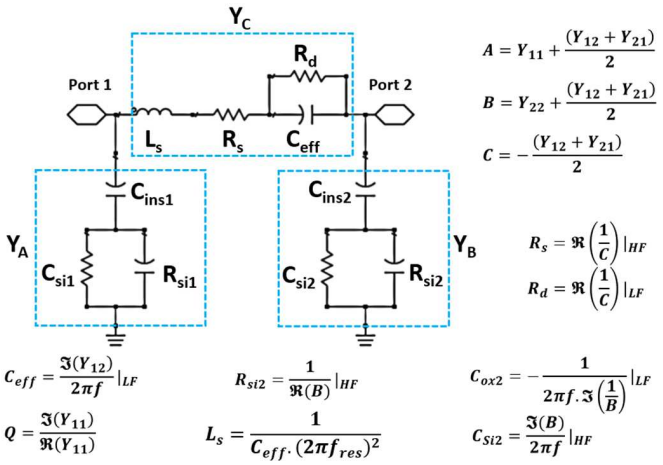

Fig. 2. Lumped-element equivalent electrical circuit of the on-chip MIM capacitor and their extraction equations.

Y-parameters [17]. Using the Open de-embedding method [9], [17], the parasitic contributions from the ground and the pads are removed, yielding the de-embedded Y-parameters of the intrinsic MIM capacitor, as

$$Y = Y^{\text{DUT}} - Y^{\text{open}}. \tag{1}$$

III. Capacitor Characteristics Extraction

A. Lumped-Element Model Description

On-chip MIM capacitors can be represented by a lumped π-network, justified by their small dimensions compared with the wavelengths in the frequency range used in practice [9]. The proposed π model (Fig. 2) uses three complex admittances, Y_A, Y_B, and Y_C. The relationship between these admittances and the de-embedded admittance matrix is expressed as [17]

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_A + Y_C & -Y_C \\ -Y_C & Y_B + Y_C \end{bmatrix} \tag{2}$$

where Y_C is the mutual admittance that couples the two ports, and Y_A and Y_B are the admittances seen to ground at ports 1 and 2, respectively (Fig. 2). The main (interelectrode) branch Y_C of the model contains the effective capacitance (C_{eff}), which represents the capacitance between the two metal plates; the series resistance (R_s), which models the resistive losses in the metal electrodes and interconnects (vias, tracks); the series inductance (L_s), which accounts for parasitic inductance from the interconnects and vias; and the dissipation resistance (R_d), which represents the dielectric leakage losses (dc or low-frequency losses in the insulator) linked to current leakage through the dielectric material (due to imperfections, trap states, or tunneling). Each substrate-loss branch (appearing in Y_A and Y_B) consists of the insulating dielectric capacitance, C_{ins}, between each electrode and the conductive substrate through the dielectric stacking layers, and of R_{si} and C_{si} that, respectively, represent the parasitic substrate resistance and capacitance at high frequencies, which mimic the conductive losses in the silicon substrate due to its finite resistivity and parasitic capacitance [18].

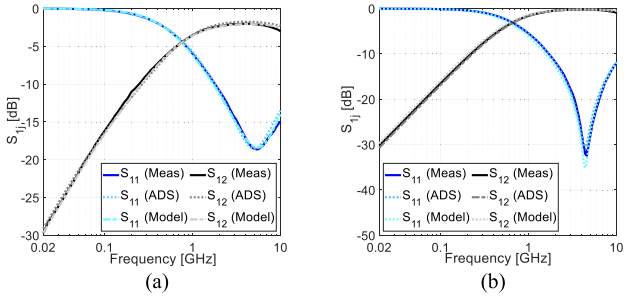

Fig. 3. Measured, lumped-element model and simulated de-embedded S_{1j}-parameters (j = 1, 2) of the MIM capacitor on (a) Std-Si and (b) HR-Si+TR substrate.

TABLE II
Extracted Lumped-Element Parameters Obtained by Fitting the Model of Fig. 2 to Measurements on the Two Different Substrates Over the Measured Frequency Range (20 MHz–10 GHz)

Lumped-element parameter		*Std-Si*	*HR-Si+TR*
Main branch	C_{eff} [pF]	2.73	2.62
	R_s [Ω]	3.8	3.95
	R_d [kΩ]	220	220
	L_s [nH]	0.83	0.79
Substrate-loss branch: Port 1/ Port 2	C_{ins1} / C_{ins2} [pF]	0.8 / 5.67	0.11 / 0.21
	C_{si1} / C_{si2} [fF]	86 / 110	65 / 90
	R_{si1} / R_{si2} [kΩ]	0.28 / 0.17	22 / 16

B. Lumped-Elements Extraction and Validation

To evaluate the proposed lumped-element model and quantify substrate effects on MIM capacitor performance, we extracted all model parameters for devices fabricated on Std-Si and HR-Si+TR substrates (Table II). Extraction is performed over 20 MHz to 10 GHz using the analytical expressions provided in Fig. 2 and the methodology established in [9] and [17]. The extracted parameters are then implemented in the π-equivalent circuit to compute the two-port S-parameters for direct comparison with measurements. As Fig. 3 illustrates, the modeled S-parameters agree closely with both the measured and ADS-simulated de-embedded responses, which 1) validates the accuracy of the lumped-parameter extraction; 2) confirms the reliability of the ADS setup and material properties; and 3) supports the robustness of the substrate advantage analysis that follows. For clarity, only S_{1j} (j = 1, 2) are plotted, since reflection coefficients and voltage gains display similar frequency trends owing to the device's structural symmetry. As shown in Table II, the main branch parameters for Std-Si and HR-Si+TR are almost close within experimental uncertainty. In contrast, branch B, associated with the bottom electrode of the MIM capacitor, exhibits a higher equivalent admittance because of its closer proximity to the substrate. The observed asymmetry between Y_A and Y_B arises from the different dielectric stacks beneath the two electrodes, which alter the field distribution and substrate-coupling paths, thereby accounting for the observed port-to-port loss differences. Finally, while R_{si} and C_{si} primarily reflect substrate-doping differences, the low-frequency insulator capacitance C_{ins2} agrees with the expected oxide value for Std-Si but is unexpectedly more than an order of magnitude smaller for HR-Si+TR; this discrepancy is examined in detail in the next sections.

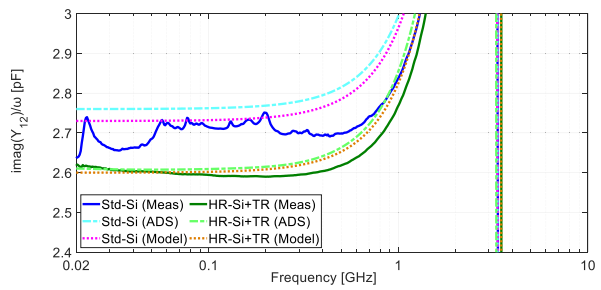

Fig. 4. Measured, simulated, and model results of the imaginary part of the admittance Y_C, representing the effective capacitance at low frequency, for the MIM capacitor on both substrates.

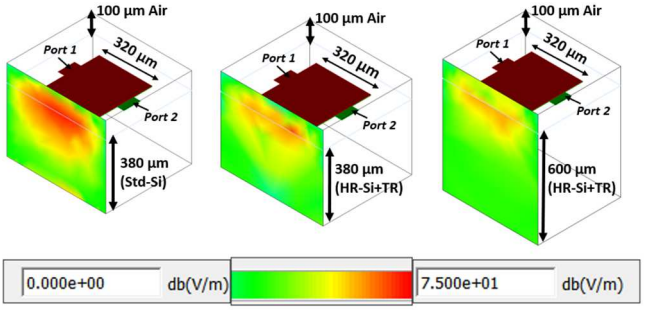

Fig. 5. Low-frequency electrostatic simulations comparing electric-field distributions for identical MIM capacitors on a 380 μm-thick Std-Si substrate and on HR-Si+TR substrates of 380 and 600 μm thickness for comparison.

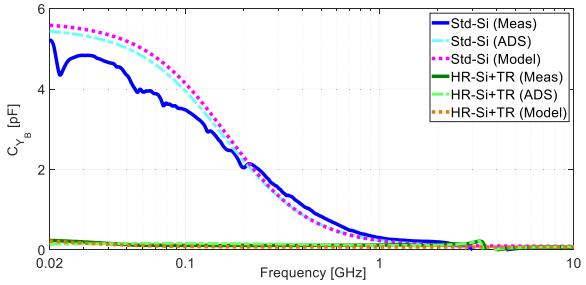

Fig. 6. Measured (solid lines), simulated (dot-dashed lines), and model (dashed lines) results for the equivalent capacitance C_B of branch B (port 2) for the MIM capacitor on both substrates, plotted from 20 MHz upward.

IV. Capacitor Characteristics Analysis

A. Effective Capacitance

The curves in Fig. 4, yielding the effective capacitance (C_{eff}) at low frequencies below the resonance, derived from measurements, simulations, and the equivalent model, show reasonable agreement, confirming the validity of our analyses. It should be pointed out that Y_{12} quantifies the port-to-port coupling, whereas Y_{11} contains both the interelectrode contribution and parasitic substrate shunts. Our extraction procedure explicitly separates these terms to obtain the intrinsic interelectrode capacitance C_{eff} and the substrate-loss branch parameters. As expected, the measured C_{eff} at low frequencies slightly exceeds the intrinsic capacitance (C_{int}) because of substrate interactions and parasitic coupling. Here, C_{int} refers to the substrate-independent ideal capacitance, defined solely by geometry and dielectric properties (including fringing effect), excluding any substrate-induced coupling and parasitics. This intrinsic value can be calculated as [19]

$$C_{\text{int}} = \varepsilon_0 \varepsilon_r \frac{wl}{d} + \varepsilon_0 \varepsilon_r \frac{w}{2\pi} \ln\left(\frac{2\pi l}{d}\right) \tag{3}$$

where w and l are the MIM electrode width and length (equal for our devices), d denotes the PECVD SiO_2 thickness, and ε_r is its relative permittivity. This analytic expression thus gives 2.54 pF, comprising the contribution of the areal field between the electrode plates (2.38 pF) and the fringing-field term (0.16 pF). This aligns quite well with measurements showing a C_{eff} of about 2.73 pF (Std-Si) and 2.62 pF (HR-Si+TR), corresponding to increases of 7.5% and 3.5% over C_{int}, respectively. The excess capacitance does not indicate a larger intrinsic dielectric capacitance but rather additional fringing-field coupling into the bottom dielectric/substrate stack [20], estimated to be 0.19 and 0.08 pF for the Std-Si and HR-Si+TR cases, respectively. In fact, a low-resistivity substrate induces stronger fringing field coupling at the edges of the MIM capacitor, whereas a HR substrate acts as a lossy dielectric at high frequencies rather than a typical semiconductor, thereby reducing the coupling strength, as will be further validated in Section IV-B. Importantly, the relative impact of this substrate-induced coupling on C_{eff} becomes significantly more pronounced as the electrode dimensions shrink, a trend also noted in other studies that, for instance, proposed substrate backside bulk etching beneath the electrodes to mitigate the additional fringing related to the substrate [9].

To highlight substrate effects, we added low-frequency electrostatic simulations (Fig. 5) comparing electrical field distributions for identical MIM capacitors on Std-Si and HR-Si+TR. The results indicate that in the 380 μm-thick Std-Si substrate, the fringing field is intense but confined to a shallow region beneath the capacitor—leading to higher C_{eff} and larger substrate losses—whereas in the HR-Si+TR substrate, either of equivalent thickness or with the 600 μm experimental substrate, the reduced carrier screening allows the field to penetrate more deeply into the bulk, effectively reducing substrate coupling and losses.

B. Substrate Leakage

Fig. 6 depicts the frequency-dependent equivalent capacitance C_B of the substrate-loss branch Y_B in the lumped-element model, representing the capacitive coupling between the bottom electrode and the backside substrate ground. Small ripples visible in the Std-Si C_B and C_{eff} traces (Figs. 4 and 6) originate from measurement noise and error propagation during de-embedding on the more lossy substrate, where small phase/amplitude errors in the S-parameters produce larger variations in $\Im(Y)/\omega$. These fluctuations are within the experimental uncertainty and do not alter the reported trends or conclusions.

Given the proximity of the bottom electrode to the substrate, analyzing C_B provides a more effective indicator for evaluating substrate-related losses. Theoretically, the substrate-loss branch's equivalent capacitance decreases from the low-frequency plateau C_{ins} and, as frequency increases, asymptotically approaches the series combination of C_{ins} and C_{si}, where C_{si} is typically dominant given its relatively smaller

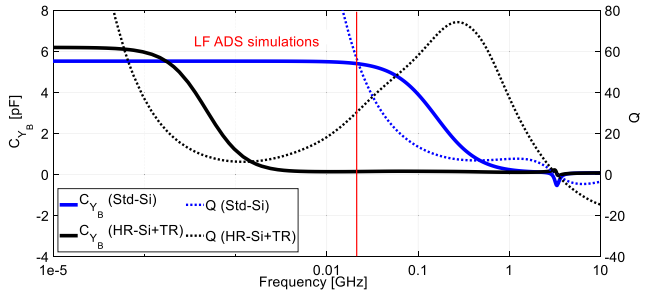

Fig. 7. Simulated equivalent capacitance of branch B (solid lines) of the MIM capacitor is shown together with the corresponding Q-factor (dashed lines), starting from 10 kHz (the vertical red line, located at 20 MHz, indicates the transition between simulation-only results and those validated by measurements).

value (due to the large thickness of the silicon substrate). In Fig. 6, measurements, simulations, and circuit modeling follow this behavior and converge above 1 GHz toward comparable minimum capacitances of roughly 90–110 fF, consistent with C_{si} for both Std-Si and HR-Si+TR. However, the measured band (20 MHz–10 GHz) does not extend low enough to reach the C_{ins} plateau, particularly for the HR-Si+TR devices. To address this, Fig. 7 presents ADS simulations of C_B down to 10 kHz, from which we estimate $C_{ins} \approx 6.2$ pF for HR-Si+TR and $C_{ins} \approx 5.52$ pF for Std-Si. These intrinsic, low-frequency values are not directly observable with our instrumentation because at 20 MHz, the experimentally measurable apparent capacitance for HR-Si+TR is already only ≈ 0.21 pF. Accordingly, Table II reports fit parameters extracted within the experimental band (20 MHz–10 GHz), whereas the low-frequency simulations down to 10 kHz recover the intrinsic insulator capacitance, which is slightly larger for HR-Si+TR. This apparent discrepancy arises because of C_B transitions from the low-frequency plateau C_{ins} to the high-frequency limit C_{si} at a characteristic frequency that is strongly influenced by the effective substrate resistivity. This frequency, referred to as the inflection frequency (f_i), is identified by examining the change in curvature of the C_B curves through a second derivative calculation and is given by

$$f_i = \frac{1}{2\pi R_{si}\sqrt{C_{si}\,(C_{ins}+C_{si})}} \approx \frac{1}{2\pi R_{si}\sqrt{C_{ins}C_{si}}}. \quad (4)$$

For the Std-Si, f_i appears at around 160 MHz in both measurements and simulations; consequently, at 20 MHz (the lowest measured point), the substrate-branch capacitance has essentially reached its low-frequency plateau C_{ins}. In contrast, for HR-Si+TR, f_i is shifted downward to approximately 480 kHz, meaning that at operating frequencies above 20 MHz, the substrate-branch capacitance C_B has effectively reached its low-frequency asymptote ($\approx C_{si}$). This downward shift of f_i is driven primarily by an increase in the effective substrate resistance R_{si}, roughly three orders of magnitude larger in HR-Si+TR, which moves the inflection frequency to much lower frequencies. Physically, f_i marks the transition of the substrate to a dielectric-like behavior, in which capacitive coupling dominates over resistive conduction, which occurs at much lower frequencies in the HR-Si+TR substrate. Indeed, the TR layer inhibits surface conduction and parasitic charge motion, reducing the dielectric-mode transition frequency by more than 300×, allowing a wider operating RF range. We also observe a modest reduction in the substrate capacitance C_{si}, from 110 to 90 fF, as shown in Table II, likely due to the altered effective substrate thickness of the HR-Si+TR substrate. This reduction in C_{si} further promotes the transition of the substrate into the dielectric-mode operation, as described by (4), thereby enhancing isolation and overall device performance across the target frequency band.

To achieve improved isolation, it is generally preferable to minimize the insulator capacitance (e.g., via thicker oxides, low-κ dielectrics, or grounded shields) while pairing the stack with a HR substrate. Our simulations reveal, however, that the intrinsic C_{ins} for the HR-Si+TR stack appears to be larger than for Std-Si at the same oxide thickness, primarily because the HR-Si+TR stack uses PECVD SiO_2 with a higher relative permittivity ($\varepsilon_r \approx 5$) than the thermal SiO_2 ($\varepsilon_r \approx 4$) on Std-Si. Although a larger C_{ins} increases the loss-branch admittance at low frequency (and is therefore detrimental to low-frequency isolation), it concomitantly contributes to lowering the inflection frequency, as described by (4), thereby reducing the effective C_B across the intended RF band, and thereby improves high-frequency isolation.

Finally, the impact of the C_B loss branch can be characterized as frequency-dependent and is discussed here before analyzing its effect on the MIM Q-factor in the next section. At low frequencies, C_{ins} acts as a high-impedance barrier, restricting current flow into the substrate and resulting in negligible losses. Around the inflection frequency ($f \approx f_i$), C_{ins} permits increased current flow into the substrate, while R_{si} dominates over C_{si}, leading to peak resistive losses and maximum power dissipation. At higher frequencies, C_{ins} behaves as a low-impedance path, enabling strong coupling to the substrate, while C_{si} increasingly shunts current away from R_{si}, significantly reducing resistive losses and enforcing the dielectric-like behavior of the substrate. Thus, power dissipation through the substrate decreases with increasing frequency, and f_i marks the worst-case scenario for power loss and noise coupling through the C_B branch. It is noteworthy to mention that the higher R_{si} of the HR-Si+TR further suppresses substrate losses around f_i, resulting in reduced substrate losses as indicated by the improved Q-factor in Fig. 7 and discussed in detail in the following section.

C. Quality Factor and SRF

The Q-factor of an on-chip capacitor is defined as the ratio of energy stored to energy dissipated per cycle and is typically calculated as the ratio of the imaginary to the real part of Z_{11}, thereby accounting for all loss mechanisms (including electrode resistance and substrate coupling). Fig. 8 compares Q-factor curves from measurements, simulations, and the equivalent model for both substrate types, showing good agreement across datasets. Overall Q-factor degradation is primarily governed by three distinct loss mechanisms: dielectric leakage, substrate conduction (or coupling), and metallic resistive dissipation, each dominating within a specific frequency range.

At low frequencies, dielectric losses (via R_d), which represent the leakage current through the dielectric, dominate

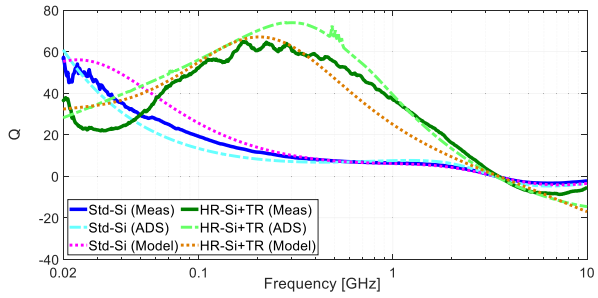

Fig. 8. Measured, simulated, and modeled results of MIM capacitor: Q-factor versus frequency for the two substrate cases.

and increase with frequency. The higher the value of R_d, the smaller the impact of these losses. At intermediate frequencies, around f_i, resistive substrate losses through the C_B branch become dominant, as discussed in Section IV-C. The Si-HR+TR substrate shifts f_i to much lower frequencies, thereby confining substrate-related losses to a narrower frequency band. As a result, the Q-factor for HR-Si+TR undergoes a sharper dip compared with the Si-Std (Figs. 7 and 8) but quickly recovers due to the dominance of C_{si} in higher frequencies, indicating a rapid transition to dielectric-like substrate behavior. In contrast, in the case of Si-Std, this transition is characterized by a short stagnation of the Q-factor, as shown in Figs. 7 and 8.

At higher frequencies, approaching the SRF, losses are dominated by the interaction between the series inductance and C_{eff}, further exacerbated by the skin effect, which leads to a renewed decline in the Q-factor (Figs. 7 and 8). The SRF ($\propto 1/(L_s C_{\text{eff}})^{1/2}$) is identified as the frequency at which the capacitive and inductive reactances cancel each other out (i.e., $\Im(Z) = 0$) and corresponds to the zero crossing of the Q-curve. Notably, the HR-Si+TR-based capacitor exhibits a higher SRF of approximately 3.5 GHz compared to around 3.4 GHz for the Std-Si-based capacitor (Fig. 8), primarily due to the reduction of C_{eff}, which is attributed to the lower fringing capacitance discussed in Section IV-A. As a result, the HR-Si+TR capacitor achieves a significantly higher Q-factor across a wide frequency range from 50 MHz to 3 GHz, benefiting simultaneously from the downward shift of f_i and the upward shift of the SRF.

More concretely, at 20 MHz, the Q-factor for Std-Si is approximately 58 but decreases rapidly with increasing frequency due to substrate dielectric losses and then substrate losses (Fig. 8). By contrast, the HR-Si+TR capacitor exhibits an initially sharper drop in Q-factor but then recovers to reach a peak, reaching a Q peak of about 65 at 170 MHz (compared to only 13 for Std-Si) before declining again at higher frequencies (Fig. 8). This enhanced Q-factor behavior is sustained over a wide frequency range and is primarily attributed to the significantly lower f_i in the HR-Si+TR substrate. These findings confirm that HR-Si substrates with an integrated poly-Si TR layer offer clear advantages for high-frequency, low-loss MIM capacitor applications, particularly in RF circuits.

D. Geometric Parameters Impact

Additional ADS simulations varying interelectrode dielectric thickness and capacitor footprint on both substrates reveal that increasing oxide thickness lowers capacitance density but also weakens fringing-field penetration, thereby improving isolation. On Std-Si, this leads to a strong Q-factor enhancement by mitigating conduction losses, whereas on HR-Si+TR, the incremental benefit is smaller since substrate losses are already suppressed and the device is approaching the dielectric-loss limit. Both substrates therefore benefit from thicker oxides, though the improvement is far more pronounced on Std-Si, while HR-Si+TR provides greater advantages for thin dielectrics and compact layouts where fringing fields dominate. Scaling down the footprint further reduces both intrinsic and substrate capacitances, but as device area shrinks, fringing fields become increasingly significant, making HR-Si+TR particularly valuable for maintaining or even enhancing Q-factor in small MIM capacitors.

V. Comparison to State-of-the-Art

Unlike previous studies that have primarily focused on optimizing MIM capacitor design [1], [2], [9], [12], [13], our work investigates, for the first time, the use of an HR-Si substrate combined with an additional undoped TR layer. This substrate technology, which is fully compatible with large-scale CMOS manufacturing, has already proven significant improvements with CPW lines as well as on-chip inductors [14], but has not yet been explored for capacitive devices. Practically, the use of an HR-Si+TR substrate leads to a substantial increase in the substrate resistance R_{si} from 0.17 to 16 kΩ, while slightly reducing C_{si2} from 110 to 90 fF. These changes effectively suppress substrate-related conduction losses and directly enhance MIM capacitor performance. Specifically, the rapid reduction in the equivalent capacitance C_B, and similarly C_A, yields an approximately fivefold improvement in the Q-factor at 170 MHz and sustained superior performance over a broadband (50 MHz to 3.5 GHz). The enhanced isolation provided by HR-Si is attributable to the TR layer that suppresses mobile carrier parasitic conduction near the Si/SiO_2 interface. Deep-level traps capture carriers and thereby increase the effective substrate resistivity seen by the fringing fields [21]. In our devices this manifests electrically as the large increase in the effective substrate resistance R_{si} ($\times 10^3$) and a downward shift of the substrate inflection frequency f_i (Std-Si ≈ 160 MHz → HR-Si+TR ≈ 480 kHz), so the substrate enters a dielectric-like, low-loss regime at much lower frequencies. The net effect is a reduced effective substrate capacitance C_B across the RF band, a Q-peak shifted into the hundreds of megahertz, and a substantial improvement of MIM capacitor performance for RF applications.

For the same purpose, other studies have employed substrate backside etching to suspend MIM structures of various dimensions, resulting in significant improvements in the Q-factor [9]. Specifically, increases in Q-factor by approximately 32.3% (for 100 × 100 μm^2), 38.9% (for 100 × 50 μm^2), and 70.3% (for 150 × 100 μm^2) were reported. These enhancements are attributed to the substantially higher measured equivalent substrate resistance (R_{si2} = 2560 kΩ) and reduced parasitic capacitance (C_{si2} = 7.52 fF) achieved through substrate removal. Furthermore, suspended structures exhibit a notable shift in the peak Q-factor frequency and a reduction in C_{eff} by around 5% compared to that of their unsuspended counterparts.

TABLE III
COMPARATIVE ANALYSIS BETWEEN THIS WORK AND PREVIOUS STUDIES

Ref	substrate	Area (μm^2)	C_{eff} (pF)	Q_{max}	f_{Qmax} (GHz)	f_{res} (GHz)
[2]	Std-Si / Shield	20×20	0.374 /0.374	--	--	--
[9]	Std-Si / Suspended	100×100	3.46 /3.27	46.8 /61.9	0.35 /0.65	~7
		100×50	1.78 /1.69	40.1 /55.7	0.45 /1.3	--
		150×100	5.11 /4.86	44.8 /76.3	0.25 /0.35	--
This work	Std-Si / HR-Si+TR	320×320	2.73 /2.62	13.5 /65	0.02 /0.17	3.4 /3.5

While these results demonstrate the potential of substrate etching to improve performance, this technique poses significant manufacturing challenges, including increased process complexity, incompatibility with standard CMOS workflows, and heightened risk of structural damage due to thin oxide layers and fragile interconnects. As an alternative, integrating MIM capacitors with a ground shield has been proposed to reduce unwanted coupling into the substrate [2], [20]. However, this approach introduces additional shunt capacitances between the signal ports and the shield, which must be carefully managed as they can significantly degrade performance in dual-port configurations [20]; a phenomenon commonly referred to as the kink effect [22]. Finally, Table III provides a comparative overview of our findings alongside selected prior studies, highlighting how the HR-Si+TR substrate offers a compelling solution for high-frequency MIM capacitor design, combining enhanced performance with compatibility for standard CMOS integration and a simplified manufacturing process.

VI. CONCLUSION

This study highlights the critical role of the substrate in optimizing the performance of MIM capacitors for RF applications. The findings demonstrate that the use of HR-Si+TR substrates significantly outperforms Std-Si, delivering a fivefold improvement in Q-factor (reaching 65 versus 13) at 170 MHz and maintaining superior performance across a broad frequency range from 50 MHz to 3 GHz. The slight reduction in the effective capacitance contributes to a slight increase in the self-resonance frequency, from 3.4 to 3.5 GHz. These performance enhancements are primarily attributed to a lower inflection frequency associated with the HR-Si+TR, which effectively reduces substrate-related losses by confining the substrate-related loss mechanisms to lower frequencies and pushing the self-resonance frequency to higher frequencies. Together, these effects result in an improved Q-factor, enhanced resonance behavior, and better substrate isolation. Considering these advantages, along with its compatibility with standard CMOS manufacturing processes, the HR-Si+TR confirms its role as a promising solution for high-performance large integrated MIM capacitors.

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