The Environmental Footprint of IC Production: Meta-Analysis and Historical Trends

Thibault Pirson†, Thibault Delhaye†, Alex Pip‡, Grégoire Le Brun†, Jean-Pierre Raskin†, David Bol†
†*ICTEAM Institute* - ‡*IMMC Institute*, Université catholique de Louvain, Belgium
Email: {thibault.pirson, thibault.delhaye, alex.pip, gregoire.lebrun, jean-pierre.raskin, david.bol}@uclouvain.be

***Abstract*—Given the ubiquity of electronic devices and the increasing technical challenges to continue CMOS technology downscaling following Moore's Law, it becomes critical to better quantify the environmental impacts of IC production. In this context, this paper compares 22 key relevant sources, from scientific literature, commercial state-of-the-art databases, industry roadmaps, and foundries CSR reports, over the period 2010-2020. Three environmental indicators, i.e., carbon footprint, primary energy, and water consumption, are considered and normalized per silicon area. Despite a significant variability between the sources, we observe a clear increase of the environmental footprint with technology downscaling. We then use historical data from foundries to analyze the long-term evolution of environmental impacts normalized to the silicon area over 40 years. We highlight the arduous challenge of further decreasing environmental indicators per cm^2 below these values. As the global IC production volumes keep on increasing, it raises serious concerns regarding the sustainability of the IC production sub-sector and calls for rethinking the road ahead with sobriety.**

***Index Terms*—life-cycle assessment, sustainability, carbon footprint, integrated circuits, semiconductors, sobriety.**

I. Introduction

THE worldwide production of integrated circuits (ICs) is continuously growing, supported both by the increasing pervasiveness of electronic devices in our societies and the very low re-usability of these components. Even though the size of electronic components is usually very small, their production is known to be very intensive in terms of resources and energy due to the complex processes involved [1]. As these electronic devices are the building blocks of information and communication technologies (ICTs) which support current digital products and services, it becomes critical to better evaluate their environmental impacts. This is even more important given the high investments in the ICT sector [2] and the need for environmentally-aware roadmaps and policies. Although there is no consensus regarding the future trend of the ICT environmental footprint, its carbon footprint was evaluated at about 1000–2000 MtCO2-eq in 2020, or equivalently 2%–4% of the world greenhouse gas (GHG) emissions [3]. A significant part of this footprint is attributed to the production of ICT equipments, i.e., 281-543 MtCO2-eq [3]. More specifically, the production of IC is known to be responsible for an important share of cradle-to-gate impacts [4]–[6], therefore justifying special attention.

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To support the evaluation of environmental impacts over multiple indicators, a standardized methodology known as life-cycle assessment (LCA) [7] is generally used. However, unlike the environmental impacts from the use phase, the impacts related to the production are more difficult to measure directly and usually out of reach for people outside of semiconductor foundries [4], [8]. This relates to a limitation pointed out for years in the field of semiconductors [4], [6], [8], [9], i.e., the lack of up-to-date data due to confidentiality barriers as well as the complexity and quick evolution of manufacturing processes. This hinders a proper understanding of the environmental footprint of the IC production sub-sector.

To tackle this issue, in this work we gather 22 relevant sources from different literature categories to provide a clear overview of the data available. In addition, we identify the gaps and similarities between the sources. To the best of our knowledge, this is the first study of this kind, going well beyond previous scientific literature and covering multiple environmental indicators. The paper is structured as follows. Section II outlines the methodology while Section III presents and interprets the results, which are then put in perspective with historical data. Finally, Section IV highlights the main conclusions.

II. Methodology

A. Four Different Literature Categories

In order to cover a wide range of data while avoiding field-related biases, four categories of sources are considered, i.e., foundry reports, semiconductor industry roadmaps, scientific literature, and commercial state-of-the-art databases.

Foundries must report annually their environmental performance in corporate social responsibility (CSR) reports which ensure a systematic source of information. Four *pure-play* foundries are considered, i.e., TSMC, UMC, SMIC, and GF, together with one integrated device manufacturer, i.e., STMicroelectronics. The data for Samsung and Intel are either too aggregated or not available, which prevents us from including them in this study. Roadmaps provide targets rather than actual data from on-site measurements. A group of industry experts from Europe, Japan, Tawain, United States and Korea published the International Technology Roadmap for Semiconductors (ITRS), including guidelines for *environment, safety and health (ESH)*. Apart from the ITRS roadmaps, no other official document with explicit target for the environmental impacts of semiconductors was found. Scientific literature is an important source of information as several peer-reviewed

studies have been carried out for years. Let us mention that we also included three relevant non peer-reviewed reports in this literature category. Finally, commercial databases provide specific LCA data and usually benefit from maintenance. Three commercial state-of-the-art databases are considered, i.e., GaBi, EIME, and Ecoinvent.

B. Functional Unit and Scope

In this study, we focus on the environmental impacts of IC production over three indicators, i.e., primary energy demand (PED), global warming potential (GWP), and water consumption. Even though these indicators do not provide a comprehensive picture of all environmental impacts [6], they already cover important aspects. In addition, they are the ones usually reported in the different literature categories, which makes the analysis possible. The core results of this study are based on data published over the time period 2010-2020.

Choosing the most appropriate functional unit and metrics to characterize the environmental impacts of IC production still remains an open question, especially because semiconductor manufacturing is a fast-evolving sector [1], [9]. In this study, we choose to normalize all environmental indicators by the silicon die area in cm^2, as done in [9] and [10]. This is also supported by the presence of area in the common power-performance-area-cost (PPAC) targets.

A well-known challenge for LCA practitioners is the concordance of scopes when gathering data from different sources. Consequently, a transparent methodology is critical to ensure reliable conclusions in the identification of gaps and similarities. To tackle this challenge, we define 10 criteria which are then used to compare all sources included in this study, i.e., (1) technology type and inclusion of front-end/back-end; (2) CMOS technology node; (3) wafer size; inclusion of (4) production yields and of (5) infrastructure and upstream materials; (6) geographical location; (7) covered environmental indicators; (8) process details and transparent normalization; (9) assessment method; and (10) primary data and dependencies.

III. Results

A. Transversal Analysis of the Sources

Table I shows the classification of all sources with respect to the 10 selected criteria. This clearly shows the existing mismatch between the scope and LCA approach of the considered sources, revealing the complexity to implement a proper harmonization across all sources. We decided not to perform such an harmonization as sufficient level of information was rarely disclosed. Nevertheless, two clusters can be identified: scientific literature and databases on the one side and foundry reports and industry roadmaps on the other side. While the first cluster allows for a node-wise analysis as illustrated in Fig. 1, the second one provides node-aggregated temporal trends as shown in Fig. 2. These two clusters cannot be directly compared to each other, but they both bring useful insights to better understand the environmental impacts of IC production from different yet complementary perspectives, as explained in the following sections.

B. The Environmental Impacts of Technology Downscaling

There is an obvious inter-sources variability within the scientific literature and databases cluster as shown in Fig. 1, mainly due to the mismatch of scopes. Consequently, comparing the absolute values is of limited interest and relevance. However, focusing on the general trend depicted in Fig. 1 reveals a more compelling conclusion: the environmental impacts per area are clearly increasing with technology downscaling below 0.13 µm. This is observed both in the scientific literature and in databases, despite the scope mismatch. It seems also that this increase is accelerating for advanced nodes.

C. The Impact of Pursuing Advanced Scaling for Foundries

We found no public data or evidence disclosed by foundries to allow a consistent estimation of the environmental impacts with respect to the technology node. Consequently, we analyzed the evolution of aggregated environmental impacts per area with respect to time instead of the technology node, as illustrated in Fig. 2. This highlights two opposing trends: the impacts per area either (slightly) decrease over the period 2010-2020 for most of the foundries while they increase for TSMC. More importantly, these trends seem to be foundry-dependent but consistent for all environmental indicators. Aside from the geographical location, the maturity of their process, and the output production volume, an important difference is the mix of technology nodes in the foundry production volume. Indeed, TSMC is the only industry in this study engaged in the production of technology nodes below 10 nm, which could well explain why it demonstrates a net increase in the impacts per area. This is not due to a lack of effort from the foundry to pursue efficiency but rather to the introduction of more demanding processes such as extreme ultra-violet (EUV) lithography for scaling purpose [10]. Other foundries keep demonstrating slight overall impacts reduction per cm^2, suggesting that a reduction of the impacts per area is possible, provided that advanced scaling is not pursued.

The comparison between the foundry impacts and the roadmap targets shows that the industry is still facing huge challenges to reach these targets. The high impact of EUV is also explicitly pointed out in ITRS roadmaps and illustrated in Fig. 2(a).

D. Long-Term Perspectives from Historical Data

Although LCA is generally used either to evaluate, compare, and optimize the impacts of a specific device or service, it can also be useful to analyze trends over time. In this context, we gathered historical data reported for the period 1980-2010 and we used the same 10 criteria to support the analysis and the identification of scope mismatch, as depicted in Table I. This aims at providing long-term perspectives on the evolution of environmental impacts per cm^2, while it does not intervene with the core results. For most of the historical data, impact values were disclosed in the scientific literature, although they were directly coming from the foundries.

TABLE I

CLASSIFICATION OF ALL SOURCES CONSIDERED IN THIS STUDY ACCORDING TO THE 10 CRITERIA DEFINED IN SECTION II.

Criteria	**(1)**			**(2)**	**(3)**	**(4)**	**(5)**		**(6)**	**(7)**	**(8)**		**(9)**	**(10)**	
	Tech. type	**Front-end**	**Back-end**	**Tech. node (nm)**	**Wafer size (mm)**	**Yield**	**Infra.**	**Upstr. materials**	**Geogr. location**	**Indic. coverage**	**Process details**	**Transp. norm.**	**Assess. method**	**Prim. data**	**Depend-encies**
Foundry reports															
TSMC, CSR & 20-F (2010-2020)	mix	✓	✗	mix	mix	⊖	✓	✗†	GLO	Full	✗	✗	↓	✓	✗
UMC, CSR & 20-F (2011-2020)	mix	✓	✗	mix	mix	⊖	✓	✗†	GLO	Full	✗	✗	↓	✓	✗
SMIC, CSR (2011-2020)	mix	✓	✗	mix	mix	⊖	✓	✗†	GLO	Full	✗	✗	↓	✓	✗
STmicro, CSR & 20-F (2011-2020)	mix	✓	✗	mix	mix	⊖	✓	✗†	GLO	Full	✗	✗	↓	✓	✗
GF, CSR & F-1 (2011-2020)	mix	✓	✗	mix	mix	⊖	✓	✗†	GLO	Full	✗	✗	↓	✓	✗
Industry roadmap															
ITRS ESH (2015)	⊖	✓	✗†	⊖	200;300	✗	✓	✗	⊖	PED;W	✗	✓	⊖	⊖	✗†
Scientific literature															
Boyd, PhD (2012)	L;M	✓	✗†	350→32	200;300	✓	✓	✓	USA	Full	✓	✓ †	⇅	✓	✓
Schimdt, Int J LCA (2012)	L;M	✓	✗	⊖	300	✓	✓	✗	GLO	GWP	✓	✓	⇅	✗	✓
Prakash, ProBas report⋆ (2013)	M	✓	✓	45	300	✓	✗	✗	⊖	PED;W	✓	✓	⊖	✗	✓
Bol, FTFC (2013)	L	✓	✓ †	130;65	⊖	⊖	⊖	✗†	⊖	GWP	✗	✗	↑	✗	✓
Jones, ICCAD (2013)	mix	✓ †	⊖	45	⊖	⊖	⊖	⊖	⊖	PED;GWP	✗	✓	↓	✗	✓
Teehan, PhD (2014)	⊖	✓ †	✗	⊖	⊖	⊖	⊖	✓	⊖	GWP;PED	✗	✗	⇅	✗	✓
Andrae, Challenges (2014)	mix	✓	✗	⊖	⊖	⊖	⊖	⊖	⊖	GWP	✗	✓ †	⊖	✗	✓
Proske, FF2 report⋆ (2016)	L;M	✓	✓	32	300	✓	⊖	✗†	CN	GWP	✓	✓	⇅†	✗	✓
Ercan, ICT4S (2016)	L;M	✓	✓	⊖	⊖	✓	✓	✓	⊖	GWP;PED	✗	✓	⊖	✓	✗†
Andrae, Challenges (2017)	L	✓ †	⊖	⊖	⊖	⊖	⊖	⊖	GLO	GWP	✗	✓	↑†	✗	✓
Bardon, IEDM (2020)	L	✓	✗	28→3	300	✗†	✓	✗†	GLO	Full	✗	✓	↑	✓	✓
Proske, FF3 report⋆ (2020)	L;M	✓	✗†	60;45;32	300	✓ †	✓	✗†	CN	GWP	✓	✓	⇅†	✗	✓
Das, SEGAN (2020)	M	✓ †	⊖	57	⊖	⊖	⊖	⊖	⊖	PED	✗	✓	⊖	⊖	✓
Commercial databases															
Ecoinvent v3.5 (2018)	L	✓	✓	⊖	200	✓	✓	✗	GLO	Full	✓	✗	⇅	✗	✓
EIME, Bureau Veritas (2019)	mix	✓	✗	130→7	300	✗	✗	✓	TWN	Full	✗	✓	↑	✓	✓
GaBi, Sphera (2020)	L;M	✓	✓	250→14	⊖	✓	✓	✓	GLO	Full	✗	✗	⇅	✓	✓
Historical data															
Williams, EST (2002|1996-1998)	mix	✓	⊖	⊖	150	⊖	✓ †	✗†	GLO	PED◇;W	✗	✓	↓	✓	✗
Williams, EST (2002)	M	✓	✓	⊖	200	✓	⊖	✓	GLO	PED◇	✓	✓	↑	✗	✓
Plepys, PhD (2004|1983-2003)	mix	✓	✗†	mix	150;300	⊖	⊖	✗†	GLO	PED◇;W;GWP◇	✗	✓	↓	✓	✗
Krishnan, EST (2008)	L	✓	✗	130	300	✓	✓	✓	USA	PED	✓	✓	⇅	✓	✗
Deng, JCP (2011|1995-2006)	mix	✓	✗†	⊖	⊖	✗	✓ †	✗†	GLO	PED	✗	✓	↓	✓	✗
Ercan, ICT4S (2016|1995)	mix	✓	⊖	⊖	⊖	✓	✓ †	⊖	⊖	GWP;PED◇	✗	✓	⊖	✓	✗

L : logic M : memory ↑ : bottom-up ↓ : top-down ⇅ : hybrid ⊖ : not available † : implicit, deduced by the authors ⋆ : not peer-reviewed (scientific literature only) ✓ : included ✗: excluded
◇ : converted from the electrical consumption in kWh (PED: assuming a primary energy factor (PEF) of 2.5 | GWP : assuming an average carbon intensity of 0.475 kgCO2eq/kWh)

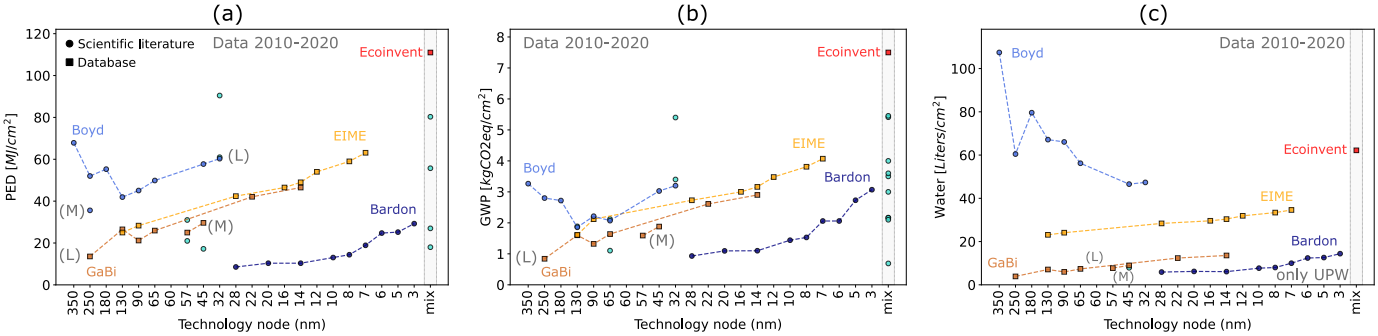

Fig. 1. Node-wise trends based on data from the scientific literature and the databases. This shows the environmental impacts per cm^2 with respect to (a) PED, (b) GWP, and (c) water consumption.

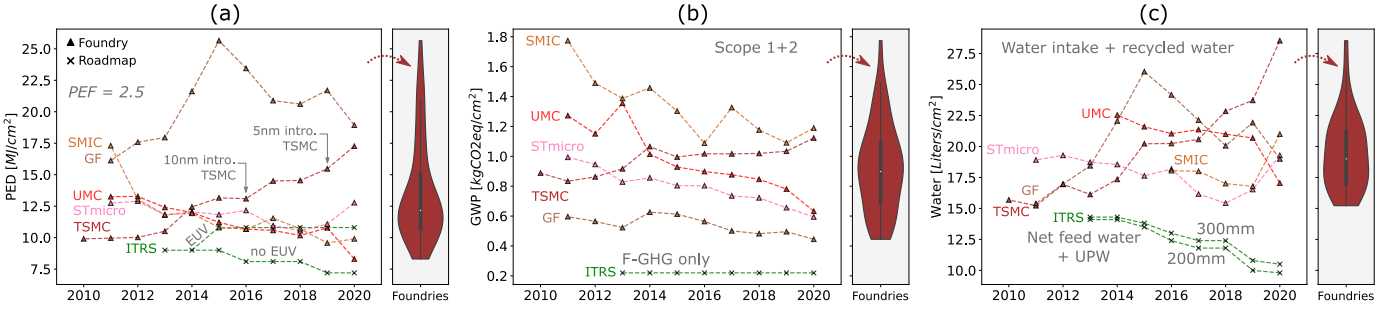

Fig. 2. Node-aggregated temporal trends based on data from foundry reports and industry roadmaps. This shows the environmental impacts per cm^2 with respect to (a) PED, (b) GWP, and (c) water consumption. The left sub-figure exhibits the data for each source while the right sub-figure reflects the aggregated data for all the foundries considered in this study. Assumptions made by the authors are shown in *italic*.

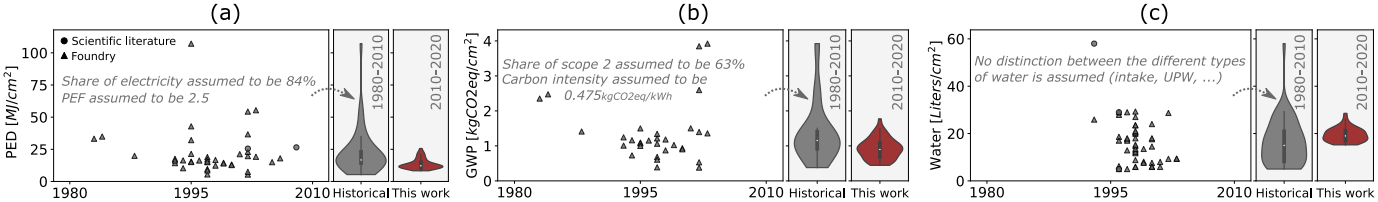

Fig. 3. Long-term perspectives between the results presented in this work (2010-2020) and historical data (1980-2010). The comparison per cm^2 is done only for data from foundries, with respect to (a) PED, (b) GWP, and (c) water consumption. Assumptions made by the authors are shown in *italic*.

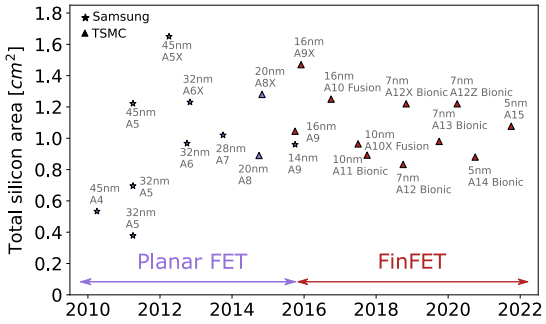

Fig. 4. Evolution of the average chip area of Apple's application processors.

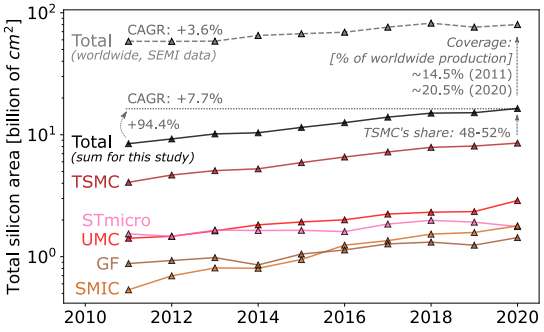

Fig. 5. IC production volumes for the foundries considered in this study and for the worldwide production.

The comparison of the data from the foundries over the period 1980-2010 and 2010-2020 reveals an important finding: environmental indicators normalized per cm^2 did not significantly decrease compared to historical values from 1980-2010, as shown in Fig. 3. Undeniably, the number of transistors fitted on the same area of silicon has tremendously increased since then, as captured by Moore's Law. Nevertheless, the computational demand and the constant increase of functionality also surged in the meantime [1], [9], [11]. The increase in functionality is at the heart of Moore's Law, which explains the almost constant die size despite technology downscaling. When analyzing the evolution of application processor chips from Apple over the last 10 years, Fig. 4 shows that the average die area is roughly constant even though technology node shifted from 45 nm to 5 nm. The environmental consequences of this increase of functionality were already pointed out more than 10 years ago [1]. They can be seen as a rebound effect (Jevons' paradox) of technology downscaling which improves the environmental indicators per transistor [1], [11]–[13].

Focusing on GWP, the Paris Agreement sets an explicit reduction target of global GHG emissions at a rate of 7.6%/year to limit climate change, assuming a start in 2020 [14]. This would therefore require a reduction of the GWP/cm^2 close to 11-14%/year if we assume that the total IC production keeps increasing at the same rate as last decade, as shown in Fig. 5. Therefore, conflicting trends are to be expected if the IC production sub-sector pursues aggressive downscaling with increasing production volumes while committing to rapid reduction in GHG emissions. Nevertheless, advanced nodes could be game changing if used to provide constant functionality and performance with less area, rather than more functionalities with constant area.

IV. Conclusion

It appears very unlikely that optimization of the environmental impacts per cm^2 will be sufficient to quickly reduce the global absolute environmental footprint of the IC production sub-sector, especially for advanced nodes. Moreover, the trend towards more functionalities observed over the last decades reveals a clear rebound effect at the hardware level, absorbing or backfiring efficiency improvements captured by Moore's Law. This is likely to continue as long as higher performance is available, which attests the limits of technology downscaling in being an effective solution for sustainability.

Therefore, we conclude that sobriety must be integrated into technological innovation and technology usage, which calls for rethinking our socio-economic models and innovation roadmaps currently fostering growth in the IC production. Nevertheless, an important question holds: could downscaling remain economically viable if the global IC production volumes flatten or decrease in the long term?

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