The Low-Frequency Noise Behavior of Graded-Channel SOI n-MOSFETs

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1. Abstract

The low-frequency noise of graded-channel (GC) Silicon-on-Insulator (SOI) n-MOSFETs is studied in function of different parameters: the doped channel length L_{eff} and the implantation dose. It will be shown here that there exists a positive correlation between g_m and the corresponding input-referred noise spectral density S_{VG}. The possible trade-off between high gain and low (1/f) noise will be investigated and the physical mechanisms responsible for the observed trends discussed.

2. Introduction

It has clearly been established that the so-called graded-channel (GC) architecture yields advantageous analog and RF performance for SOI MOS transistors in saturation [1-3]. The GC structure consists of an asymmetric channel, whereby a threshold voltage (V_T) implantation is performed at the source side of the device, while a length ΔL at the drain side is screened from it (see experimental). This results in a higher transconductance g_m in saturation, as shown in Fig. 1 and, hence, in a higher open loop gain A_V [1-3].

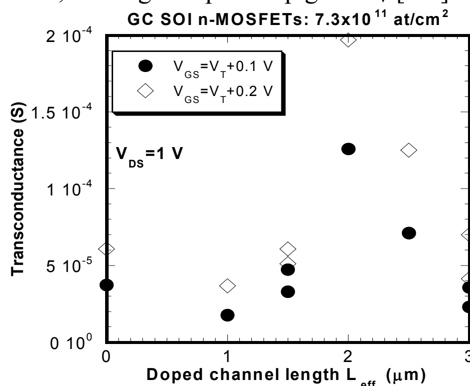

Fig.1: *Transconductance in saturation (V_{DS}=1 V and V_{GS}-V_T=0.1 and 0.2 V) for a GC SOI n-MOSFET array versus doped channel length.*

One aspect that has not been covered so far is the low-frequency (LF) noise of GC SOI MOSFETs. It should be remarked that for asymmetrically implanted Fully Depleted (FD) SOI and bulk MOSFETs a lower 1/f noise has been obtained in conjunction with a higher intrinsic DC gain [4,5]. It is the aim of the present work to present the results of a detailed LF noise study, whereby the focus lies here on the behaviour in the saturation regime (V_{DS}=1 V).

3. Experimental

N-channel transistors have been processed on 3 inch diameter SmartCut SOI substrates. The gate oxide, silicon film and buried oxide thickness are 30, 80 and 400 nm, respectively. GC n-MOSFETS have been fabricated with a total width of 9 μm (3 fingers of 3 μm) and a physical mask length L=3 μm. Various values of ΔL are present in the array, ranging from 0 (channel uniformly doped) to 3 μm (intrinsic doping). A channel implantation dose of $4.4x10^{11}$ and $7.3x10^{11}$ at/cm^2 was employed in different structures, leading to threshold voltages V_T of 0.2 and 0.4 V, respectively. On-wafer noise measurements have been performed in linear operation (drain voltage V_{DS}=0.05 V) and saturation (V_{DS}=1 V) and for a gate voltage overdrive (V_{GS}-V_T) of 0.1 and 0.2 V. Generally, the spectra were of the $1/f^\gamma$ type, with γ close to 1 (Fig. 2), although occasionally, generation-recombination spectra were found as well.

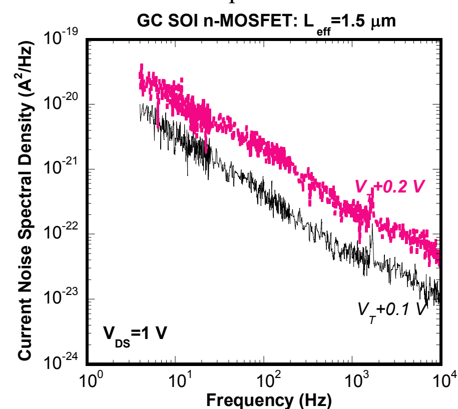

Fig.2: *Low-frequency noise spectra for an L_{eff}=1.5 μm (ΔL=1.5 μm) GC SOI n-MOSFET in saturation. V_{DS}=1 V and V_{GS}=V_T+0.1 V and V_T+0.2 V.*

4. Results and Discussion

As shown in Fig. 3, the S_{VG} at a frequency f=10 Hz in

saturation for most devices of an array increases with the doped channel length L_{eff}=L-ΔL, for a fixed physical gate length L=3 μm, whereby the intrinsic un-doped n-MOSFET (lowest V_T and FD operation) exhibits lower 1/f noise. Maximum noise is found for L_{eff}=2 μm, which according to Fig. 1 also corresponds with maximum g_m for the same operation conditions. This correlation is explicitly shown in Fig. 4, whereby two groups of data points can be identified.

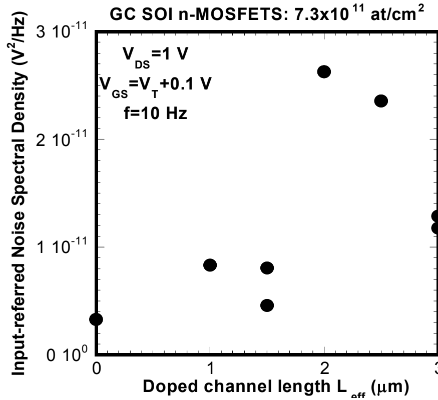

Fig.3: *Input-referred noise spectral density versus doped channel length for a GC SOI n-MOSFET array. The frequency f=10 Hz and V_{DS}=1 V and V_{GS}=V_T+0.1 V.*

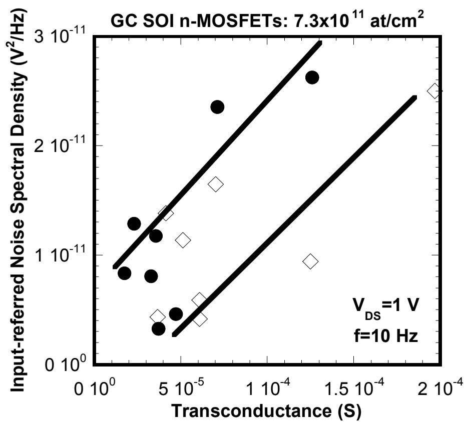

Fig.4: *Correlation between the transconductance and S_{VG} in saturation for a GC SOI n-MOSFET array. V_{DS}=1 V; V_{GS}-V_T=0.1 and 0.2 V; f=10 Hz.*

A possible origin for the higher flicker noise is the presence of the ion implantation (damage) over the channel length L-ΔL near the source. Due to pinch-off in saturation, one expects a different behavior if source and drain are switched. According to Fig. 5, there are indeed some differences, whereby in most cases an increase in the noise is observed in the switched arrangement. This can be explained by the fact that when the V_T adjust is at the drain, the carriers will be more confined to the front surface and, hence, experience a stronger impact of trapping and scattering by front-gate oxide traps. As noise modelling in saturation is not straightforward, the same trend has also been investigated in linear operation for the same set of devices (Fig. 6). Most devices follow a line given by an empirical model S_{VG}~exp(βg_m). Translated to drain current noise (S_I), the differences are even more pronounced as S_I=$g_m^2 S_{VG}$.

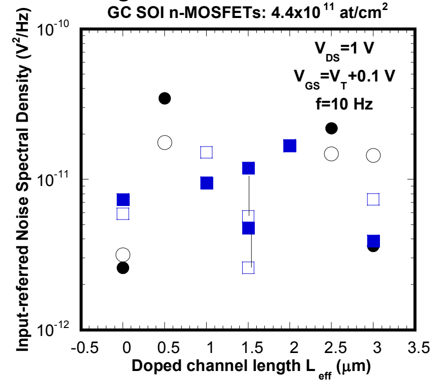

Fig.5: *Asymmetry of S_{VG} versus doped channel length for a GC SOI n-MOSFET array. Open symbols in regular configuration; closed symbols correspond with source and drain interchanged.*

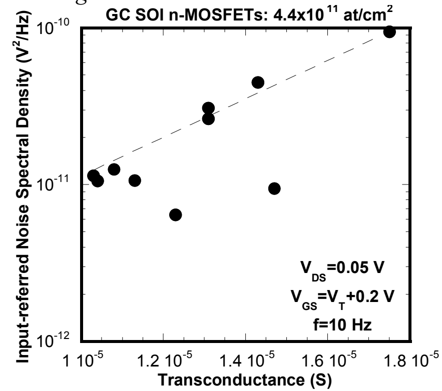

Fig.6: *Correlation between S_{VG} and g_m in linear operation (V_{DS}=0.05 V and f=10 Hz) and at V_{GS}=V_T+0.2 V for a GC SOI n-MOSFET array.*

5. Conclusions

In conclusion, one can state that to achieve high gain and low 1/f noise in GC SOI n-MOSFETs, one has to make an optimal choice of the experimental conditions, i.e., ΔL, implantation dose, etc.

6. Acknowledgment

This work has been partially support by the European Community (Network of Excellence SINANO and EUROSOI project).

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