

**Simulation, Fabrication and
Characterization of Advanced
MOSFETs:
Graded-Channel and Multiple-Gate
Devices in SOI Technology for Analog
and RF Applications**

Chung Tsung Ming

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Jury:

Luc VANDENDORPE (UCL) - President

Jean-Pierre RASKIN (UCL) - Supervisor

Denis FLANDRE (UCL)

Vincent BAYOT (UCL)

Benjamin INIGUEZ (Universitat Rovira i Virgili)

Alastair AMSTRONG (Queens University)

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Abstract

The evolution of semiconductor has been growing since the first transistor was invented in 1900. This industry today is a very important market and worldwide sales in the past few years have been growing rapidly and it is now an industry worth approximately \$400 billion. In the semiconductor industry, the main monitor level is what is known to have originated when Thomas Moore from Intel came out with what is known today as *Moore's rule*. This leads to the industry answer by the creation of the International Roadmap for Semiconductors.

This brought to the industry a whole new dimension. Indeed, this roadmap is the main indication of the direction of the technology and the goals it should achieve in the coming years. It is a roadmap that is edited and reviewed every year to meet the challenges and future predictions. However, in order to meet the requirements set out by the ITRS, technology in all forms related from the beginning till the end of the fabrication and design of the semiconductor device needs to be examined. In the past century, semiconductor transistors have moved rapidly and nodes have been shrinking every two years in response to the prediction by Moore. Materials used for the fabrication of semiconductor devices especially the Metal-Oxide Semiconductor Field Effect transistors have changed from bulk silicon wafers to Silicon-on-Insulator wafers due to the various advantages of using this kind of wafer. Within the Silicon-on-Insulator (SOI) wafers, there have been also various changes moving from thick (a few hundreds of nm to a few microns) to thin SOI wafers (a few tens of nm) leading to MOS transistors in Partially-Depleted to Fully-Depleted modes, respectively. However, in the past few years, technologists have come to a point where they have recognized that this shrinking phenomenon and high demand for the capability of the transistors in the semiconductor industry is coming to a halt if no new

design or technology can be found. Some of the problems that will arise due this shrinking process and demand of the capability of the transistor are such as:

- short-channel effects related to the increase control of the drain on the channel, for instance, Drain Induced Barrier Lowering (DIBL), roll-off of the threshold voltage, decrease of the Early voltage, etc;
- increased of gate leakage current due to the thinner gate oxide;
- increased of the relative importance of parasitic capacitance such as Miller capacitance (direct capacitive coupling between the gate and the drain), overlap and fringing capacitances between gate to source/drain;
- increased device access resistances because of the size reduction of the contacts and the increase complexity of the silicide process;
- fabrication difficulties such as lithography, patterning and many more.

In order to overcome these problems and to ensure that the ITRS roadmap can continue to move beyond, various suggestions have been brought to the table from the various research centers and the semiconductor industries. Among some of the suggestions that have been presented and have shown positive results from initial results are:

- strained silicon which have shown to enhance the carriers mobility which leads to an increase of the driving current;
- Silicon-on-Nothing MOS architecture which have shown reduced short-channel-effects;
- introduction of high-k materials and metal for the gate stack;
- use of asymmetrical channel doping (graded-channel MOSFET) for improving the analog performance, such as the voltage gain;
- moving from single-gate devices to transistors with more than one gate, which are known as multiple-gate devices and many other more ideas.

In this work, among the main ideas that will be used are those based on channel engineering and having devices with more than one gate. These two concepts have been chosen because from their initial results, they have shown very promising applications and viability to satisfy the requirements listed in the ITRS.

In order to analyze and present the viability of these devices from fabrication to end product and to analyze the electrical characteristics, these devices were fabricated, measured and 2- and 3-D numerical simulations were carried out to further expand our understanding of these devices. The development in TCAD numerical simulation software has made it into a very important tool for studying new devices and contributing to a much better understanding of various physical phenomena in these novel devices. Numerical simulations based on commercially available software give a global outlook of the potential of novel devices. All the necessary models and materials are available in these software with more flexibility for the user to change the parameters to adjust it to their needs. We will show in this study that using numerical simulation, we are able to explain the various effects and to show a global outlook of the potential of novel devices.

The graded-channel design was first introduced to minimize inherent bipolar effects in fully-depleted SOI devices. The devices studied here will be the single-gate and double-gate graded-channel SOI MOSFET. The study will be carried out using 2-D numerical simulation, experimental result and analytical modeling. We will show that the double-gate graded-channel SOI MOSFET can achieve high saturation drive current, high values of Early voltage and then an improved DC gain compared to a conventional single-gate SOI MOSFET. The results here have taken into account the different combination of the length and doping of the high and low doped regions. We will also show that the experimental and numerical simulations obtained agree well with the analytical model. Optimization in terms of doping level along the channel of a graded-channel MOSFET will be proposed for applications in future high performance analog circuits.

The fabrication of novel MOS devices raises most of the time a series of important technological issues. In this PhD theses, several original fabrication steps for building graded-channel on planar double-gate MOSFETs are presented. Based on wafer bonding technology, we are

able to fabricate working planar double-gate SOI and SON MOSFET with a promising yield. The various critical points involved in this process have also been addressed. The fabricated devices were electrically characterized and results have shown that they meet the expected double-gate behavior. We have also shown that with this technology, we have managed to also fabricated Silicon-on-Nothing devices which showed good electrical characteristics.

The quasi double-gate analysis performed here is focused on trying to emulate a double-gate device from a single-gate SOI MOSFET. In the study, we will look at the possibility of emulating the electrical characteristics of the double-gate device from a single-gate device. From the performed analysis, we can conclude that it is not possible to emulate the double-gate mode from a single-gate device over all the electrical regimes, especially in the weak inversion regime. We will show that in the strong inversion regime, this is a reliable method to study the double-gate device without having the device itself. This is especially interesting for study of submicron devices since the fabrication of planar double-gate device in this submicron region is not optimized. Analytical analysis was used to show the limitation of using this emulation method.

The ITRS roadmap has identified a special group of novel devices, the multiple-gate architecture as a potential device to meet the demands in the future. Due to the limitation of study done on these devices, we will show in this work a global overview of the potential of these devices. The various devices studied in this work are non-planar (Fin-FET, Triple-gate, Pi-gate) and planar (double-gate) SOI MOSFET compared to the single-gate SOI MOSFET. Based on experiments and 3-D numerical simulations, we show that these various devices have much better electrical performances compared to the single-gate architecture. We show that in the subthreshold regime, the multiple-gate architecture have a very much improved short-channel effects control even when the gate length is reduced to tens of nanometer compared to the single-gate architecture. In the strong inversion and saturation region, we see that the intrinsic gain and the cut-off frequency of the multiple-gate (MuG) architecture have much increased values compare to the single-gate SOI MOSFET especially when the gate length is less than approximately 50 nm. Such improvements is especially clear in the weak inversion

regime thanks to the volume inversion phenomenon taking place in the thin MOSFETs MuG.

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List of Abbreviations

AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
BHF	Buffered Hydrofluoric acid
DG	Double-Gate
ench	Enhancement
EPB	Extended Planar Bulk
FD	Fully-Depleted
GC	Graded-Channel
GCDG	Graded-Channel Double Gate
GCGAA	Graded-Channel Gate-All-Around
GCSG	Graded-Channel Single-Gate
HD	High doped
LD	Low doped
MEMS	Micro Electro-Mechanical Systems
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
NEMS	Nano Electro-Mechanical Systems
OTA	Operational Transconductance Amplifier
RMS	Root Mean Squared
PD	Partially-Depleted
SCE	Short-channel effects
SG	Single-Gate
UD	Uniformly doped
UTB	Ultra-thin body
QDG	Quasi Double-Gate

List of Symbols

$\alpha_{n,p}$	Ionization coefficient of the electron and hole respectively
ϵ_{Fn}	Related to $-q\phi_n$
μ	mobility [$cm^2/V.s$]
$\mu_{ench}, I_{d,sat}$	Mobility Enhancement Factor for $I_{d,sat}$ [μm]
ν_{sat}	Saturated velocity [m/s]
$\text{\AA}$	Angstrom
A_{VO}	DC gain [dB]
$C_{g,total}$	Total capacitance for calculation of CV/I [$F/\mu m$]
$C_{g,ideal}$	Ideal NMOS Device Gate Capacitance [$F/\mu m$]
C_{it}	Interface capacitance [$F/\mu m$]
C_L	Load capacitance [$F/\mu m$]
C_{ox}	Gate oxide capacitance [$F/\mu m$]
C_{Si}	Capacitance of silicon layer [$F/\mu m$]
D_{it}	Surface trap density [$eV^{-1} cm^{-2}$]
e	Electronic charge ($1.6 \times 10^{-19} C$)
F_α	Fermi-Dirac integral of order α
G	Total generation rate of electron-hole pairs [$cm^{-3} sec^{-1}$]
g_{ds}	Output conductance [S]
g_m	Transconductance [S]
$g_{mplateau}$	Transconductance at the plateau level [S]
g_m/I_{ds}	Transconductance to current ratio [mV/dec]
I_{bs}	Back gate current [A]
$I_{d,sat}$	Saturated current [A]
I_{dSub}	Subthreshold current [A]
I_{ds}	Drain current [A]
$J_{n,p}$	Current density of the electron and hole, respectively [A/cm^2]
L	Gate length [nm or μm]

L_g	Physical gate length [nm or μm]
L_{eff}	Effective channel length [nm or μm]
L_{HD}	High-doped length [nm or μm]
L_{LD}	Low-doped length [nm or μm]
n_o	Thermal equilibrium concentration of electrons [cm^{-3}]
n_i^2	Intrinsic concentration of electrons [cm^{-3}]
p_o	Thermal equilibrium concentration of holes [cm^{-3}]
T_L	Lattice temperature [K]
t_{ox}	Gate oxide thickness [nm]
S	Subthreshold slope [mV/dec]
V_{bs}	Back gate voltage [V]
V_{ds}	Drain bias [V]
V_{EA}	Early Voltage [V]
V_{go}	Gate overdrive [V]
V_{gs}	Gate voltage [V]
V_{th}	Threshold voltage [V]
W	Width [nm or μm]

Chapter 1

Introduction

1.1 History

The beginning of electronics dates back to the 1740's when Cunneus and Mechenbrock, two Dutch scientists discovered the *Leyden jar*, the first electrical capacitor [TME]. This was followed by the discovery of static electricity by Benjamin Franklin around the same time. He charged the *Leyden jar* and stored the electric charges. These beginnings were the first steps towards the birth of semiconductor devices.

1.2 Timeline of Semiconductor Devices

In 1874, Braun discovered the asymmetrical nature of electrical conduction between metal contacts and semiconductors such as copper, iron and lead sulphide [Nea97]. These devices were ones of the first metal-semiconductor contacts and used as detectors in radios. In the following years, more discoveries were made such as the point Contact (Pickard) and the publishing of rectifying characteristics of diodes (Pierce). In the years to come, the need for detector diodes and mixers increased with the invention of the radar. This pushed the development of such devices further. An important step in the development was the discovery of purer materials for the fabrication of such devices which improved its performance drastically. Semiconductor physics played an important role in the development of these devices as scientists began

to understand the working mechanism of these devices better.

In 1948, an important discovery was made at the Bell Laboratories by William Shockley, John Bardeen and Walter Brattain [TME]. They invented the first transistor which was tested at Bell's. This transistor was the first point contact device made with polycrystalline germanium. The three inventors were awarded the Nobel Prize in Physics for this invention in 1956. The transistor was further improved when the material used was replaced with a single crystal material. Transistors were later improved with the discovery of the diffusion process to form junctions in the transistors. This process was applied to silicon materials in 1958 and this led to the development of the fabrication of more than one transistor on the silicon slide.

The next important invention was the discovery of integrated circuits (IC). The first IC was demonstrated at Texas Instruments by Jack Kilby [TME] on germanium technology. The first IC on silicon material was demonstrated in 1958 by Robert Noyce of Fairchild Semiconductor where the IC was fabricated on planar technology. In the early years of the IC technology, the main device found on the circuit board was the bipolar transistor.

The modern Metal-Oxide semiconductor field effect transistors (MOSFETs) devices first appeared in the late 1960's when the compatible Metal-Oxide semiconductor (CMOS) technology was growing [Nea97]. These MOSFETs evolved from what was known as Insulated-Gate Field Effect Transistors (IGFET). The first working MOSFET was realized by Kahng and Atalla. Such a device was made possible thanks to the development in the fabrication quality of gate oxides which improved drastically [Col97].

1.3 Development of SOI MOSFET's

The development of the Silicon-on-Insulator (SOI) resulted from the idea of the Silicon-on-Sapphire (SOS) by Manasevit and Simpson in 1963 [Col97]. From the birth of such technology, various other SOI wafers have been fabricated, among them Silicon-on-Zirconia (SOZ), Silicon-on-Spinel, Silicon-on-Nothing (SON) and the most famous of them, the Silicon-on-Oxide usually known as a UNIBOND® wafer

have been seen in the technological scene. A SOI wafer is actually just a piece of pure silicon wafer placed on an insulating device such as glass or silicon dioxide. The transistors are then built onto this thin silicon layer. One of the main advantages of this wafer is the drastic reduction of all the parasitic effects coming from the silicon substrate. Figure 1.1, shows the difference between a (pMOS) transistor in bulk silicon technology and on SOI technology. The main difference is the existence of the buried oxide which acts as an insulator. On the SOI wafer, a substrate is present to act as a support. In the bulk wafer the continuation of the silicon contributes to some of the disadvantages of this technology compared to SOI technology as described in the following.

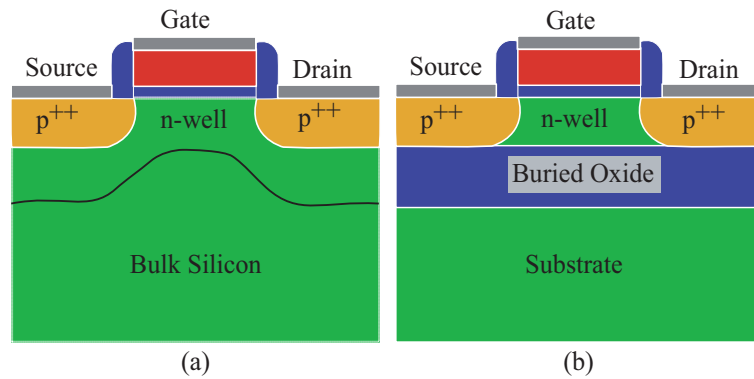


Figure 1.1: Cross-section of (a) Silicon Bulk and (b) SOI wafer.

Some of the advantages of using SOI wafers to develop CMOS devices [Col97] are

- Lower voltage operation with the same performance output compared with bulk technology that must be operated at higher voltage operation, thus leading to lower power consumption (about 40-50% less) compared to the bulk technology;
- Elimination of junction capacitances (parasitic capacitance) and body effect leading to an increase in a jump of about 30% in performance compared to the bulk technology for example in the switching state;

- Reduction in the influence of radiation such as the soft-error rate which affects the data storage in memories;
- Reduction in leakage current, leading to better digital applications with reduced power consumption;
- Higher density of devices fabricated on the same wafer of the same dimension compared to bulk technology because of the use of lateral and vertical isolation. The fabrication process for devices built on SOI wafers are less complex because of the reduced number of masks needed which also helps to reduce the size of the layout;
- Elimination of latch-up effects (this is an effect caused by the switching on of a bipolar mechanism in the device);
- Better temperature operational range;
- Reduced short-channel effects (SCE) when shrinking the device.

However, as usual, there are also some disadvantages in using SOI technology. Some of the major disadvantages of this technology are

- Self-heating in the device due to the presence of the insulator which is not able to conduct heat away from the device fast enough. This can lead to a degradation of the current in the device at high current dissipation;
- High cost of the wafer (which could be eliminated in the coming years as more suppliers are available to provide such SOI wafers). Presently, the cost of the wafer is about 2-3 times the cost of a bulk wafer, but after the completion of the process, the overall increase in cost is only about 20-30%.

In general, it is clear that the advantages of using SOI technology for CMOS devices outweighs the disadvantages. It is believed that in the coming years, it will be even more difficult to continue developing devices on bulk wafers due to the limitation of this technology. In recent years, the boom in major companies shifting to SOI technology is clear. Major companies such as IBM, AMD, Sony, Freescale and many others

are already implementing SOI based transistors in their products. Sony and Microsoft are going for SOI technology in their new entertainment products, the Playstation 3 and the XBox 360 [Bro05].

SOI technology can be classified again into two main groups, the Fully Depleted (FD) and the Partially Depleted (PD) MOSFETs. The main difference between these two groups is related to the thickness and doping of the silicon film on to which they are made. For each of these different devices, different behaviors will be observed due to the changes within the film. Table 1.1 shows the main difference between FD and PD SOI MOSFETs compared to bulk devices.

Physical Parameters	Partially Depleted	Fully Depleted
Mobility	N	+
Transconductance	N	+
Short-Channel Effects	N	+
Source & Drain Capacitance	+	+
Subthreshold slope	N	+
V_{th} sensitivity on t_{Si} change	N	-
Parasitic Bipolar	-	- or N
Total-dose hardness	+	+

Table 1.1: *Rough comparison of FD and PD SOI devices with standard silicon bulk MOSFET on various electrical characteristics. N: neutral, +: better than bulk and -: worst than bulk [Col97]*

1.4 Why Novel Devices based on SOI Technology?

In the previous section, we have already seen the main reasons for the move from bulk to SOI technology. However, even within this SOI technology, devices are already reaching limitations. The main drive to move from classical devices such as the Single-gate (SG) MOSFET's is due to the demanding microelectronics industry and particularly the demand of the industry to shrink devices in the nanometer dimensions. Nowadays, electronic devices are not only getting smaller, but they also need to be multi-functional with requirements that are more demanding. In order to meet such requirements, the core of these electronic devices must be the first to be reinvented and redesigned.

In the last decade, we have seen some remarkable technology at work, from just a few devices on a single silicon wafer, to Very-Large-Scale-Integration (VLSI) and in just the last few years, this has moved to what is known as Ultra-Large-Scale-Integration (ULSI). As this scale expands (or shrinks in other words) this means more and more devices are being fabricated onto the integrated circuit board. This integration level has been forecasted by Gordon E. Moore, the co-founder of Intel in 1965. He observed that since the first IC was produced, the number of transistors on the wafer doubled after every 18 months. He came to predict that this trend would continue in the coming years and that it will only slow down slightly in the future. This prediction can be seen in Figure 1.2 [Moo65]. This law has become a rough guideline to the expansion of the IC board.

Due to the demanding requirements and needs in the field of semiconductor technology, the International Roadmap on Semiconductor (ITRS) [http://www.itrs.net] has been defined. This method of assessment is called 'roadmapping'. This assessment has been compiled by both the private and governmental organizations and research centers to predict and achieve these demanding requirements. According to the ITRS roadmap, these novel devices (known also as non-classical CMOS devices) are an alternative to meet the demanding requirements to shrink these CMOS transistors further down with better functionality and less electrical problems. These novel devices are made using new transistor structural designs. In Table 1.2 [http://www.itrs.net], we see these various novel

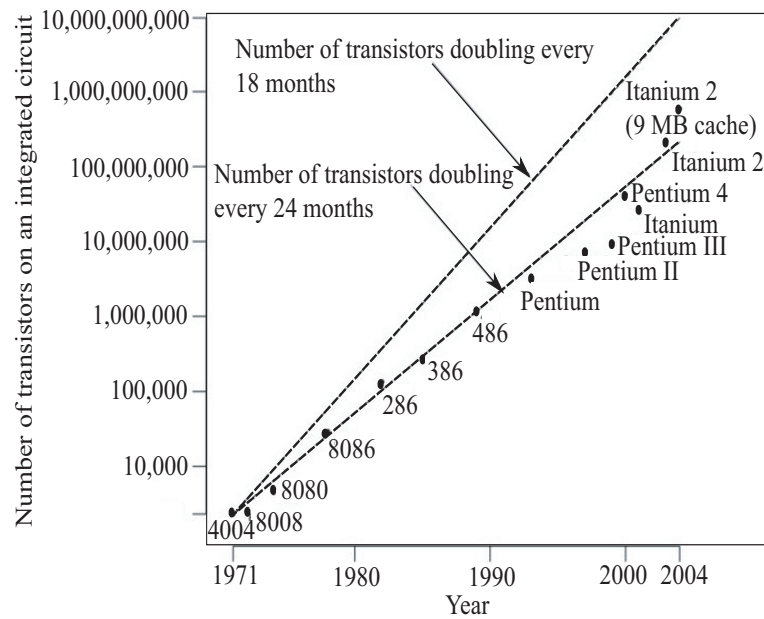


Figure 1.2: Moore's Law over the growth of the amount of transistors on a wafer in the future. [Moo65]

devices that have been proposed so far.

Another device that should be of interest here but not seen in the ITRS Table is the Graded Channel Single-Gate (SG) (or Double-Gate (DG)) MOSFET. This is a MOSFET for which the doping level is not uniform along the channel from the source to the drain regions. Indeed, the channel is highly and lowly doped at the source and drain sides, respectively. Such a device have been proven to show various advantages over the normal doped channels [PMF00c], especially in terms of analog performance.

Table 1.3 shows the ITRS prediction for analog application for the years to come.

In Table 1.4, we see that it is already predicted that DG devices are part of the prediction. This means that DG technology (or even multiple-gate architectures) are not just devices that are deemed possible, but are already considered as devices for the long term when the extended planar bulk (EPB) devices reaches its limit in scalability (predicted around 2014) [hta].

1.5 Multiple-gate devices

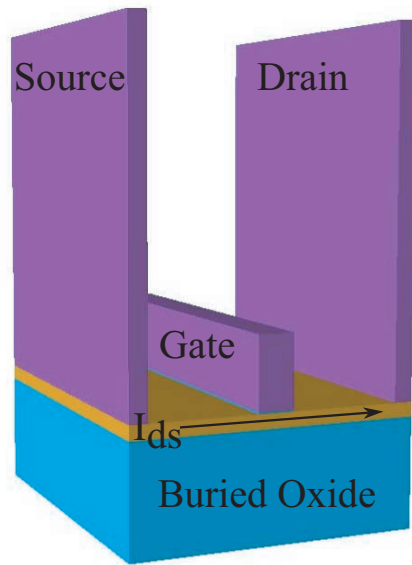
1.5.1 Introduction

Multiple-gate transistors are devices that are included in the group of novel devices. They are devices with more than one gate operating simultaneously on the channel of a MOSFET. The idea of multiple-gate device was first introduced in the early 1980's. Sekigawa [SH84] exhibited his dual-gate device which was named the XMOS due to the resemblance of the structure to the greek letter, Ξ , in 1984. However, the first fabricated device was only made in 1989, where the DELTA (Depleted Lean channel TrAnsistor) devices was introduced by Hisamoto [HKKT89]. In 1987, Balestra proposed the Gate-All-Around structure (GAA) [BCB⁺87]. He simulated and experimented with the GAA device on a SIMOX wafer and showed that there was a big improvement in the subthreshold slope, current drive, transconductance. From these first devices, it was shown that the multiple-gate architecture have some interesting characteristics. One of the most prominent characteristic was the gate control over the electrostatic charges. This increase charge

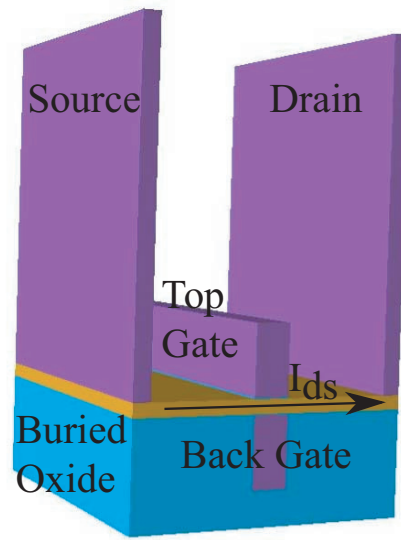
control in the channel translates into improved short channel effects. Another distinct characteristic of multiple-gate devices is the increased current. The various multiple-gate devices that have evolved since then are devices such as the cylindrical MOS, the FinFET (a derivative of the DELTA structure), triple-gate MOS (another derivative of the DELTA structure), the Pi-gate MOS (a derivative of the triple-gate structure), quadruple-gate MOS, the planar double-gate and other derivatives of the the various structures.

Multiple-gate devices can also be grouped into various categories based on the conduction characteristics. The planar double-gate structure exhibits a conduction in the planar horizontal direction. This means that the current flows parallel to the top substrate surface and along the $\langle 100 \rangle$ crystalline plane. The FinFET and other similar architecture also exhibits flow in the horizontal direction but it is different compared to the DG devices because the current flows in the $\langle 110 \rangle$ crystalline plane. However, for the triple-gate and the quadruple-gate devices, the current flow is a combination of flow in both the $\langle 100 \rangle$ and $\langle 110 \rangle$ planes but still in the horizontal direction. Vertical MOS will have a conduction flow in the vertical direction. Among all the multiple-gate devices, one of the only device that can be planarly built is the planar double-gate device.

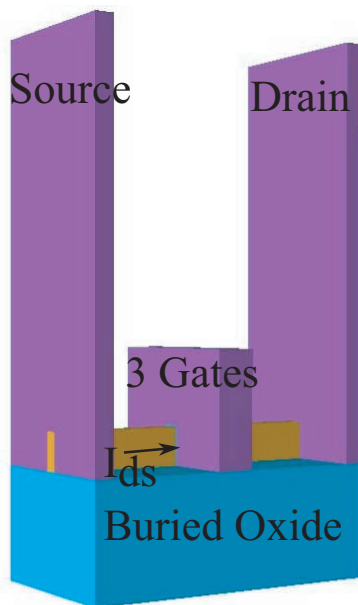
The definition of the various multiple-gate structures can be easily mistaken if not defined properly based on their physical gate dimensions. The double-gate architecture can be characterized into two different type, planar or non-planar. The FinFET can be seen as a non-planar double-gate MOS if the two side gates are more prominent in dimension compared to the the top (third) gate. If all 3 gates of the FinFET becomes more comparable in dimension, this changes the structure into the triple-gate MOS structure. A quadruple-gate or GAA device can also be seen as a 3-dimensional double-gate if the two side gates are so far apart that they become ineffective compared to the two top and bottom gates. Figure 1.3 shows the various main multiple-gate devices that will be of main interest in this current research work. In these figures, the devices shown have extended drain, source and gate contacts which is important here as will be shown in Chapter 6 that they contribute a significant part of the extrinsic capacitances. It is worth nothing here that for simple DC simulations, such extensions can be omitted.



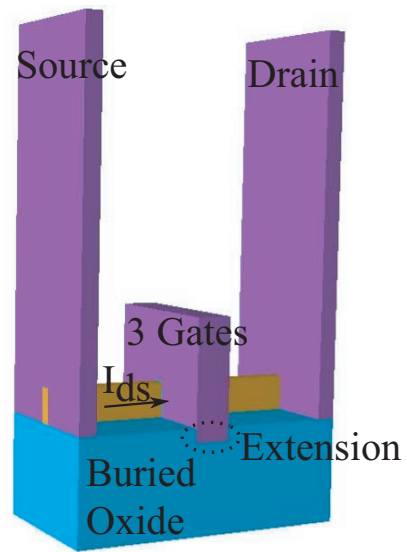
(a)



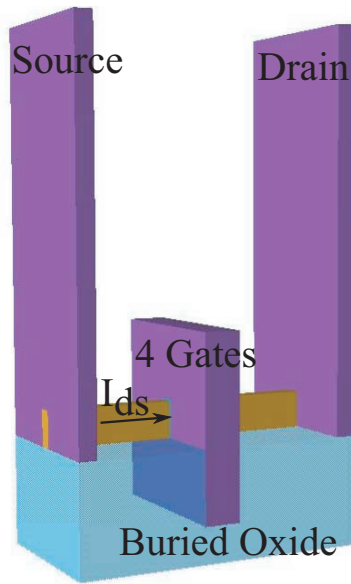
(b)



(c)



(d)



(e)

Figure 1.3: Schematic figures of the various multiple-gate architectures. (a) Single-gate, (b) Planar Double-gate, (c) Triple-gate, (d) Pi-Gate, (a derivative of the triple-gate, but with an extension into the buried oxide) and (e) Quadruple-gate.

1.5.2 Why the move to multiple-gate devices?

The main push to move from the traditional single-gate MOS (bulk or SOI) towards multiple-gate architecture and in general towards novel devices is because of the foreseeable limitation of the single-gate architecture. In the last years, various modifications have been applied to the conventional single-gate architecture to further increase its electrical performance. However, it has been shown that even with the most advanced modifications such as channel engineering, gate engineering and source-drain modification, the electrical characteristics of the single-gate SOI MOSFET cannot be improved further. It has been shown that a single-gate with a channel length of 16 nm and engineered with super halo implantation and a ultra thin gate oxide of 1.2 nm, it remains difficult to reduce the short-channel effects [BDP⁺04]. The short-channel effects for SG devices become difficult to control when the channel length is reduced below the 40 nm limit even with the various halo implantation and adjustment of the spacer length. The only way to improve slightly the SCE of single-gate devices is to form very steep halos or by using adapted channel formation. However, such technology is highly difficult and not cost effective with relation to the result obtained. The increased use of halo also increases the series resistances in the transistor. In order to reduce these series resistances the trade-off would be an increase in the SCE. The mobility in such technologically advanced SG SOI MOSFET is also a question. The velocity overshoot and ballistic transportation in the SG SOI MOSFET is limited to the reduced low longitudinal field mobility. The implantation of the halo causes a huge reduction in the mobility when the device is operating in the high transverse field which again is a set back for further reduction of the SG SOI MOSFET [BDP⁺04].

Due to such constraints in developing/modifying the single-gate architecture, new architectures need to be investigated. That is why one of the most promising architecture to look ahead are the multiple-gate architecture.

1.5.3 Advantages of the multiple-gate structure

The introduction of multiple-gate structures have led to various advantages especially for thin-film devices. As pointed in the last section, among these advantages are the improved electrostatic control of the charges in the channel, an increase in current gain and a reduction in the junction capacitances. The existence of the second gate in the buried oxide increases the control in the channel because it reduces the influence of the penetrating lateral electric field which competes for the available depletion charges. This extra second gate or multiple-gate also increases the number of conducting surfaces which in turn increases the total current flow. An interesting characteristic of multiple-gate devices is what is known as the *volume inversion* phenomenon. This phenomenon is very advantageous to the operation of the device. However, this phenomenon is only limited to certain operation conditions. The mobility in multiple-gate devices are increased compared to the normal single-gate MOS transistor due to the reduced transverse electrical field and during the operation in the volume inversion mode.

1.5.3.1 Subthreshold Regime

One of the main advantages of using multiple-gate devices is the highly improved electrical characteristic in the subthreshold regime. These characteristics are further enhanced when the multiple-gate architecture is combined with the use of a thin film silicon film. As explained in Section 1.3, the silicon film can be divided into either partially depleted (PD) or fully depleted (FD) SOI. The combination of multiple-gate and fully depleted silicon film increases the electrical characteristics of such a transistor. The threshold voltage roll-off of FD SOI multiple-gate devices are very much improved compared to the single-gate MOS transistors. This improvement in the threshold voltage roll-off is related to the reduction of the body effect. The body effect (γ) is already lowered due to the use of an SOI wafer, but with the combination of extra gates, this body effect is decreased further. Equation 1.1 [Col97] shows the correlation between the body effect and the threshold voltage for a thin-body (FD) device.

$$dV_{th} = \gamma \times dV_{G2} \quad (1.1)$$

where V_{G2} is the back gate voltage.

The drain induced barrier lowering (DIBL) characteristic of a FD multiple-gate transistor is very much improved compared to a normal single-gate MOS transistor [Jaj]. DIBL is the effect of the drain on the source barrier. This means that as the channel length is reduced, the threshold voltage will be influenced by the drain voltage leading to a drastic reduction as the drain voltage increases. This change is caused by the increased control of the drain towards the charges in the channel as the gate length is reduced. This improved DIBL characteristic is related to the increased control of the gate on the charges in the channel. It has been shown that the DIBL is much improved in SOI devices compared to bulk devices [VF89]. With the addition of the multiple-gate architecture, the control of the charges in the channel will be increased further thus reducing the influence of the drain on these charges even though the channel length is further reduced.

The subthreshold slope is the inverse of the drain current to gate bias derivative in the subthreshold regime. The behavior of the device in the subthreshold regime is reflected with the subthreshold slope as it shows the change of the subthreshold current to the change in gate voltage. In an ideal transistor, the subthreshold current (drain current) is zero when the gate-to-source bias is less than the threshold voltage. However, such an ideal behavior is never obtained in reality. The ideal value of the subthreshold slope is 60 mV/dec at room temperature. A steep subthreshold slope is desired because as mentioned, it reflects on the subthreshold current with the change in the gate bias. Equation 1.2 shows the relation between the subthreshold current and the gate-source bias [Nea97].

$$I_{dsub} \propto \left[\exp\left(\frac{eV_{gs}}{\frac{S}{\ln(10)}}\right) \right] \cdot \left[1 - \exp\left(\frac{-eV_{ds}}{kT}\right) \right] \quad (1.2)$$

where e is the electronic charge, k the Boltzman's constant and T the temperature.

Another figure of merit to measure or predict the short-channel effect for devices is what is known as the natural length, λ . This characteristic length determines how far the electric field lines will penetrate the device and affect the depletion zone area. λ depends on the gate oxide and silicon thickness. This characteristic length was first introduced by Yan R.-H. as a guide for scaling devices [RHAK92]. It is desirable to have λ as short as possible. The λ concept is used to estimate the silicon film thickness and width of the device in order to reduce as much as possible the short-channel effects in a device as described by J. P. Colinge [Pro03].

1.5.3.2 Increased drain current

One of the main advantage of the multiple-gate architecture is the increased of the total current generated in the device. The current in a multiple-gate SOI MOSFET devices is proportional to the total gate width. The increase of the drain current per channel is related to the increase number of gates. For example, the current drive in a planar double-gate SOI MOSFET is twice that of a single-gate SOI MOSFET if the width and gate length is the same. Thus, the drive current would simply be $I_{dsDG} = 2I_{dsSG}$.

In order to increase the current density (I_{ds} /occupied die area), we will have to expand the design of the devices. Among the factors that can increase the current density would be to modify the architecture of the device, increasing the number of devices on each die, introducing spacing between the fins creating multi-fingered devices, etc. Figure 1.4 shows a schematic cross-section of a multi-fingered triple-gate transistor. The current in multi-fingered devices such as the FinFET and triple-gate devices can be expressed in general as in Equation 1.3 [Pro03]. The FinFET is also known as a vertical double-gate device.

$$I_{ds} = I_{do} \frac{(W_{fin} + 2H_{fin})}{S_{fin}} \quad (1.3)$$

where I_{do} is the current of a unit-width, planar, single-gate device and W_{fin} is the width of each individual fin, H_{fin} is the silicon film thickness and S_{fin} is the fin pitch. From Equation 1.3, for the FinFET, the drain current per unit device is reduced to Equation 1.4.

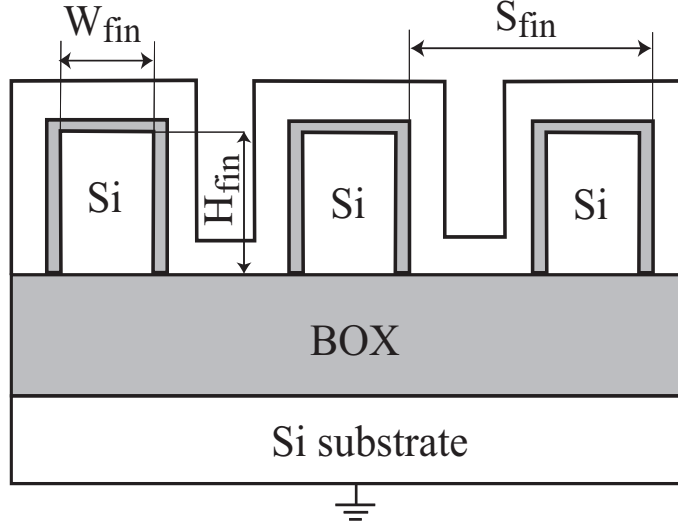


Figure 1.4: Schematic cross-section of a multi-fingered triple-gate transistor.

$$I_D = I_{Do} \frac{2H_{fin}}{S_{fin}} \quad (1.4)$$

because the top gate, would not be effective in generating current, thus it can be omitted.

For a triple-gate device, since the width of the device is equal to the thickness of the silicon film, the current drive for the triple-gate device can be expressed as in equation 1.5.

$$I_D = I_{Do} \frac{3H_{fin}}{S_{fin}} \quad (1.5)$$

One other main advantage of multiple-gate devices compared to the single-gate device is the volume inversion. When the multiple-gate transistor is biased in the weak inversion regime, we can benefit from this volume inversion phenomenon which further increases the drive current. This phenomenon will be discussed later in this chapter.

1.5.3.3 Speed superiority

Results have shown that the double-gate architecture exhibit excellent unloaded-circuit (CV/I) speed superiority compared to the single-gate device (SOI or bulk) [FLMH02]. The increase in the parasitic capacitances of the double-gate architecture compared to the SG device does not seem to deteriorate the overall speed. The operation of the DG architecture in lower supply voltage shows that it is a very promising candidate for future nodes. The increase in the overall speed superiority of the DG device is contributed to the much improved subthreshold slope and the on-state currents of more than a factor of 2. It was also shown that at low gate voltage and saturation region the gate capacitances is relatively low [FLMH02]. This is because in the DG devices, at low V_{gs} , it does not need to support the dynamic charge as compared to the SG device. The dynamic charge is related to the common speed metric (CV/I) which tends to overestimate the intrinsic delay of the DG MOSFET relative to the SG counterpart at low- V_{gs} .

1.5.3.4 Volume inversion

The volume inversion regime is a special phenomenon found only in multiple-gate architectures. A device is said to be operating in volume inversion if there is a strong coupling between two conducting channels [BCB⁺87]. This phenomenon happens only in certain region of operation usually around the threshold voltage for certain film thickness and doping concentration in the channel. When a device operates in volume inversion, the whole silicon film is inverted and there is an increase in the minority carriers leading to an increase in current and a reduction in the surface induced scattering effects. Because of the reduction in the scattering effects, there is an increase in the mobility which leads to an overall increase in the transconductance characteristic of the device. Figure 1.5 shows the electron concentration and corresponding mobility for a double-gate n-MOSFET transistor biased at various gate bias and drain bias at 1.0 V (with an extracted $V_{th} = 0.32$ V). From Figure 1.5 it is clear that when the device is operating in volume inversion, the electron concentration in the center of the film is the same as at the two gate oxide-silicon interfaces. This increase in the electron concentration contributes also to an increase in the mobility in the center of the silicon

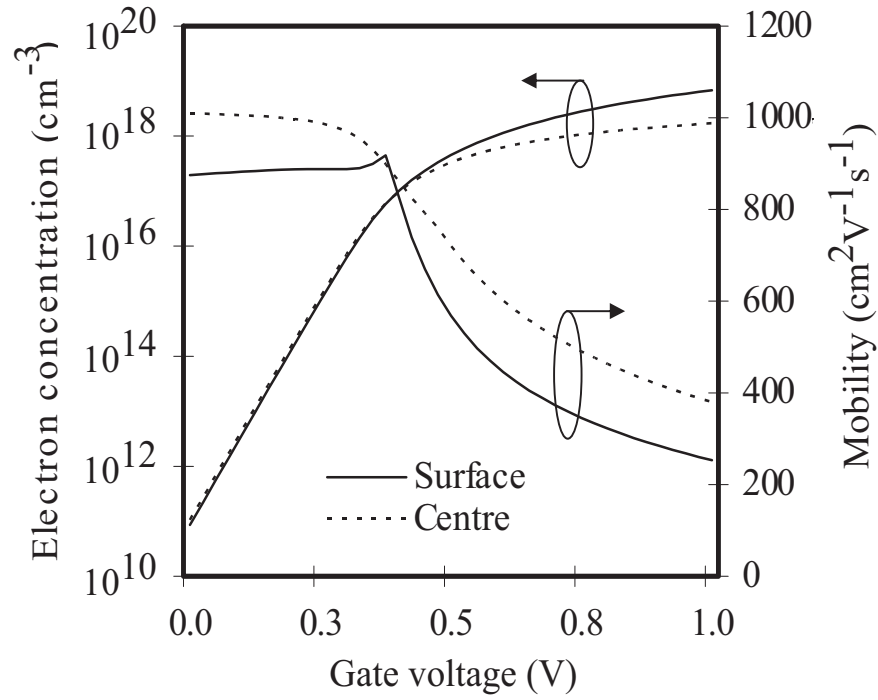


Figure 1.5: Carrier concentration and mobility versus gate bias at $x = L/2$, 1 nm below the surface and at the center of the silicon channel (center) for a DG of $L = 100$ nm, at $V_{ds} = 1.0$ V

film.

However, as mentioned before, in order to achieve this volume inversion mode, certain criteria as mentioned before have to be met. For example if we have a thin silicon film, but the doping of the film is too high, it does not necessary mean that a few hundred millivolts above threshold the volume inversion mode can be achieved. This is because the Fermi level of such a device cannot be overcome due to the high doping. The same can be said if we have an intrinsic doping but the silicon film is thicker than a certain value, the volume inversion mode cannot be assured. Thus, care should be taken before any conclusion of devices working in volume inversion can be made.

It is clear that multiple-gate architecture is one of the most promising novel devices that will be able to move forward with the ITRS demands. The multiple-gate architecture has been proven to show good electrical characteristics even when the gate length is reduced to the nano regime and thus making it very suitable for deep submicron devices. They have been shown to reduce the short-channel effect even further compared to the technologically advanced single-gate devices. We have also seen that even for the technologically advanced single-gate device, there is a limitation in pushing it further into the future node. One of the main reason for the good electrical characteristics of the multiple-gate architecture is due to the excellent control of the charges in the channel.

1.6 Present Work

As explained previously, one of the way to move forward to keep to Moore's law in maintaining the current trend of scaling, we are left with very limited choices to the parameters that can be changed or modified to keep the transistors of the future. In order to keep up with this ITRS roadmap, attention has now been focused onto the so-called new generation devices with new architectural design to keep the technology moving at optimal performance level. The need to reduce cost in such a volatile industry is also pushing the limits of the performance of these transistors.

The main purpose of this research work is to compare and study in details the various novel transistors built on SOI MOSFET technology

and its foreseen position with reference to the ITRS roadmap. For most of the novel devices analyzed here, its application will be important for technological nodes down to 45 nm and beyond. As we have seen in Table 1.2, some of the devices that would be playing an important role in the progress towards smaller nodes are multiple-gate devices. From initial results obtained from these multiple-gate devices, it has been shown that they have good subthreshold characteristics [Col97] [Pro03] [BCB⁺87]. One of the main objective of this research is to show that in analog and digital applications, these multiple-gate devices are also able to meet the requirements set out by the ITRS as seen in Tables 1.3 and 1.4 to satisfy the future low power applications. Another interesting structure that will be studied is the graded-channel SOI MOSFET. In order to achieve this, methods that will be used are based on numerical simulations and also characterization of various available devices. In order to further explore the suitability and compatability of these devices, the fabrication process of these devices will also be studied to a certain extend. We will also look into the possibility of utilizing current available advanced single-gate SOI MOSFETs to emulate the operation of a multiple-gate SOI MOSFET.

Chapter 2 gives an in-depth introduction into the various models used in numerical simulation. As explained earlier, multiple-gate architectures and the devices with channel engineering are seen to be devices with the most promising future to fulfill the requirements of the ITRS roadmap. However, in order to examine the potential of such devices, the current situation limits such characterization to using the available tools. Due to the limitation of fabrication technology, cost and time, the best available tool for characterization of advanced devices is by using simulation tools. Numerical simulation involves the use of the various models available which will be described in this chapter. In order to effectively simulate the devices, it is advantageous to understand the different events that happens in the device for the different dimensions. In order to present simulated results as trustable results, the simulations must be validated based on experimental results. The justification of the use of the various models must also be made. These two basic requirements will be carried out to validate the results shown in this work.

In **Chapter 3**, the Graded-Channel Gate-All-Around (GCGAA) and Graded-Channel Single-Gate (GCSG) MOSFETS will be analyzed. The

GCGAA is a MOSFET for which the doping level is not uniform along the channel from the source to the drain regions. The advantages of these devices over the traditional SG SOI MOSFET will be shown. These devices are compared in the static regime and the important parameters will be shown. In this work, we will show that these graded-channel devices are very promising devices to be used for high analog performance devices. We will also show that for the various graded channel ratios (the length of the doped section to the length of the channel) studied, there is a maximum ratio that will be beneficial before such channel engineering becomes ineffective. In this part of the study, the important region of analysis will be in the middle inversion to the strong inversion and from linear regime to the saturation regime. The results from experimental devices will be compared to the simulated results.

The Gate-All-Around (GCGAA) Graded-Channel MOSFET introduced in **Chapter 3**, is an interesting device that will prove to be one of the most promising device in the coming years. However, the fabrication of such a GCGAA or planar double-gate device using the traditional method of silicon island formation and etching has limitations. A literature study of the various available techniques currently will be presented to show the advantages and disadvantages of these methods. In order to overcome some of the current fabrication limits, a new method of fabrication which is compatible to the current CMOS fabrication process will be introduced in **Chapter 4**. This method will be known as the wafer bonding method over prepatterned cavities. In this chapter, we will see that this new simple method is viable not only for small scale fabrication but can easily be adapted to the current facilities available in the semiconductor industries. Electrical characterization will be presented to show the viability of this wafer bonding method not only for the fabrication of planar double-gate devices, also for various other devices such as the Silicon-on-Nothing transistor.

Chapter 5 looks into the emulation of Double-Gate (DG) SOI MOSFET devices, which is known as a Quasi Double-Gate (QDG). Here, we look into the possibility of emulating a DG device from the measurement of SG SOI MOSFET. In the current technology environment, it is currently difficult to built all the desired multiple-gate devices such as planar double-gate devices with advanced halo, very short gate-length or ultra-thin body. Thus, this is an important concept because with this

possibility, it will be an advantage for future analysis or characterization of advanced DG devices when such devices cannot be built due to the current technology available. The emulation of such a DG from a SG transistor can also be used for simple verification of analytical or numerical simulation of DG devices. The limitation of this technique will also be presented.

The electrical properties of multiple-gate devices will be studied in details in **Chapter 6**. Multiple-gate devices have been identified as devices that have the most promising properties to bring the ITRS roadmap further into the future as seen in Table 1.2. Here, the devices will be studied in both the static and dynamic regimes. In the study of the analog characteristics of the device, the transconductance-to-current ratio (g_m/I_{ds}) versus normalized drain current ($I_{ds}/(W/L)$) will be used. This is a good representation because it has two major advantages when comparing various devices: threshold voltage independent and to the first order, length independent for devices with no dominant short channel effects in weak inversion or velocity saturation in strong inversion [KNV⁺03]. The second main analog figure of merit will be the Early voltage. This eliminates the dependent conductance (g_d) of the devices on the drain current. In the dynamic region, the intrinsic and extrinsic capacitances as well as the cut-off frequency (f_T) for multiple-gate will be analyzed and compared with single-gate. The f_T is an interesting parameter for high-speed digital applications as it takes into consideration both the intrinsic and extrinsic elements. The intrinsic elements are dependent on the bias conditions and the size of the active zone while the extrinsic elements are supposed to be independent of the bias conditions [KNV⁺03]. The advantages of each different architecture will be highlighted. Here, the main method of study will be with a numerical simulator available commercially, SILVACO®. One of the main objective here is not to quantitatively present the results, but to show the trends for each of these devices with the evolution of the technological nodes in the ITRS roadmap. Simulation results for FinFETs will be compared with static and dynamic measurements in order to confirm the validity of the simulated trends for the multiple-gate devices. In this chapter, one of the analysis carried out is on the various factors that will potentially influence the parasitic capacitances such as the influence of the W/L ratios and the justification of using an gate-extension into the

buried oxide compared to a structure without any extension. We will show that these multiple-gate devices have the potential to be scaled even further than what is expected as listed in the ITRS requirements for each technological nodes.

Device	Ultra-thin body SOI	Band-engineered Transistor	Vertical Transistor	FinFET	Double-Gate Transistor
Concept	Fully depleted SOI	SiGe or Strained Si channel, bulk Si or SOI	Double-gate or surround-gate Structure	Double-gate or surround-gate Structure	Double-gate or surround-gate Structure
Application	Higher performance, higher transistor density, Lower power dissipation	Higher performance, higher transistor density, Lower power dissipation	Higher performance, higher transistor density, Lower power dissipation	Higher performance, higher transistor density, Lower power dissipation	Higher performance, higher transistor density, Lower power dissipation
Advantage	Improved subthreshold slope, V_{th} controllability	Higher drive current, Compatible with BULK and SOI CMOS	Higher Drive current, Lithography independent L_g	Higher drive current, Improved S, Improved SCE, Stacked NAND	Higher current drive, Improved S, Improved SCE, Stacked NAND
Scaling Issues	Si film thickness Gate Stacked Worse SCE than bulk CMOS	High mobility film thickness in case of SOI, gate stack, Integration	Si film thickness, Gate stack, Integrability, Process complexity, Accurate TCAD including QM effect	Si film thickness, Gate stack, Process complexity, Accurate TCAD incld QM effect	Gate alignment, Si film thickness, Gate stack, Process complexity, Accurate TCAD incld QM effect
Device challenges	Device characterization, Compact model and parameter extraction	Device characterization	Device characterization, PD versus FD, Compact model and parameter extraction, Applicability to mixed signal applications	Device characterization, PD versus FD, Compact model and parameter extraction, Applicability to mixed signal applications	Device characterization, PD versus FD, Compact model and parameter extraction, Applicability to mixed signal applications
Maturity	Development	Development	Development	Development	Development

Table 1.2: Overview of the novel devices that are being researched into and developed by the various private and governmental research centers. [http]

Year	$L_{min}/node$ (nm)	t_{ox} (nm)	g_m/g_{ds} at $5.L_{min}$	Parasitic cap. (fF/ μm)	f_T (GHz)
2005	45/80	2.1	100	0.24	140
2006	37/70	1.9	100	0.24	170
2007	32/65	1.6	100	0.24	200
2009	25/50	1.4	100	0.24	280
2012	18/35	1.2	100	0.24	400
2015	12/25	1.0	100	0.24	700

Table 1.3: Predicted Values from the ITRS for the analog figures of merits [htta]

Year	Device	μ_{ench} at $I_{d,sat}$	$C_{g,ideal}$ (fF/ μm)	$C_{g,total}$ (fF/ μm)	EOT (Å)	L_g (nm)
2005	EPB	1.11	0.821	0.106	21	65
	DG	-	-	-	-	65
2006	EPB	1.11	0.696	0.936	20	53
	DG	-	-	-	-	53
2007	EPB	1.10	0.614	0.854	19	45
	DG	-	-	-	-	45
2009	EPB	1.11	0.606	0.846	15	32
	DG	-	-	-	-	32
2012	EPB	1.16	0.470	0.640	13	22
	DG	1.00	0.446	0.686	-	22
2015	EPB	-	-	-	-	16
	DG	1.06	0.368	0.598	11	16

Table 1.4: Predicted Values from the ITRS for application in low standby power technology [htta] EPB: Extended Planar Bulk and DG: Double-Gate. - in the table delineate one or two time periods: either before initial production roadmap has started for the technology or beyond when EPB have reached the limits of practical scaling. Further explanation can be found at the ITRS website [htta].

Chapter 2

Numerical simulation tools

2.1 Numerical simulations

Semiconductor numerical simulation can be grouped into what is known as TCAD (Technology Computer Aided Design). TCAD has been growing since the development of first process and device simulator at Stanford in the late 1970s and early 1980s. These first tools allowed users to understand and develop various new processing ideas in the semiconductor industry. Numerical simulation is a very powerful tool in the semiconductor industry especially for predicting various properties of novel devices from fabrication processes to electrical characterization. Such simulations are possible because of the versatility of numerical simulations which has the ability to include various materials, simulation in 1-D, 2-D and 3-D structures, implementation of various fabrication processes for the various steps involved, wide-band frequency simulations, different physical models for the various effects that needs to be considered and many other properties.

In the last few years, the use of numerical simulation has become ever more important in the semiconductor industry because it is a tool that has proven to be able to provide good accurate prediction on future devices. This is important as we move towards the fulfillment of the ITRS predictions which require drastic changes in todays available technology. Another factor that has pushed the use of numerical simulation as a major tool today is the cost factor. Due to the rise in costs today invested in researching new methods and materials to fulfill the ITRS

demands, numerical simulation is now a cheap but efficient method to analyze and predict the characteristics of future devices before fabricating the real device or even before the technology becomes available.

2.2 Monte-Carlo Simulation

The Monte-Carlo simulation is the basis for the numerical simulator. The Monte Carlo algorithm uses the corresponding mathematical equations to solve the problem and can be easily integrated into the various TCAD softwares for electrical characterization predictions. The Monte-Carlo simulator solves the Boltzmann Transport Equation (BTE) to predict the electron flow based on the input provided. In the Monte-Carlo simulator, the carriers are treated as point-like semiclassical particles which are further broken down into smaller particles [IBMc]. The Monte-Carlo algorithm uses quantum mechanics to compute the scattering probability and the probability distribution of the final states.

One of the main advantage of the Monte-Carlo method is the ability of it to provide a solution of the BTE without making additional approximations on the basic physics.

2.3 Challenges and needs

Numerical simulation like any other software face many challenges and requirements in order to meet the ever changing face in the semiconductor industry. Some of the main challenges faced in developing these TCAD tools further are [Dua99]:

- advantages gained based on the investment;
- providing better extrapolation of results aiding the educated guess of the engineer;
- TCAD must be able to meet the various demands and to give better predictability compared to the various tools available now including those of the experience of an engineer;
- moving from investigating the real devices to looking at devices virtually and trusting the results from a TCAD simulator;

- to have accurate models and codes to adapt to the changing technologies;
- to move fast enough to this fast changing technology in the semiconductor industry.

In order to meet these challenges and demands, an advisory board known as the SEMATECH process integration advisory board has been set up to provide the necessary recommendations for TCADs to adapt to the different demands of the users [Dua99] since 1984. Among the recommendations are:

- the need to have more users demanding for TCAD rather than the developers pushing users to use the tool;
- to have better prediction of future technology and demands, thus a better telescope and not a better microscope;
- less attention for the development of coefficients in models due to the already sufficient development in the models for the various devices including for advanced devices;
- the use of TCAD should also be applied to building circuits and not limited to devices;
- combine tuning/calibration efforts to improve on balancing the need to develop models and to obtain faster and more accurate results;
- to provide a direction for the code developer so that they are meeting the requirements of the technology;
- share solution methods to common problems;
- and most importantly to exhibit the importance of using TCAD as a major tool in predictive technology.

These various challenges and needs in developing TCAD have succeeded in some way and currently we have now a large choice of options within the various available TCADs available in the market.

2.4 Different numerical simulation tools

The development in the last years in the area of TCAD for the semiconductor industries has been very active. Currently, users have a wide variety to choose from. Normally, such choices are very much dependent on the applications and desire of each individual organization of institute. The cost of the product also plays an important role in the choice of the users which in this time and age is one of the more important factor since most of the available softwares have more or less the same capability. Some of the most frequently used tools today in the semiconductor industry by the various research centers and industrial sectors are:

1. Damocles;
2. MicroTec;
3. FEMLAB currently known as Comsol Multiphysics;
4. SimWindows;
5. Crosslight Software;
6. ISE TCAD currently known as Synopsys;
7. Silvaco.

1) Damocles [IBMa]: This is a numerical software that uses a self-consistent Poisson/Monte Carlo computer program for simulation of electronic transport in semiconductor devices. This software has been developed by IBM and Damocles stands for Device Analysis Using Monte Carlo and Poisson solver. The main purpose for the development of this software was because of the advancement in the semiconductor devices environment. The shrinking of the device into the nano regime changes as their dimensions begin to approach the wavelength of the electron. Electrons must then be fully treated as full-fledged quantum mechanical particles. This software aims to provide the necessary models and physical basis to accurately model semiconductor devices in this regime. This software uses the various different models and the various

phenomena associated with nanodevices. The input for these various phenomena is obtained from the various universities around the world.

2) MicroTec [IBMb]: This numerical software is rather limited to 2-D simulation. This is a very simple program that was built mainly for use in the Windows environment. This limited the use of it based on the capability of the processor of the computer and the memory. However, this is a very simple software for use in analysis of devices processing and simple electrical characterization. However, in the current environment of research, this software is not very suitable as it cannot be adapted to the analysis of nanodevices.

3) Comsol Multiphysics [Com]: This is a modeling package with various modeling templates installed mostly based on using the partial differential equations as the solver. This numerical software is capable of simulation from 1-D devices to 3-D devices. In simulation of MOSFET devices, this tool is still rather limited as concentration are given to the magnetostatic, electrostatic and bipolar operational devices. The models available for MOSFET devices especially for novel device are still limited.

4) SimWindows [oC]: This software is a very simple software for simulation of semiconductor devices. It simulates only in the 1-D environment but it is a simple software for simulation. However, this software is very outdated and is not compatible especially in today's environment of advanced MOSFET devices.

5) Crosslight software [Cro]: This software is a software that works in the computer aided design (CAD) environment. It is capable of simulating advanced semiconductor devices including advanced MOSFET devices such as multiple-gate devices, strained silicon MOS, high-k gate MOSFETs and the other novel MOSFET devices. It is also capable of simulating the various fabrication process steps of the novel devices such as the use of high-k materials or the source/drain engineering technology. The fabrication process is not limited to 2-D but it can also be applied to 3-D simulation. This 3-D simulation environment is also applicable in the analysis of the devices physics during the various electrical characterization of the devices. The codes used for this software are based on the SUPREM IV codes developed first at Stanford University which has proven to be effective and accurate in predicting the trend/behavior of the electrical characteristics of the devices. The

main application for use in MOSFET analysis is the APSYS (Advanced Physical Models of Semiconductor Devices) package. In this package, various advanced and novel MOSFET devices can be simulated in both the 2-D and 3-D environments. This package contains all the necessary models to take into account all the effects that will happen or predicted in nanodevices. This software tool is very powerful as it can simulate from the static to dynamic regions of operation of a device.

6) ISE TCAD [Syn]: This numerical software is known currently as Synopsys. It is a product that is very similar to the Crosslight APSYS software. It is capable of most of the features seen in the APSYS package. The software is capable of accurate and fast analysis for deeply scaled devices. In the Synopsys software, the packages available for simulation of device electrical characterization are the Sentaurus package and the Taurus-Medici package. Both packages have the necessary models to simulate the different kinds of devices based on the application of the user. The main principle behind this software is the use of finite volume method. This finite volume method is also known as the box integration method introduced by Macneal [Mac52]. This method when combined with the Scharfetter-Gummel scheme produces an integrated domain which is partitioned into well defined boxes with positive cross-sections. This method is normally used in TCAD numerical simulation software especially for semiconductor devices simulation [Fle00].

7) Silvaco [Sof00] [Sil]: The packages available from Silvaco for numerical simulation are similar to those seen in the Crosslight software and the Synopsys software. It is also a software where the Monte Carlo code is the basis of the software. There are various packages available in this software for device fabrication and device characterization. The advantage of the this software compared to the Crosslight software and the Synopsys software is that it is a rather simple software for users. The various models needed for application in deeply scaled MOSFET devices are also available with this software. The main package used for device electrical analysis is the ATLAS package. In this package, simulations can be carried out for various conditions and various applications. Electrical simulations in both the static and dynamic regions are available.

2.5 Numerical simulation: ATLAS Package

In this work, the main method used will be numerical simulation although in some sections analytical analysis will also be carried out, used more as a confirmation tool rather than the main tool. In this work, the numerical simulator used is a commercially available numerical simulator from Silvaco© with the Atlas package which is specifically used for electrical characterization in both the DC and AC regimes. In order to obtain accurate results from numerical simulations, it is important that the physical models used or specified in the simulator be as accurate as possible in order to take into account the effects that occur in the working devices. Some of the physical models available are used for the recombination and generation of the carriers, the mobility behavior of the carriers, the use of the Fermi-Dirac and Boltzman statistics, the effect in the bandgap such as bandgap narrowing, tunneling and other band effects, the effect of the electric field, carrier energy, the lattice temperature-dependent impact ionization, and the effect of the interface charges.

The basic equation that is the main backbone of the movement of the carriers is the Poisson equation which relates the electrostatic potential to the space charge density. Equation 2.1 shows the Poisson equation for a 3-dimensional body.

$$\frac{d^2\phi(x, y, z)}{dx^2} + \frac{d^2\phi(x, y, z)}{dy^2} + \frac{d^2\phi(x, y, z)}{dz^2} = -\frac{\rho(x, y, z)}{\epsilon_{Si}} \quad (2.1)$$

where ϕ is the electrostatic potential, ρ the charge density per unit volume at point x , y and z and ϵ is the local permittivity. From this Poisson equation, the electric field can be obtained from the gradient of the potential as given in equation 2.2.

$$E = -\nabla \phi(x, y, z) \quad (2.2)$$

2.5.1 Theory of Carrier Statistics

There are two main theories related to the carriers statistics, the Fermi-Dirac and the Boltzman Statistics. In the Fermi-Dirac statistics, the

electrons in thermal equilibrium at a lattice temperature, T_L follow this rule. It states that the probability, $f(\epsilon)$ that an available electron state with energy, ϵ is occupied by an electron is

$$f(\epsilon) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT_L}\right)} \quad (2.3)$$

where E_F is the spatially independent reference energy known as the Fermi level and k is the Boltzmann's constant [Sof00].

However, with the limit of $E - E_F \gg kT_L$, equation 2.3 reduces to

$$f(\epsilon) = \frac{E_F - E}{kT_L} \quad (2.4)$$

Equation 2.4 is known as the Boltzmann statistics [Sof00]. This is mainly used when the devices are not heavily doped or when T_L is not very low, thus calculations can be simplified. However, if the device is highly doped, the Fermi-Dirac statistics needs to be used. From these two statistics, various important functions can be derivated such as the effective density of state, the intrinsic carrier concentration, bandgap energy, etc.

2.5.2 Transport model

In the simulator, the transport model is based on the Boltzman Transport Equation [Sof00]. Equation 2.5 gives the general Boltzmann Transport Equation.

$$\begin{aligned} \frac{\partial f}{\partial t} + \nu \cdot \nabla_r f + \frac{eE}{\hbar} \cdot \nabla_k f = \sum_{k'} [S(k', k) f(r, k', t) [1 - f(r, k, t)] \\ - [S(k, k') f(r, k, t) [1 - f(r, k', t)]] \end{aligned} \quad (2.5)$$

where r is the position, k is the momentum, $f(k, t)$ is the distribution function i.e. the Fermi-Dirac in equilibrium, ν is the group velocity, E is the

electric field, $S(k, k')$ is the transition probability between the momentum states k and k' and $[1-f(k', t)]$ is the probability of non-occupation for a momentum state k' . The summation as given in the right hand term is the collision term which accounts for all the scattering events. The terms on the left hand side indicate, respectively, the dependence of the distribution function on time, space (related to the velocity) and momentum (related to the electric field) [httb]. From this main Boltzmann equation, different assumptions can be made which result in 3 main transport models, i.e. the drift-diffusion mode, the energy-balance model and the hydrodynamic model. For each model, there is a limitation to it.

2.5.2.1 Drift-diffusion model

The drift-diffusion model is the simplest model of the three. This model is easily derived from the Boltzmann Transport Equation with the relaxation time approximation. Equation 2.6 shows the drift-diffusion current equation valid for both carriers.

$$J_n = qn(x)\mu_n E(x) + qD_n \frac{dn}{dx} \quad J_p = qp(x)\mu_p E(x) - qD_p \frac{dp}{dx} \quad (2.6)$$

where q is the absolute value of the electronic charge. These equations are valid for very small changes of the equilibrium state (low fields) and that the Einstein equation holds. It can be easily extended to include the field-dependent mobility and diffusion coefficient [httb]. The setback of this drift-diffusion model is the limitation when devices are shrunk in size. The approximation obtained for devices with small dimensions becomes less accurate. This is because the model does not take into consideration the non-local effects such as nonstationary carrier transport and underestimates the on-currents of short-gate MOSFETs. Channel lengths below $0.1 \mu\text{m}$, velocity overshoots dominates the whole of the channel length [hh04]. In this work, for devices with channel lengths in the micrometer range, the drift-diffusion model will be used for the numerical simulations.

2.5.2.2 Energy Balance model

Thus, in order to perform more accurate analysis when analyzing deep submicron devices it is appropriate to use either the energy-balance model or the hydrodynamic model. The chosen model here is the energy balance model. Figure 2.6 shows the difference in using the drift diffusion model compared to the energy balance model for a SOI nMOSFET with $t_{Si} = 30$ nm and $L = 0.30$ μm at $V_{gs} = 0.50$ V. From Figure 2.6,

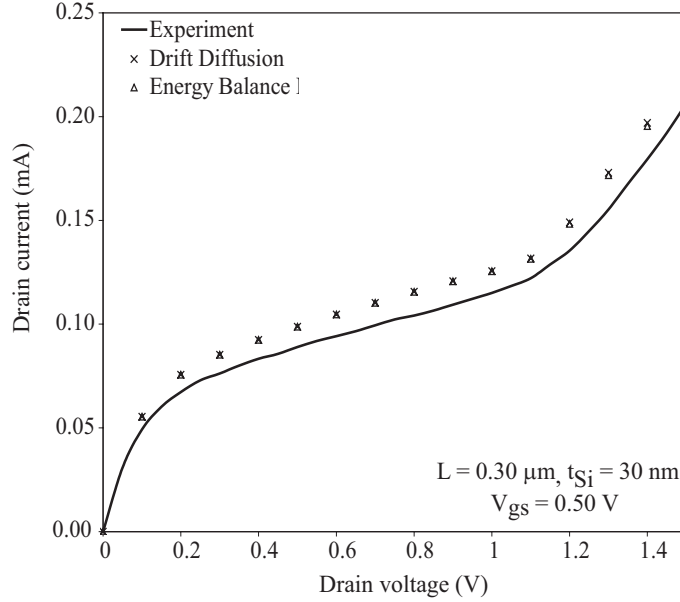


Figure 2.1: I_{ds} - V_{ds} curve for a nMOSFET SOI device with $t_{Si} = 30$ nm and $L = 0.30$ μm showing the simulation differences using the drift diffusion model and the energy balance model at $V_{gs} = 0.50$ V.

we see that there is an insignificant difference in using either models. As opposed to the rule of thumb stated earlier, we see that for devices with gate length close to 0.5 microns as in the case here, the drift diffusion seems to be still valid. However, we have decided that in this work, we will still follow this rule of thumb and use the energy balance model for $L < 0.5$ micron as the main purpose of this work is to show the result qualitative between the different devices and not quantitative.

It has been shown that even for $L < 0.5$ micron, this energy balance model is still valid as shown in the work of Granzner [GPS⁺03]. In this work, we do acknowledge that the energy balance model with the default settings provided by Silvaco© has not been optimized which has been shown by various investigations such as from Granzner [GPS⁺03]. However, this non-optimization is also seen in the drift diffusion model. Since this energy balance model has been designed to be theoretically for short channel devices, we will thus in this work use this energy balance model when necessary since as seen in Figure 2.1, the difference is nearly insignificant between the use of the drift diffusion model and the energy balance model.

2.5.3 Recombination and generation of carriers

The recombination and generation of carriers is a process that occurs due to the need for the semiconductor material to return to a equilibrium state after being agitated from this state. In a steady state balance equilibrium, the concentrations in a homogeneous doped semiconductor material would be given as in equation 2.7.

$$n_o = p_o = n_i^2 \quad (2.7)$$

n_o and p_o represents the electrons and holes concentration in equilibrium when in the quasi-neutral zones. The recombination and generation processes can be classified into 6 main categories [Sof00],

- phonon transitions;
- photon transitions;
- Auger transitions;
- surface recombination;
- impact ionization;
- tunneling;

In this work, the main model that will be used to approximate the carriers recombination-generation behavior will be the Shockley-Read-Hall (SRH) Recombination model [Sof00]. This model is the best for the needs of this work because it takes into account the leakage currents that exist due to the thermal generation by the minority carriers. This is important here because of the different SOI structures that will be simulated and this combined with the use of thinner dielectric layers can increase the leakage current in the devices. Another advantage of using this model is that if the need arises to modify the electron or hole lifetime, this can easily be done by adjusting the parameters specified in this model. This model is also advantageous because it takes into account the effect of the silicon-oxide interface. This model is also normally used because of its flexibility to be combined with other models where needed.

In situations where high current densities are expected, another model that should be added is the Auger model. This is a direct recombination model which involves three particles transition that are either emitted or captured. However, until now, there are no clear physical explanation of this phenomenon in a semiconductor material [Sof00].

2.5.4 Impact Ionization

Impact ionization is an important phenomenon especially in devices where high biases are involved. This is because there will be a high electric field presence which will accelerate the free carriers up to the point where they are able to collide with the atoms of the crystal to again generate more free carriers. Normally in order for the free carriers to obtain energy of this level, two main criteria need to be met, i) the electric field must be sufficiently high and ii) the distance between the collisions of the free carriers are sufficient to allow the carriers to achieve the velocity needed [Sof00]. Such collision, if it happens frequently enough, will lead to what is known as an avalanche breakdown and this can cause a sudden increase in the current of the device which can damage the device. This generation process is expressed by equation 2.8.

$$G = \alpha_n J_n + \alpha_p J_p \quad (2.8)$$

with G representing the total generation rate of the electron-hole pairs, $\alpha_{n,p}$ the ionization coefficients for the electrons and holes and $J_{n,p}$ the respective current densities. The ionization coefficients represent the number of electron-hole pairs generated by a carrier per unit distance traveled, though an exact value is always difficult to obtain due to the various factors affecting it.

The impact ionization models can be again divided into two different categories, local and non-local. The local categories assumes that the ionization at a certain point happens only due to the effect of the electric field, while the non-local model is a bit more complex as it also takes into account the energy the carrier gains.

In this work, the impact ionization model that will be used will be a combination of the local and non-local models, the Selberherr and Toyabe Impact Ionization model. The Selberherr model takes into consideration the local model while the Toyabe model considers the non-local events which are especially important when the energy balance model is used for deep submicron device simulations. This model was chosen because it is sufficient to cover all the needed and expected situations in our devices. It also covers all the temperature range where the device will be examined. This model is activated in the simulation by the command IMPACT SELB. However, when the energy balance model is used, the simulator automatically changes to the non-local Toyabe model which also changes automatically the analysis based on the velocity-field dependent model [Sof00]. Figure 2.2 shows the simulated drain current versus drain voltage for a SOI MOSFET of $0.3 \mu\text{m}$ channel length when the IMPACT SELB is used or not. From Figure 2.2, we see that by introducing the IMPACT SELB model, we have a much better agreement with the experimental values. This shows that the inclusion and choice for taking into account the impact ionization effect on the device is a relatively important factor in simulating devices.

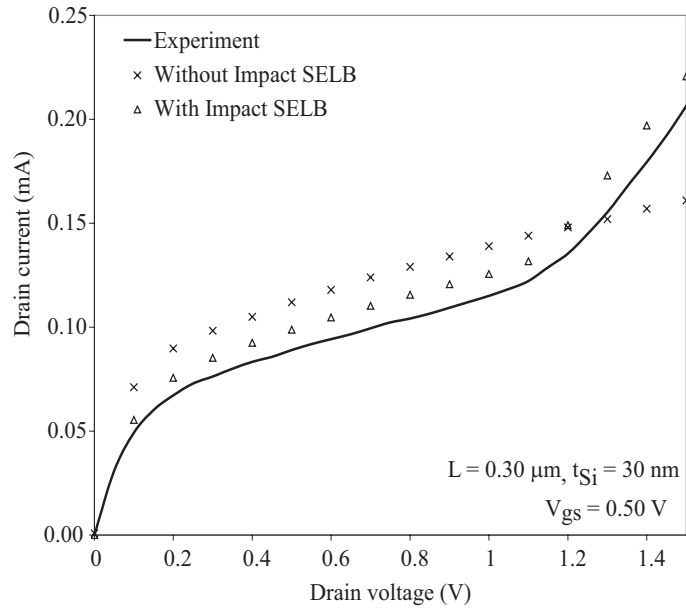


Figure 2.2: I_{ds} - V_{ds} curve for a nMOSFET SOI device with $t_{Si} = 30 \text{ nm}$ and $L = 0.30 \mu\text{m}$ showing the simulation differences when the IMPACT SELB model is on or off at $V_{gs} = 0.50 \text{ V}$.

2.5.5 Interface charge

The interface charges originates from the abrupt termination of the perfect periodic nature of the idealized single-crystal lattice [Nea97]. They exist within the bandgap at the semiconductor surface. This charge consists of 4 parts; oxide fixed charge, oxide trapped charge, mobile ionic charge and interface trap charge (also known as fast surface-state charge). These interface charges play an important role in the operation of the device. It mainly has a big impact on the mobility and capacitances at the interface which leads to changes in the electrical characteristics of the device. It is thus an important factor especially in the simulation of SOI devices that a model is used to include the effects of the interface charges since in an SOI material, there are 2 interfaces between silicon and oxide. The interface charges are especially important between the silicon film and the buried oxide. Normally in numerical simulations, there are not many models available for the approximation of the interface charges. In order to simulate the behavior of the interface charges, this can be specified directly in the simulation. In the simulator used in this work, this is done by using the INTERFACE command and adding a value needed. The value normally associated with the interface charges are between 3×10^{10} - 10^{11} cm^{-2} [RRBR06].

2.5.6 Mobility

The carriers in a semiconductor material are accelerated by applying an electric field. However, these carriers will eventually lose their momentum due to various events such as collisions, lattice vibrations, presence of impurity ions, other carriers, imperfection in the material and surfaces within the material. These events are grouped together and known as scattering processes. It is clear that the scattering process is very much related to the doping of the semiconductor, the lattice temperature, the electric field, the purity of the material, etc. Thus, the mobility model available needs to be able to take into account all these scattering effects and its origins. The modeling of the mobility behavior in the material can be divided into 4 main categories [Sof00],

1. low field behavior;
2. high field behavior;

3. bulk semiconductor regions;
4. inversion layers.

It is also important that the model takes into consideration the behavior of carriers in the inversion layer of a MOS device. This is because the events that happen in this layer are more complex than the normal scattering events. Additional events such as surface scattering, extreme carrier-carrier scattering and quantum mechanical size quantization effects can take place in addition to the effects mentioned earlier.

In this work, the most appropriate model to use is a model that takes into account the events that happen in the inversion layer. The model chosen is the Lombardi CVT model [Sof00]. This model takes into account all the necessary parameters such as the lattice temperature, the doping, the transversal and the longitudinal electric fields. It has also been designed for analysis of non-planar devices which is important in our case since devices such as the FinFET and triple-gate transistor are non-planar devices. This model has been designed in terms of a simple Matthiessen's rule, which provides a careful description of the MOSFET operation in a wide range of normal (or gate) electric fields, channel impurity concentrations ($5 \times 10^{14} \text{ cm}^{-3} < N_a < 10^{17} \text{ cm}^{-3}$), and temperature ($200 \text{ K} < T < 460 \text{ K}$) [LMS98]. Due to various factors that have been taken into account with this model, the other mobility models available were not chosen. For example, the Klaasen model is more suitable for simulation of bipolar devices, the Modified Watt model is only suitable for planar MOS devices and the Yamaguchi model is only limited to an operating temperature of 300 K [Sof00].

2.5.7 Self-heating

It is proven that when the MOSFET operates, there is heat generated in the device [Col97]. However, this self-heating effect in the MOSFET increases in SOI devices [GT06]. This is because in the bulk material, there is no buried oxide layer which retains the heat, while in the SOI material, the buried oxide prevents the generated heat from escaping due to the bad thermal conductance of the oxide. In SOI materials, this self-heating effects can cause a degradation of the device operation such as a reduction in the driving current. In order to take into account

this self-heating (in Silvaco this is referred to as lattice heating), this is done by adding the `lat.temp.` parameters together with the other models parameter.

2.5.8 Carrier heating

Another heating effect that should be added is the heating of the carriers itself. This is important especially for deep submicron devices because the probability of energy exchange between the carriers and the lattice increases. The use of this model is especially important when the energy balance model (or hydrodynamic model) is used because than the influence of this important towards the device. The inclusion of this in the model statement is also important because this is a more meaningful basis compared to modeling based on the electric field. The dependent on the velocity-field relationship is more closely modeled leading to more accurate simulations of the breakdown voltage and substrate current. The use of this statement introduces the more advanced non-Maxwellian approach based on the carrier temperatures for the impact ionization modeling. This model is activated by using either the `hcte.el`, `hcte.ho` and `hcte` for the considering of the electrons, holes or both respectively in the simulation.

2.6 Doping Profile

In the ATLAS package, it is possible to choose between two different types of analytical doping profile, uniform or Gaussian profile. To choose the doping profile to be used, it is only necessary to state in the doping statement, `UNIFORM` or `GAUSSIAN`. An abrupt doping profile in the device will create a sudden change in the doping profile between the source/drain junction and the channel region. In a Gaussian doping profile, this doping profile between the source/drain junction and the channel is a gradual change in doping profile following the Gaussian distribution. In the work presented here, we have used the abrupt profile. As a first approach, being more interested in analyzing the intrinsic and qualitative behavior of different MOS devices we considered a uniform profile for source/drain region as well as the channel. This

doping profile for simulation of advanced devices is common [KFC91] [STT⁺93]. Figure 2.7 shows the final doping profile using this uniform doping for a SOI MOSFET with intrinsic doping. However, it should

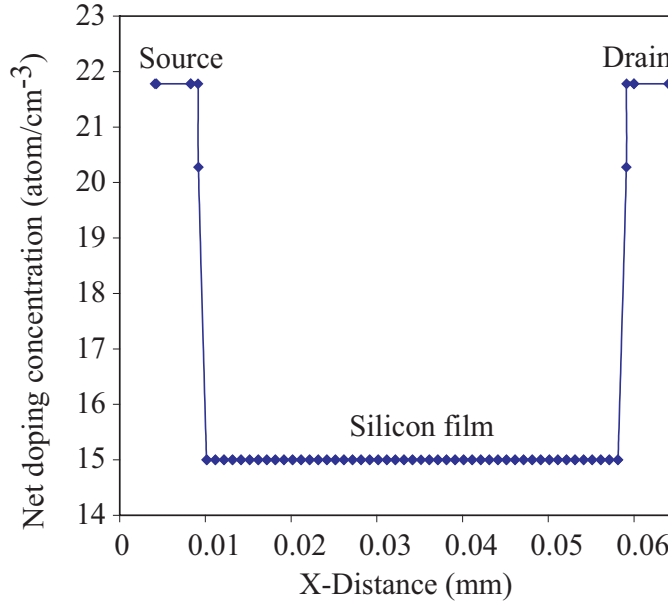


Figure 2.3: Doping profile based on the uniform doping profile for a SOI MOSFET device with intrinsic doping for the channel extracted at $0.01 \mu\text{m}$ below the silicon film.

be noted that the choice of the doping profile is important especially when reducing the thickness of the silicon film for nanodevices. There is an increase in the external parasitic resistance and this influences the electrical characteristics of the device. In such instances, it would be wise to perform some optimization steps in the context of the design of the source/drain junction. In this work, since the thinnest silicon film thickness that will be simulated is around 15 nm, it is expected that the results obtained will still be reliable especially in the strong inversion and saturation regime. The influence of this source/drain junction for thin advanced devices have been studied with the various necessary adjustment [LSH⁺03] [KSO04]. However, since in this work, we are not concern about thin silicon film devices, we have chosen to keep with the abrupt doping profile.

2.7 Conclusion

In this chapter we have shown that numerical simulation is a powerful tool for obtaining good predictability of future technologies due to the various models and methods available now. They are a good alternative compared to examining the real devices because we can also use them to analyze the physics of the device where it will be difficult in the real device. The simulation tools available now can also reduce the cost of research and development because they are cheap and efficient compared to trying to fabricate the device itself. In the current generation of simulators, they have proven to be able to work just like a virtual cleanroom and moving on to characterizing them. The power of using numerical simulation will be shown in the following chapters as it will be proven that they can be a good substitute for the real devices in analysis of novel devices.

However, we have seen that for some models, adjustments may be needed if the main purpose of the simulation is to analyze results quantitatively especially when deciding in between the drift diffusion and energy balance (hydrodynamic) models. In this work, since we are more interested in the qualitative analysis between the devices and from initial results, we have chosen to follow the guidelines as listed in the operating manual of the simulator.

Chapter 3

Graded-Channel Single-Gate and Double-Gate SOI MOSFETs

3.1 Introduction

Graded-channel (GC) single-gate (SG) SOI MOSFET devices corresponds to a SG SOI MOSFETs for which the channel doping is not uniform from the source to the drain. In this modified channel architecture, a different threshold implantation is applied. At the drain end the natural impurity level is preserved. Meanwhile, the source end is implanted for fixing the threshold voltage of the device. This channel engineering is done at layout level by the protection of a (relevant) photolithography mask on the drain side of the channel. This channel engineering method is fully compatible with the existing conventional CMOS fabrication process. Figure 3.1 shows a schematic cross-section of a GCSG SOI MOS device.

In Figure 3.1, it is clear that the channel length is divided into 2 sections, the intrinsic doped (referring to the natural doping of the SOI film) channel length, L_{LD} , and the doped channel length (known also as the effective channel length), L_{HD} , which can be defined as in Equation 3.1,

$$L_{HD} \approx L - L_{LD} \quad (3.1)$$

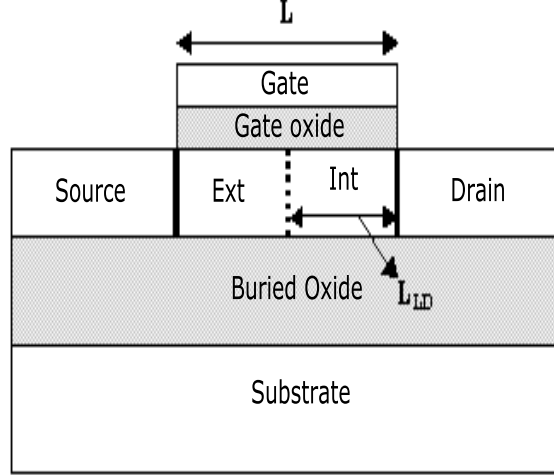


Figure 3.1: Schematic cross-section of a GCSG MOSFET transistor.

where L is the total physical gate length of the on-chip polysilicon.

The intrinsic region under the channel will exhibit a negative or a very small value of threshold voltage (V_{th}). This intrinsic region can be regarded as an extension of the drain region. Meanwhile, the doped region will exhibit the 'normal' threshold voltage of the device according to the doping in the doped region.

This architecture is also known as the laterally asymmetric channel devices. Although this is not the first time that such devices have been investigated [OSO⁺90] [BOR⁺89] [DCW01] [OH97] [CVG⁺99] [SWS93] [KLL⁺03] [PMDf00] [PMDf03] [PMF00a] [PMF02] [DR02] [Deh03], further possibility of such a device remains unexplored especially its application for DG SOI MOSFETs.

One of the main reasons for the introduction of the SG GC device with a modified channel doping was initially to reduce the inherent bipolar effects in SG FD SOI transistors [PMDf03]. Now, such devices are used to overcome other deteriorating effects such as hot electron degradation, reduction of the V_{th} roll-off, and other analog degradation characteristics [DR02].

In previous studies carried out on the GC structures [PMF00b], it

has been clearly shown that these devices are promising for low power, high performance analog/digital applications. This is because in such applications, the channel length can be maintained in the micrometer regime but gaining the performance of a submicron device. In VLSI technology, GC devices have shown an improvement of 30 % in the speed improvement compared to normal CMOS devices [JLK⁺96].

The GC structure is not only useful for the high performance applications, but it has also been shown that they are potential architectures for application in the growing wireless communication applications such as bluetooth, GPS applications and other wireless RF applications. It has been shown that in applications for wireless technology, 0.4 μm printed gate length can produce the same results as to a 0.25 μm gate technology due to the graded-channel technology [CKI⁺]. Some of the electrical results obtained from the longer gate length devices with graded-channel technology are even better compared to the shorter gate length devices.

The GC technology has also been applied in analog circuit design [PMF02] and promising results have been shown on this technology. In circuit design, the graded-channel design has demonstrated very high-gain in wide-bandwidth Operational Transconductance Amplifiers (OTA's). The GC structure has also improved the characteristics of microwave OTAs. These have been achieved using a die area that is either similar or reduced in dimension because of the advantages obtained from the graded-channel structure.

Due to these promising results in the various fields of applications, it is of utmost interest to further develop and investigate the prospective of these GC architectures. It is especially interesting to go one step further and combine the GC architecture with the double-gate structure to investigate how far such a combination can add to the already advantageous characteristics of these individual architectures. Besides, there is yet more work to be done in terms of the modeling/simulation of such a device to further exploit the potential of this GC architecture.

In this work, the potential of the GC design will be investigated further based on numerical simulation, modeling and characterization of the physical device itself. The potential of a graded-channel double-gate MOSFET will also be investigated. The fabrication of the GC channel is described and critical process steps are mentioned.

3.2 Fabrication of Graded-Channel devices

The fabrication of these devices are exactly the same as the normal CMOS fabrication process. The number of steps and masks used in the fabrication of this channel architecture is the same as in the normal CMOS process. The only difference here from the normal CMOS device fabrication is the placement of the V_{th} implantation mask. For example, in the fabrication of GC nMOS SOI devices, the mask used for the V_{th} implantation is designed at the desired position to protect the drain side from being implanted with impurities (boron in this case). Thus, in order to create a transistor with an undoped channel, this mask can be used to protect the whole channel length from being doped. To obtain a doped device, this mask is not used and thus dopant atoms can be implanted into the channel. Figure 3.2 shows the use of the implantation mask named GC for protecting the drain side of the channel from implanted species to form the GCSG nMOSFET transistor. The area covered by the mask (at the source side) will be doped over a length noted L_{HD} .

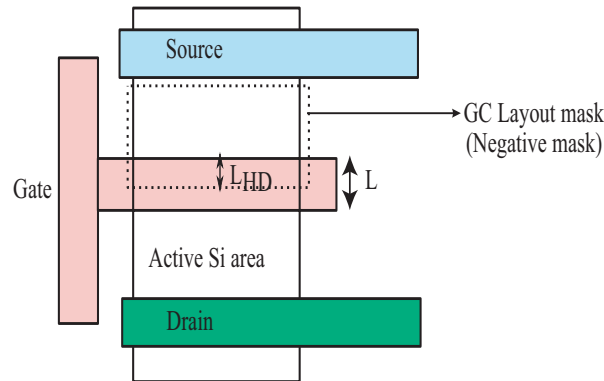


Figure 3.2: Schematic layout of GCSG nMOSFET transistor.

Although the fabrication of the graded-channel devices is very much similar to normal CMOS devices, there are still a few critical points that should be highlighted. One of the main points is the alignment of the graded-channel masks. In the fabrication of the GC device, it is important that the misalignment of the masks to form the graded channel structures is as small as possible in order to control the desired doped

and undoped channel lengths, respectively, L_{HD} and L_{LD} . If the misalignment is not kept to the minimum, the final graded-channels would lead to different electrical characteristics. As will be seen later in the electrical characterization, slight changes in the graded-channel dimension will have a rather significant effect on the device electrical characteristics.

Figure 3.3 shows a schematic example of a GC array designed used in the experiment.

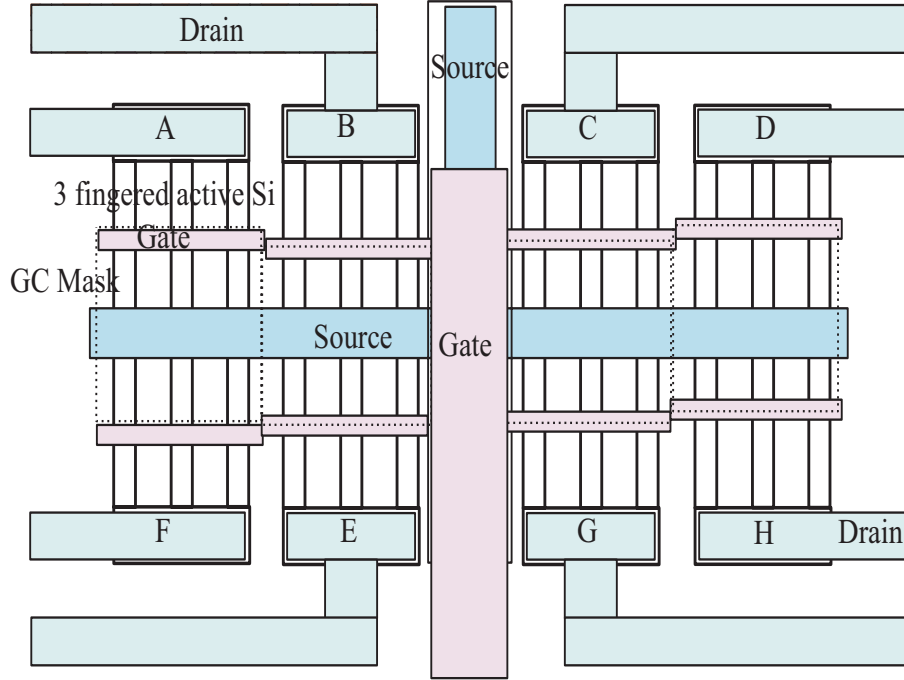


Figure 3.3: Schematic example of a GC array layout with the photolithographic masks used for the fabrication resulting from the various shifts of the GC mask. The transistors here have 3 fingers with a common source and common gate.

The identification of the different GC arrays seen in Figure 3.3 is listed in Table 3.1.

These GC arrays have been designed in order to study the effects of the different L_{HD} lengths (in other words, the L_{LD}/L ratio) on the electrical characteristics. The aim of this was to find the optimal L_{LD}/L

Device Identification	High doped mask length (μm) - L_{HD}	Low doped mask length (μm)- L_{LD}
A (Doped)	3.00	0.00
B	2.50	0.50
C	2.00	1.00
D	1.50	1.50
E	0.50	2.50
F (Intrinsic)	0.00	3.00
G	1.00	2.00
H	1.50	1.50

Table 3.1: Identification of the different GC arrays as seen in Figure 3.3.

ratio that would be useful for the different analog/digital applications as it can be imagined that for each ratio, there would be some advantages and disadvantages with respect to the various figure of merits such as transconductance, Early voltage, threshold voltage roll-off, etc. The devices in the GC array have 3 fingers connected in parallel with a width, W of $3 \mu m$ per finger. However, one of the factors in the fabrication process that will eventually affect the validity of the GC array shown in Figure 3.3 would be related to the precision of the alignment of the GC mask. Indeed, such misalignment does happen during the fabrication process of this GC array. Two extra designs were introduced on this GC array: doped (normally doped) and intrinsic (undoped) SOI MOS. In this new design, the GC mask was still used, but the size of the mask was extended in both vertical and horizontal direction to ensure a full coverage of the array that was to be an doped device. The intrinsic device was formed by leaving the gate area without any use of the GC mask. The two extra designs will be compared with device A and F for evaluating the degree of misalignment of the fabrication process. Figure 3.4 shows this modified layout to form the fully doped and undoped devices.

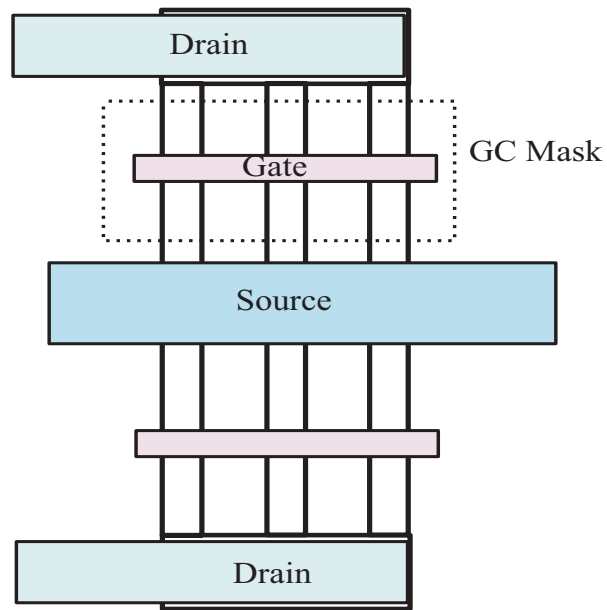


Figure 3.4: Schematic example of the additional reference layout showing the doped and undoped devices formed. The area covered by the GC mask will be an doped device. As seen, the GC mask to form the doped device is designed with some extensions to ensure that misalignment does not affect the final channel doping.

Device Identification	High doped mask length (μm)	Low doped mask length (μm)
A (Doped)	3.00	0.00
B	2.50	0.50
C	2.00	1.00
D	1.50	1.50
E	0.50	2.50
F (Intrinsic)	0.00	3.00
G	1.00	2.00
Doped	3.00	0.00
Intrinsic	0.00	3.00

Table 3.2: Identification of the different GCSG SOI MOSFETs transistors with the original length as drawn on the layouts. A and F are fully doped and undoped devices respectively with the non-extended mask.

3.3 Graded-Channel Single-Gate SOI MOSFET

The electrical characterization for the devices were done using the HP4145 Semiconductor Analyzer. The main extracted characteristics are the V_{th} , subthreshold slope (S), transconductance (g_m), transconductance-to-current ratio (g_m/I_{ds}) and Early voltage (V_{Ea}). These parameters are important for applications in both digital and analog electronics.

The devices investigated were fabricated at UCL with a 3 μm technology on a p-type UNIBOND©wafer with a starting impurity concentration of $10^{15} cm^{-3}$. The final thicknesses of the gate oxide, t_{ox} and the silicon film, t_{Si} are 30 and 87 nm, respectively. The thickness of the buried oxide was approximately 400 nm. The impurities implanted for the doped part of the device under the channel was $10^{17} cm^{-3}$ of boron atoms. Several ratios of L_{LD}/L were fabricated for investigation on the influence of these ratios. As in Figure 3.3, each device have 3 fingers. Table 3.2 shows the identification of the different devices with different ratios that were investigated. In order to investigate the influence of the channel engineering effect, these devices are compared to a SG SOI

nMOSFET (reference device) with a channel mask length of $3\ \mu\text{m}$, W of $3\ \mu\text{m}$ and 1 finger. In order for a fair comparison, the values obtained will be normalized against the width and the number of fingers.

3.3.1 Threshold voltage and Subthreshold-slope at Low-

$$V_{ds}$$

Table 3.3 shows the various threshold voltage extracted for the various GC and the fully doped and undoped SG SOI nMOSFET with the double derivative method extracted at $V_{ds} = 50\ \text{mV}$. A SG SOI MOSFET transistor with doping will be used as the reference to the GC array. Devices A-D are devices that have been fabricated to behave as doped devices with positive V_{th} while devices E-G have been fabricated to return back negative V_{th} , thus behaving as intrinsic devices. This reference device is a separate device built on the same wafer but located outside of the GC array. From Table 3.3 all of the GCSG devices have

Device Identification	$V_{th}(V)$	Subthreshold slope, S (mV/decade)@ $V_{ds} = 0.05V$
Reference	0.15	62.5
A (Doped)	0.14	62.4
B	0.10	62.4
C	0.08	61.9
D	0.08	62.2
E	-0.10	64.1
F (Intrinsic)	-0.10	64.4
G	-0.08	63.9

Table 3.3: V_{th} and subthreshold slope extracted from the different GCSG SOI MOSFETs transistors and the SG SOI nMOSFET at $V_{ds} = 50\ \text{mV}$. The reference device is a simple SG MOSFET device built on the same wafer with a impurities concentration under the channel $= 10^{17}\text{cm}^{-3}$

subthreshold slopes which are comparable to the reference device. This improvement in the subthreshold slope translates also to better transcon-

ductance to current ratio (g_m/I_{ds}). It is noticeable that all the different ratio of L_{LD}/L have nearly the same subthreshold slope values compared to the reference doped transistor. From these results, we can see that there are no severe degradation of the GC devices compared to the uniformly doped reference device in the subthreshold region.

Figure 3.5 shows the extracted transconductance-to-current ratio at $V_{ds} = 50$ mV for some GCSG devices and the reference SG MOSFET with the L_{eff} used for the normalization. This extraction of the L_{eff} will be discussed later in Section 3.3.2.

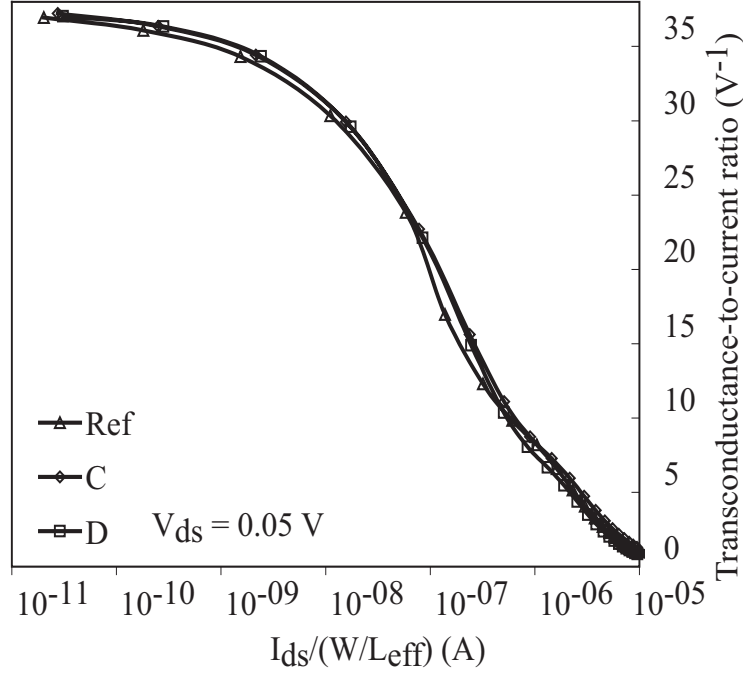


Figure 3.5: g_m/I_{ds} for various GCSG and the referenced SG SOI MOS devices extracted at $V_{ds} = 0.05$ V, where $W = 3 \mu\text{m}$ and L_{eff} are the respective values extracted shown in Table 3.4.

In Figure 3.5, we see that there is no significant improvement in the transconductance-to-current ratio values of the GC devices compared to the doped device. It is clear from Table 3.3 and Figure 3.5, that in the subthreshold region, the GC SG MOSFETs does not show any significant improvement over the normal doped SG MOSFETs.

3.3.2 Saturation Current

Figure 3.6 shows the $I_{ds}-V_{go}(=V_{gs}-V_{th})$ curve for the SG and GCSG SOI nMOS transistors extracted at a drain bias, $V_{ds} = 0.95$ V. From Figure 3.6, it is clear that the majority of the GCSG devices have higher level of current compared to the SG devices. This increase in the current is due to the existence of the low doped region where the increase in the V_{ds} is dropped across (and limited) in this region [PMF00a] [PMF02]. Due to this characteristic, the change in the concentration of the electrons in the inversion layer (the high doped region) is limited. This small change in this region results in the improvement of the analog and digital characteristics. .

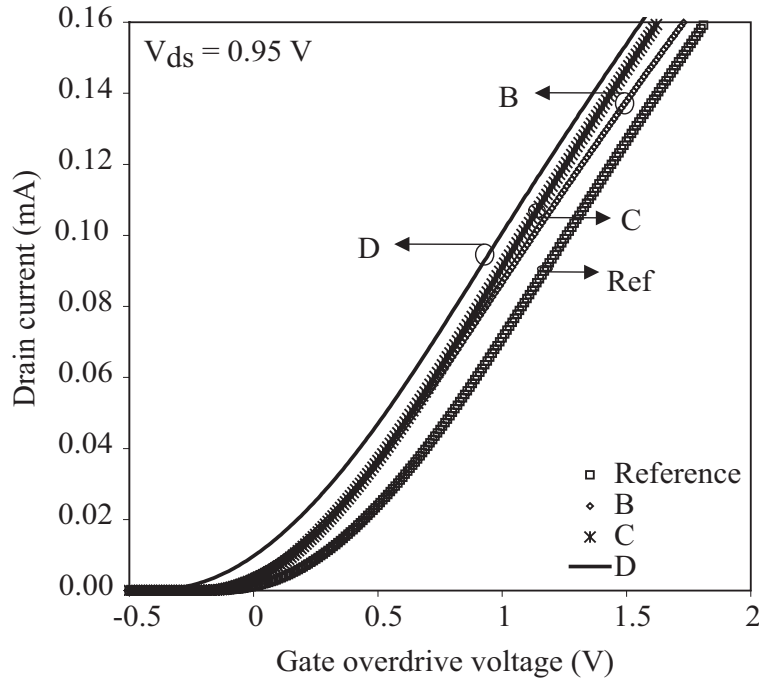


Figure 3.6: $I_{ds}-V_{go}(=V_{gs}-V_{th})$ curves extracted at $V_{ds} = 0.95$ V for various GC SG nMOSFETs and the reference SG nMOSFET transistor.

In Figure 3.7, the $I_{ds}-V_{ds}$ curves shown were extracted at a gate voltage overdrive (V_{go}) of 0.10 V. From Figure 3.7, it is again clear that

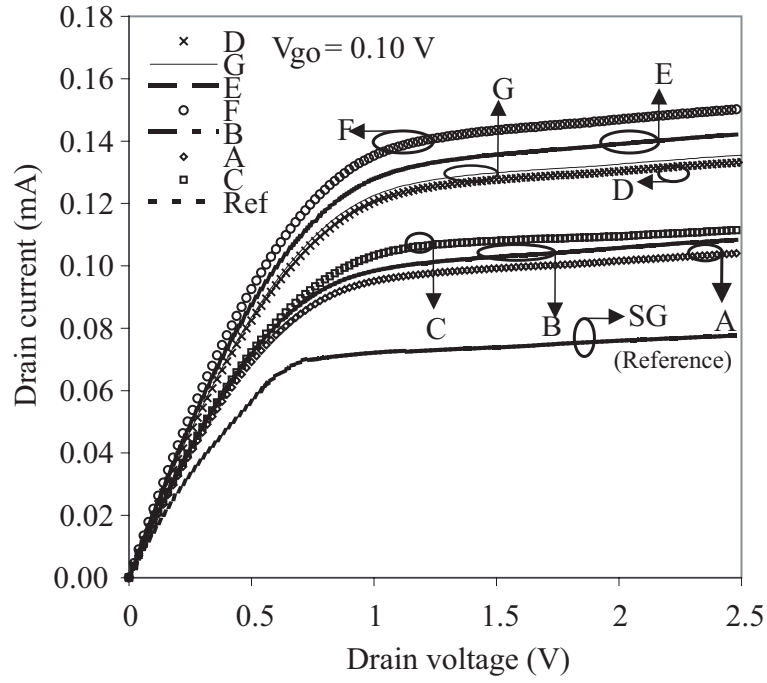


Figure 3.7: I_{ds} - V_{ds} curve extracted at $V_{g0} = 0.10$ V for GCSG and the reference SG SOI nMOS transistors.

most of the GCSG devices exhibit higher saturated current compared to the SG SOI nMOS transistors. From these I_{ds} - V_{ds} curves, an extra parameter that can be obtained is the effective channel length (L_{eff}) of the device. In this analysis, equation 3.2 shows the mathematical expression used [PMF00c],

$$\left(\frac{L_{LD}}{L} \right)_{eff} = 1 - \frac{I_{ds,FD}}{I_{ds,GC}} \quad (3.2)$$

where L_{LD} is the length of the undoped region, L is the mask channel length, $I_{ds,FD}$ is the drain current of the conventional fully depleted device and $I_{ds,GC}$ is the drain current of the GC device. This expression has been developed based on the assumption that the effective length is just the difference between the drawn channel length and the length of the low doped region, $L_{eff} = L - L_{LD}$. It is important that the extraction of the respective current is obtained in the saturation region, i.e. $V_{go} < V_{ds}$. However, one set-back of this expression is that it is not a very reliable method especially when used for analyzing graded-channel devices where the doped length is very small. This is because when the undoped length under the channel increases with regards to the doped length, this means that the difference in the mobility of the carriers also changes making the carriers mobility in the undoped region about 2-3 times much higher compared to the doped region. This difference is too big to be taken into account as the original equation assumes that the carriers mobility is the same along the channel in both doped and undoped regions. The solution to this would be to simply extrapolate the effective length from the I_{dsat} - L_{HD} curves at saturation for all the devices. This method eliminates the dependence on the carriers mobility. Figure 3.8 shows a schematic diagram of this extraction method.

In Table 3.4, the extracted L_{eff} from the extrapolation method for the various GCSG is shown.

3.3.3 Analog Characteristics

One of the main analog characteristics is the transconductance (g_m). This parameter represents the capability of the device to drive the cur-

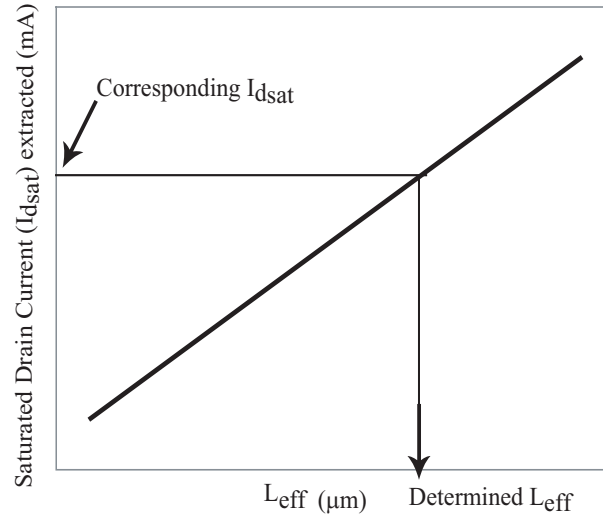


Figure 3.8: A schematic figure showing the method of extraction of the effective channel length (L_{eff}).

Device	$V_{th}(V)$ at $V_{ds} = 50$ mV	Mask $L_{eff}(\mu m) = L_{HD}$	Measured $L_{eff}(\mu m)$
Reference	0.15	-	-
A (Doped)	0.14	3.00	2.90
B	0.10	2.50	2.50
C	0.08	2.00	2.40
D	0.08	1.50	1.70
E	-0.10	0.50	-
F (Int.)	-0.10	0.00	-
G	-0.08	1.00	-

Table 3.4: V_{th} , the designed and the extracted L_{eff} from the various GC and reference SG SOI nMOSFET. (Measured values for Devices E, F and G are not shown due to the uncertainty due to the low V_{th})

rent because it shows the effectiveness of the gate voltage in controlling the drain current. g_m for a MOSFET is given as in equation 3.3 [Col97],

$$g_m = dI_{d,sat}/dV_{gs} \quad (\text{for } V_{ds} > V_{dsat}) \quad (3.3)$$

In Figure 3.9, the transconductance for GCSG devices C and D are shown in comparison to the SG MOSFET extracted at $V_{ds} = 0.95$ V. From Figure 3.9, it is clear that device C ($L_{eff} = 2.40 \mu m$) has the

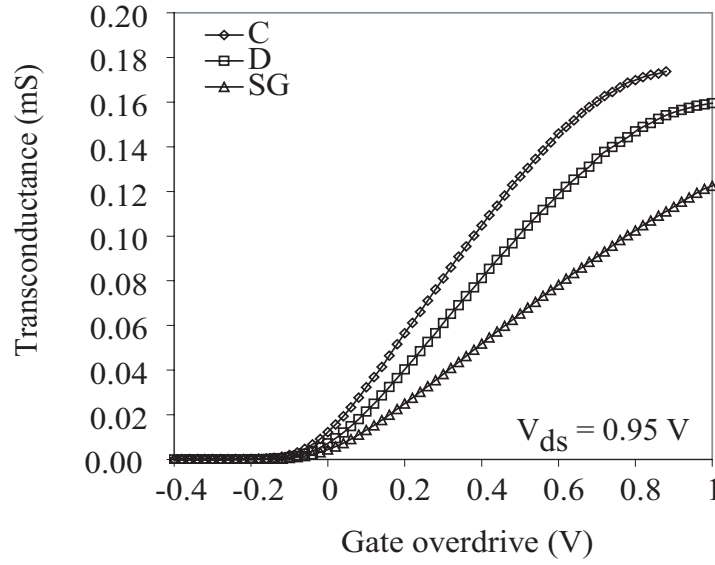


Figure 3.9: g_m for various GCSG and SG SOI MOS devices extracted at $V_{ds} = 0.95$ V.

highest g_m . This high g_m value translates into the better current gain of the device. It is clear that there is an improvement of approximately 1.4 times between uniformly doped SG and device D at the same V_{go} . This increase in g_m between device C and the uniformly doped SG is approximately 1.6 times at the same V_{go} . This increase in the g_m translates also into a higher Gain Bandwidth Product ($GBW = \frac{g_m}{2\pi C_L}$) where C_L is the load capacitance.

Another parameter that will be of importance for the analog characteristic of the device is the Early Voltage (V_{EA}) which reflects on the output conductance of the device. The Early voltage is related to the output conductance as shown in equation 3.10

$$V_{EA} = g_{ds}/I_{ds} \quad (3.4)$$

The higher the V_{EA} , the lower the conductance (g_d) and this leads to a higher output voltage gain. Figure 3.10 shows the Early voltage

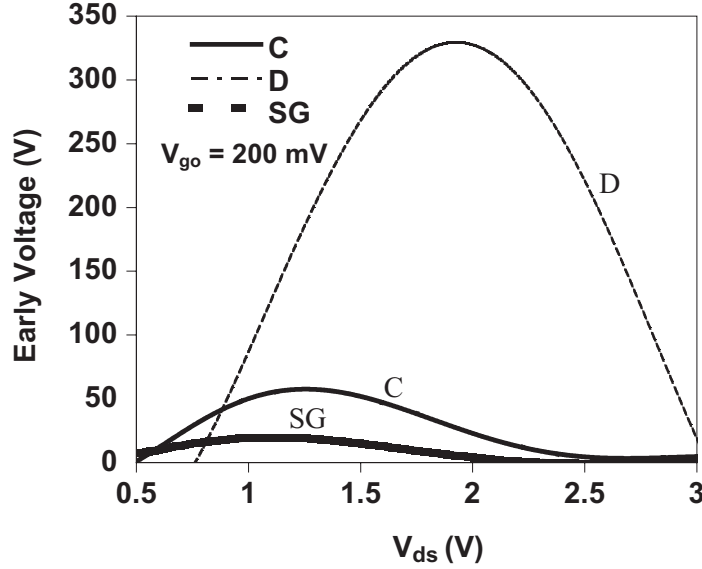


Figure 3.10: Early Voltage for various GCSG and SG SOI MOS devices extracted at $V_{go} = 200$ mV.

extracted at V_{go} of 200 mV for a few GCSG SOI MOS and the reference SG SOI MOS transistor. In this figure, it is clear that the GCSG devices have much higher values of V_{EA} compared to the uniformly doped SG device. The value of V_{EA} reached for device D is nearly 330 V while that of the uniformly doped SG is only about 25 V. Such an increase in Early voltage for the GCSG devices show its superior characteristics in generating higher output gain. Such Early voltage figures for SG devices with $L = 3 \mu m$ can only be achieved with GCSG structures.

An explanation for these high g_m and Early voltage values for GCSG devices is related to the reduced channel length modulation due to the strong depletion region below the low doped region. In order to understand further the effect of this undoped region under channel and its

effects on the characteristics of the device, numerical simulations were carried out. The results from these simulations will be presented later in this chapter.

From the electrical characteristics results obtained from the GC Single-gate architecture, it is clear that in the strong inversion region, there are lots of advantages to be gained from these devices. However, in the sub-threshold region, these SG devices do not shown any big improvement in comparison to the referenced uniformly doped SG SOI MOSFET. Thus, in order to have a device that would also perform well in the sub-threshold region, it will be interesting to see the effect of combining the graded-channel architecture to a double-gate architecture. It has been shown that the double-gate architecture is a very promising device for improvement in the subthreshold region [Col97].

3.4 Graded-Channel Double Gate devices

3.4.1 Introduction

The Graded-Channel Double Gate SOI MOSFET transistors is a combination of the graded-channel structure and the double-gate MOS planar architecture. Figure 3.11 shows a schematic overview of a GCSG, uniformly doped DG and a GCDG SOI MOSFET. A double-gate is just a

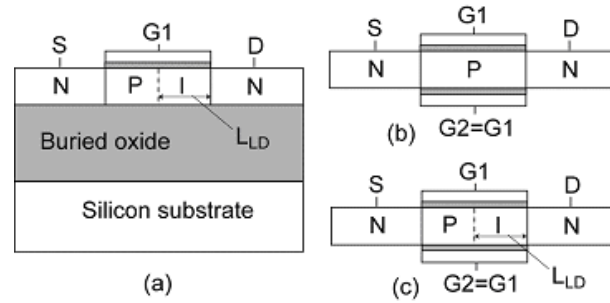
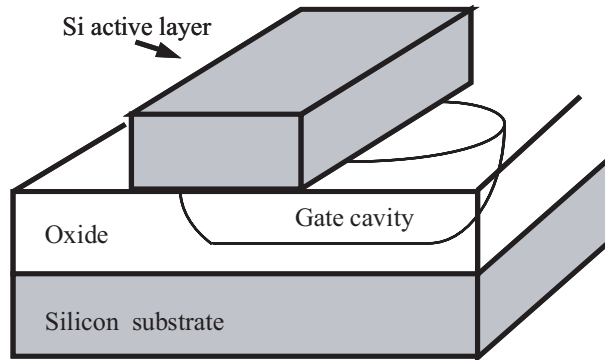


Figure 3.11: Schematic overview of (a) Graded-channel single-gate SOI MOSFET, (b) Double-gate SOI MOSFET and (c) Graded-channel double-gate SOI MOSFET.

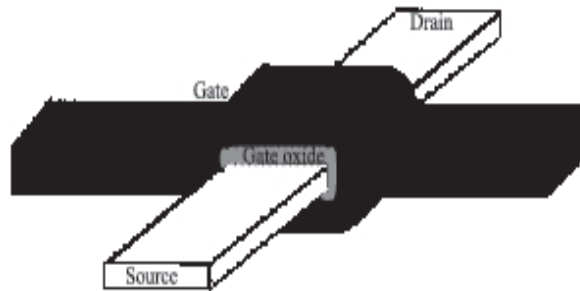
SG SOI MOSFET with an additional gate located precisely at the bottom of the silicon film. This DG structure will be looked into more

closely in Chapter 4. The DG structure has been identified as the most promising structure in accordance with the requirements listed out in the ITRS [hta]. However, in the concept presented here, one of the advantages that will be shown will not focus on the ability to move to a smaller dimension, but more importantly its capability as a device for use in high performance analog applications such as high gain wide bandwidth operational transconductance amplifier (OTA's), current mirrors and precision analog applications. Its capability to be combined with the fabrication of MEMS devices allows for easy integration with high gain applications [DRR⁺95] [MNMI97]. DG structures are devices that have already been recognized as devices with superior control on short channel effects thanks to the excellent ability to control the charges in the channel [STT⁺93] [FTFdW94] [FTF92]. Thus, with the combination of both the advantages of a DG structure and the GC structure, a GCDG SOI MOSFET should exhibit excellent characteristics for both analog and digital applications.

The devices investigated here are the devices fabricated in the same condition as the GCSG devices investigated in the last section. These DG structures were fabricated with the Gate-All-Around method first proposed by J.P. Colinge [Col97]. The important steps in the formation of the DG structure begins with the formation of silicon islands by removing the buried oxide underneath the top thin silicon film. This etching is performed using a buffered hydrofluoric chemical etch. This leaves a silicon bridge where the gate oxide layer is grown followed by the channel implantation and the formation of the surrounding gate with the CVD (Chemical Vapor Deposition) of the polysilicon gate. After the patterning of the polysilicon gate, the source and drain regions are implanted. Figure 3.12 shows a schematic illustration of this process. In order to analyze these devices in detail, they were simulated using SILVACO®. In these simulations no optimization on the default coefficients were carried out, thus leaving them as *per se* [Sof00]. The dimension of the devices were: $t_{ox} = 30$ nm, buried oxide thickness of 150 nm, silicon film thickness equal to 87 nm, intrinsic-doping of 10^{15} cm^{-3} , doped doping = 10^{17} cm^{-3} of boron with abrupt doping profile. The polysilicon used for the gate material was left as the default n-doped polysilicon with no change in the workfunction. Interface charges were also included at the silicon-oxide interfaces with a value of around 3



(a)



(b)

Figure 3.12: Schematic figure illustrating the GAA formation by (a) isotropically etching the buried oxide to form a silicon bridge and (b) 3-D view of the final device.

$\times 10^{10} \text{ cm}^{-2}$ for both the top and bottom interface. Analytical modeling [KCFR04] and experimental results from the devices available were also used to verify the numerical simulations. These GCDG devices were compared with a uniformly doped DG SOI MOSFET, GCSG SOI MOSFET and a uniformly doped SG SOI MOSFET.

3.4.2 Analytical Modeling

In this section, a short description over the analytical model used in the verification of the numerical simulations is presented. To obtain the compact model needed, the channel region of the graded-channel was divided into two parts; high doped (HD) and low doped (LD). For each of these parts, using the charge density, an expression for the drain current was developed taking into account the effects of the doping and the length of high/low doped regions.

In building this model, a steep transition with regards to the silicon film doping at the boundary of high/low doped regions was assumed. This means that we have assumed here that no lateral diffusion of the doping between the high and low doped regions. We have also assumed that there would be no volume inversion effect in the weak inversion region due to the thickness of the silicon film analyzed here. The analytical model is divided into three main parts; linear, saturation and subthreshold region.

Linear Region

In this region, the drain current can be expressed as Equation 3.5.

$$I_{ds}(x) = (Q_{ni}(x)W) \frac{\mu \left(\frac{dV_c(x)}{dx} \right)}{1 + \frac{1}{E_{sati}} \left(\frac{dV_c(x)}{dx} \right)} \quad (3.5)$$

where W is the device width, $E_{sati} = 2v_{sat}/\mu_{ni}$ and μ_{ni} are the critical field and mobility in the high and low doped regions respectively. v_{sat} is the saturation velocity and $Q_{ni}(x)$ the surface charge density. To obtain enable a compact form of the drain current in this region, the drain current in the high and low doped regions are equated resulting in Equation 3.6.

$$V_{HD}(V_{gs} - V_{thHD})\frac{\mu_{nHD}}{L_{HD}} = V_{LD}(V_{gs} - V_{thLD})\frac{\mu_{nLD}}{L_{LD}} \quad (3.6)$$

where V_{HD} and V_{LD} are the voltage drops in the high and low doped regions, respectively.

Saturation Region

In this region, the drain current is shown in Equation 3.7.

$$I_{ds} = 2WC_{ox}(V_{gs} - V_{th} - V_{dsat})v_{sat} \quad (3.7)$$

where V_{sat} is the drain saturation voltage. In order to obtain a smooth translation between the linear and saturation region, a smoothing function was used. The channel length modulation effect was incorporated into this model by considering the voltage drop over the velocity saturation region. The change in the total channel length was replaced with $(L - \Delta L)$. Further explanation of this model can be found in [KCFR04].

Subthreshold Region

In the subthreshold region, the drain current is expressed as in Equation 3.8.

$$I_{sub} = \frac{WD_{HD}}{L_{HD}}(Q_n(0) - Q_n(LD)) \quad (3.8)$$

where D_{HD} is the electron diffusion constant for the high doped region, $Q_n(0)$ and $Q_n(LD)$ are the surface charge density at the source and drain, respectively. In order to analyze the subthreshold region for a double-gate MOSFET, some modification needs to be made to the drain current expression in Equation 3.8. Detailed explanation can be found in the paper by A. Kranti [KCFR04].

In general, in order to have a analytical model that models a valid drain current from subthreshold to saturation, the functional form of the effective gate overdrive (V_{go}) is used. The effect of channel length modulation and drain induced barrier lowering were also taken into account for the modeling. The impact ionization current is also included in the model resulting in a total drain current given in Equation 3.9.

$$I_{dtotal} = I_{ii}(M - 1) + I_{ds} \quad (3.9)$$

where I_{ii} is the impact ionization current, M is a constant given in [KCFR04] and I_{ds} the drain current.

The above is a small overview of the analytical model used here in the analysis. Details of the derivation of the various equations can be found in reference [KCFR04].

3.4.3 Subthreshold Regime

Table 3.5 shows the identification of the different devices with different length ratios that were investigated. From Table 3.5, all the DG devices

Devices	L_{HD} (μm)	L_{LD} (μm)	$V_{th}(V)$ at $V_{ds} = 50$ mV		S at $V_{ds} = 0.8$ V (mV/decade)	
			Model	Simulation	Model	Simulation
A	2.20	0.00	0.240	0.240	59.66	59.97
(Ext.)						
B	2.10	0.10	0.230	0.230	59.65	60.40
C	1.64	0.56	0.194	0.190	59.87	60.03
D	1.06	1.14	0.194	0.190	59.64	60.07
E	0.15	2.00	-0.022	-0.020	70.43	68.55
F	0.00	2.20	-0.300	-0.300	59.96	60.10
(Int.)						
G	1.10	0.00	0.240	0.240	60.26	60.36
SG-A	2.20	0.00	0.300	0.300	69.35	67.72
SG-D	1.06	1.14	0.258	0.260	73.80	71.07

Table 3.5: Properties of the GC and uniformly doped DG and SG SOI MOSFET devices analyzed.

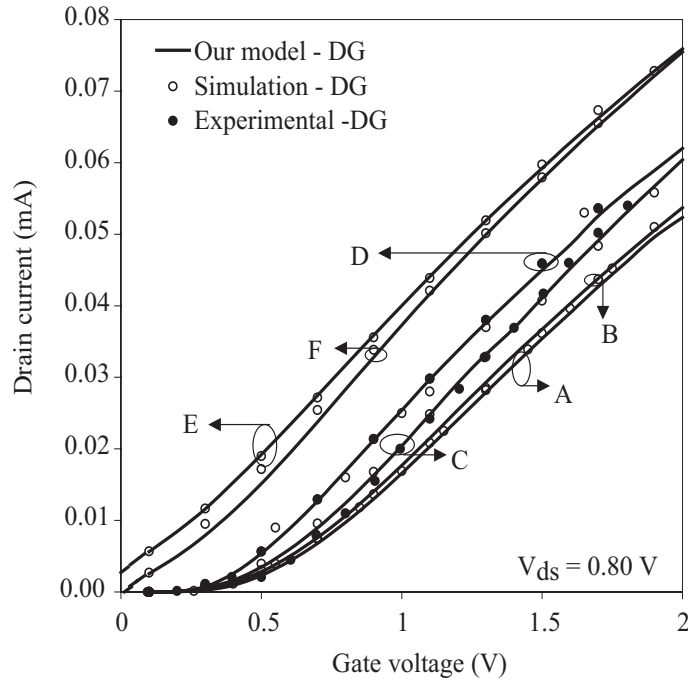
(A-G) with the exception of device E, show near ideal subthreshold slope values (≈ 60 mV/decade). Such values are obtained in the DG devices due to the excellent control of the charges from the top and the bottom gates. In device E, a deviation from this ideal S is due to the short channel effects due to the extremely short effective channel length

($L_{eff} = 0.15 \mu m$). Such improvement in the S values for the GCDG devices demonstrates the ability of the device to be used in digital applications. From the values in Table 3.5, we can see that there are good agreements between the simulation and analytical models. Figure 3.13 shows the I_{ds} - V_{gs} curves for the all the devices at $V_{ds} = 0.80$ V in linear scale and in logarithm scale in Figure 3.14 at the same bias point.

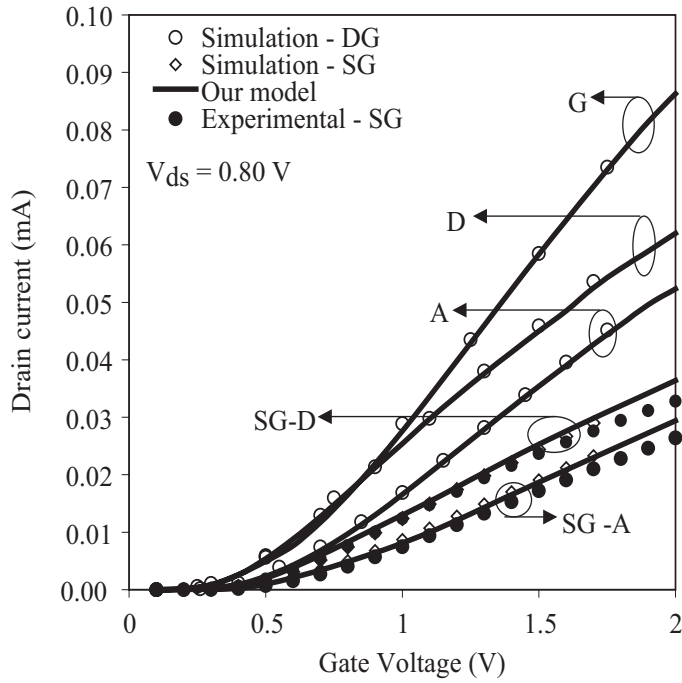
From Figure 3.13 and Figure 3.14, devices B, C, D and E all have much better I_{ds} - V_{gs} characteristics compared to device A (uniformly doped DG). If V_{gs} is fixed, all the GCDG devices have higher I_{ds} compared to the uniformly doped device. We also see that the superiority of the GCDG architecture in comparison to the GCSG structure. From these two figures, it can also be concluded that there is not only good agreement between the analytical and numerical simulations, but also between these simulations and the experimental values.

3.4.4 Saturation Current

Figure 3.15 shows the I_{ds} - V_{ds} curve for the various devices extracted at $V_{gs} = 400$ mV. In the I_{ds} - V_{ds} curves, we see that the GCDG devices exhibit excellent output characteristics compared to the uniformly doped DG and SG SOI MOSFET in the saturation regime. With the GCDG architecture, the breakdown voltage (V_{break}) is improved compared to the premature V_{break} of the uniformly doped DG and SG devices. To show the clear advantage of the GC structure, two devices with the same L_{eff} is used here, device D and G. Looking at the characteristics of these devices, it is clear that device D has a near flat saturation current compared to device G. This translates into a tremendous increase in the Early voltage which translates into an extremely reduced output conductance (g_d). Such a device is certainly a device to be considered for low-power, low-voltage analog circuit applications. Such values in V_{EA} and g_d is obtained due to the low doped region in the GC channel absorbing the drop in the drain voltage leaving the electron concentration in the inversion layer unaffected as seen also for the GCSG device previously. From Figure 3.15, it is clear that device E has the highest saturation current due to its doped region which is the shortest among all the other GCDG devices.

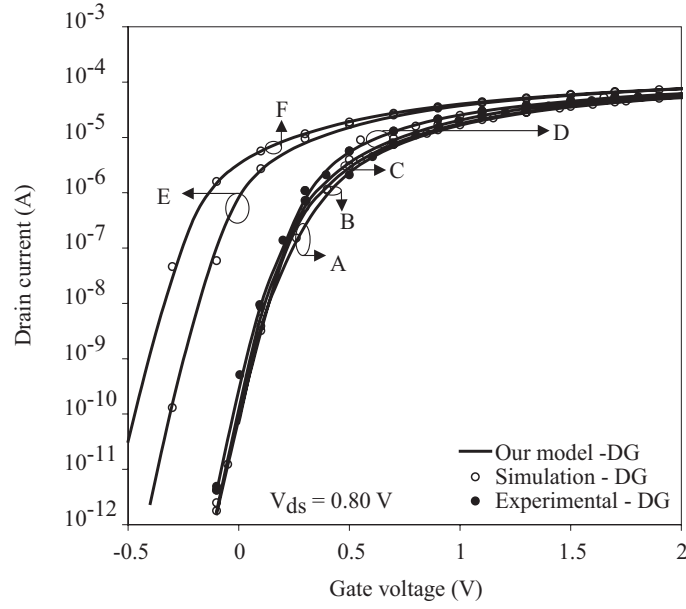


(a)

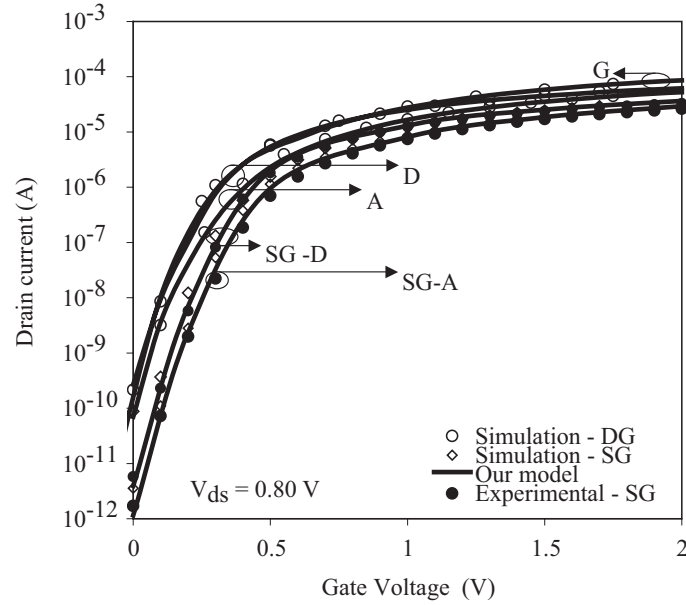


(b)

Figure 3.13: (a) I_{ds} - V_{gs} curve for the GCDG SOI MOSFET devices and uniformly doped DG SOI MOSFET at $V_{ds} = 0.80$ V. (b) I_{ds} - V_{gs} curve for the GCDG and GCSG SOI MOSFET and uniformly doped DG and SG SOI MOSFET at $V_{ds} = 0.80$ V.



(a)



(b)

Figure 3.14: (a) I_{ds} - V_{gs} curve for the GCDG SOI MOSFET devices and uniformly doped DG SOI MOSFET extracted at $V_{ds} = 0.80$ V with logarithm scale. (b) I_{ds} - V_{gs} curve for the GCDG and GCSG SOI MOSFET and uniformly doped DG and SG SOI MOSFET extracted at $V_{ds} = 0.80$ V with logarithm scale.

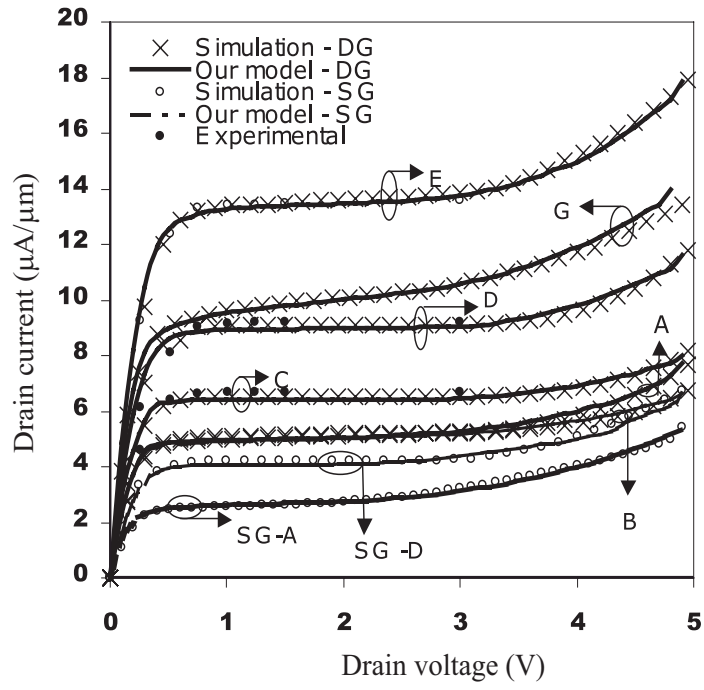


Figure 3.15: I_{ds} - V_{ds} curves for the GCDG and GCSG SOI MOSFET devices and uniformly doped DG and SG SOI MOSFET extracted at $V_{go} = 400$ mV.

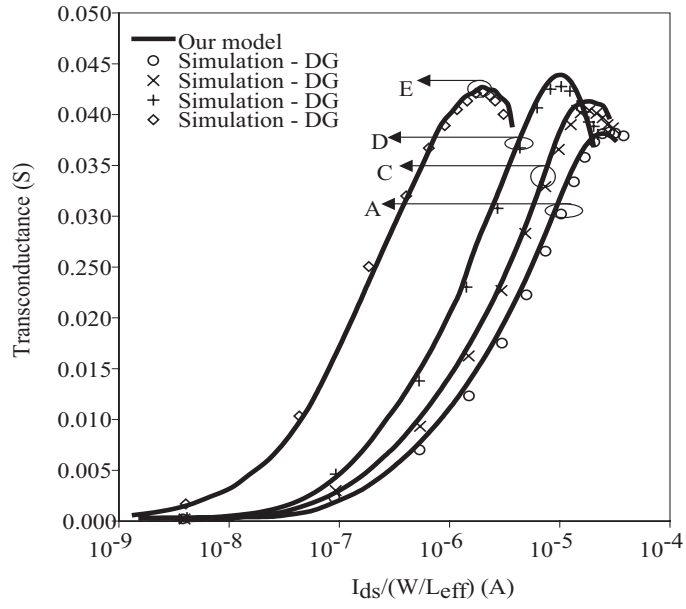
3.4.5 Analog characteristics

The three main analog characteristics that will be analyzed here are the gate transconductance, the subthreshold slope which is related to the transconductance to current ratio, the Early voltage and the voltage gain.

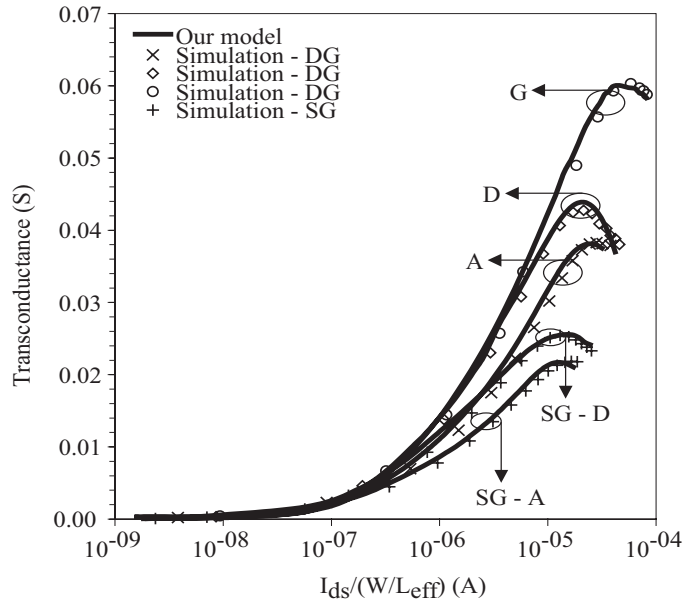
3.4.5.1 Gate transconductance

The gate transconductance is a parameter that is related to the DC gain and the GBW performances of the device. Thus, an increase in the g_m can translate into an increase in the DC gain ($A_{VO} = g_m/g_{ds}$) and GBW (g_m/C_L). Figure 3.16 shows the extracted transconductance with the corresponding normalized current at $V_{ds} = 0.8$ V for some of the devices analyzed here.

From Figure 3.16, at low drain current levels, we see that the g_m of device D is very close to that of device G, however, as the current increases, the g_m of device D ($L_{HD} = 1.06 \mu m$) moves closer to device A ($L_{HD} = 2.2 \mu m$) making the two peak g_m of the device nearly the same at this higher current. From this observation, it can be said that we can use a GC device to achieve the same value of g_m but biased at a lower drain current. This shows that we can have better DC gain at lower bias for a GCDG device compared to a uniformly doped device which makes it excellent for use in analog applications. If the normalized drain current is fixed at 10^{-5} A, the g_m of device A and D is 224.5 mS and 575.4 mS respectively whereas g_m for devices SG-A and SG-D is 158.0 mS and 204.0 mS respectively. At this fixed normalized current value, the g_m of the uniformly doped DG devices as compared to the SG devices is 1.4 times higher and about 2.8 times higher in the GC devices as compared to the SG GC device for the same L_{LD}/L ratio. This improvement in g_m at a fixed current level translates to a better Gain Bandwidth product. In Figure 3.16, it is clear that as the $L_{HD} = L_{eff}$ decreases, the g_m is always much higher for the GC devices compared to the uniformly doped DG device in the moderate and strong inversion regions. However, it should be pointed out that there is an optimized ratio (L_{LD}/L) that can be used as observed. As L_{LD} increases (as in the case of device E), there is also an increase in the length of the pinch-off region which leads to a high series resistance under the channel. This increase in series resistance reduces the advantages of the GC structure



(a)



(b)

Figure 3.16: (a) $g_m-I_{ds}/(W/L_{eff})$ curves for some of the GCDG and GCSG SOI MOSFET devices and uniformly doped DG and SG SOI MOSFETs extracted at $V_{ds} = 0.8$ V. (b) Variation of g_m with normalized I_{ds} for DG devices at $V_{ds} = 0.8$ V

thus, lower values of g_m are obtained. Thus, there is no beneficial gain with the increase of this (L_{LD}/L) above a certain optimized value.

3.4.5.2 Transconductance-to-current ratio

The g_m/I_{ds} ratio is an important parameter as it is related to the subthreshold slope ($S = \ln(10)/(g_m/I_{ds})$). This parameter can be used to compare devices with different dimensions because it is dimension independent [SFJ96]. Figure 3.17 shows the g_m/I_{ds} ratio for the various GCDG and GCSG and uniformly doped DG and SG SOI MOSFETs extracted at $V_{ds} = 0.8$ V. From Figure 3.17, it is clear that the GCDG

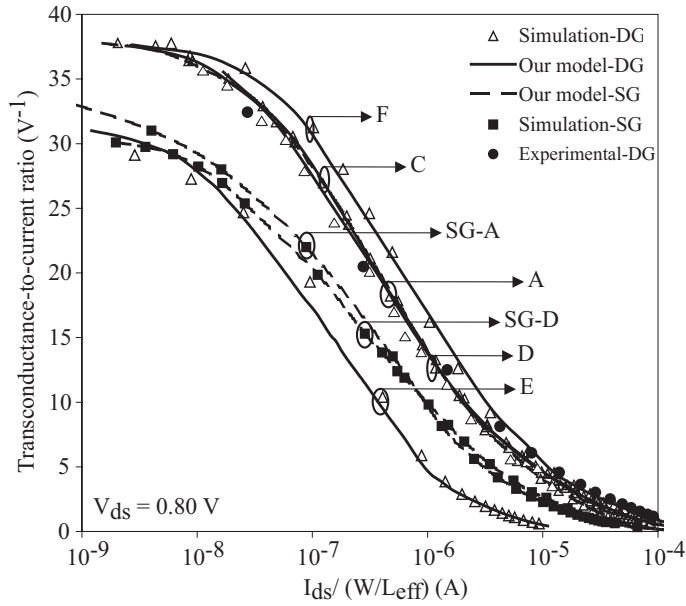


Figure 3.17: g_m/I_{ds} ratio for the various GCDG and GCSG and uniformly doped DG and SG SOI MOSFETs extracted at $V_{ds} = 0.8$ V.

devices have near ideal g_m/I_{ds} values of 38 V^{-1} . The GCSG devices show a slightly lower value of 32 V^{-1} . The only exception here is for device E which has a very much lower value due to the short channel effects bringing it to values close to uniformly doped SG devices. The GC combination with the DG architecture clearly makes it possible to

achieve relatively high g_m/I_{ds} in device E even when L_{eff} is as small as $0.15 \mu\text{m}$. The presence of the high doped region near the source end seems to strengthen considerably the resistance to barrier lowering thus improving the SCE immunity and improving the value of the g_m/I_{ds} . These values of g_m/I_{ds} translates into excellent S values as seen in Table 3.5. From Figure 3.17, we can also see that there is a bigger increase in the current drive for the GCDG devices compared to the GCSG devices. At a fixed g_m/I_{ds} value, an increase in the current drive by a factor of approximately 2.5 is recorded. This increase in drive current is related to the DG structure.

3.4.5.3 Early voltage

The Early voltage parameter is related to the drain conductance of a device through the expression in Equation 3.10. The extraction of V_{EA} allows us to compared the output characteristics of different devices independently of the driving current which is different for the GC and uniformly doped devices.

$$V_{EA} = g_{ds}/I_{ds} \quad (3.10)$$

Figure 3.18 shows the plot of the Early voltage for the different GC and uniformly doped devices extracted at $V_{go} = 400 \text{ mV}$.

It is clear that all the GC devices have much better V_{EA} compared to the uniformly doped devices in the saturation region. Looking only between the DG and SG uniformly doped device, the values of the Early voltage are much higher in the DG structure compared to the SG devices. At a fixed V_{ds} of 2.0 V , the V_{EA} for the DG device is 57 V compared to the SG device with only a $V_{EA} = 27 \text{ V}$. This improvement in the DG device is related to the improved control of the gates over the charges which reduces the influence of the drain on the drain current (i.e reduced electric field). Such a reduction in the influence of the drain reduces the drain conductance which then improves the Early voltage. With the combination of the DG structure and the GC engineering, the improvement of the transistor output characteristic is even better. This is reflected in the extremely high V_{EA} values obtained

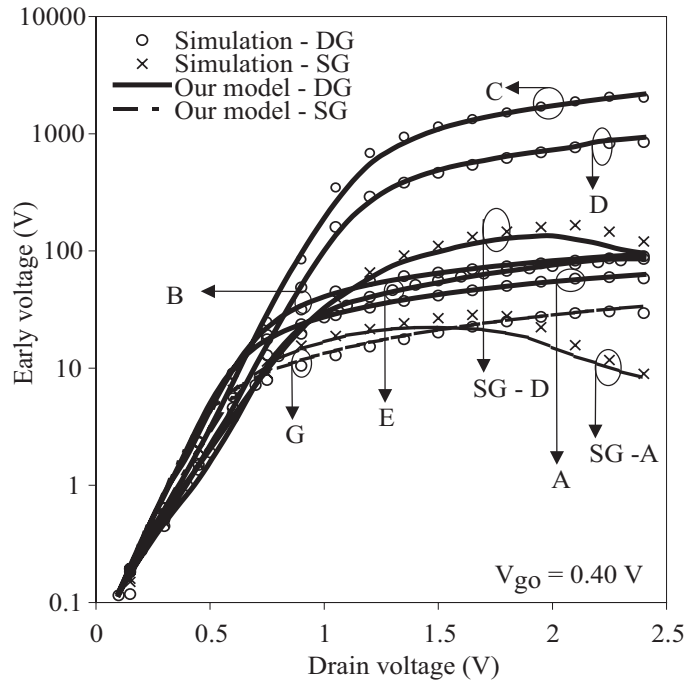


Figure 3.18: Early voltage for the various GCDG and GCSG and uniformly doped DG and SG SOI MOSFETs extracted at $V_{go} = 400 \text{ mV}$.

as seen in Figure 3.18. In device C, we have V_{EA} of more than 1600 V in the saturation region. For the other devices, the values of Early voltage obtained although less than 100 V, they are still much higher compared to the V_{EA} obtained normally in the range of 7-10 V/ μm for uniformly doped SG SOI MOSFETs. Such improvement in the Early voltage values for the GC structures can be analyzed qualitatively by viewing such a structure as a series combination of two sub transistors connected in series and controlled by a common gate [Deh03]. Under that condition, the Early voltage of a GC MOSFET can be expressed as in equation 3.11:

$$V_{EA} = (V_{EA})_{HD} \times \left(\frac{g_m}{g_{ds}}\right)_{LD} \quad (3.11)$$

where $(V_{EA})_{HD}$ is the Early voltage in the high doped region, and $\left(\frac{g_m}{g_{ds}}\right)_{LD}$ is the intrinsic DC gain in the low doped region. In order to clearly show this analysis, two separate uniformly doped devices with two different dopings and gate lengths were simulated for each DG and SG structure. Table 3.6 shows the values obtained from this simulation. From the values in Table 3.6, the corresponding Early voltage

Device	L (μm)	$(V_{EA})_{HD}$ (V)	$\left(\frac{g_m}{g_{ds}}\right)_{LD}$ (dB)
DG_{HD}	1.5	38	-
DG_{LD}	0.6	-	28
SG_{HD}	1.1	12	-
SG_{LD}	1.1	-	21

Table 3.6: Values of the uniformly doped DG and SG devices simulated with two different channel lengths at $V_{ds} = 1.5$ V.

calculated using Equation 3.11 expected are, respectively, 950 V for the GC devices and 130 V for the uniformly doped SG device. These values are very close to the values that were obtained from the numerical simulation and the experimental values as shown previously. The high Early voltage value obtained for device C is attributed to the reduced variation in the channel potential to the change in drain bias in

high doped region. This reduction in the variation of the channel potential leads to a reduction in the velocity saturation length which thus increases the Early voltage as a whole because of the increase in the output resistance. Thus, when the L_{LD}/L ratio is increased, the V_{EA} will also increase. However, if this L_{LD}/L ratio is further increased, the V_{EA} decreases in value. From the simulation and experimental results, the optimized L_{LD}/L ratio is approximately 0.3. In Figure 3.18, we see a deviation in the V_{EA} value for the SG devices at higher drain voltage bias due to the non-inclusion of the parasitic bipolar effects from the simulations coefficients [PMDF00].

3.4.5.4 Voltage gain

The voltage gain is an important factor of merit for designing Operational Transconductance Amplifiers. Currently, in single stage OTA, high voltage gain is obtained by using long channel transistors and/or cascades structures with their intrinsic limitations affected by die area, output swing, power consumption, stability and bandwidth [PMF02] [ECF⁺96] [GMSL94]. Such limitations are overcome by the GC structure as will be shown. Table 3.7 shows the values of the DC gain for the DG and SG GC and uniformly doped SOI MOSFETs extracted at $V_{go} = 400$ mV. It is clear that the GCDG devices C and D show a sig-

Device	L_{HD} (μm)	L_{LD} (μm)	$A_{VO} = (\frac{g_m}{g_{ds}})_{LD}$ (dB) at $V_{ds} = 2.0$ V, $V_{go} = 400$ mV
A	2.2	0.0	49.26
B	2.1	0.1	52.58
C	1.64	0.56	77.58
D	1.06	1.14	70.77
E	0.15	2.0	47.44
F	0.00	2.2	48.35
G	1.1	0.0	43.36
SG-A	2.2	0.0	39.04
SG-D	1.06	1.14	52.36

Table 3.7: DC Gain values of the uniformly doped and GC DG and SG devices simulated at $V_{go} = 400$ mV.

nificant increase of ≈ 30 dB in A_{VO} compared to the uniformly doped DG devices. An obvious trend which is related also to the increase in the Early voltage in the last section is that an increase in the L_{LD}/L ratio increases the value of A_{VO} . Another observation is that between $L_{LD}/L = 0.255$ to $L_{LD}/L = 0.518$, there is no significant increase in the A_{VO} but remains constant, ≈ 65 dB. Again if $L_{LD}/L > 0.518$, this leads to a degradation of the A_{VO} due to the increase in SCE. From Table 3.7, the values of A_{VO} in saturation of the GCDG devices are much higher compared to the GCSG devices due to the DG structure. Figure 3.19

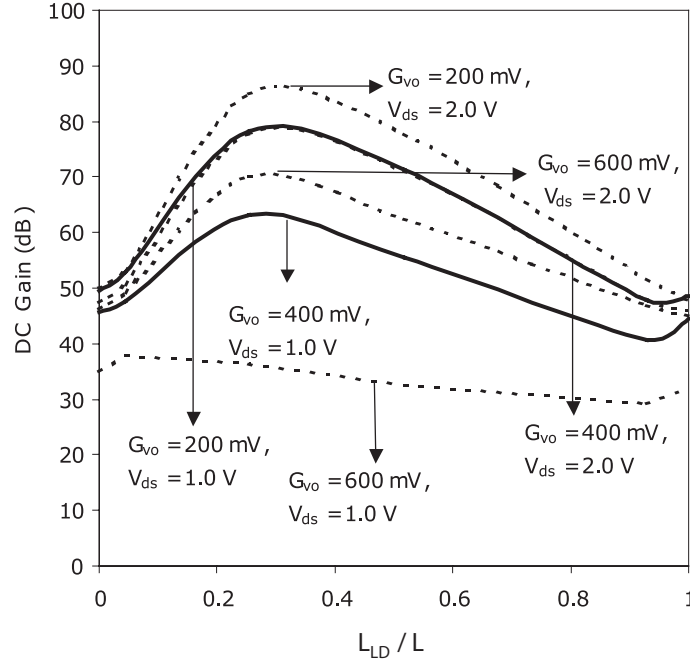


Figure 3.19: DC gain for the various GCDG and uniformly doped DG SOI MOSFETs extracted at various V_{go} and V_{ds} .

shows the DC gain for the various devices analyzed here with various L_{LD}/L ratio and various V_{go} and V_{ds} . The L_{LD}/L ratio of 0.3 gives the higher DC gain. If the L_{LD}/L ratio is kept constant, it is clear that the highest DC gain is obtained when the gate overdrive is around 200 mV above threshold and in saturation. In order to reduce the power dissipation for low voltage analog applications a low V_{go} and V_{ds} is preferred.

Such a requirement is achievable with the GCDG devices as seen in Figure 3.19 where A_{VO} values of up to 85 dB can be achieved. Figure 3.20 shows the dependence of the DC gain extracted at $V_{go} = 200$ mV with the variation of threshold voltage (V_{th}) which corresponds directly to the channel doping channel of the device for the various GCDG SOI MOSFETs. Figure 3.20, shows that higher difference in doping level

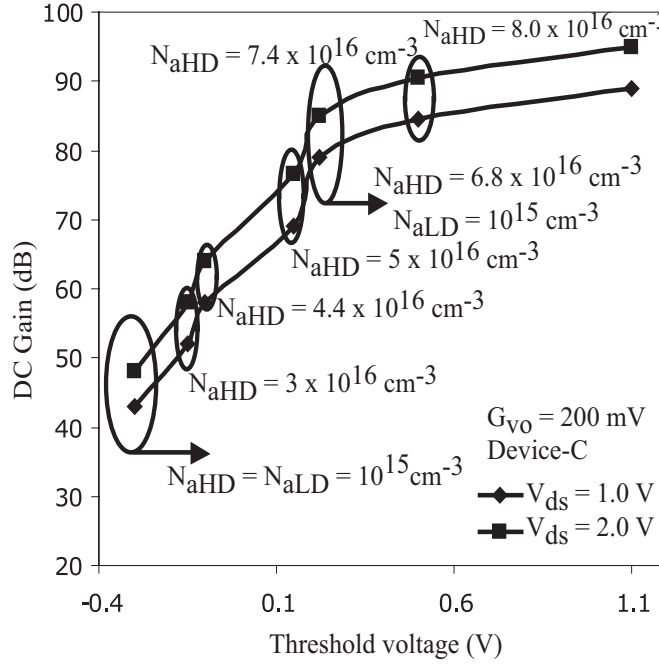


Figure 3.20: Dependence of the DC gain extracted at $V_{go} = 200$ mV with the variation of threshold voltage (V_{th}) for GCDG SOI MOSFETs with the low-doping concentration constant.

between the low and high-doped regions leads to higher Voltage Gain. V_{th} values of -0.3 V corresponds to a uniformly low-doped transistor while V_{th} of 0.6 or higher corresponds to a uniformly high-doped transistor and in between a V_{th} of around 0.2 V corresponds to a GCDG transistor (device C). It is clear that when V_{th} goes above 0.3 V, there is a small change in the DC gain obtained. Thus in order to benefit fully from this GC design and at the same time maintaining a higher DC gain, the difference between the low-doped region and the high-doped region

should be kept sufficiently high. However, one set-back on such a design is that the doping level on the high-doped region is limited to the power supply constraint. Another main observation from Figure 3.20 is that we noticed that after this doping that returns a threshold voltage of around 0.3 V, there is no major gain obtained from the device as the DC gain reaches saturation at both drain bias. This means that after this point, there is no major advantages with regards to the gain of the device, to further increase the doping in the high doped part of the GC architecture. It is also be predicted that increasing the doping of the device will also lead to a decrease in the transconductance of the device because of the decrease in the current drive.

From the basic concept of the SG OTA, it can be seen that if we want to obtain the same high values of A_{VO} of the GC devices, these SG devices need to be fabricated with channel lengths of more than an order of magnitude larger creating unrealistic frequency and die area limitations [PMF02] [ECF⁺96] [SFJ96]. These GC devices are seen as a cascade of series resistance with the combination of a normal high-doped SG and low-doped SG transistor in series. Such a combination will be able to reproduce the high A_{VO} values as seen in the GC devices.

3.4.6 Graded-Channel architecture: Physics

In general, all the improvements seen in the analog and digital parameters of the GC devices (SG and DG) are due to the architecture itself with the combination of the high-doped region and the low-doped region side by side. In this section, the internal physics of this architecture will be studied in the saturation region to understand deeper how it contributes to the outstanding results as seen in the GCDG and the GCSG SOI MOSFET devices.

Figure 3.21 shows the electric field of the device in both the doped and undoped region of the GCSG structure. It is clear that as V_{ds} increases, the effect of the electric field on the devices also increases. From this plot of the electric field, it is clear that for the GC structure, the effect in the electric field is limited to the intrinsic region while for the uniformly doped transistor, the effect in electric field is throughout the channel. This reduction in the electric field on the drain side for the GC architecture leads to a much better operational condition in the

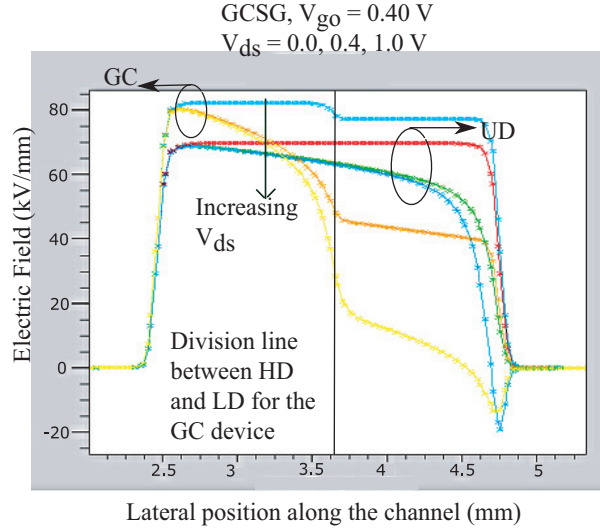


Figure 3.21: Cross section showing the vertical electric field in a GCSG and SG uniformly doped transistor biased at $V_{gs} = 0.6$ V and from $V_{ds} = 0$ V to $V_{ds} = 1.0$ V at silicon film depth = $0.01 \mu\text{m}$.

transistor due to a reduced charge sharing effects and a reduction in the impact ionization phenomenon.

Figure 3.22 shows the cross-section of a GC (SG/DG) and uniformly (SG/DG) doped SOI MOSFET device showing the potential distribution along the lateral position of the channel in the saturation region and $V_{go} = 400$ mV at depth = $0.01 \mu\text{m}$. The effect of the graded-channel architecture on the potential distribution can be clearly seen at $x=1.5 \mu\text{m}$ (GC) and $x=2.5 \mu\text{m}$ (UD).

It is clear that for GC architecture, the potential is not affected by the drain bias in the highly doped region which remains nearly unchanged, while that for the uniformly doped device, there is a change in potential as V_{ds} changes. This change in the uniformly doped device is due to the penetrating longitudinal electric field into the channel. Whereas for the GC device, this drop happens mainly in the low-doped region, leaving the high-doped region nearly unaffected by this change. This potential drop which is concentrated in the low doped region of the GC architecture contributes to the improvement seen in the saturation operation. This same change is also observed for the longitudinal electric

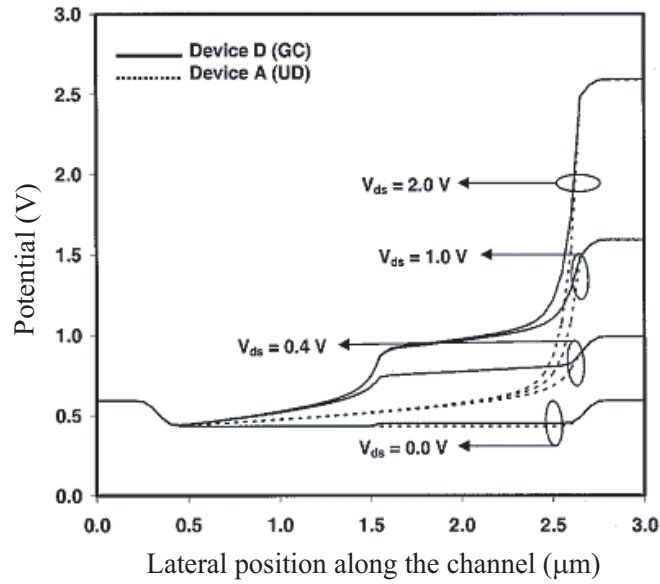


Figure 3.22: Cross-section of a GC architecture and uniformly doped (SG/DG) device showing the potential distribution along the lateral position of the channel in the saturation region and $V_{go} = 400 \text{ mV}$ at silicon film depth = $0.01 \mu\text{m}$. The effect of the graded-channel architecture on the potential distribution can be clearly seen at $x = 1.5 \mu\text{m}$ (GC) and $x = 2.5 \mu\text{m}$ (UD).

field along the channel. Figure 3.23, shows the variation in the longitudinal electric field of the GC and uniformly doped device for various V_{ds} and $V_{go} = 400$ mV. One of the main advantage of the GC architectures

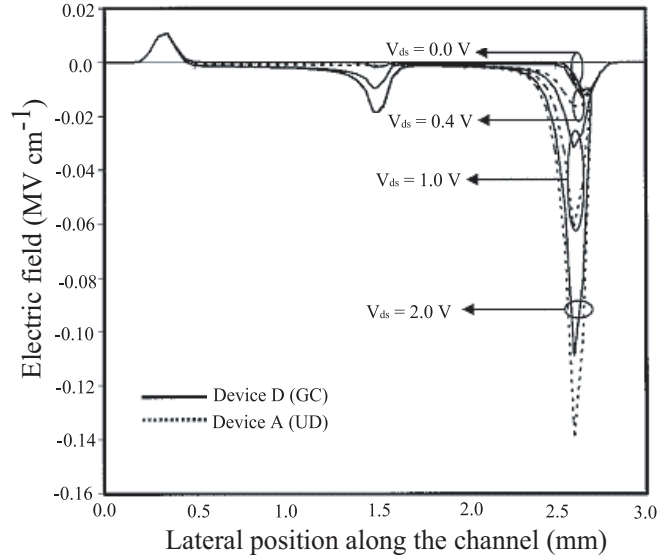


Figure 3.23: Cross-section of a GC (SG/DG) and uniformly doped (SG/DG) device showing the variation in the longitudinal electric field of the GC device for various V_{ds} and $V_{go} = 400$ mV at silicon film depth = $0.01 \mu\text{m}$.

on the electric field is that it modifies the channel potential distribution and this causes a reduction in the electric field. As a result of this reduction, there is a decrease in the impact ionization, hot carrier effects and the breakdown voltage effects. From Figure 3.23, on the interface between the low-doped and high-doped region, the electric field is higher (based on magnitude) for the GCDG architecture compared to the uniformly doped DG device at all bias of V_{ds} . This allows the reduction of the lateral electric field at the drain, which results in lower values of the output conductance leading to the much higher value of gain as observed. The reduction in the electric field is approximately 20 % in the GCDG compared to the uniformly doped DG device.

The concentration of electrons in a GC (SG/DG) and uniformly doped

(SG/DG) devices will obviously differ. In Figure 3.24, this electron concentration lateral distribution is shown for various V_{ds} and $V_{go} = 400$ mV. The horizontal dotted lines indicate the doping levels for the low and high-doped region, respectively. From Figure 3.24, it is clear that in

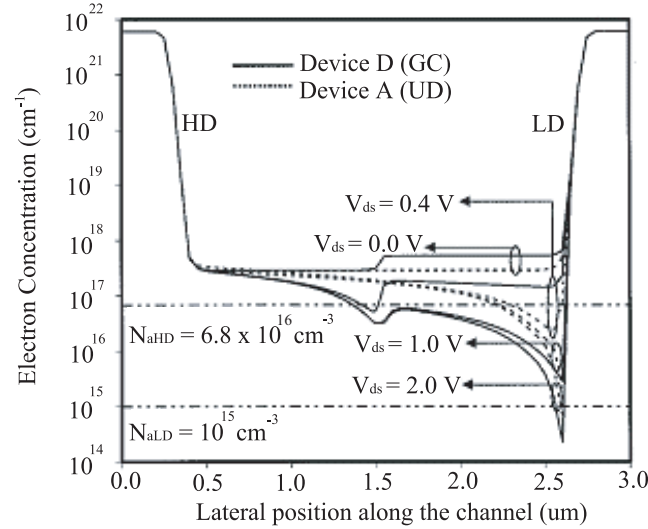


Figure 3.24: Cross-section of a GC and uniformly doped device showing the variation in the electron concentration lateral distribution is shown for various V_{ds} and $V_{go} = 400$ mV at silicon film depth = $0.01 \mu\text{m}$.

the high doped region of the GC devices, there are hardly any changes in its electron concentration for the various V_{ds} bias. Such a condition happens because all the potential drop happens in the low-doped region and thus leaving the high-doped region free from such a change in its electron concentration. Such a phenomenon contributes to the excellent DC gain as seen in the GCSG and GCDG devices. Such a condition does not happen in the GC structure leading to a smaller channel length modulation which improves the Early voltage values. From Figure 3.24, at $V_{ds} = 0$ V, in the GC device, the whole channel length is in inversion thus working in linear regime operation. As V_{ds} increases to 0.4 V, the electron concentration in the high-doped region falls below the $(N_a)_{HD}$ line indicating the beginning of a pinch off region. At this same bias,

the low-doped region is still in inversion. As V_{ds} increases further to 1.0 V, the high-doped region in the GC is further pinched off but the low-doped region is still in inversion. With a further increase in the V_{ds} to 2.0 V, the low-doped region experiences pinch off but in the high-doped region, no change is seen as all the voltage drop is limited only to the low-doped region. However, for the uniformly doped device, at this bias, the whole region experiences further pinch off. It is under such a condition where the high-doped region does not experience any further pinch off and where both the low-doped and high-doped region are in pinch off that such low values of output conductance is obtainable.

3.5 Conclusion

In this chapter, two different graded-channel architectures were presented, one on the single gate structure and the other on the double-gate structure. The graded-channel structure has shown that it is a unique structure in itself. This channel engineering gives an alternative for keeping the physical gate length long, but at the same time having a short effective channel length which leads to much better output conductance thus higher DC gain. The improvement in these parameters makes the graded-channel devices a promising device for application in low voltage analog applications. Another advantage of these structures is that they are fully compatible with the current CMOS process with just some small modification in the lithography mask.

We have shown that both the analytical model and numerical simulation fit well with the experimental results which is a good indication because this would be an useful tool for designing and optimization of these novel devices for future applications/predictions.

It is clear that the GC architecture is an interesting architecture with respect to analog performances. We have shown that with the GC architecture, we can achieve higher Early voltage due to the lower impact of the drain in saturation on the channel. The transconductance values are increased due to the reduction of influences from the drain. This combination results in a generally higher Voltage Gain of the device. The various influences from the drain in saturation with respect to the potential, electric field and electron at various drain bias have shown

the principle behind the GC architecture to obtain the various improvements in the figure of merits.

The advantages of using the GC architecture have been proven with long channel MOS devices. From the results obtained, it is interesting to apply it for high performance low-power applications such as implementing it as associated electronics for MEMS applications.

We have also seen that the combination of the graded-channel and the double-gate architecture brings even more exciting analog and digital characteristics. The double-gate structure will be analyzed further in the next chapter. However, such a double-gate architecture fabricated using the silicon-island etching method is limited to a width to length ratio (W/L) of approximately 1. It is also expected that as the technology nodes reduces in the future years, problems will arise in the fabrication of the GC architecture. Some of the expected problems would be related to the alignment of the mask for implantation, the different L_{HD}/L ratios would be limited, etc. These limitations will be valid for both SG and DG architectures. In order to increase the flexibility of the W/L ratio, another method of fabrication of the planar double-gate architecture will be studied in the Chapter 4.

Chapter 4

Planar Double-Gate SOI MOSFET with prepatterned cavities

4.1 Introduction

The interest in the fabrication of planar Double-Gate (DG) devices is related to their superior electrical characteristics, such as significantly reduced short channel effects (SCE) compared to Single-Gate (SG) transistors. The superior electrical characteristics of DG compared to their SG counterpart originate from their better electrostatic control on the channel carriers by the increase of the gate area. For DG structures characterized by a thin active silicon channel their electrical performance are even further improved thanks to the well known volume inversion (VI) phenomenon present in thin DG structures under appropriate bias conditions [KCFR04].

Earlier, planar DG Silicon-on-Insulator (SOI) Metal Oxide Semiconductor (MOS) devices have been fabricated by chemically etching the buried oxide (BOX) to form a silicon bridge [Col02] following the well known Gate-All-Around (GAA) method. However, a major drawback of this technique is the limitation of the width to gate length (W/L) ratio to a value close to 1.

In order to overcome this problem, fabrication of planar DG transistors by wafer bonding have been proposed [VPW⁺05a] [GSZ⁺01].

Basically, a single gate SOI MOSFET is fabricated and flipped over a handle wafer, the silicon substrate of the SOI wafer as well as the BOX are removed to reach the silicon channel for aligning and depositing the gate stack of the second gate (top gate). However, such process does not solve the problems of gate misalignment as well as the possible difference in gate oxide properties between the bottom and top gates. Indeed, due to the change in the fabrication environment, there is a high probability that the thickness of the gate oxide of second gate will differ from the thickness of the firstly built gate leading to an asymmetrical device characterized by lower electrical performance. The misalignment between the top and bottom gate leads to uncontrolled part of the channel and increase of the overlap parasitic capacitances. It is worth noting that in the case of GAA, there is also an excess of overlap capacitance related to the isotropic underetch of the BOX below the source and drain regions. We propose here a new approach for the definition of top and bottom gates with well defined dimensions. The main advantages of our method are a) the flexibility to fabricate other devices such as the Silicon-on-Nothing (SON) transistors with the same process on the same wafer, b) the ability to form separate control for the top and bottom gate if needed c) the W/L ratio flexibility, d) simultaneous formation of both gate stacks (symmetrical DG devices), e) the ability to fabricate SG and DG devices on the same process and wafer and f) ability to fabricate various other devices such as the quadruple-gate structure with the combination of e-beam lithography.

4.2 Planar double-gate MOSFET fabrication techniques

4.2.1 Gate-All-Around by isotropic etch of buried oxide

Double-gate devices manufactured through this method is very similar to the normal CMOS fabrication method. With this method, the only difference is an additional use of a mask and a wet etch step [Col97]. The first step in this method is the formation of silicon islands which are the active areas. This is followed by a local oxidation step to form

rounded edges. In order to form the silicon bridges, a mask is introduced which covers all areas except these silicon bridges. With the protection of the resist, the wafer is immersed in buffered hydrofluoric acid (BHF) to etch the buried oxide to form the silicon bridge. After this step, the device will have a silicon bridge with its extremities as the support. These extremities are transformed later to the drain and source. After this step, the wafer goes through the normal CMOS process with the formation of the gate oxide, the doping of the channel, the deposition of the polysilicon to form the gate and formation of the drain and source finishing off with the formation of the contact vias and metal pads. Figure 4.1 shows this GAA process by isotropic etching of buried oxide.

This fabrication method was keenly explored by J.-P. Colinge [Col97] which was also used in the fabrication of the GCDG devices discussed in the previous chapter.

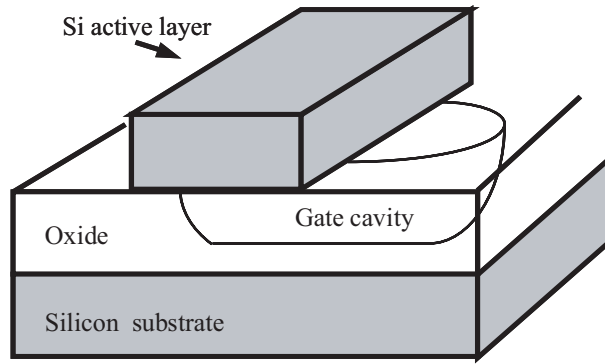
However, this fabrication technique has its own disadvantages. One of the main disadvantage is its limitation of the achievable width to channel length (W/L) ratio. This limitation of the ratio is due to the isotropic etching to form the cavities. Another disadvantage of this fabrication technique is the overlap capacitances between the bottom gate and the source and drain regions. Indeed, due to a classical overetch of the buried cavity the deposited bottom gate is often larger than the top gate.

4.2.2 CEA-LETI wafer bonding

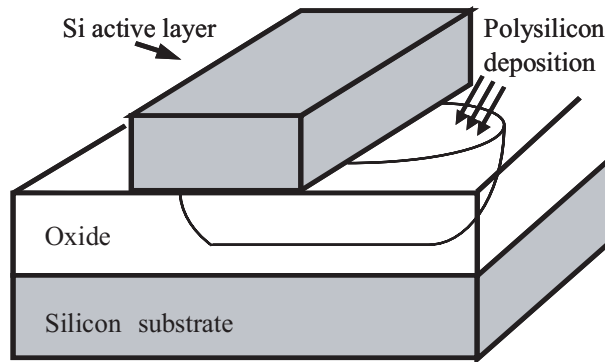
In this fabrication developed by CEA-LETI [VPW⁺04] [VPW⁺05b], the fabrication of the double-gate architecture is based on the wafer bonding technology. Within this technology, CEA-LETI has introduced two different method, a non-self-aligned and a self-aligned process.

4.2.2.1 Non-self-aligned double-gate wafer bonding process

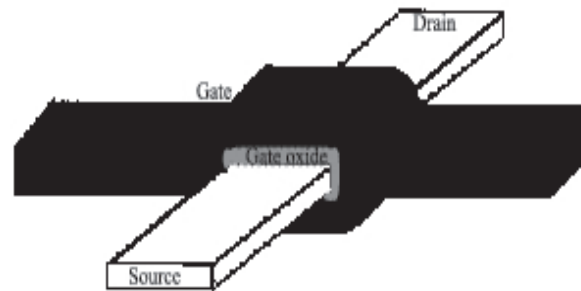
In this method [Vin05], the backgate/second gate is first fabricated on a SOI wafer. After this, an oxidized bulk wafer is bonded to the SOI wafer and the handle wafer and buried oxide of the SOI wafer are etched away. This leaves behind the silicon of the SOI wafer. After this, the



(a)



(b)



(c)

Figure 4.1: Schematic figure illustrating the GAA formation by (a) isotropically etching the buried oxide to form a silicon bridge, (b) schematic drawing showing where polysilicon will be deposited and (c) 3-D view of the final device.

conventional CMOS process is carried out to form the front gate on this revealed silicon layer and the formation of the drain and source and the completion of the fabrication process. Figure 4.2 shows the main steps of this process.

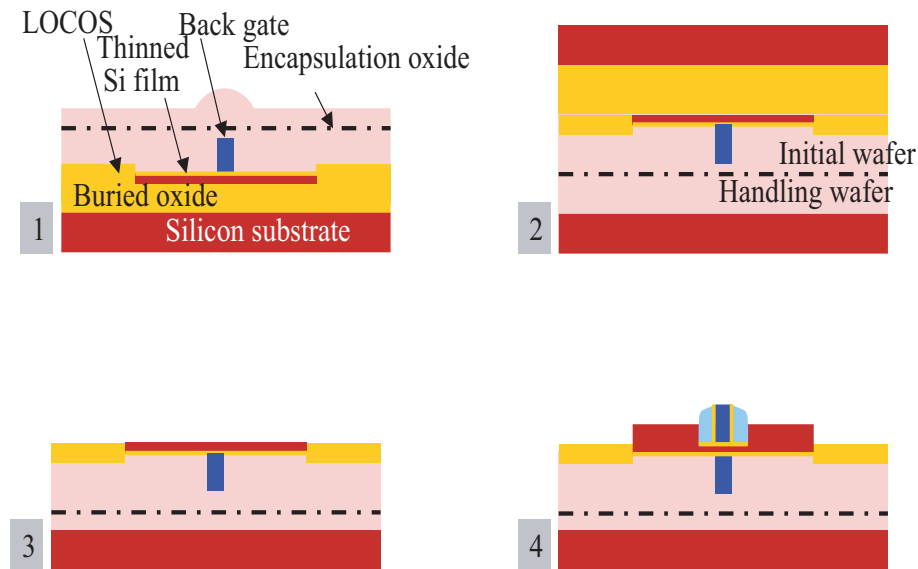


Figure 4.2: The various steps in the non-self-aligned wafer bonding process by LETI-CEA: (1) Formation of the back-gate/second gate of the double-gate, (2) Flipping of the initial wafer and bonding of the wafer to a oxidized bulk wafer, (3) Removal of the handling wafer and oxide of the SOI wafer, (4) Formation of the rest of the device following the conventional CMOS process [Vin05].

In this method, one of the main setback is the possible formation of asymmetrical gate oxide thicknesses due to the fact that both gates are not built simultaneously. Such a problem can happen because of the variations in the process conditions. Another foreseeable problem is the misalignment of the gates. Indeed, due to the change in the fabrication

environment, there is a high probability that the thickness of the gate oxide of second gate will differ from the thickness of the first built gate leading to an asymmetrical device resulting in reduced electrical performances. The misalignment between the top and bottom gates, leads to uncontrolled part of the channel and increase of the overlap parasitic capacitances. It is worth noting that in the case of the GAA, there is also an excess of overlap capacitance related to the isotropical underetch of the BOX below the source and drain regions. Figure 4.3 shows a SEM example of the double-gate architecture fabricated by the CEA-LETI non-self-aligned wafer bonding process.

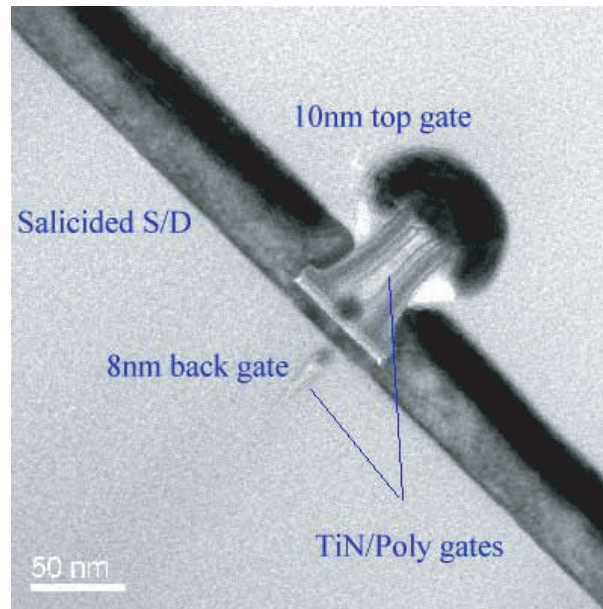


Figure 4.3: SEM example of a double-gate transistor fabricated using the non-self-aligned wafer bonding CEA-Leti process. [Vin05].

4.2.2.2 Self-aligned double-gate wafer bonding process

In this self-aligned double-gate wafer bonding method [VPW⁺05a], the advantage over the non-self-aligned method is that here only one lithography is needed to design the top and bottom gates. The back-gate lay-

ers are first deposited to form a blanket stack. This is followed by the bonding process of this stack to an oxidized bulk wafer. After this, the top gate stack is deposited with an extension implantation and spacer etching. This is followed by an etching process along the sides to allow the access to the back-gate. This is followed by another etching step and undercut. The source and drain are formed due to the existence of the silicon sidewalls. Figure 4.4 shows the various steps in the self-aligned double-gate wafer bonding process.

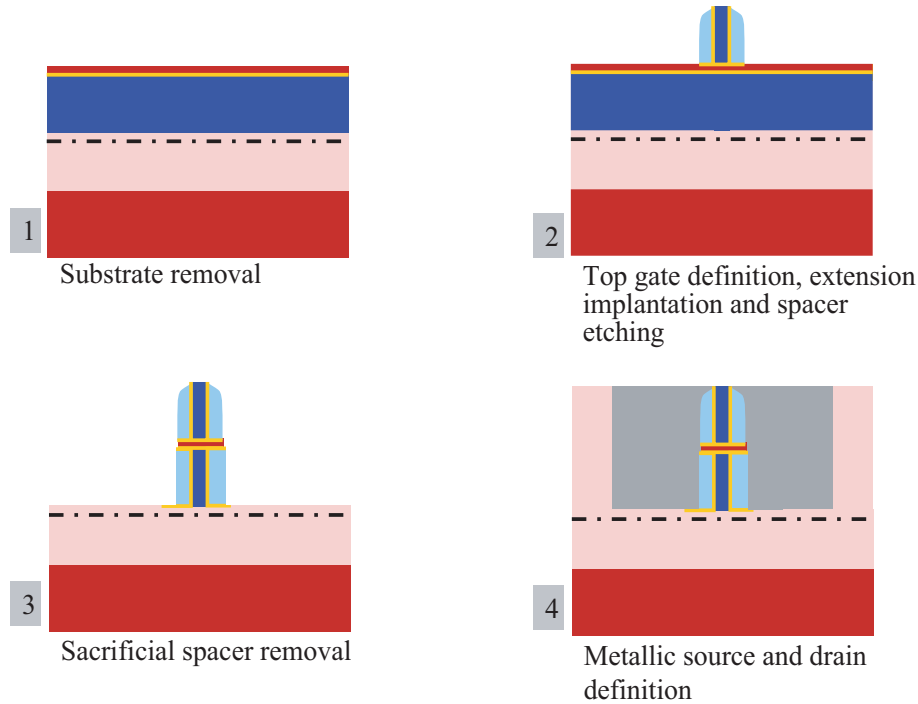


Figure 4.4: The various steps in the non-self-aligned wafer bonding process by LETI-CEA: (1) Bonding of the oxidized bulk wafer to the blanket stack, (2) Formation of the top gate above the back-gate stack with extension implantation and spacer definition, (3) Etching process along the sides to allow the access to the back-gate, (4) Formation of the source and drain (metallic) thanks to the existence of the silicon sidewalls [Vin05].

This self-aligned wafer bonding process to form planar double-gate is an improvement in the non-self-aligned process. However, experimental results showed (i) the difficulty to control the undercut of the back-gate formation (ii) the gates are still fabricated separately and (iii) the poor quality of sidewall which affects the source/drain formation. Figure 4.5 shows a SEM example of the double-gate architecture fabricated by the CEA-LETI self-aligned wafer bonding process.

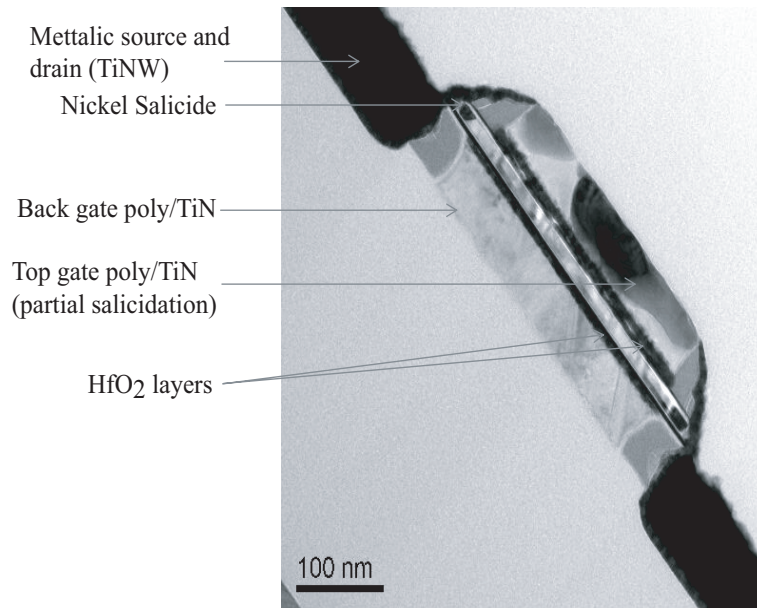


Figure 4.5: SEM example of a double-gate transistor fabricated using the self-aligned wafer bonding CEA-LETI process. [Vin05].

4.2.3 Double-gate devices fabricated based on the Silicon-on-Nothing device

ST Microelectronics has shown that the planar double-gate device can be fabricated using the Silicon-on-Nothing fabrication technique. The main fabrication step to form a Silicon-on-Nothing device is explained later in this chapter. The alteration to the conventional SON fabrication is before the formation of the gate, the silicon germanium is selectively

etched away. This is followed by a deposition of a thin gate oxide followed by the deposition of the in-situ doped polysilicon gate all around the silicon bridge [HCL⁺03]. This is followed by the rest of the CMOS process steps. Figure 4.6 shows the final device formed with this process. The fabrication of planar double-gate devices based on the SON

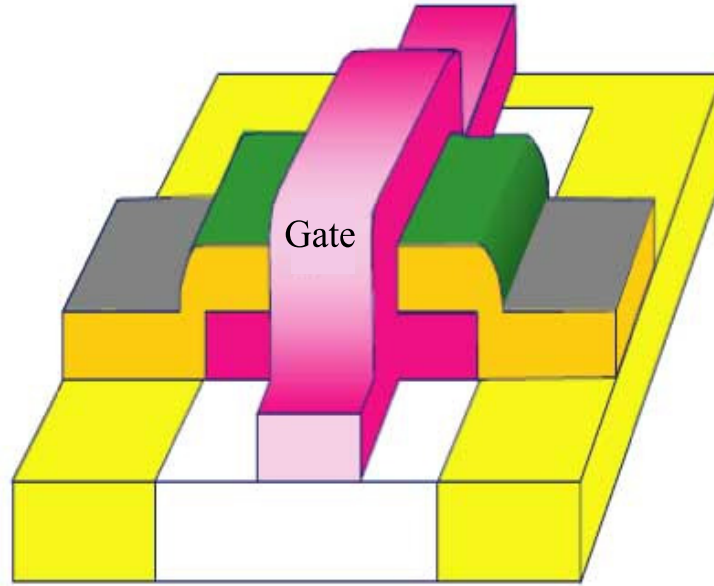


Figure 4.6: 3-D view of the planar double-gate formed using the Silicon-on-Nothing process [HCL⁺03].

technique have nearly the same related parasitic capacitances problem as seen in the Gate-All-Around method.

4.3 Double-gate fabrication with prepatterned cavities and wafer bonding

Fabrication of double-gate devices with wafer bonding has been done before [TSHS94]. However, fabrication of double-gate transistors using the wafer bonding method remains difficult since the bonding process is critical to achieve high quality surfaces. Such a procedure becomes even more difficult as the silicon film required gets thinner.

The wafer bonding method offers some excellent advantages over the Gate-All-Around method. Some of the main advantages are that we can have different W/L ratios, thus giving flexibility to the various dimensions desired for the devices. Different sorts of devices such as the Silicon-on-Nothing (SON) transistor can easily be fabricated with some slight adjustments to the lithographic mask and with the combination of e-beam lithography, quadruple-gate devices can also be realized.

The principle of the fabrication process of DG structures proposed here is the transfer of a high quality thin silicon layer onto a thermally oxidized bulk silicon wafer containing dry etched cavities into the oxide layer. These cavities will be used to form the back gate. The fabrication process can be divided into two sections, the preprocess and the standard CMOS process. The preprocessing is the section where the bulk and the SOI wafers are joined to form the starting wafer for the next main process. In this preprocessing, the cavities for the second gate are prepared using a lithography mask. This preprocessing step is the most important part of the process because it influences the final outcome of every step in the future standard CMOS process. Another advantage of this wafer bonding process is that there are no additional steps needed in the CMOS process to fabricate the planar double-gate devices using this method. In this section, attention will be given only to the preprocessing part as it is the most crucial part to obtain a good working device.

In the preprocess, the first step is the preparation of the bulk handling wafer and of the SOI wafer. This is followed by the formation of an oxide layer (which later becomes the new buried oxide) on the bulk wafer by thermal oxidation, then by the lithography step to form the gate cavities which will become the bottom gate. The cavities are formed by a SF_6 based RIE plasma recipe. Figure 4.7 shows the two starting wafers and the formation of the gate cavities.

Next, the bulk and the SOI wafer are bonded together. Before this bonding process, the silicon bulk and the SOI wafer surfaces to be bonded are activated. After this bonding process, the wafers are annealed to strengthen the bond between the two wafers and to dissipate any remaining water. This annealing process is performed in a high temperature environment for a long period of time. Figure 4.8 shows the activation and bonding process and the final bonded wafers.

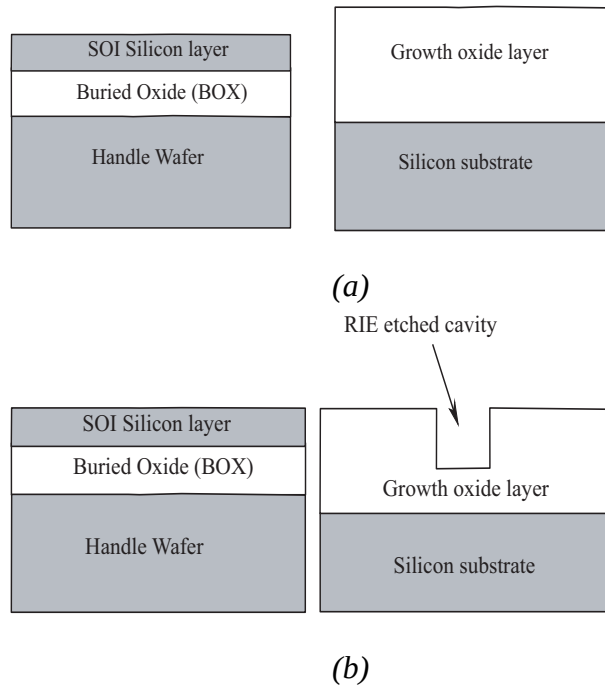
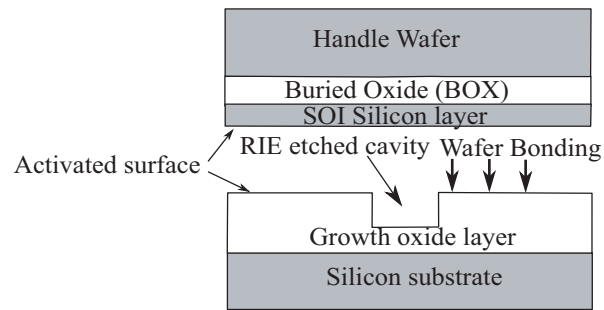
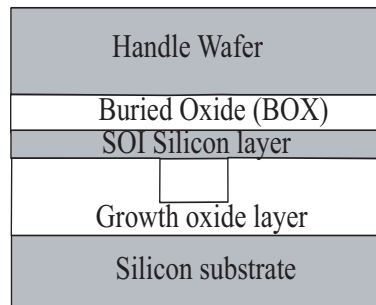


Figure 4.7: (a) Starting bulk wafer with thermally grown oxide and SOI wafer, (b) Bulk wafer with etched cavities



(a)



(b)

Figure 4.8: (a) Activated bulk and SOI wafers before bonding, (b) Bonded wafers

After the annealing process, the handle wafer of the SOI wafer is removed with mechanical grinding. The majority of this silicon layer is removed, leaving just a few microns. Following this grinding process, a nitride layer using a LPCVD deposition is deposited to form a protection layer. This protection layer is important for the next step because it protects the bonded interface on the wafer and edges from any possible underetch by the TMAH solution along the bonding interface. The nitride layer deposited on the silicon surface that will be etched with TMAH in the next step is removed by plasma etching using CHF_3 . The remaining few last microns of the silicon is removed in a 10% TMAH solution at 90°C. These two process are shown in Figure 4.9.

After the complete removal of the silicon layer, the BOX of the SOI wafer is chemically etch away using buffered hydrofluoric acid (BHF) solution. The wafer is dipped into the BHF solution for about 10 minutes depending on the thickness of the buried oxide and concentration of BHF used. Due to the hydrophobic properties of the BHF solution with silicon, this is used as an indication that all the buried oxide has been removed. After the removal of this BOX layer, the wafer is ready for the CMOS process which also represents the end of the preprocess. Figure 4.10 shows the wafer before the BOX removal and the final wafer from the preprocessing stage.

Figure 4.11 shows the final devices, with a longitudinal cross-section and a transversal cross-section of the final device after the CMOS process. Figure 4.12 shows an example of a device fabricated with the wafer bonding over prepatterned cavities as seen under the microscope.

4.4 Critical points

Several critical points have been identified in the fabrication of this particular planar double-gate architecture in both the preprocessing and main CMOS process. It is necessary for these points to be addressed in order to obtain a good working device.

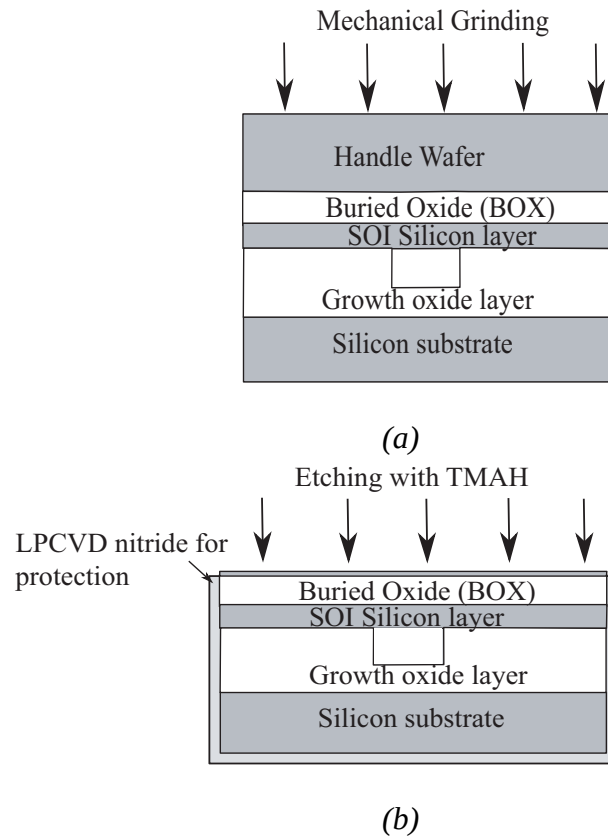


Figure 4.9: (a) Grinding of the silicon of the handle wafer, (b) LPCVD nitride deposition and removal of silicon with TMAH solution.

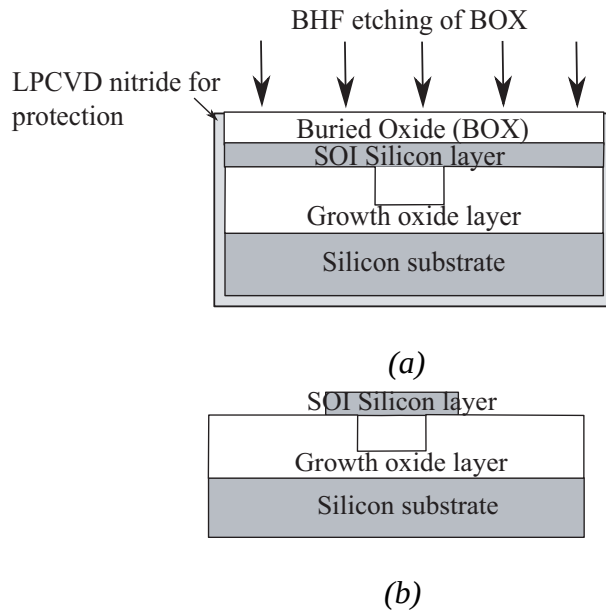


Figure 4.10: (a) Removal of BOX with buffered hydrofluoric acid, (b) Final wafer from the preprocessing steps.

4.4.1 Surface activation

The activation of the bulk and the SOI wafers surfaces prior to bonding is one of the most important process steps where care is needed. As described in [OZB⁺05] [LG01] and [HG03], the common requirements of wafer bonding deals mainly with the surface roughness and the surface cleanliness. The main purpose is to make a thin film transfer (including membranes) over patterned cavities, to achieve this, two points are critical: to achieve a maximum effective transfer area and to maintain the integrity of the small membranes that will be the future transistors channels. In the context of surface roughness, from measurements performed, it has been shown that the measured RMS (Root Mean Squared) roughness for both the oxidized surface and the SOI surface is around 1 angstrom on a $1 \mu m^2$ AFM (Atomic Force Microscopy) scan area. This value obtained is low enough that it poses no further concern to the process. The next criteria is the cleanliness of the surface from contaminants. These contaminants can act as growth

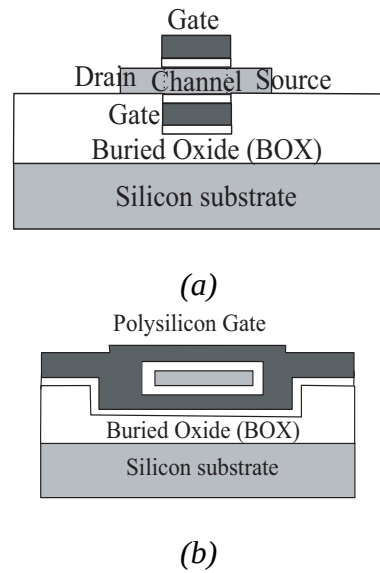


Figure 4.11: (a) Longitudinal cross-section of the final double-gate architecture, (b) Transversal cross-section of the final double-gate architecture.

nucleus for stress propagation which can lead to reduction in the bonding energy and cracking of the wafer during subsequent processing. In order to reduce such a problem, the wafers were cleaned twice in a Pirhana-like solution ($H_2SO_4:H_2O_2 = 5:2$) at $110^\circ C$ during 10 minutes followed by 10 minutes of rinsing in deionized water (D.I.). In our process, we have used warm acid nitric with a concentration of 70%. This step is important because it involves two main chemical reactions for the bonding of the wafers. The presence of the silanol groups (Si-OH) formed from the reaction will be converted to hydrogen bonds which is much stronger than only the Van der Waals force [OZB⁺05]. Another advantage of using this solution is that it can also remove organic residuals on the surface. This is important because it reduces the presence of particles which can cause the formation of bubbles and stress points which can significantly reduce the surface energy and yield area. One more advantage of this acid nitric solution is its 'softness' reaction on the surface, thus it does not destroy or in anyway disturb or destroy the crystalline structure of the silicon layer. In order to maintain the in-

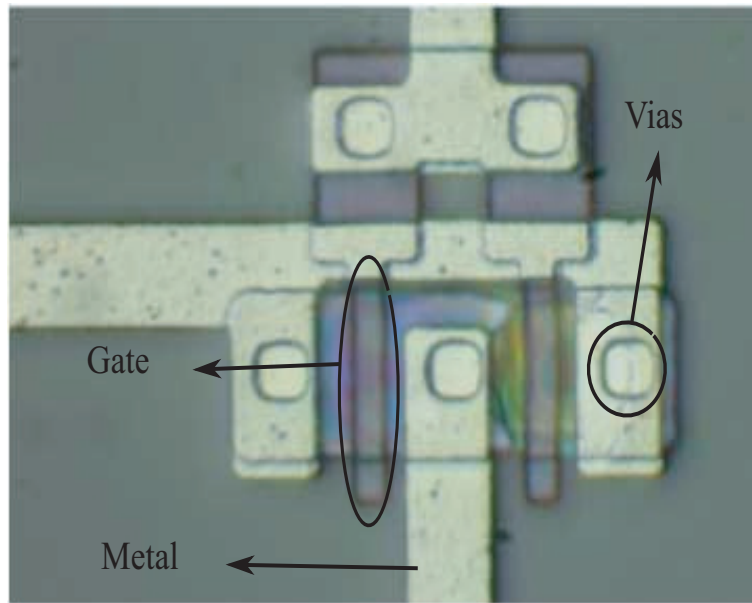
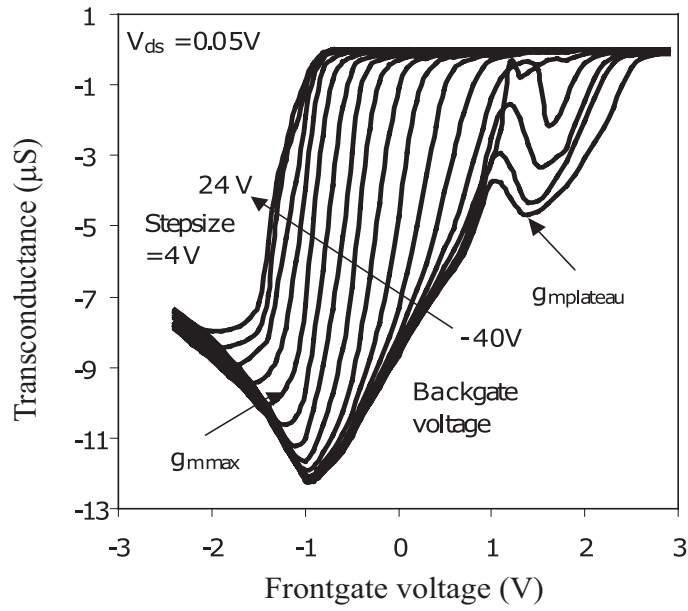


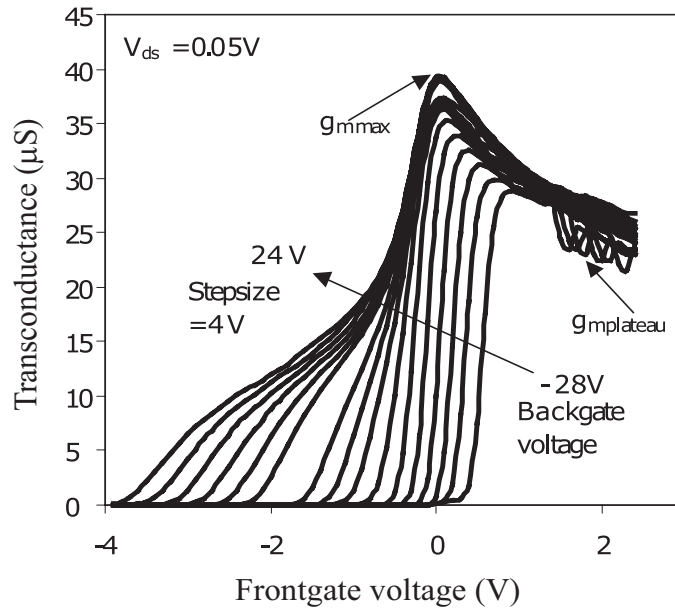
Figure 4.12: *Example of a DG MOSFET transistor fabricated by the wafer bonding over prepatterned wafer technique as seen under the microscope.*

tegrity of the cavities during the future steps, the wafers are outgassed completely before being bonded. This operation is important because it reduces as much as possible the by-products of the bonding reaction and hence it reduces the pressure inside the cavities to a value as low as possible. The bonding is performed using a mask aligner at room temperature and atmospheric pressure. Different types of surface activation is applied for different materials. Normally for oxide surfaces, oxygen plasma surface engineering is performed. This oxygen plasma activation is used because it has been proven to be an effective method to increase the surface energy of the bonding surface. It is advantageous as it is a dry process which reduces any chances of contamination and eliminates stiction problem [OZB⁺05]. As for the active silicon on the SOI wafer, the activation was performed using warm acid nitric because in previous attempts, it was shown that if oxygen plasma was used, this will destroy the surface.

In previous tests, it has been shown that if the surface activation is performed with plasma oxide on the silicon layer, damage to the crystalline structure happens. This damage is detrimental to the working performance of the double-gate transistor because the carriers mobility at the bottom gate is reduced or completely destroyed making the action of the double-gate useless. Indeed, the plasma activation introduces extra defects which results to a reduced carriers mobility. Figure 4.13 shows the extraction of the mobility at the top (μ_1) and bottom (μ_2) gate interfaces from several SG devices for which plasma oxidation on both surfaces was applied. In this process, the surface of the SOI silicon wafer was damaged leading to a decrease in the mobility and increase of surface states density. The mobility was extracted from wafer bonded SG transistors with 2 different doping, one with n^+-i-n^+ device and the other with a $p^+-p_{12}-p^+$ doping. The 'i' doping refers to an undoped device and the ' p_{12} ' doping is a boron doping of approximately 10^{11} cm^{-2} . The mobility of the device can be extracted by considering the maximum transconductance at either the front or the back gate under depletion bias condition. Table 4.1 shows the extracted mobility from the front (μ_1) and the back surface (μ_2). The mobility for the n^+-i-n^+ device was extracted using Equation 4.1:



(a)



(b)

Figure 4.13: (a) Transconductance of a wafer bonded SG $n^+ - i - n^+$ device with the related maximum transconductance value. (b) Transconductance of a wafer bonded SG $p^+ - p_{12} - p^+$ device with the related maximum transconductance value.

Mobility	n^+-i-n^+	$p^+-p_{12}-p^+$
$\mu_1 (cm^2V^{-1}s^{-1})$	930	265
$\mu_2 (cm^2V^{-1}s^{-1})$	440	256

Table 4.1: Estimation of charge carriers mobility extracted from the front and back surfaces of the different wafer bonded SG MOS transistors.

$$\mu_X = \frac{g_{mXmax} \times L}{W \times V_D \times C_{oxX}} \quad (4.1)$$

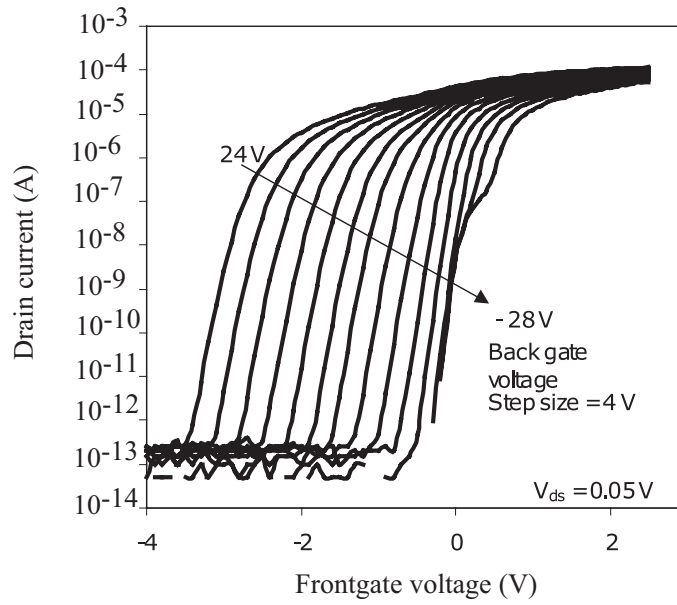
X represents the surface at which the carrier mobility is extracted, if it is the front surface, the capacitance taken would be the gate oxide capacitance with the related maximum transconductance. If the back channel charge carrier mobility is extracted, the corresponding maximum transconductance is used with the capacitance of the buried oxide.

However, for the $p^+-p_{12}-p^+$ device, the expression for the extraction of the mobility at the back channel is a bit different compared to the n^+-i-n^+ device due to the existence of the 'plateau' transconductance. Equation 4.2 shows the expression used for this particular back channel extraction.

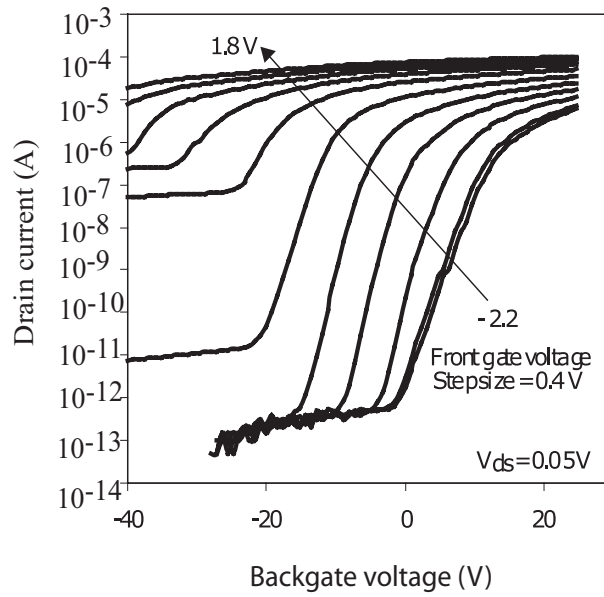
$$\mu_2 = \mu_1 \frac{g_{mplateau}}{g_{mmax}} \left(1 + \frac{C_{Si}}{C_{ox1}} + \frac{C_{it1}}{C_{ox1}} \right) \quad (4.2)$$

In equation 4.2, the gate oxide/silicon film interface surface state capacitance, C_{it1} is neglected to obtain a minimal estimation of the back channel mobility.

Another method to check the quality of the activation and its effects on the surface behavior, is by extracting the surface trap density. The extraction of the surface trap density can be easily obtained by first extracting the subthreshold slope of the device in depletion mode. In devices for which the surfaces have not been activated correctly, this will result in an increase in the surface trap density (typical values are normally around $10^{10} - 10^{11} eV^{-1} cm^{-2}$).



(a)



(b)

Figure 4.14: (a) I_{ds} - V_{gs} of a n^+ - i - n^+ device with the back gate ramped. (b) I_{ds} - V_{bs} of a n^+ - i - n^+ device with the front gate ramped.

Figure 4.14 shows the I_{ds} - V_{gs} and I_{ds} - V_{bs} curves extracted at $V_{ds} = 0.05$ V for various back and front gate voltages correspondingly. Equation 4.3 shows the expression used for the extraction of the surface trap density for the front and back channel in the depletion mode.

$$S = \frac{dV_{G1}}{d\log(I_{ds})} = \frac{kT}{q} \ln(10) \left[\left(1 + \frac{C_{it1}}{C_{ox1}} + \frac{C_{Si}}{C_{ox1}} - \frac{\frac{C_{Si}}{C_{ox2}} \cdot \frac{C_{Si}}{C_{ox1}}}{\left(1 + \frac{C_{it2}}{C_{ox2}} + \frac{C_{Si}}{C_{ox2}} \right)} \right) \right] \quad (4.3)$$

From Equation 4.3 [Lyu93], the interface capacitance, C_{it} can be extracted and this value can be inserted into equation 4.4 which will produce the final extracted surface trap density, D_{it} .

$$D_{it} = \frac{C_{it}}{q} \quad (4.4)$$

In Equation 4.4, q is the electronic charge. From Equations 4.3 and 4.4, the surface trap density extracted from the n^+ -i- n^+ are approximately $2.43 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ for the front surface and $1.65 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$ for the back surface. From these approximations of the surface trap density for both the front and back surfaces, it is clear that there is an increase in the surface trap density at the back surface which results in a degradation of the carriers mobility.

Figure 4.15 shows the I_{ds} - V_{gs} curve for DG devices that were fabricated with the interface between the silicon and the second gate oxide layer destroyed by harsh activation process (plasma oxidation). This shows the importance of having the right activation step in order to avoid such problems.

From Figure 4.15, we see that the DG transistors with the interface between the silicon and the second gate oxide layer destroyed by harsh activation process is not able to achieve doubled level of current as expected theoretically compared to the SG device.

It is thus clear here that if the activation process is not optimized or not carried out with care, the gate interface quality and then the carriers mobility will deteriorate leading to poor electrical characteristics.

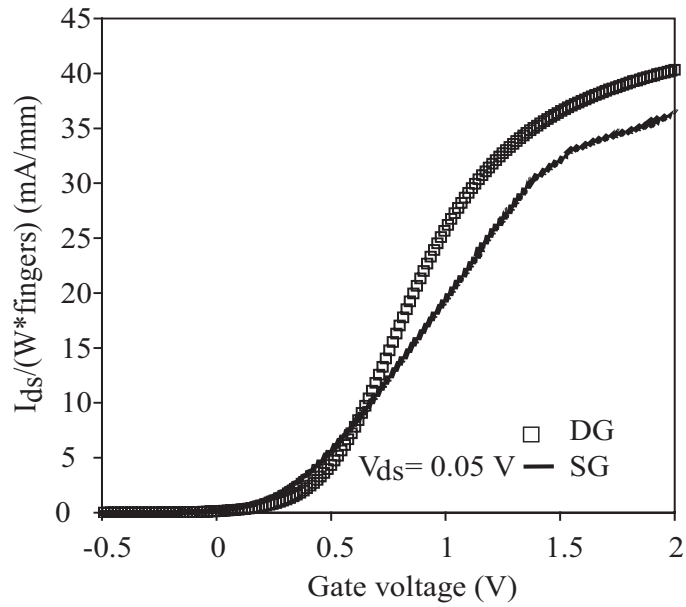


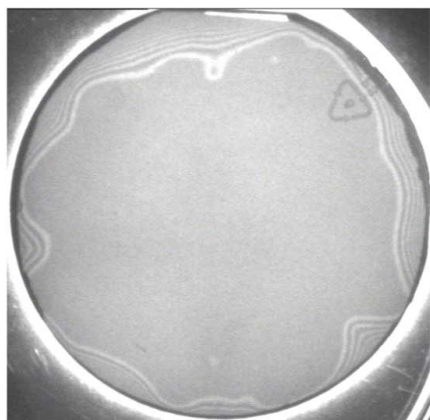
Figure 4.15: I_{ds} - V_{gs} curves for a DG and SG devices that were fabricated with the interface between the silicon and the second gate oxide layer destroyed by harsh activation process compared to a SG device extracted at a drain bias of 50 mV.

4.4.2 Annealing

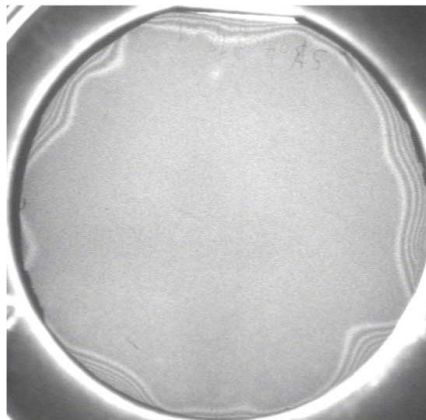
The annealing process is another important step in the wafer bonding process. A thermal annealing is needed after the bonding to complete the chemical bonding reactions and thus strengthen the surface energy. Annealing is also used as a tool for the release of excess moisture which can transform into unnecessary excess stress points which weakens the bonding. If the annealing temperature is too low, this can lead to an incomplete and insufficient for the completeness of the chemical reaction and removal of all the moisture. If the temperature is too high, this can also cause problems such as thermal stress. The time for the annealing is also important as it also determines the final bonding energy between the two wafers. In order to maximize the by-products diffusion through the interface and in order to partly consume them by silicon oxidation, the wafers were annealed at 1000 ° for 20 hours in a nitrogen induced atmosphere. Figure 4.16 shows some of the effects of the annealing to the bonding.

As seen in Figure 4.16, it is clear that the annealing process increases the bonded area and reduces the presence of the bubbles. The present of these bubbles are critical because they can act as stress initiation points which can spread with consecutively processing steps and can lead to the wafers cracking unexpectedly.

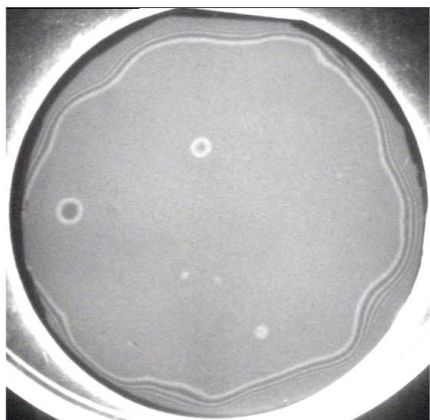
The removal of extra moisture and gas is also important because if not removed, they form a bubble and this bubble will eventually spread. Areas where these bubbles are present are useless because when the gate cavities are filled with polysilicon, the polysilicon will be present in the bubble cavities leading an increase of parasitic capacitance so high that the device becomes useless. If these bubbles are large enough to cover a large area, the polysilicon filling will act as an interconnect between the devices creating a short circuit between them. Thus, it is evident that the removal of these bubbles or the reduction of their presence is important. Figure 4.17 shows the end effect of the bubbles on a complete fabricated wafer.



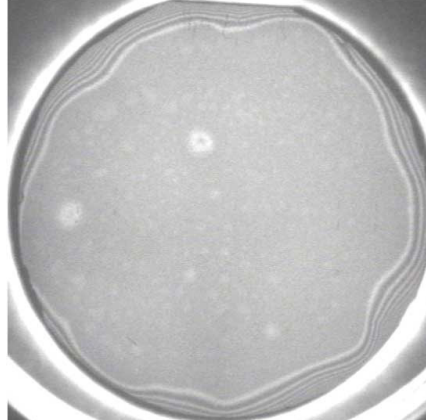
(i)



(ii)



(i)



(ii)

Figure 4.16: (i) Before annealing, (ii) After annealing.

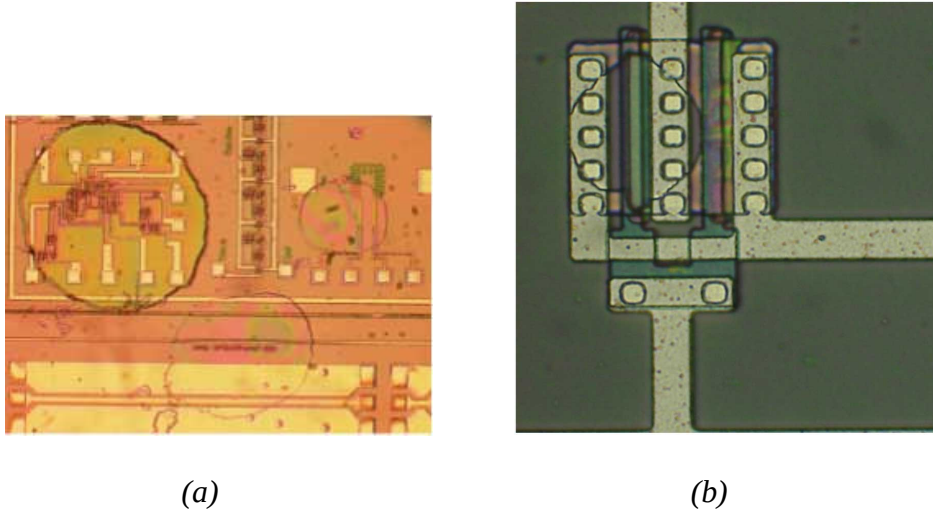


Figure 4.17: (a) *Effect of bubbles on a wafer*, (b) *Effect of bubbles on the DG transistor*.

4.4.3 Cleanliness

The environment where the bonding is performed and the cleanliness of the surfaces before bonding is a very important criteria. Particles presence on the surface of the wafer act as stress points and can lead to significant reduction in the surface energy and yield of the final product. This can be very detrimental to the post treatment of the bonded wafer. These dust particles form a concentration point of stress which becomes non-uniformly distributed stress that leads to the destruction of the wafer at the interface during the thermal processes.

4.4.4 TMAH etching

Tetra methyl ammonium hydroxide (TMAH) etching is used for the removal of thin silicon film. It is a selective etching process where only silicon based materials are etched. However, due to its harsh etching action on silicon material, this sort of etching can be dangerous to the bonded interface. In order to prevent the silicon material at the interface from being etched, the bonded wafers are encapsulated with a layer of nitride with a low pressure chemical vapor deposition process. As

would be expected, such a layer cannot provide a complete protection from the etching effect of the TMAH solution due to problems such as non-uniformly deposition or present of voids in the deposition where the TMAH can underetch the silicon at the bonded interface. However, the deposition of the nitride layer cannot be too thick to prevent stress on the whole bonded structure. Thus, it is vital that etching of the silicon film with the TMAH solution is done with care.

4.4.5 Chemical vapor deposition of Polysilicon into buried cavities

During the deposition of the polysilicon material using chemical vapor deposition (CVD), there is a chance that the gate cavities are not properly filled. This problem exists because of the vortex flow of the polysilicon deposition. Due to this vortex flow, there is a very high probability for a device with a large width, that the cavity will not be filled completely because the flow to the middle can be obstructed due to the distance from the openings. However, an easy method (which was not done here) to verify the limitation of deposition of the polysilicon material into the devices, such an experiment is easily carried out with the availability of scanning electron microscope (SEM) structures where they can be sliced and examined under the SEM for the various dimensions to check on process devices that will be fully filled and those that will not be filled. Such a variation depends on each process cycle. Another method to check the filling of the polysilicon material is by carrying out a Focus Ion Beam (FIB) microscopic check. Figure 4.18 shows a transistor with a well filled gate cavity and one with a non-uniformly filled gate cavity.

Another sub-problem related to the deposition of the gate polysilicon is the diffusion of the dopants into the polysilicon material. In this process, the doping of polysilicon gate is performed by diffusion of dopants from a solid source. The doping atoms migrate mainly along the grain boundaries and since the deposited polysilicon exhibit a columnar microstructure, the diffusion of dopants into the back gate polysilicon along the cavity in the X-Y direction is not efficient. If the polysilicon located in the bottom cavities are not properly doped, this will lead to different resistance values for the top and bottom gates. However, be-

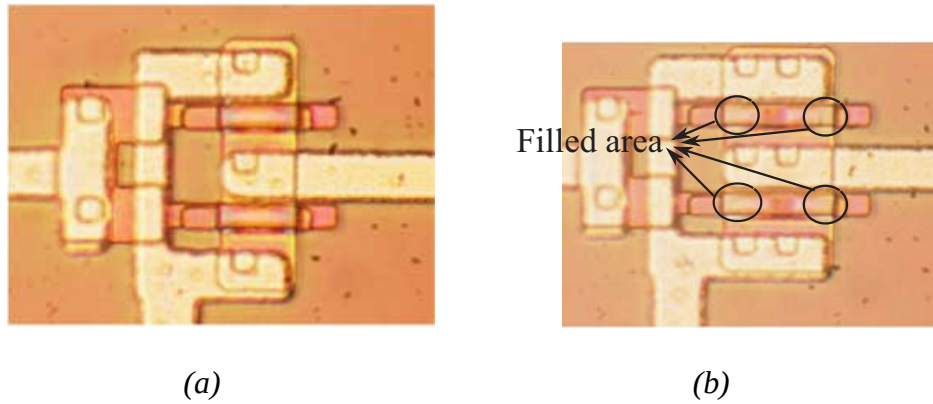


Figure 4.18: (a) A well filled and (b) misfilled back gate cavity.

cause gate resistance does not impact the static characteristics of MOS transistors, AC measurements have to be performed to highlight this technological problem. To analyze this effect of the gate resistance discrepancy between the top and bottom gates (i.e. higher gate resistance value for the bottom gate), AC measurements of the built SG SOI and DG SOI MOSFETs have been performed from 100 Hz up to 1 MHz. Figure 4.19 shows the impact of the gate resistance discrepancy on the gate transconductance of the DG SOI MOSFETs. At low frequency, we observe that the gate transconductance of the DG transistor is twice the one of the SG transistors as expected from the theory when the device are biased in the strong inversion condition. However, as the frequency increases, we can clearly see a considerable drop in the gate transconductance of the DG transistor. This decrease of the effective gate transconductance for the DG MOSFET is related to the higher bottom gate resistivity leading to a high RC constant linked to the bottom gate dynamic control. In other words, the higher resistance characterizing the bottom gate contact leads to a lower cut-off frequency for the bottom MOS transistor. However, this problem can be easily solved by performing an *in-situ* doping during the CVD process for the polysilicon gate material.

Another significant effect of the polysilicon is related to mechanical problems. It was discovered that there is a mechanical stress that exists between the polysilicon film and the silicon film. The difference in

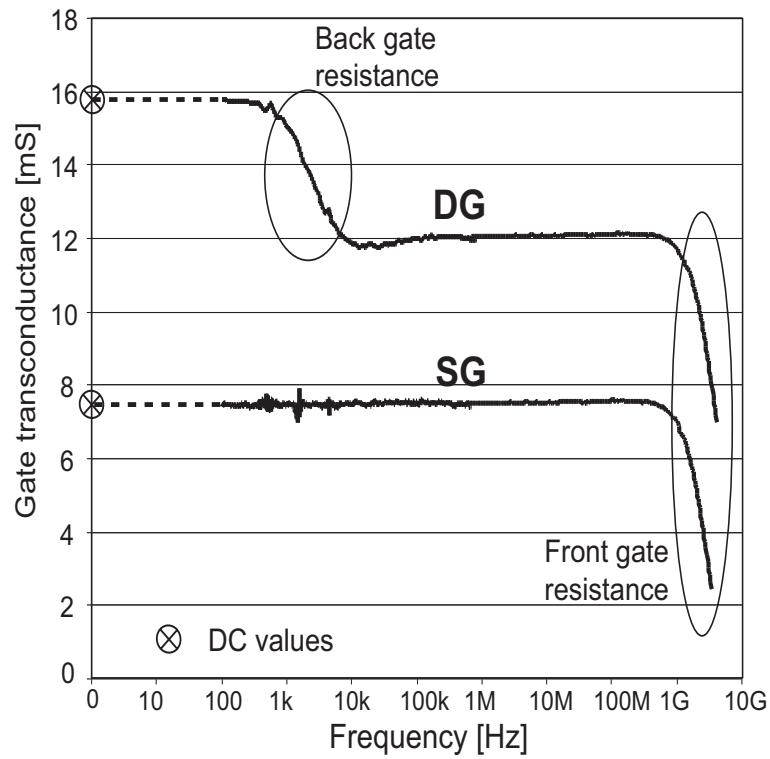


Figure 4.19: Gate transconductance for a DG and a SG SOI MOSFET in stauration and strong inversion versus frequency.

mechanical properties between the material manages to cause a periodic bending of the silicon film. Such a bending in the silicon film can cause unexpected electrical characteristics. Figure 4.20 shows two devices with such mechanical stress caused by the deposition of the polysilicon film. Such a situation is not observed in the normal single-gate devices could be due to the small stress in only one dimension, but with the filling of the gate cavity, this makes the situation into a two dimension situation or even a 3-dimensional effect. It should also be noted here that in our case, this observation was only seen in devices with large width.

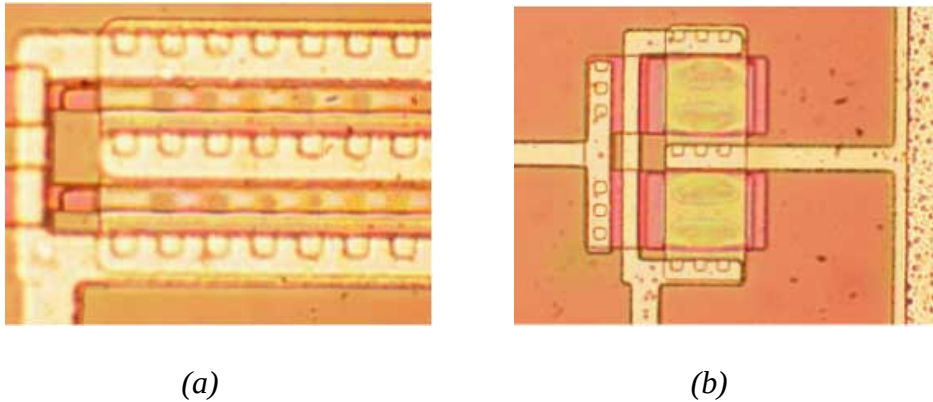


Figure 4.20: *Two examples of transistors with mechanical stress due to the mismatch of mechanical behaviour between polysilicon and silicon.*

4.4.6 Alignment of top and bottom gates

In order to reduce misalignments between the two gates, several steps have been taken into account. Although it is common that alignment marks are present already in current lithographic processes for the other layers and levels, in building the double-gate devices with wafer bonding over prepatterned cavities, these levels must be correctly aligned with reference to certain layers. In this process, it is important that the lithography mask for the active silicon layer is well aligned to the gate cavity mask before the other masks can be referenced to this active

layer later. An alignment mark between the gate cavity and the top gate should also be available to optimize this alignment process.

Another important step that should be taken seriously is the optical visibility of the gate cavities after the bonding process. In our process, it has so far been clear that even after the bonding process, we are still able to see through the thin silicon film layer to identify the gate cavities formed. However, to even further enhance and to avoid any problems if the silicon film is made thicker, is the availability of what is known as the 'open windows' which are just holes of micron size that permit one to see the gate cavities directly as in this area, the silicon layer is etched away. Figure 4.21 shows an example of such an opening window on the wafer and Figure 4.22 presents the location of the alignment marks.

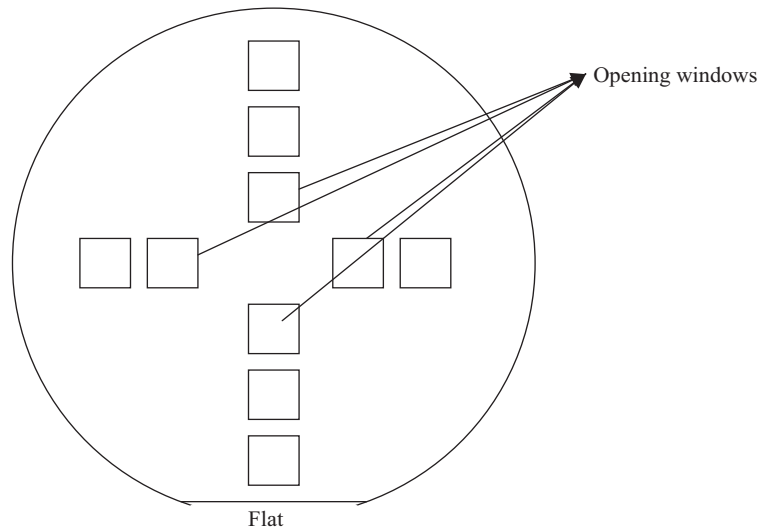


Figure 4.21: Example of some of the opening windows on a wafer and the alignment marks.

However, even with such tools available on the lithographic masks, misalignment can still occur simply due to the accuracy limit of optical alignment.

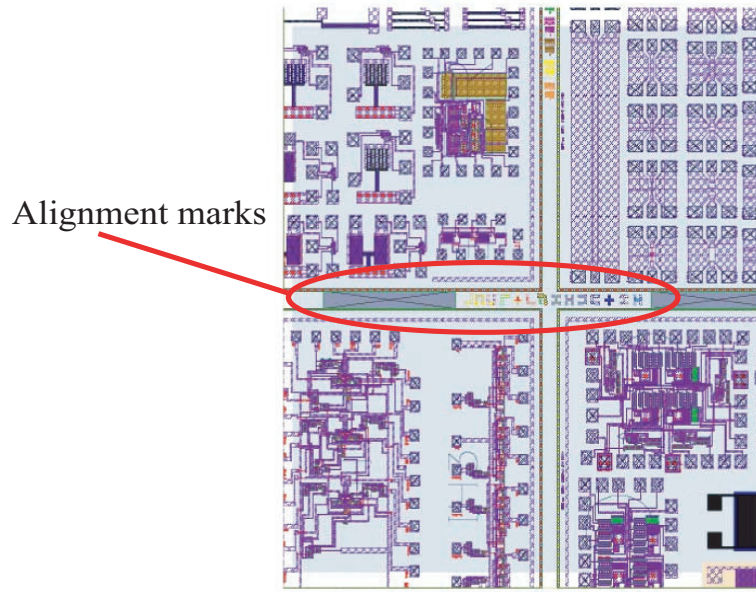


Figure 4.22: Location of the alignment marks.

4.5 Electrical characterization of built planar DG MOSFETs

Several DC electrical characterization were performed on the transistors fabricated to analyze the electrical properties of the devices. From these electrical characterization carried out, we can show that with the technique of wafer bonding over prepatterned cavities, the aim to fabricate double-gate transistors was achieved.

The devices were characterized using a Semiconductor Parameter analyzer, HP 4145B.

In Figure 4.23, the I_{ds} - V_{gs} curve extracted at a drain bias of 0.45 and 1.25 V is shown for DG devices with the correct activation process with $L = 3 \mu m$ and $W = 6 \mu m$. From Figure 4.23, it is clear that with correct processes and activation processes, functional DG transistor can be fabricated. Figure 4.23 already shows that the DG transistor fabricated with this wafer bonding method over prepatterned cavity has the characteristic of the DG MOSFET theory. Figure 4.24 shows the drain current dependent on the drain bias extracted at various gate bias. This

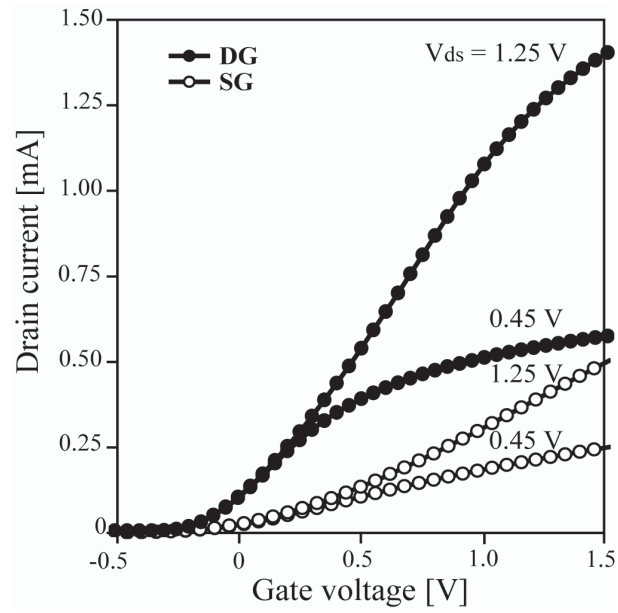


Figure 4.23: I_{ds} - V_{gs} curve for DG devices that were fabricated with a good activation process extracted at a drain bias of 0.45 and 1.25 V.

figure clearly shows that the DG transistor fabricated shows a driving current in saturation and strong inversion to be approximately 2 times higher compared to the single-gate devices. These experimental results are in agreement with the double-gate MOSFET theory.

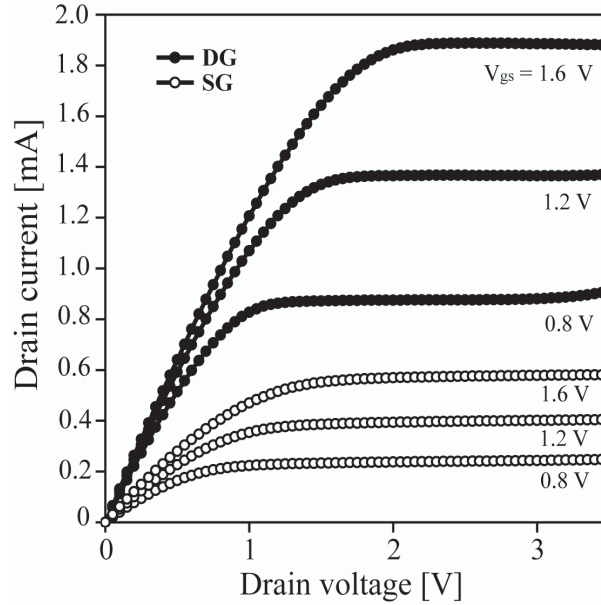


Figure 4.24: I_{ds} - V_{ds} curve for DG and SG devices extracted at various gate bias ($= 0.8, 1.2$ and 1.6 V).

Figure 4.25 shows the transconductance-to-current ratio extracted at a drain bias of 50 mV for both the DG and SG transistors. In the curves, the DG transistor is nearly able to reach the ideal subthreshold slope of 60 mV/dec compared to the SG transistor which is only able to reach a subthreshold slope of 83 mV/dec. If the g_m/I_{ds} value is kept constant, at $g_m/I_{ds} = 12 \text{ V}^{-1}$, the DG has a current drive of approximately 3.1 times higher compared to the SG due to the volume inversion phenomenon. At $g_m/I_{ds} = 4 \text{ V}^{-1}$, this current drive factor reduces to around 2 which is expected as the DG transistor then operates mainly as a two channel device.

To further prove and show that the wafer bonding over prepatterned cavities is a viable method to produce functional DG transistors, the transconductance of the device is analyzed with regards to the SG de-

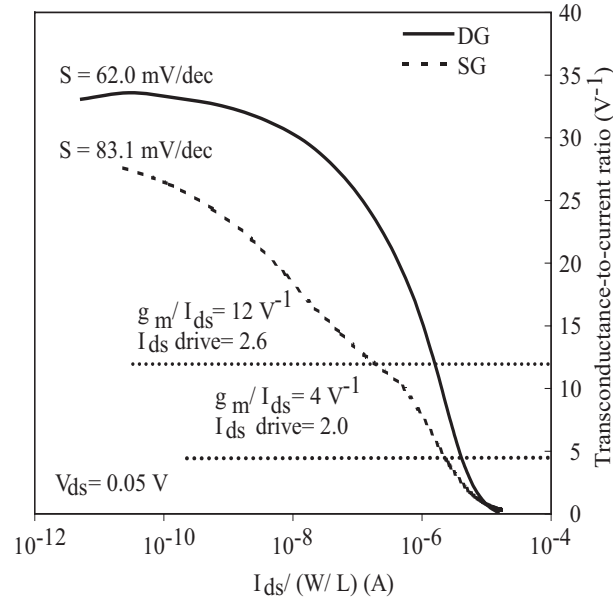


Figure 4.25: Transconductance-to-current ratio extracted at a $V_{ds} = 50$ mV for the DG and SG devices.

vice fabricated on the same wafer and technology. Figure 4.26 shows the ratio between the transconductance of DG to the transconductance of the SG (g_{mDG}/g_{mSG}) extracted at drain bias of 1.05 V. In the g_{mDG}/g_{mSG} ratio, it is again obvious that at low gate overdrive, the ratio is higher than 2 because of the volume inversion phenomenon in the DG transistor. As the gate overdrive increases, this ratio reduces to 2 which is expected due to the efficiency loss of the volume inversion phenomenon. Such electrical characteristics of the DG proves that a successful working DG device has been fabricated with this wafer bonding method.

Figure 4.27 shows the Early voltage extracted at $V_{gs} = 0.6$ V for the DG and SG transistors. The Early voltage of the DG is clearly higher than the SG device which again is an expected behaviour for a DG device. This again shows the viability of fabrication of the DG transistor with this wafer bonding method.

This fabrication method as mention has the flexibility that the range of W/L ratio is not restricted. This flexibility is seen when we look at a device with a gate length of $3 \mu m$ and width of $60 \mu m$ which gives

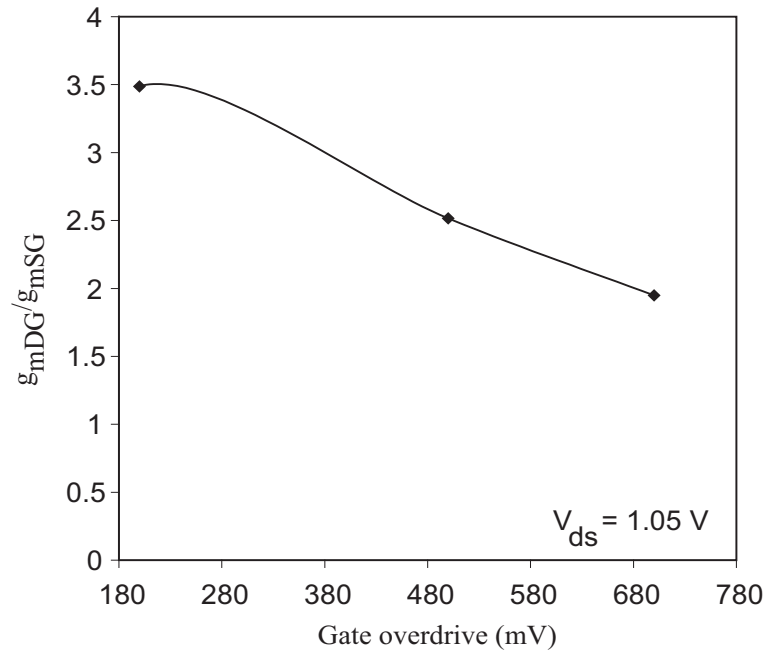


Figure 4.26: g_{mDG}/g_{mSG} extracted at $V_{ds} = 1.05 \text{ V}$ at various gate overdrive voltages.

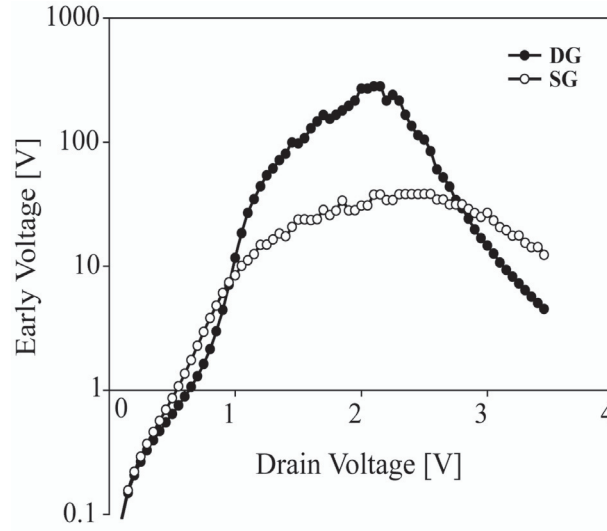


Figure 4.27: Early voltage for the SG and DG MOSFETs at $V_{gs} = 0.6$ V for $L = 3$ μm and $W = 6$ μm

a ratio W/L of 20. We show that such a ratio also works well with this fabrication method. Figure 4.28 shows the extracted I_{ds} - V_{gs} curve extracted at various V_{ds} for an intrinsic doped device with $W/L = 20$. It is clear that the DG device is working well as it demonstrates a current of nearly twice that of the SG. This DG behavior is again seen when we look at the I_{ds} - V_{ds} curves. Figure 4.29 shows the I_{ds} - V_{ds} curves extracted for the $W/L = 20$ ratio device with an intrinsic doping at various gate bias.

4.6 Silicon-on-Nothing

To further demonstrate the flexibility on this proposed fabrication method, Silicon-on-Nothing (SON) MOSFET devices presenting good electrical performances have been built and measured. The SON technology is another growing technology which has been identified as part of the challenge to meet the requirements of the ITRS. It has also been identified as a possible replacement for SOI technology [Kal01]. It has been reported that the SON technology has several advantages over the SOI

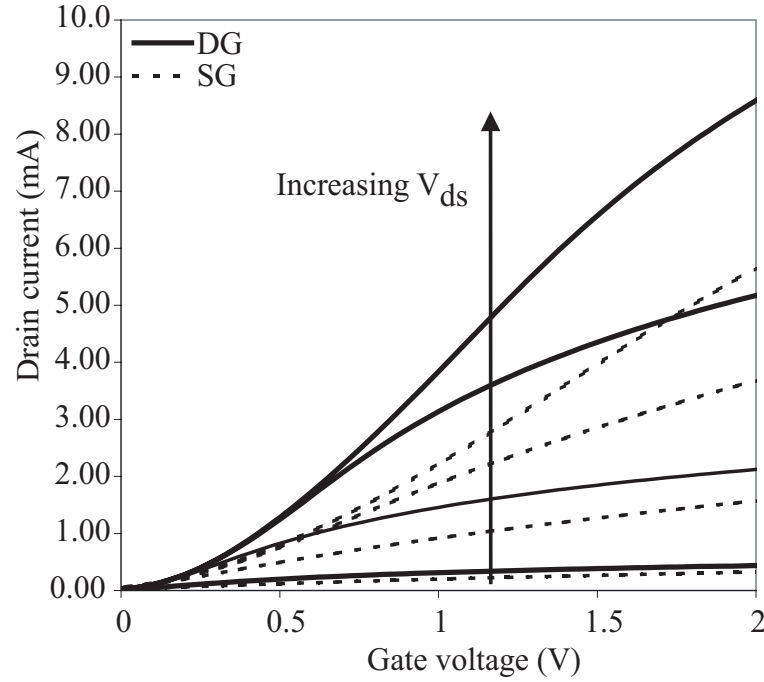


Figure 4.28: I_{ds} - V_{gs} curve extracted at various V_{ds} ($= 0.05, 0.25, 0.65$ and 1.25 V) for SG and DG devices with $W/L = 20$ and intrinsic doping.

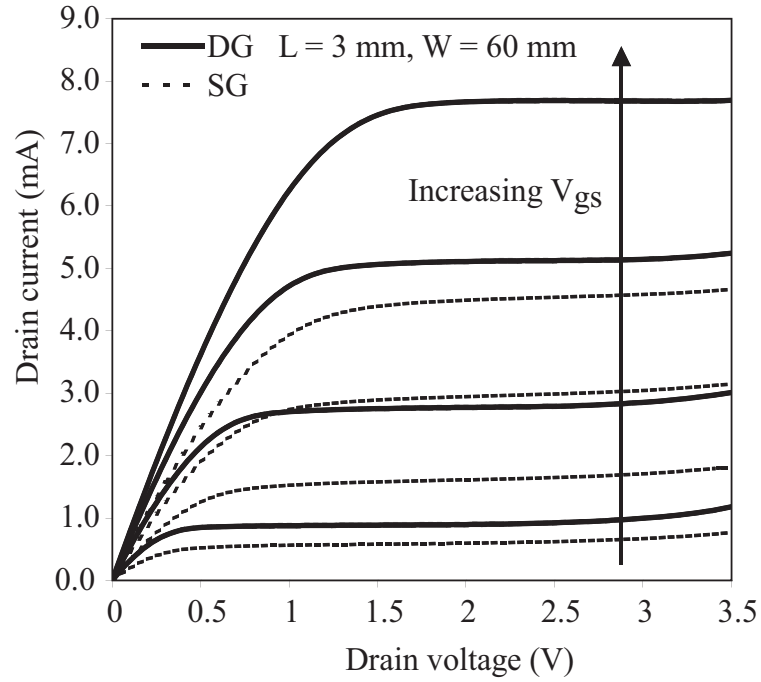


Figure 4.29: I_{ds} - V_{ds} curve extracted at various V_{gs} ($= 0.40, 0.80$ and 1.60 V) for SG and DG devices with $W/L = 20$ and intrinsic doping.

in terms of manufacturability and performance. This technology has also been shown to be more cost effective as it is about 75% cheaper compared to the SIMOX SOI process. ST Microelectronics, France, has also shown that the SON device is very promising device which can work along with SOI devices in moving along with the ITRS predictions [Mic02] ¹. SON technology is capable of moving towards the nanoscale silicon film thickness. Other advantages of the SON devices are the excellent I_{on}/I_{off} , suppressed self-heating ², low source/drain series resistance, near ideal subthreshold slope and high immunity to short-channel effects for device dimensions as low as 30 nm [Mic02]. The SON devices fabricated by ST Microelectronics are based on using a stack of silicon and silicon germanium (SiGe). Figure 4.30 shows the main steps used by ST Microelectronics to fabricate their SON devices.

Figure 4.31 shows a scanning electron microscopic photo of the final SON device built by ST Microelectronics.

Thus, from these preliminary results, it is thus an advantage that this wafer bonding over prepatterned cavities process can also be used to fabricate such SON devices alongside the double-gate devices without any changes to the fabrication procedure.

In order to fabricate a SON device with the prepatterned cavities and wafer bonding process as discussed in Section 4.3, the only modification that needs to be made is to define the cavity smaller than the size of the silicon island as shown in Figure 4.32. Figure 4.33 shows the longitudinal cross-section of the final SON device.

Figure 4.34 shows the extracted $I_{ds}-V_{gs}$ curves extracted at various drain bias for a SON with gate length of 2 μm and gate width of 10 μm . Figure 4.35 shows the extracted $I_{ds}-V_{ds}$ curves extracted at various gate bias (= 0.4, 0.8, 1.0 and 1.2 V) for a SON with gate length of 2 μm and

¹As seen later in this section, the SON device fabricated by ST Microelectronics and France Telecom is not actually the same SON device as we have fabricated. This is because the device discussed by ST Microelectronics contains a very thin layer of oxide under the silicon film rather than air as in the devices fabricated here at UCL. Although the technique used by ST Microelectronics to fabricate the device was based on the SON technique.

²This property is true only for the ST Microelectronic device and not if it contains air under the silicon film. This is because air has a lower thermal conductivity compared to oxide.

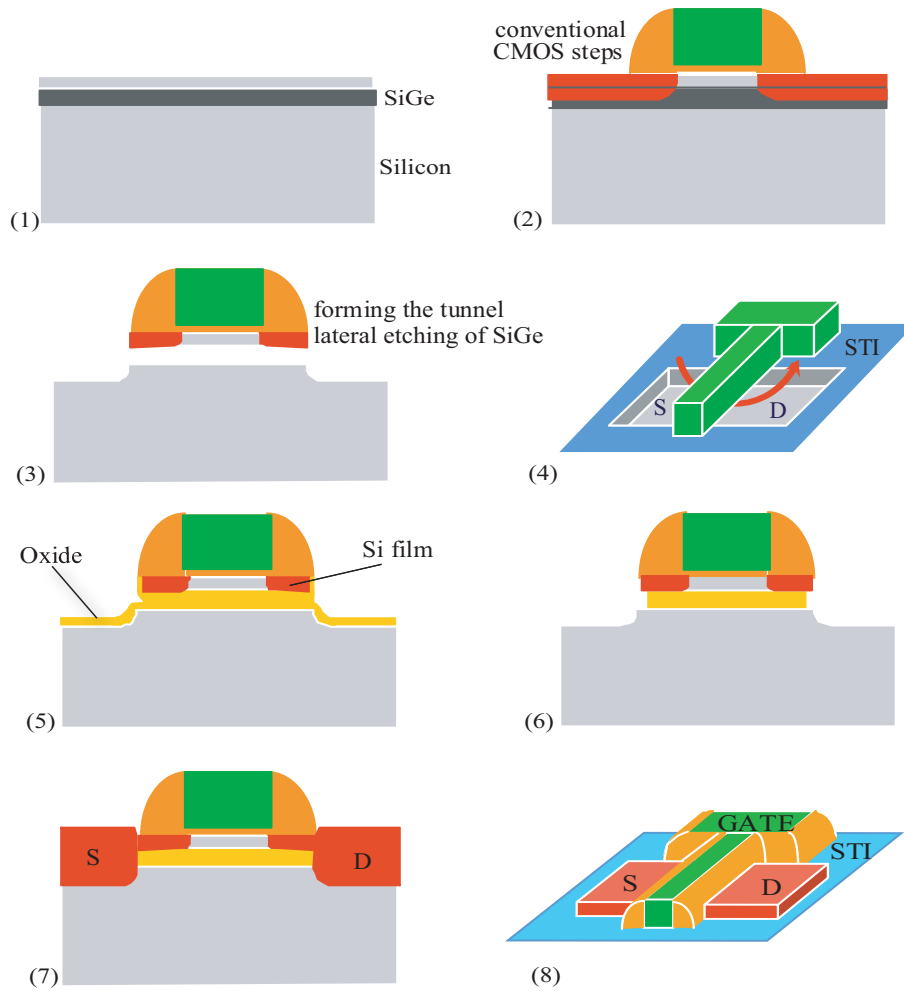


Figure 4.30: (1) Silicon and Silicon Germanium selective epitaxy on a Silicon wafer, (2) Channel implantation, formation of the gate, spacer and extension implantation as in a conventional CMOS process, (3) Etching of the source/drain regions and tunnel formation by a lateral etching of the SiGe, (4) 3-D view of the tunnel formed with the future source-drain region, (5) The tunnel is filled with oxide (optional), (6) Cleaning followed by selective epi etching of the source/drain, (7) Source/drain implantation if needed, (8) 3-D view of the final device [JTP⁺]

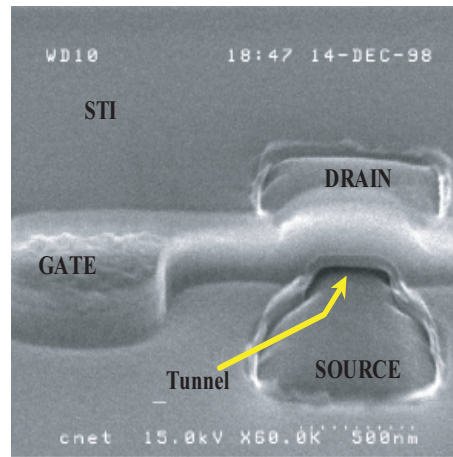


Figure 4.31: Scanning electron microscopic photo of the SON device fabricated by ST Microelectronics [JTP⁺].

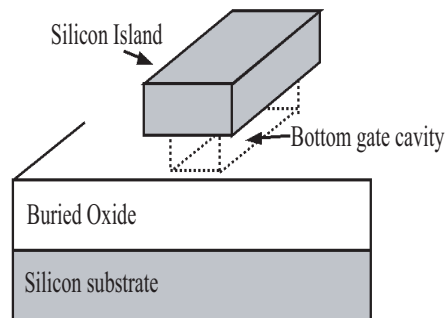


Figure 4.32: 3-D view of the SON cavity below the silicon island.

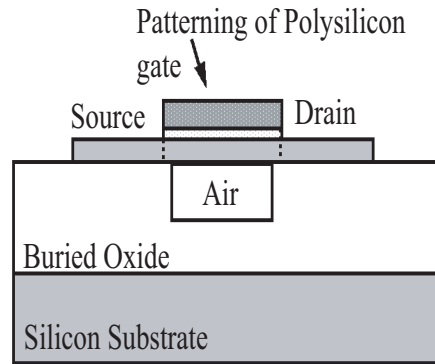


Figure 4.33: Longitudinal cross-section of the final SON device.

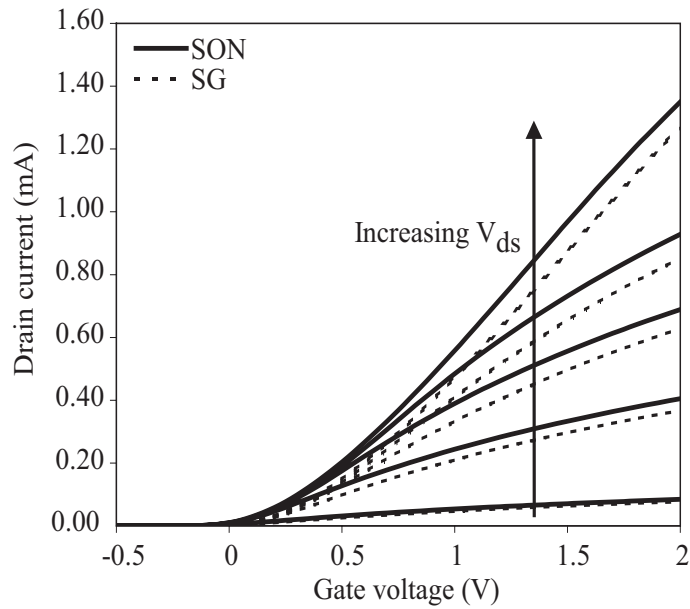


Figure 4.34: I_{ds} - V_{gs} curve extracted at various V_{ds} ($= 0.25, 0.65, 0.85$ and 1.25 V) for a SON device with gate length $= 2 \mu m$ and width $= 10 \mu m$ with a channel doping $= 4.4 \times 10^{11} \text{ atom/cm}^2$ and SG SOI device with the same dimensions and doping.

gate width of $10\ \mu\text{m}$. From Figures 4.34 and 4.35, it is clear that there

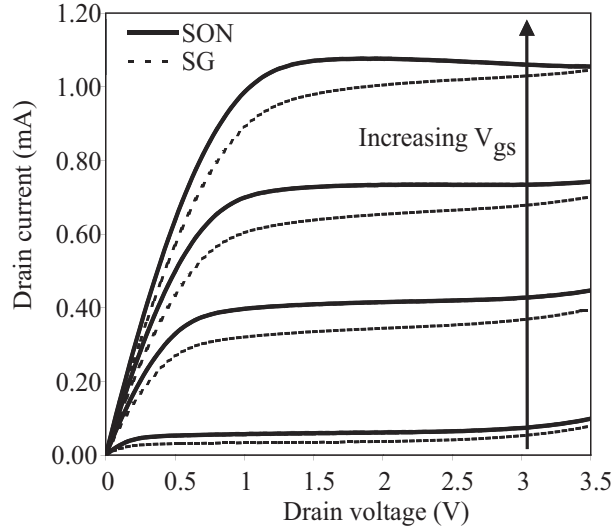


Figure 4.35: I_{ds} - V_{ds} curve extracted at various V_{gs} for a SON device with gate length = $2\ \mu\text{m}$ and width = $10\ \mu\text{m}$ with a channel doping = $4.4 \times 10^{11}\ \text{atom/cm}^2$ and SG SOI transistor with the same dimensions and doping.

is an improvement of 15% in the current drive between the SON and the SOI device. In Figure 4.35, we see that there is an indication of self-heating effect for SON device because of the lower thermal conductivity of air compared to the SON device by ST Microelectronics which is actually lying on a ultra thin layer of oxide.

Figure 4.36 shows the extracted g_{ms}/I_{ds} curves extracted at $V_{ds} = 0.05\ \text{V}$ for a SON with gate length of $2\ \mu\text{m}$ and gate width of $10\ \mu\text{m}$. From this curve, the subthreshold-slope can be extracted from the transconductance-to-current ratio value. The SON devices clearly show a much better subthreshold-slope value compared to the SOI device. This improvement in the subthreshold-slope value for the SON is most probably due to the improved body contact factor of the silicon film of the SON device to the thick buried oxide by a reduction of the film to substrate capacitances. Although the channel length of the devices here is not short enough for significant SCE, it can be seen already that there is an improvement when air is present between the silicon film and the

buried oxide which most likely have reduced the coupling between the drain and the channel. Such effect has been shown by Monfray *et al.* for short channel devices [MSFB⁺04].

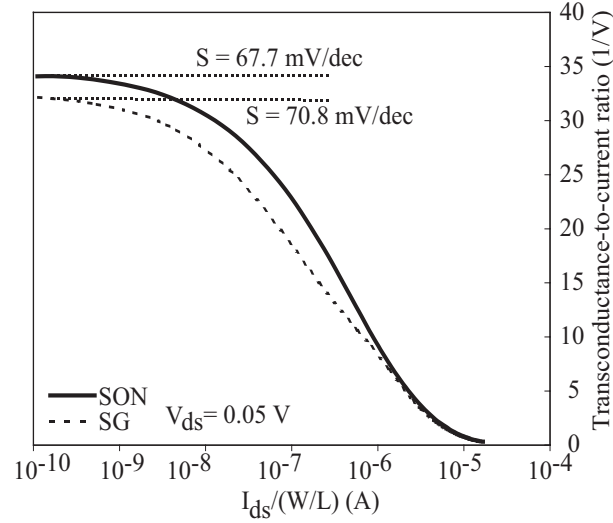


Figure 4.36: g_{ms}/I_{ds} curves extracted at $V_{ds} = 0.05$ V for a SON with gate length of $2 \mu m$ and gate width of $10 \mu m$ with a channel doping = 4.4×10^{11} atom/cm² and SG SOI transistor with the same dimensions and doping.

Figure 4.37 shows the transconductance curves extracted at various drain bias for a SON with gate length of $2 \mu m$ and gate width of $10 \mu m$. It is clear that there is a slight improvement in the transconductance value for the SON device of about 12%. This improvement in the transconductance values means an increase in the overall gain of the SON device compared to the SOI device. Such an increase in the SON device is highly attributed to the reduced effect of the buried oxide which reduces the parasitic effects of the device, thus improving the gain of the device.

It is thus clear that the SON device fabricated together with the DG devices shows promising results. With further development, we can combine the multiple-gate architecture on the SON type wafer.

It has also been shown that the wafer bonding process is flexible enough for the material used for the buried oxide to be replaced. As

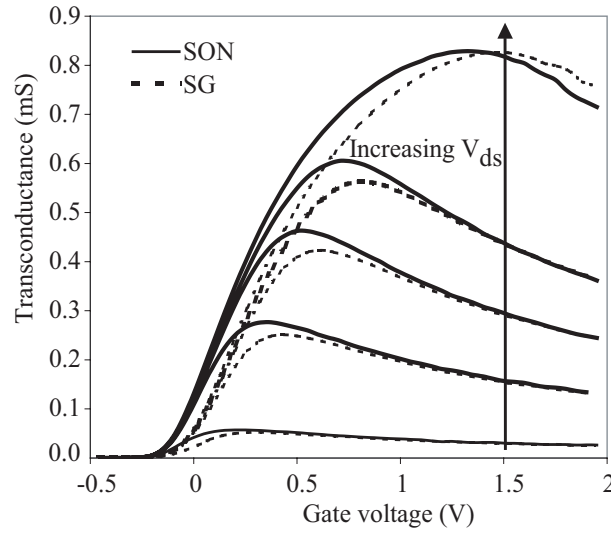


Figure 4.37: Transconductance curves extracted at various V_{ds} for a SON device with gate length = $2\ \mu\text{m}$ and width = $10\ \mu\text{m}$ with a channel doping = $4.4 \times 10^{11}\ \text{atom/cm}^2$ and SG SOI transistor with the same dimensions and doping.

known widely, one of the set backs of using SOI wafers is the self-heating effect. This effect can lead to a degradation of the current [FCF97]. In order to reduce this, one method is to substitute the silicon dioxide material used for the buried oxide with alumina oxide (Al_2O_3) [dBMR⁺06]. It has been exhibited that this alumina oxide can be deposited using atomic layer deposition (ALD). The electrical measurements [dBMR⁺06] from devices with the silicon dioxide replaced with alumina show that there is a significant reduction in the self-heating effect of the devices. This reduction is contributed to the much better thermal properties of alumina compared to silicon dioxide. Alumina at room temperature has a thermal conductivity of 23.08 W/m/K compared to silicon dioxide of only 1.38 W/m/K [AS00]. This shows the much improved thermal conductivity of alumina compared to silicon dioxide which contributes to this reduction or even the total elimination of the self-heating effect.

4.7 Conclusion

From the electrical characteristics, it is clear that the double-gate transistors fabricated using the wafer bonding over prepatterned cavities are functional and working with the expected DG behavior in the various operating region.

This fabrication method has proved to be a promising method for fabricating double-gate devices on SOI materials, SON or any other materials that would be technologically advanced for the electrical performances of the double gate transistors. Besides changing the insulator material, we can even fabricate quadruple-gate devices with some modification to the process or even double-gate devices with separated control gates. However, further research should still be carried out to further optimize the critical steps during the wafer bonding process. This is valid especially for the activation of the surfaces as it has been shown. It is also clear that with this fabrication method for planar DG devices, different W/L ratio can be fabricated without any major complications compared to the GAA method.

In this chapter, we have also seen that the DG architecture has very good electrical properties compared to the single-gate transistors. The potential of this process in fabricating other width to gate length ratio of more than 1 and fabricating other sort of devices such as the SON have also been shown. The electrical results from these devices show the expected characteristics. However, since the double-gate devices studied so far have been limited by the technology available to long channel devices, it is interesting to look into an alternative method to investigate the behavior of the double-gate devices with short channel lengths. This alternative method involves the use of single-gate devices emulated to behave as double-gate devices which are known as Quasi double-gate transistors. These quasi double-gate devices will be studied in detail in Chapter 5.

Chapter 5

Quasi Double-Gate SOI MOSFET

5.1 Introduction

'Quasi' means to simulate/create something to resemble the object/device we are interested in to have the same or close to the properties/attributes of that certain object/device/process as close as possible. Thus, a quasi double-gate is a device that should have as many as possible characteristics of a real double-gate SOI MOSFET transistor. This means that the working mechanism of the quasi double-gate should also work as close as possible to a real double-gate device. This quasi double-gate emulation should not be confused with what some authors such as Lindert [LCC⁺01], Landgraf [LRL01] and Tang [TCL⁺01] have defined as quasi double-gate operation as using a FinFET architecture operating as a planar double-gate due to the passive operation of the third gate on the FinFET device. In our analysis here, we have used the common SG SOI MOSFET to emulate the DG SOI MOSFET operation.

To emulate the quasi double-gate device, there are two main methods available that have been explored by Balestra [BCB⁺87] and Pretet [Con03]. The quasi double-gate device was first proposed by Balestra *et al.* to introduce the properties of the double-gate architecture [BCB⁺87]. In order to emulate the operation of the double-gate device from a single-gate device, the single-gate SOI MOSFET was applied with a back gate voltage (V_{g2}) equal to the front gate voltage (V_{g1}), multiplied by the ra-

ratio of the back to front gate oxide thicknesses. The ratio of the back to front oxides is shown in equation 5.1,

$$k = \frac{t_{box}}{t_{ox}} \quad (5.1)$$

where t_{ox} is the thickness of the front gate oxide and t_{box} is the thickness of the buried oxide. Thus, for the emulation of the single-gate device to work as a double-gate device, the following expression as shown in equation 5.2 is used for the applied back gate voltage,

$$V_{g2} = k \times V_{g1} \quad (5.2)$$

Figure 5.1 shows a schematic cross-section of the application of these corresponding gate voltages.

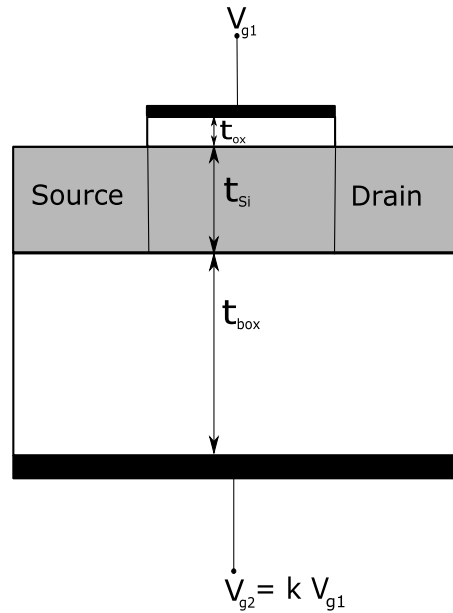


Figure 5.1: Schematic cross-section of an emulated DG MOS transistor from a SG MOS transistor.

The second method has been suggested by J. Pretet *et al.* [Con03]. In this method, the difference in both the oxide thicknesses are also taken into account, however, the difference between this method and the former one is the additional of the corresponding threshold voltages of the separate gates are also taken into consideration.

$$V_{g2} - V_{t2} = k \times (V_{g1} - V_{t1}) \quad (5.3)$$

where V_{t2} and V_{t1} is the back and front gate voltage, respectively. Due to the dependencies of V_{t1} on V_{g2} and reciprocally, this can pose a problem in determining the exact threshold voltages when both gates are biased simultaneously because of the effect they have on each other. The values obtained for each individual threshold voltage with the gate grounded will produce the expected V_{th} , but these values will not be accurate when used in Equation 5.3. This method developed by Pretet claims to be valid in both weak and strong inversion region. In order to emulate a double-gate one of the most important criteria that needs to be satisfied is to reach an inversion at both channels simultaneously. In this method, to determine the respective threshold voltages, the consideration of the silicon film thickness is important, because there is a big difference in the determination of the respective threshold voltages. If the film is thick, both threshold characteristics when drawn on the same graph will converge at one point. It is at this convergence point that we should choose the corresponding V_{t1} and V_{t2} . The thicker the films, the difference between the two curves becomes more obvious. In thick films, V_{t1} can be expressed as in Equation 5.4:

$$V_{t1} \approx -k \times \delta(V_{g2}) \quad (5.4)$$

and V_{t2} as in Equation 5.5

$$V_{t2} \approx -k \times \frac{C_{Si}}{C_{Si} + C_{ox1,2}}(V_{g1}) \quad (5.5)$$

where C_{Si} is the silicon film capacitance and $C_{ox1,2}$ is the front and back-gate oxide capacitances [Con03]. However, as the silicon film becomes thinner, the two different curves tend to converge. This is because the capacitances in the depleted film become very high dominating V_{t2} as in Equation 5.5. Figure 5.2 shows the difference in the corresponding V_{t1} and V_{t2} for a thick and a thin silicon film. Each of these methods have their own advantages and disadvantages depending on the thickness of the silicon film.

In this work, the method used for the analysis of quasi double-gate devices will be done with the first method because the thickness of the silicon film is considered to be thick enough for both methods to be valid from [Con03] as the devices analyzed have a silicon film thickness between 30 to 20 nm. Thus, in order to simplify the analysis, the first method was chosen to reduce the dependency on the threshold voltages which can complicate the analysis further if the inaccurate front and back-gate threshold voltage values are not extracted properly.

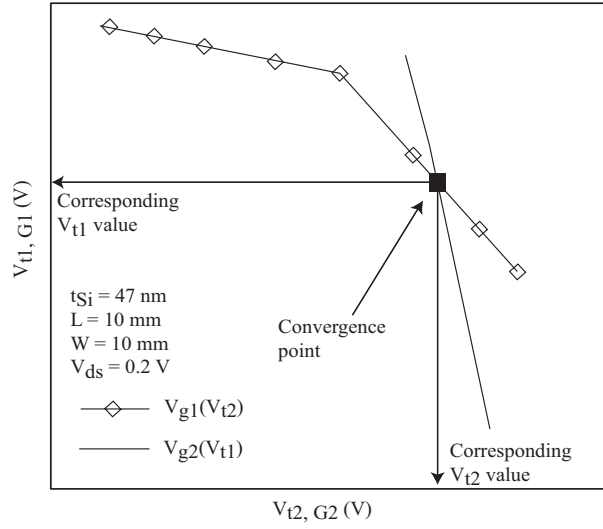
The analysis was carried out in three different situations, experimental, numerical simulation and analytical modeling. In the following sections, attention will be paid to the comparison between the experimental, numerical simulation and analytical modeling [KCFR05].

From all the previous analysis and work done on the emulation of double-gate devices, there are still some unanswered and unclear limitation of the emulation technique. The purpose of this work here is to analyze and to try to understand what the limitation of the techniques available are and to get a better overview of the various difficulties faced with the various methods of analysis.

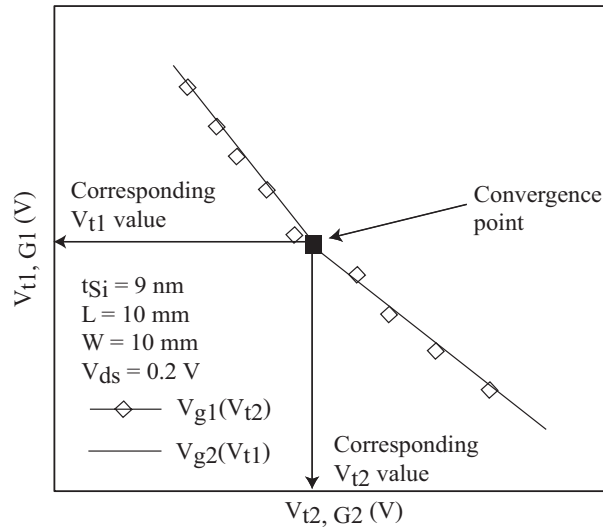
5.2 Devices analyzed

For the experimental devices, three different fully-depleted SOI single-gate transistors were used with different gate lengths. These devices are listed in Table 5.1. The experimental devices were used only for the analysis of 30 nm silicon film thickness.

The 2-D numerical simulations were carried out using the commercially available Silvaco© software. The devices were simulated using the Energy Balance model with the default values of the software [Sof00].



(a)



(b)

Figure 5.2: Schematic curves showing (a) V_{t1} and V_{t2} for a 47 nm thick silicon film, (b) V_{t1} and V_{t2} for a 9 nm thick silicon film. [Con03]

Device Identification	Gate oxide thickness (t_{ox1}) (nm)	Gate length (L_g) (μm)	Buried oxide thickness (t_{box}) (nm)	Silicon film thickness (t_{Si}) (nm)
A (LETI)	5.0	0.08-10	400	30
B (IMEC)	2.5	0.08-10	200	30
C (UCL)	30	3.0	400	32
DG (UCL)	30	3.0	400	32

Table 5.1: Identification of the different single-gate and double-gate SOI MOS transistors.

For the undoped devices, the gate material workfunction was adjusted to 4.67 eV corresponding to Molybdenum [RCH⁺02]. The purpose of the introduction of the gate workfunction is to adjust the threshold voltage to correspond to that of the experimental devices (which do not have metal gates). For SG and DG devices that had channel doping, the workfunction of the gate was left to the default of the software, i.e. n-doped polysilicon (with a default work function of 4.17 V). In the simulation, the physical models used take into account the electric field dependent carrier mobility with velocity saturation, SRH recombination/generation with doping dependent lifetime, Auger recombination, bandgap narrowing, self and lattice heating and impact ionization with electric field. In these simulations, it was expected that there would be no quantum effects as the thickness of the silicon film was thick enough, more than the expected thickness where quantum effects happen ($t_{Si} < 10$ nm). For device A (LETI) and B (IMEC), these SG devices were also simulated in DG operation mode.

5.3 Analog and Digital analysis

5.3.1 Analysis of 30 nm Si thickness devices

Table 5.1 shows the various devices used for the experimental analysis for the 30 nm silicon film thickness. Device A (LETI) was fabricated based on the process as described in Raynaud [RFP⁺88] and device B

(IMEC) was fabricated based on the process as described in van Meer [vMdM01]. The SG device from UCL was fabricated based on the process as described in Pavanello [PMF00a] and the DG device based on the process as described in Vandooren [Van00]. The main steps for the DG UCL technology are to etch the oxide on the sidewalls of the silicon islands as well as in the buried oxide and a cavity is created underneath the center part of the silicon islands. The DG device analyzed here was based on the Gate-All-Around process as described in Chapter 4. The devices were first measured experimentally followed by 2-D numerical simulation analysis. The DG devices were measured followed by a measurement of an equivalent single gate device that was measured in the quasi double-gate mode. In these devices, the ratio of t_{box}/t_{ox} (400/30) was approximately 13.3. The devices analyzed here were devices as seen in Table 5.1. Figure 5.3 shows the transconductance-to-current ratio extracted at V_{ds} of 50 mV for SG, DG and Quasi DG SOI MOSFET from the UCL technology. It is clear that there are differences between

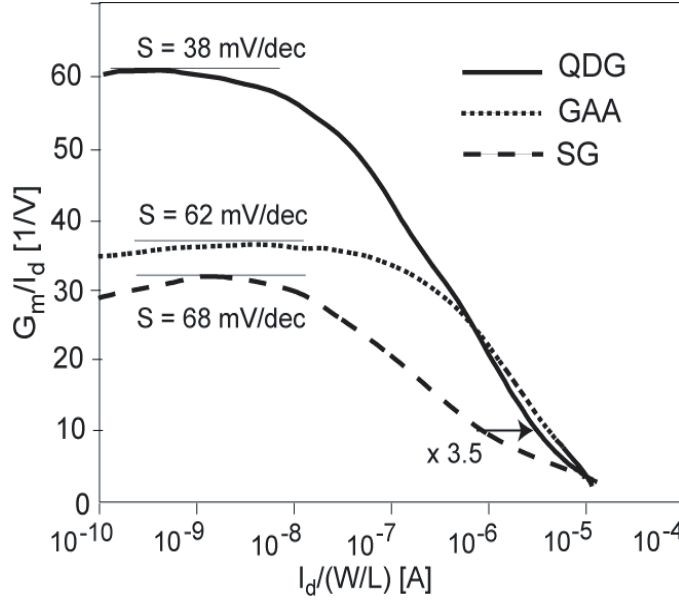


Figure 5.3: Transconductance-to-current ratio extracted at V_{ds} of 50 mV for SG, DG and Quasi DG SOI MOSFET with $L = 3 \mu m$ from the UCL technology.

the different devices in the different regions of bias. In the weak inversion regime, it is clear that the emulation of the double-gate deviates far from the real double-gate device. The emulation of the double-gate device is very good when we move into the strong inversion regime. In order to understand why such differences happens in the QDG device, numerical simulations were carried out. This is because with numerical simulations, it is hoped that the physics behind the QDG can be understood further. The characteristics obtained from the experimental values were reproduced with the numerical simulation. Figure 5.4 shows the simulated transconductance-to-current ratio extracted at V_{ds} of 50 mV for SG, DG and Quasi DG SOI MOSFET based on the devices from UCL.

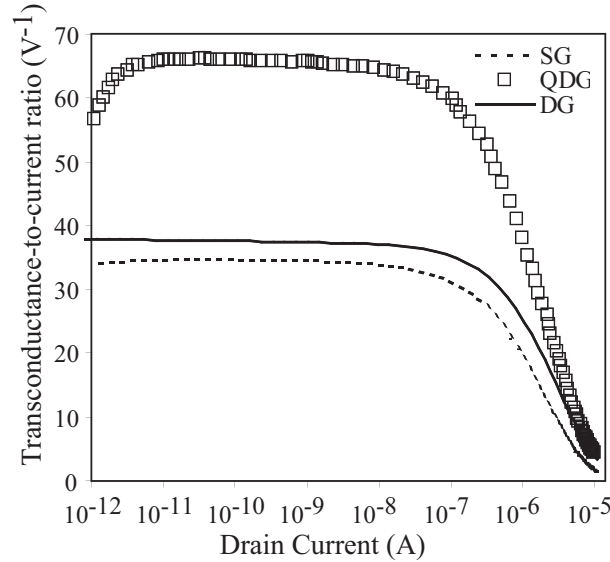


Figure 5.4: Simulation of the transconductance-to-current ratio extracted at V_{ds} of 50 mV for SG, DG and Quasi DG SOI MOSFET with $L = 3 \mu m$ from the UCL technology.

The simulation results in Figure 5.4, are in agreement with the experimental results presented in Figure 5.3 whereby in the weak inversion regime, the emulated double-gate deviates far from the real double-gate. In the strong inversion regime, it is clear that the quasi double-gate is able to emulate very well the behavior of the double-gate. Figure 5.5

shows an overview of the extracted subthreshold slope from device B (IMEC) for the various L but with the same k in weak inversion at $V_{ds} = 0.05$ V. It is clear that at all different gate lengths, there is an overestimation of the subthreshold slope value compared to the logically achievable theoretical limit value of a DG device. From Figure 5.5, we

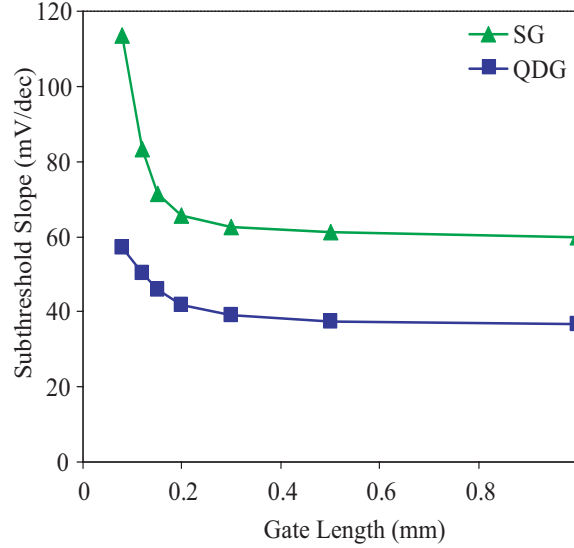


Figure 5.5: Overview of the extracted subthreshold slope from device B (IMEC) for the various L but with the same k in weak inversion at $V_{ds} = 0.05$ V.

can conclude that this overestimation in the weak inversion regime is not gate length dependent.

From the experimental and numerical simulations results, it is clear that in both experimental and simulation, we have seen the same difference in weak inversion. The subthreshold value obtained with the QDG in weak inversion is always overestimated and returns a value of approximately 30 mV/dec compared to the real DG value of approximately 62 mV/dec. A hypothesis for this difference between the QDG and DG in the weak inversion region is due to the difference in the geometrical structure of the device. When the SG device is used to emulate the DG operation regime, there is a difference in the charges at the interface between the buried oxide and the silicon film. This difference in the

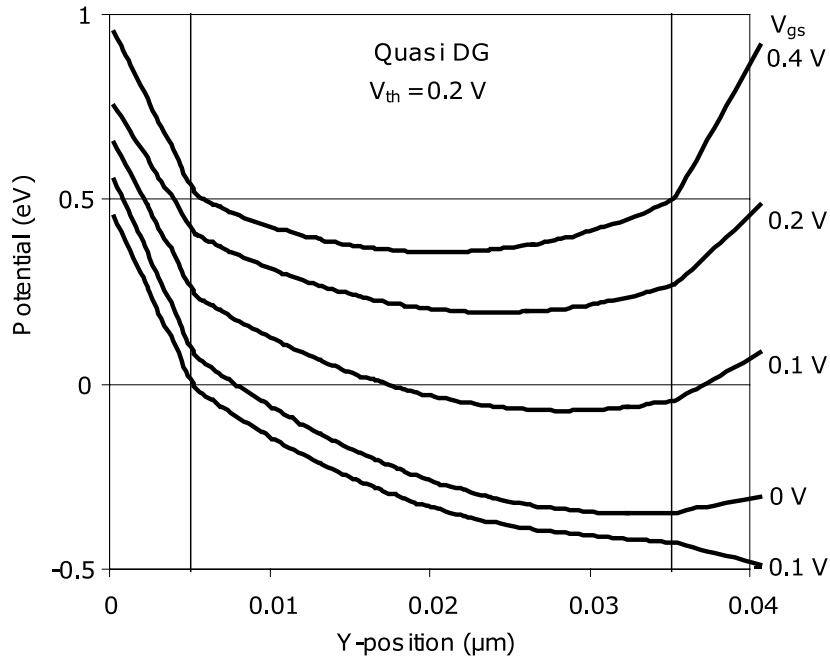
interface charges changes drastically the behavior of the back channel which leads to the overestimated subthreshold slope value obtained.

The second hypothesis is related to the electric field and the potential created at this back substrate. From the numerical simulations carried out, one of the advantage of using such an application is that we are able to extract the potential lines at the various bias points. Figure 5.6 shows the potential taken from the front gate oxide to the back interface between the silicon film and the buried oxide/second gate oxide from the simulated UCL devices.

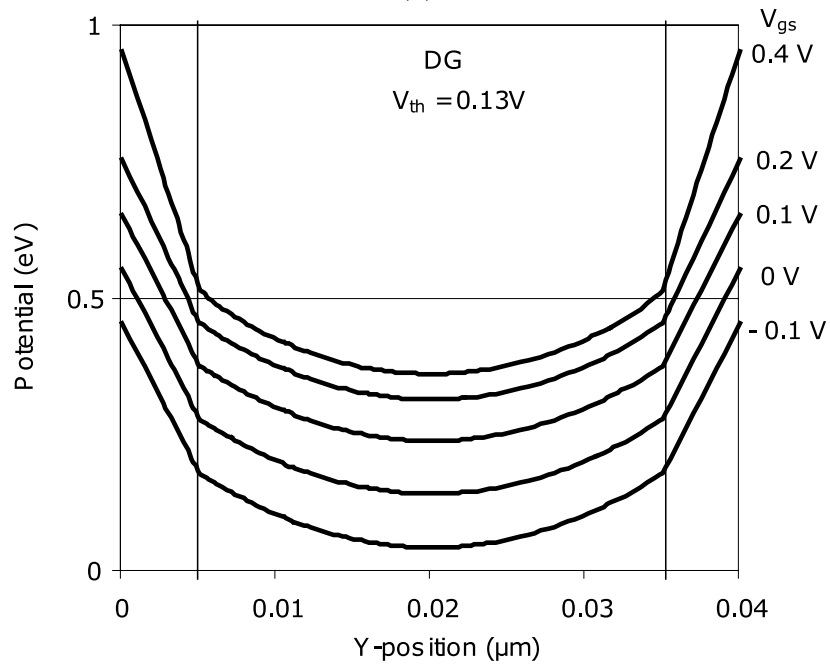
From the potential plots of both devices, we can notice the different potentials at the various gate biases. In the subthreshold region, the Quasi DG device shows an asymmetrical potential distribution compared to the DG device. As the device moves towards the strong inversion regime, this asymmetrical behavior disappears corresponding to the effect as seen in the transconductance-to-current ratio curve as shown in Figure 5.3. This analysis of the potential difference between the two devices confirms that there exists a difference in the charges at the interface between the silicon film and the buried oxide for the SG device in the quasi double gate operation region. Figure 5.7 shows the main difference in the electron distribution when the device is biased in weak and strong inversion. Figure 5.7 confirms the behavior of the potential distributions as seen in Figure 5.6. Only when the device is biased in strong inversion do we see that the QDG can copy the same electrical behavior of a DG device.¹

From the two hypothesis presented so far, it can be said that there is a link between these two hypothesis and they are both valid at the same time. This is true because we can link the differences in the potential distribution as seen in the Figure 5.6 with the difference in geometry leading to the different in the charges at the interface. Since a change in the interface charges can alter the potential behavior, we can conclude

¹From the potential distribution another characteristic that can be extracted is the threshold voltage of the device. However, it should be pointed out that this method of V_{th} extraction is not always reliable as seen in the other threshold voltage extraction methods available. For extraction of V_{th} from the potential distribution, it is only valid when the device is undoped or lightly doped. For devices that are heavily doped (extrinsic), it is not unusual that there the potential at the lines do not inverse even after the threshold voltage is reached. Further reading on this can be done in the reference of J.P Colinge [Col02]



(a)



(b)

Figure 5.6: (a) Potential extracted from the mid-point of the channel of a Quasi Double-gate transistor at various V_{gs} with the corresponding threshold voltage based on device B (IMEC), (b) Potential extracted from the mid-point of Double-gate transistor at various V_{gs} with the corresponding threshold voltage based on device B (IMEC).

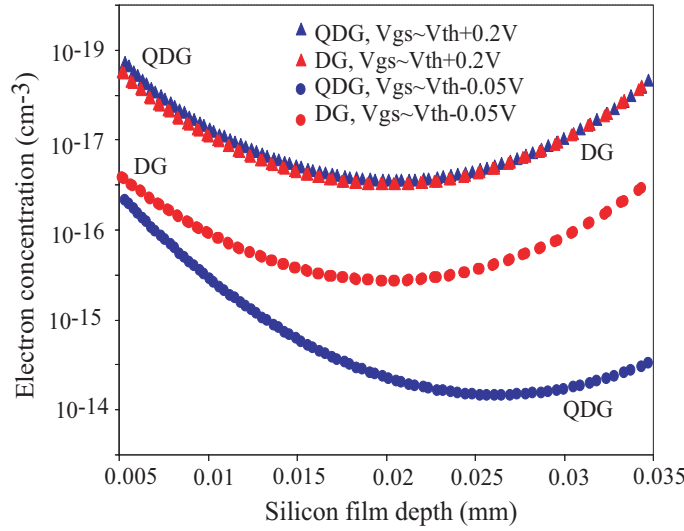


Figure 5.7: Difference in the electron distribution between the QDG and DG (IMEC) when biased in weak and strong inversion at $V_{ds} = 0.05$ V with $V_{th} = 0.20$ V for the QDG and $V_{th} = 0.13$ V for the DG.

here that indeed these two hypothesis are linked and valid at the same time.

In order to examine if such asymmetrical behavior was due to the simplicity of the method applied in this emulation, the threshold voltage of the backgate was taken into account as suggested by Pretet. However, even by applying the method proposed by Pretet, the QDG device still exhibited the same behavior in weak inversion. In strong inversion, we had again a good agreement with the QDG and the DG.

Figure 5.8 shows the transconductance-to-current ratio where the Quasi DG devices were measured using both the normal simple k-ratio method and the method proposed by Pretet [Con03]. The threshold voltage for the top gate was approximately 0.25 V and the backgate was approximately 0 V.

It is clear from Figure 5.8 that there is no significant change in the emulation of a double-gate device operation from a single-gate device in the weak inversion region. We see that the emulation works well again in the strong inversion region. This confirms again the difficulties in

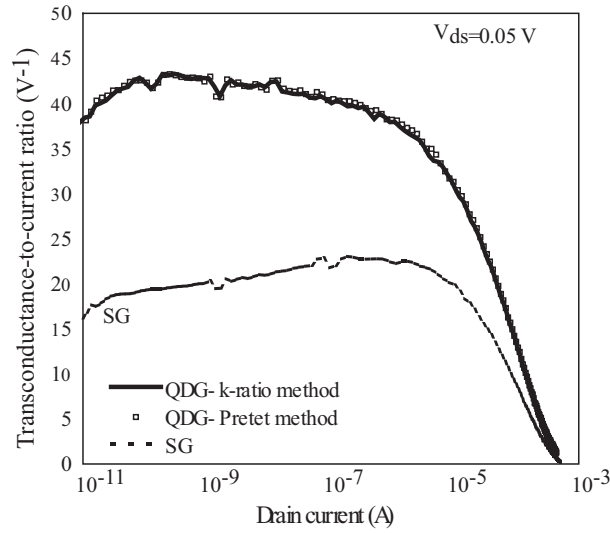


Figure 5.8: Transconductance-to-current ratio extracted at V_{ds} of 50 mV for SG and the Quasi DG SOI MOSFET by comparing the simple k -ratio method to that suggested by Pretet measured on the IMEC 0.12 μm process.

emulating double-gate operations from a single-gate device in the weak inversion region due to the difficulties in obtaining the correct charge and potential distribution at the two interfaces.

Thus, from the experimental and simulation carried out, it can be shown that the emulation of the DG device from a SG device is only valid in the strong inversion regime. If the characteristic of the Quasi DG needs to be studied in the weak inversion regime, than both method of emulation does not seem to be sufficient to simulate a similar behavior as in the real double-gate device.

5.3.2 Analysis of 20 nm Si thickness devices

In this analysis, the devices analyzed here were devices simulated in 2-D using the Silvaco© software. The thickness of the buried oxide was 150 nm with a front gate thickness (applied also for the second gate oxide for the DG device) of 2 nm. The doping used for the simulation was the natural doping of the silicon film (N_a) of 10^{15} cm^{-3} . In these

simulations, the workfunction was adjusted to match that of molybdenum. The gate length (L_g) of the devices were 100 nm. The purpose to reduce the silicon film thickness was to check if the effect of the charges at the interface between the silicon film and the BOX was dependent on the t_{Si} .

Figure 5.9 shows the I_{ds} - V_{gs} curve for the Quasi DG and DG device extracted at $V_{ds} = 50$ mV for both the simulated Quasi DG and DG transistors. Figure 5.10 shows the I_{ds} - V_{ds} curve for the Quasi DG and

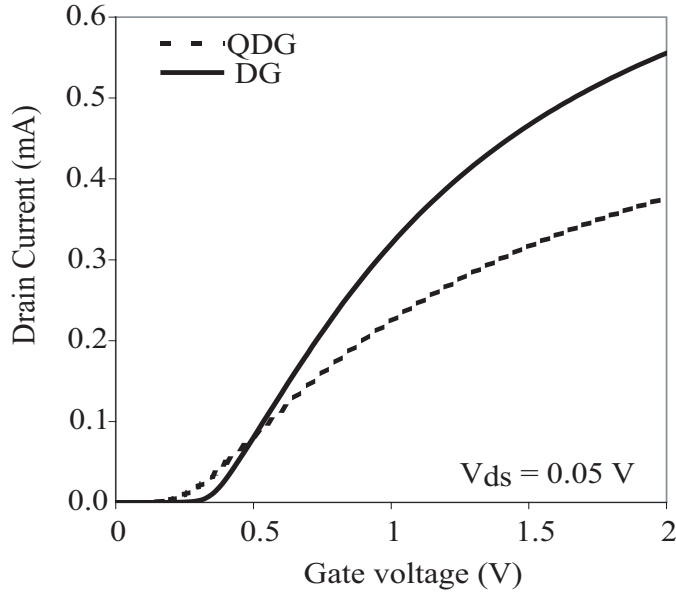


Figure 5.9: I_{ds} - V_{gs} curve for the Quasi DG and DG device extracted at $V_{ds} = 50$ mV for the Quasi DG and DG SOI MOSFET.

DG device extracted at $V_{go} = 0.70$ V for both the simulated Quasi DG and DG transistors. From Figure 5.9 and 5.10, it is clear that there is no significant effect in the reduction of the silicon film on the emulation of the DG device from a SG device. The effect of reducing the silicon film thickness has only a small effect in the weak inversion operation region. This effect can be seen in the transconductance-to-current ratio characteristic. Figure 5.11 shows the g_m/I_{ds} ratio extracted at $V_{ds} = 50$ mV for both the simulated Quasi DG and DG device with $L_g = 100$ nm.

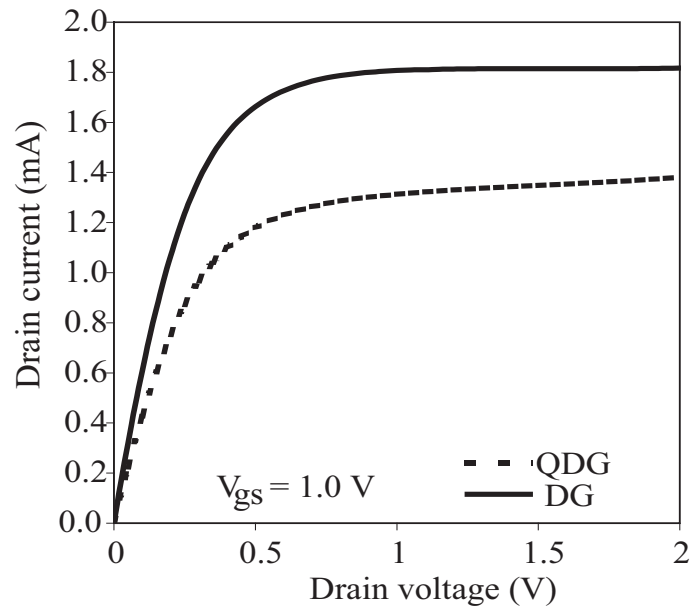


Figure 5.10: I_{ds} - V_{ds} curve for the Quasi DG and DG device extracted at $V_{go} = 0.70$ V for both the simulated Quasi DG and DG transistors.

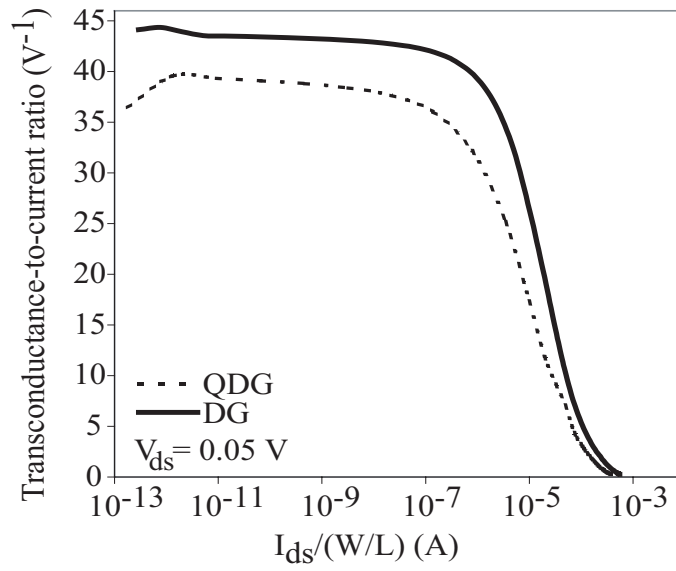
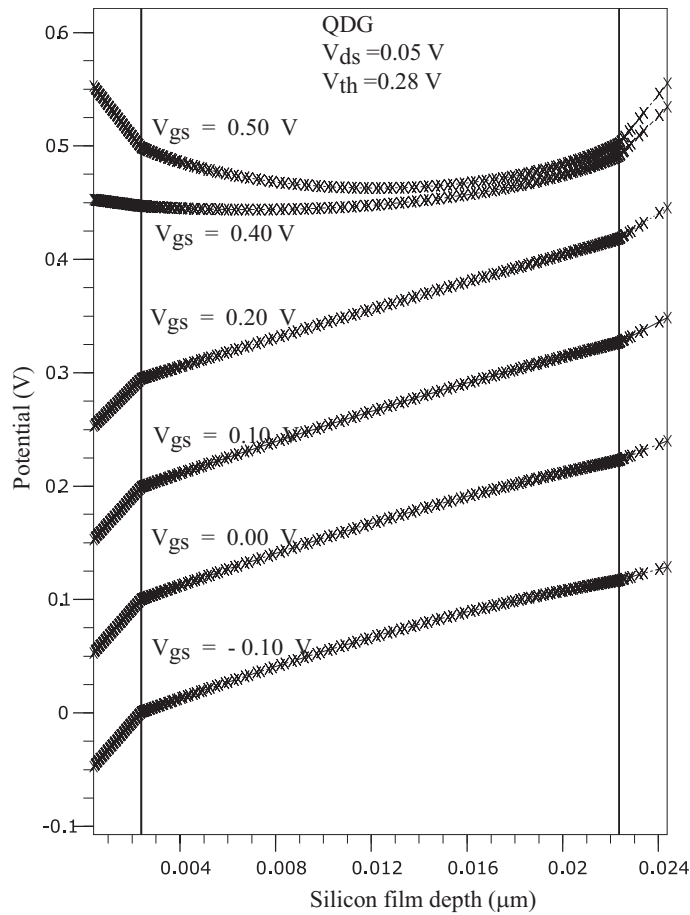


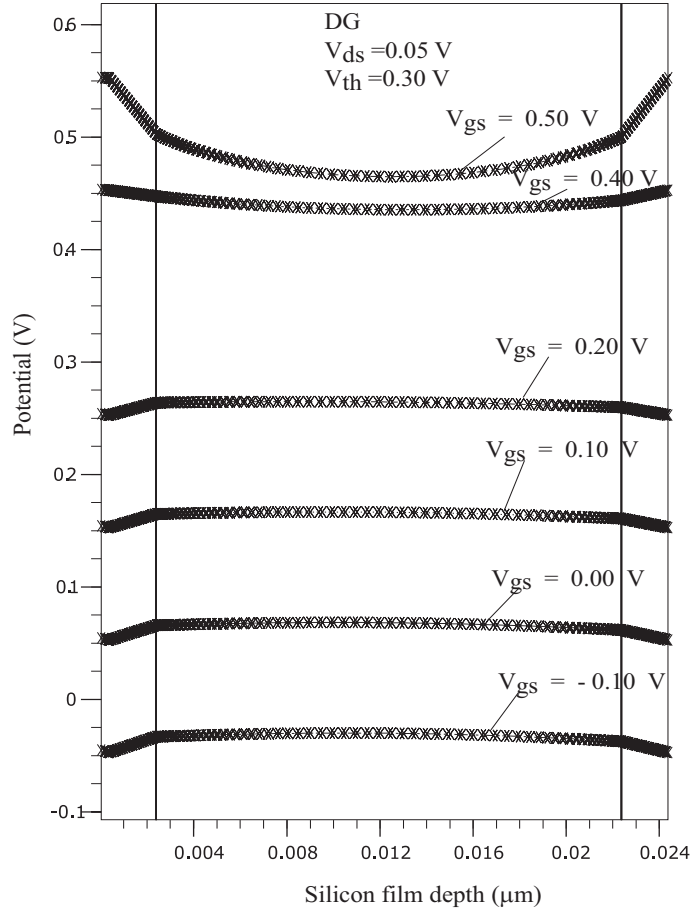
Figure 5.11: Transconductance-to-current ratio extracted at $V_{ds} = 50$ mV for both the simulated Quasi DG and DG device with $L_g = 100$ nm.

One clear observation is that in this characteristic, the emulation method has not overestimated the value of the g_m/I_{ds} ratio but instead, the value is underestimated. From this result, it is clear that in order to emulate the DG characteristic especially the volume inversion character, by just using the ratio of the thickness of the buried oxide to the front gate oxide is not sufficient. However, in order to study again the cause for this underestimation of the g_m/I_{ds} ratio value, the potential distribution in the devices will be again studied.

Figure 5.12 shows the potential plots of the Quasi DG and DG device extracted at $V_{ds} = 50$ mV and at various V_{gs} .



(a)



(b)

Figure 5.12: (a) Potential in the middle extracted from a Quasi double-gate transistor at various V_{gs} with the corresponding threshold voltage, (b) Potential in the middle extracted from a Double-gate transistor at various V_{gs} with the corresponding threshold voltage. Both the device here have $t_{Si} = 20 \text{ nm}$, $t_{ox} = 2 \text{ nm}$ and $t_{box} = 150 \text{ nm}$ with $N_a = 10^{15} \text{ cm}^{-3}$.

From the potential distribution plots as seen in Figure 5.12, it is clear that with the reduction of the Si film, there is still an asymmetrical distribution. This shows that even with the reduced Si film, the bias applied at the backgate to induce a depletion layer at the interface between the Si and BOX is still not sufficient to correctly emulate the desired charges as in a real DG transistor. From this potential distribution plot, it is clear that the underestimation in the transconductance-to-current ratio is due to the higher than estimated potential at the interface between the Si and the BOX as seen in Figure 5.12. This phenomenon is opposite to that in the 30 nm devices, where there was an overestimation in the transconduction-to-current ratio and in the potential distribution, it was lower in the Quasi DG and higher in the DG transistors.

In order to further understand how can a double-gate device be emulated from the single-gate architecture and to see the limitation of such emulation method, some analytical analysis were carried out with 2-D numerical simulation as a second tool. This will be discussed further in the next section.

5.4 Limitation of emulating a Quasi Double-gate

As seen in the previous section, the emulation of the double-gate operation from a single-gate transistor is not as simple as just taking into consideration the ratio of the thickness of the buried oxide to the front gate oxide or by taking into account the separate threshold voltage of the substrate contact and the front gate. In this section, the limitations of the emulation of a double-gate from the single-gate transistor will be presented from the linear region to the saturation region and from weak inversion to strong inversion.

The analytical analysis was used to evaluate the threshold voltage and the subthreshold slope. The basis for the analytical analysis was based on solving the 2-D Poisson's equation in the silicon film in the weak inversion region, as expressed in Equation 5.6:

$$\frac{\partial^2 \psi(x, y)}{dx^2} + \frac{\partial^2 \psi(x, y)}{dy^2} = \frac{qN_a}{\epsilon_{Si}} \quad (5.6)$$

The Poisson's equation is solved using the superposition principle [KCFR05]. Further explanation of the solving of this analytical analysis can be found in the paper by Kranti *et al.* [KCFR05] where the boundary conditions and assumptions used are explained in detail. In this analysis, the main variable to be adjusted will be the k ratio, which affects the potential distribution between the interface of the silicon film and the buried oxide. The effect of this k ratio has already been discussed in the previous section. The devices analyzed have a front gate oxide with a thickness of 2 nm, buried oxide thickness of 150 nm, silicon film thickness of 20 nm and the doping was left as the natural doping of the Si film (10^{15} cm^{-3}). The gate length (L_g) simulated were 200 and 100 nm. The gate workfunction in the 2-D numerical simulation was adjusted to match that of molybdenum. The rest of the physical models used are as those listed earlier in the chapter without any adjustments.

Figure 5.13 shows the transconductance-to-current ratio for the double-gate, single-gate and the quasi double-gate biased at $V_{ds} = 50 \text{ mV}$. It is

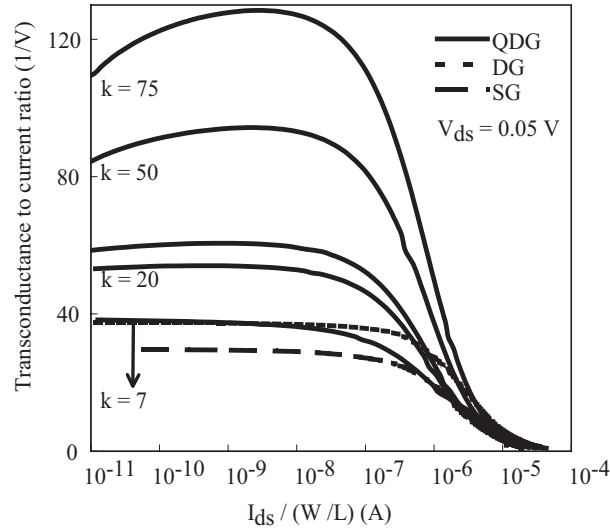


Figure 5.13: Transconductance-to-current ratio extracted at $V_{ds} = 50 \text{ mV}$ for simulated Quasi DG, DG and SG device with $L_g = 100 \text{ nm}$ for the various k ratios.

clear that in the weak inversion region at this drain bias, the value of the g_m/I_{ds} value is much higher than the ideal value obtained normally for

DG devices ($\approx 38.6 \text{ V}^{-1}$). This difference increases as the value of k increases. Such an observation was also observed in the previous section. This increase in the value of g_m/I_{ds} translates into a reduction of the subthreshold slope (S) from the ideal value. A reduction in the value of this ideal S value indicates that there is a difference between the coupling of the surface potential (φ_s) and the gate voltage. If we analyze the real DG device, the subthreshold slope obtained is near idea ($\approx 60 \text{ mV/decade}$). This shows that there is a good coupling between the φ_s and gate voltage. This translates into a symmetrical device whereby we can here conclude that when we apply a back gate voltage multiplied by the ratio, k , we are still unable to convert the single-gate transistor to work as a symmetrical device. It is thus clear that the Quasi DG device is actually an operating asymmetrical DG device forced by the introduction of the k ratio. The introduction of this k value also forces the coupling between the back and front potentials with their respective gate bias points to be higher than 1 (which is obtained in the DG device). The effect of the change of the k ratio on the Quasi DG and the DG can be seen in Table 5.2. From Table 5.2, it is clear that the emula-

DG and QDG	S-slope (mV/decade)				V_{th} (V)			
	L = 200 nm		L = 100 nm		L = 200 nm		L = 100 nm	
	Model	2-D	Model	2-D	Model	2-D	Model	2-D
k = 5	52.62	55.21	56.64	63.83	0.297	0.270	0.243	0.240
k = 10	45.54	47.40	48.06	54.80	0.242	0.240	0.196	0.210
k = 20	35.46	35.69	36.63	42.64	0.175	0.180	0.141	0.160
k = 25	31.76	31.63	32.63	37.98	0.166	0.160	0.136	0.140
k = 50	20.26	20.07	20.78	24.43	0.109	0.105	0.091	0.092
k = 75	14.46	14.67	15.00	17.93	0.077	0.076	0.064	0.068
DG	59.58	59.78	60.32	60.81	0.308	0.312	0.303	0.306

Table 5.2: Effect of the change of the k ratio on the Quasi DG and the DG.

tion of the double-gate becomes worse when the k ratio increases. Such

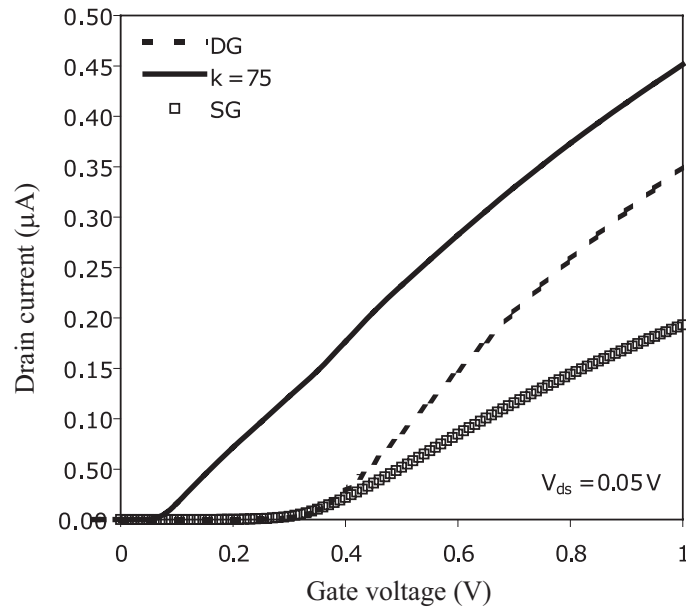
deviation is due to the increase in the asymmetrical between the two applied bias which leads to a further deviation of the value of the potential with relation to the applied gate bias ($d\varphi_s/dV_{gs}$) making it always more than unity.

However, such an asymmetrical behavior in the Quasi DG device is different from the asymmetrical devices that already exists, such as the $n^+ - p^+$ DG [KF01] or DG devices with different gate workfunction (due to different materials used for the gate material). These asymmetrical devices are different from the asymmetrical properties of the Quasi DG device because in these asymmetrical devices, the value of the ($d\varphi_s/dV_{gs}$) is still always less than unity.

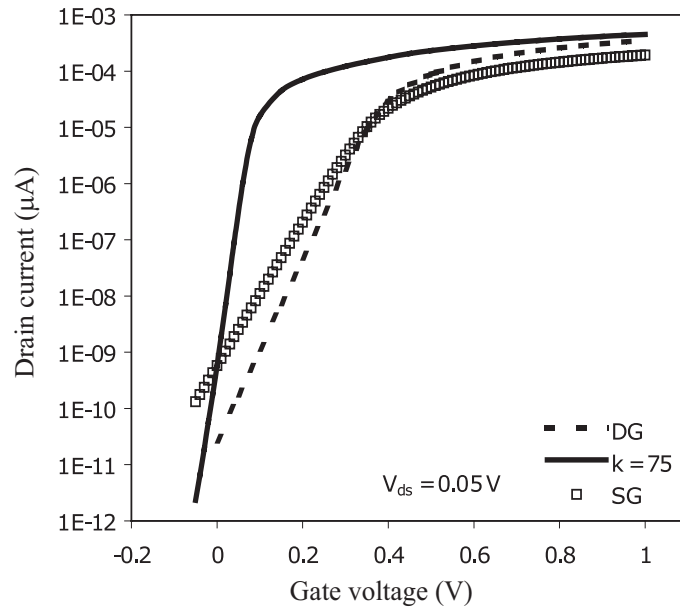
The severe deviation from the operation of the real double-gate transistor for a $k = 75$ can also be seen in the $I_{ds} - V_{gs}$ characteristic. Figure 5.14 shows the drain current versus gate bias for transistors with $L = 100$ nm at $V_{ds} = 50$ mV. It is clear that there is a big difference between the DG and the Quasi DG transistors due to the asymmetrical properties. One characteristic that is noticeable about the Quasi DG device, is that they have a much better switching characteristic compared to the real DG device. In Figure 5.14, we see that the Quasi DG device has a low current when in the off-state but there is a drastic increase of the current when it is in the on-state. However, due to the threshold voltage shift of the Quasi DG device, such an advantage cannot be seen in the real DG device because of the asymmetrical behavior in the Quasi DG.

In order to understand deeper how such an asymmetrical behavior in the Quasi DG transistors lead to such a big difference in the electrical characteristics compared to the real DG transistors with the change in the k ratio, the potential plots of the devices are analyzed. Figure 5.15 shows the potential plots for the DG device, and the Quasi DG devices with $k = 7$ and $k = 75$ with a $L_g = 100$ nm at a drain bias of 50 mV.

It is clear from Figure 5.15 that in the Quasi DG device with $k = 7$, the characteristics in the potential begins to deviate from the potential of the real DG device. As k is further increased to 75, the potential and $d\varphi_s/dV_{gs}$ ratio changes drastically compared to the real DG transistor. One of the most prominent shift is between the back surface potential (φ_{s2}) and the front surface potential (φ_{s1}). In the real double-gate transistor, both the front and back surface potentials are the same for all the

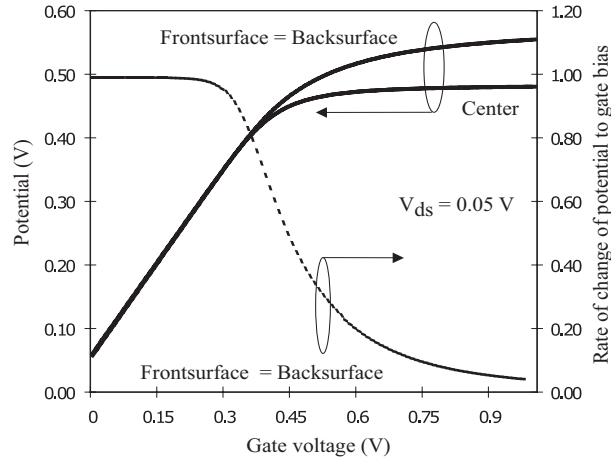


(a)

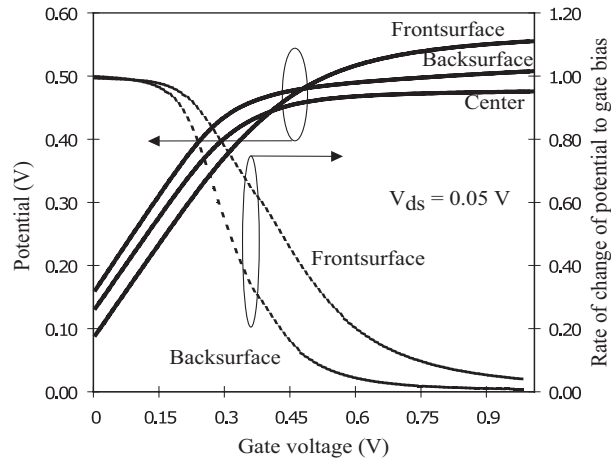


(b)

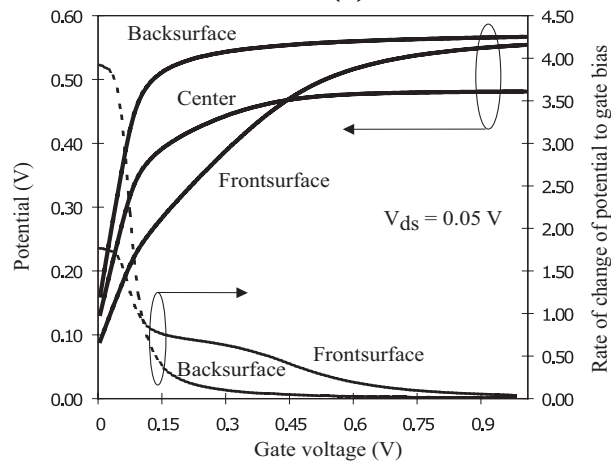
Figure 5.14: I_{ds} - V_{gs} for the SG, DG and Quasi DG transistors biased at $V_{ds} = 50$ mV in (a) linear scale and (b) in log scale.



(a)



(b)



(c)

Figure 5.15: Potential plots for the (a) DG device, and the Quasi DG devices with (b) $k = 7$ and (c) $k = 75$ with a $L_g = 100$ nm at a drain bias of 50 mV.

various applied gate currents, however, for the Quasi DG device with $k = 7$, a deviation from this begins to appear although the deviation is still relatively small. When the value of k increases to 75, this deviation between the front and back surface potential increases especially when the applied gate bias is low, but starts again to reduce when the transistor is in strong inversion in the linear region. This is because at low gate bias, the back channel begins to turn on faster before the front channel leading to such a big difference between the two surfaces. Another prominent missing feature of the Quasi DG devices compared to the real DG device is the absence of the volume inversion phenomenon. In the real DG device, we see that at low gate bias, around the threshold voltage bias, the potential at the front, back and center (φ_c) are equal. Such a feature is missing from the Quasi DG devices even with the device with a ratio of $k = 7$.

5.5 Conclusion

From the analysis of the potential at the front, back and center of the silicon film of the Quasi double-gate device compared to the real double-gate device, a general observation can be shown on the effectiveness of using the Quasi double-gate method to emulate a double-gate device. Table 5.3 shows the summary of the regions where the Quasi DG method is valid and where the limitations of this method are.

From Table 5.3, it is clear that the Quasi DG method can be used with some form of reliability if we would like to emulate devices with a small k ratio in the linear region and in strong inversion.

We can also conclude that in order to emulate the double-gate transistor from a single-gate transistor, we cannot just directly take the ratio between the thickness of the front gate oxide and the thickness of the buried oxide layer and multiple this ratio with the gate bias on the back substrate. This is due to the asymmetrical properties of the charges formed at the interface of the silicon and the buried oxide which up till now remains a rather complicated interface properties due to the constant change at this interface for each individual device. Some of the factors that can affect the interface are the interface charges, the interstitial charges and the defect densities.

Parameter	Region	Good Applicability of the Quasi DG method?
Mobility	Strong Inversion, Linear Regime	Yes
Maximum transconductance	Strong Inversion, Linear Regime	Yes
Maximum transconductance	Strong Inversion, Saturation	No
Transconductance-to-current ratio	Strong Inversion, Linear Regime	Yes
Transconductance-to-current ratio	Strong Inversion, Saturation	No
On-current	Strong Inversion	No
Off-current	Weak Inversion	No
Threshold voltage	-	No

Table 5.3: *Limitation and applicability of the Quasi DG method in the emulation of a real Double-gate in the various operation region for various important parameters.*

We have also seen that the method proposed by Pretet in which the threshold voltage of the front and back substrate are taken into account with the k ratio is also not sufficient to emulate a real double-gate device as seen in Figure 5.8.

By using analytical, experimental and numerical simulations we have

been able to analyze the limitations and effectiveness of the Quasi DG method in emulating a real double-gate device.

Chapter 6

Performance comparison of Multiple-gate MOS devices

6.1 Introduction

Multiple-gate devices are MOS transistors with more than one gate operating simultaneously. As introduced in **Chapter 1**, they are one of the promising candidate in the ITRS. One of the main reason they have received so much attention is because of their electrical characteristics. Preliminary studies have shown that multiple-gate devices have great potential especially their operation in the subthreshold region [Pro03]. In Tables 1.3 and 1.4 shows the predicted values for analog applications and RF and Analog/Mixed-signal technologies. However, the question that arises is for how long will the current technology last before the next node needs to be implemented. Research in the 45 nm technology node has already begun since the last years even though it is expected that such a node will only be required in the year 2010. In 2013, the mainstream technology will move towards the 32 nm node. This is just an example of how aggressive the scaling of the devices have been predicted by the ITRS. In the current research of the 45 nm node, technologies are already facing some difficult challenges already. It is thus clear that in order to continue this trend in scaling to meet the Moore scaling trend [Moo65], the novel devices are the most promising candidates.

Current research now has only focused on the DC analysis of these novel devices [orICoM02] [Col04], [Pro03]. In Table 1.4, we see that

RF applications are also important. In this analysis, several multiple-gate architectures will be analyzed in terms of DC and AC electrical performances. In the DC analysis, the usual figure of merits will be analyzed, i.e. transconductance, subthreshold-slope, *etc.* For the AC analysis, the figure of merits that will be used are the g_m/g_{ds} , C_{gs}/C_{gd} , the parasitic capacitances and the cut-off frequency, f_T .

The DC and AC analysis of the multiple-gate MOSFETs, the main tool that will be used is the numerical 3-D simulation. The different multiple-gate architectures will be compared mainly based on the numerical 3-D simulations, but we also present DC and AC results from available FinFETs from IMEC.

6.2 Numerical simulations of Multiple-gate MOS-FETs

The devices that have been analyzed using numerical simulations are the planar double-gate, the triple-gate and the pi-gate. A simple single-gate nMOS without any technological improvement such as channel engineering or source/drain engineering was used as the reference. The devices were simulated with a uniform doping profile with a concentration of p-type doping (boron) with a dosage of 10^{15} cm^{-3} . The thickness of the gate(s) oxide used was 2 nm with the thickness of the buried oxide of 150 nm. The silicon film thickness (t_{Si}) which is also the width of the fin (W_{fin}) used was 20 nm. The channel length (L) of the devices were varied between 25 to 200 nm. The corresponding width (W) of the Pi-gate (PG) and the triple-gate (TG) was calculated as $H_{fin} + 2 \times W_{fin}$ with $H_{fin} = 50 \text{ nm}$ making the total width of the device 120 nm. For the single-gate (SG) and double-gate (DG) transistors, the corresponding width was calculated based on the width to gate length ratio of $W/L = 10$ which is a realistic ratio because it is considered to be the optimal value for the best RF performance for MOS transistors due to the gate resistance [RGC⁺98] [DRD⁺99]. However, it should be noted that W_{DG} is twice W_{SG} ($W_{DG} = 2W_{SG}$) because of the extra gate at the bottom of the silicon film. For the PG devices, the extension into the buried oxide was 20 nm. This extension was chosen because it was already proven that it was sufficient for strongly reducing the SCEs [Col04]. In these simu-

lations, in order to take into account the parasitic capacitances in the 3-dimensional structures related to the source, drain and gate connections, the electrodes were extended up to 500 nm in the Y-direction above and throughout the Z-direction for all the devices. Simulations were done to show that having these extensions were relevant even though they contributed to the computational time. These extensions provide a more realistic environment to the analysis of the capacitances influences of the 3-D interconnections. Table 6.1 shows the differences in devices simulated with and without these drain, source and gate extensions on the C_{gs} , C_{gd} and f_T of a various transistors of gate length = 200 nm. The simulated devices can be seen in Figure 6.1 with the related extensions of the drain, source and gate contacts. In the simulations, 500 nm of oxide was used as the boundary material across the structure height. This is important so that all fringing capacitances can be fully simulated as in the real transistors. It should also be noted that no boundary condition was defined at the edges of the gate finger. This oxide boundary is not shown in Figure 6.1 for clarity reasons. The simulations were performed with the energy balance model with the commercially available simulator Silvaco© as described previously in Chapter 2. The gate electrode workfunction was set to 4.67 eV corresponding to Molybdenum [RCH⁺02] which was adequate to obtain a threshold voltage of around 0.3 V for all the devices. The physical models used in the simulation accounted for the electric field dependent lifetime, the transverse field dependent mobility, SRH recombination/generation, bandgap narrowing and carrier statistics as described in Chapter 2.

For the small-signal AC analysis, a small-signal frequency from 1 MHz to 200 GHz with an amplitude of 30 mV was applied. The gate was used as the inport and the drain as the outport with the source as the common port. It is worth mentioning that all the devices simulated are not affected by any quantum effects based on the dimensions used here because they are higher than the dimensions where quantum effects will influence the electrical characteristics [WFS⁺99]. In the analysis of the small-signal frequency, a conventional small signal equivalent circuit was assumed for the extraction of the intrinsic elements for DG and SG devices. It is assumed that this equivalent circuit should also be valid for the other multiple-gate devices. Figure 6.2 shows the small-signal equivalent used for the extraction of the intrinsic elements for the MOS

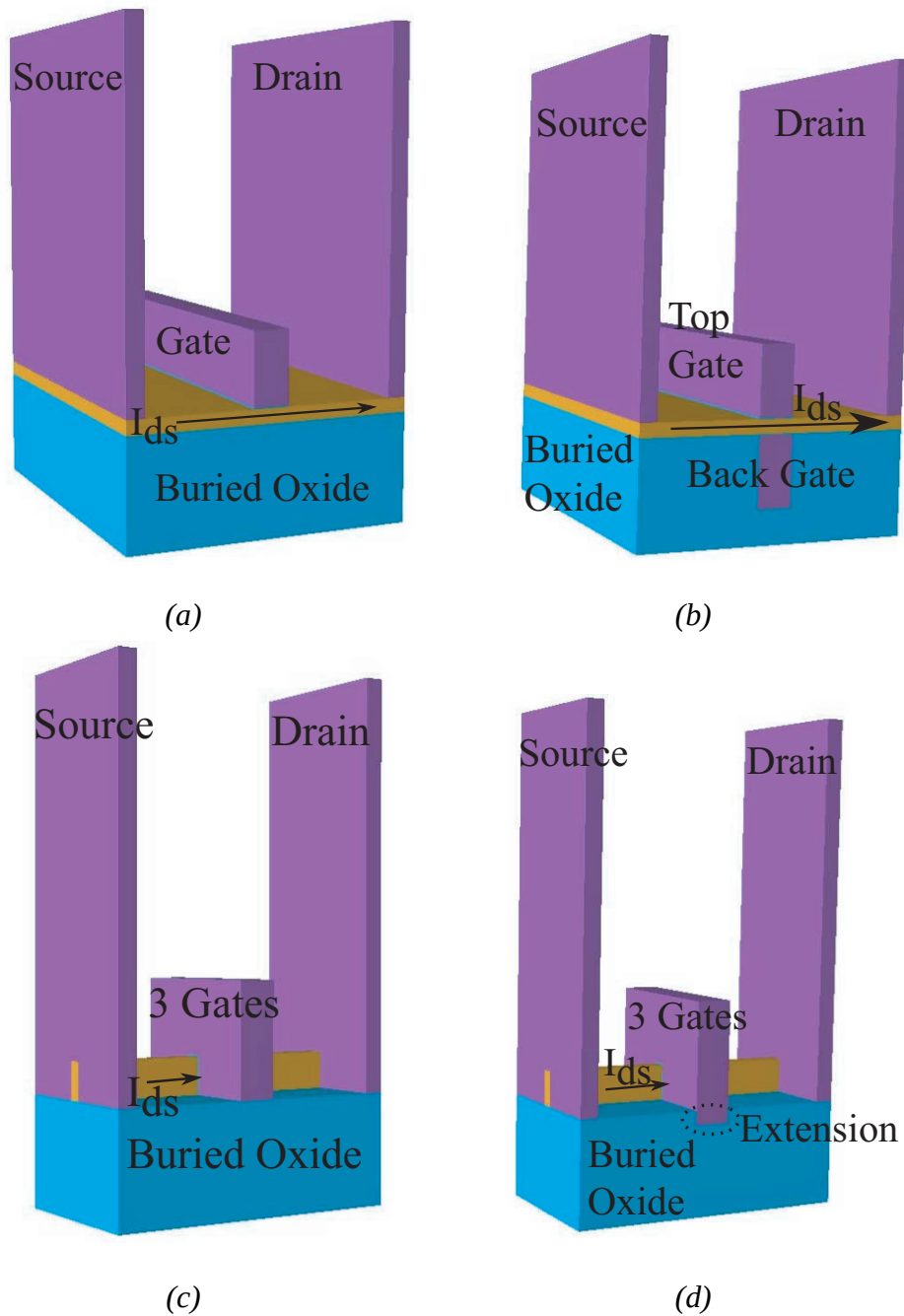


Figure 6.1: Schematic figures of the various multiple-gate architectures. (a) Single-gate, (b) Planar Double-gate, (c) Triple-gate, and (d) Pi-Gate (a derivative of the triple-gate, but with an extension into the buried oxide) with the source, drain and gate extensions. The diagrams shown here are without the oxide boundary material for clarity reason.

Device	C_{gd} (Ext) (fF/ μm)	C_{gd} (No Ext) (fF/ μm)	ΔC_{gd} (fF/ μm)	C_{gs} (Ext) (fF/ μm)	C_{gs} (No Ext) (fF/ μm)	ΔC_{gs} (fF/ μm)	f_T (Ext) (GHz)	f_T (No Ext) (GHz)	Δf_T (%)
SG	0.54	0.49	0.04	1.42	1.37	0.05	36.7	38.7	5.44
DG	0.47	0.45	0.02	1.71	1.67	0.04	29.1	30.1	3.44
TG	0.60	0.48	0.12	1.97	1.65	0.32	31.2	37.1	18.9

Table 6.1: Difference in the effect of simulations with and without the extensions of the drain and source on the various devices with $L = 200 \text{ nm}$ analyzed here at $V_{ds} = 1.0 \text{ V}$ and $V_{go} = 100 \text{ mV}$.

transistors.

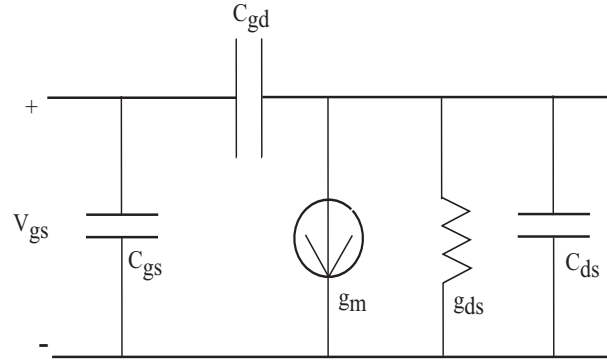


Figure 6.2: Conventional small signal equivalent circuit used for the extraction of intrinsic elements of the various MOS transistors.

6.2.1 Subthreshold static performance

Tables 6.2 and 6.3 show the description of the various single-gate, double-gate, triple-gate and pi-gate MOS simulated. The devices were first characterized in the subthreshold regime. This is an important regime for digital applications. The threshold voltage (V_{th}) was extracted using the constant-current method. In this method, the V_{th} was extracted as the corresponding gate voltage when the drain current was

at a current of $1.0 \times (W/L) \mu A$. The other figure of merits important in the subthreshold regime of operation are the subthreshold slope (S) and the drain induced barrier lowering (DIBL). From Table 6.2 and 6.3, the S and the DIBL values clearly show the advantageous of the multiple-gate architecture over the SG one. These improvements in the values for S and DIBL are attributed to the improved charge control of the multiple-gate architecture on the silicon film. When we analyze the characteristics between the multiple-gate devices alone, we see that the TG and PG architectures show improvement over the DG architecture. These improvements become evident as the channel length of the devices reduces.

L (nm)	t_{Si} (nm)	V_{ds} (V)	V_{th} (V)				S (mV/decade)			
			SG	DG	TG	PG	SG	DG	TG	PG
200	20	0.05	0.32	0.35	-	-	64.9	59.9	-	-
		1.00	0.27	0.36	-	-	65.3	59.9	-	-
100	20	0.05	0.24	0.37	0.40	0.40	91.7	61.1	59.8	60.7
		1.00	0.08	0.35	0.38	0.38	99.9	61.1	61.3	60.6
75	20	0.05	0.17	0.37	0.40	0.40	136.4	63.8	61.8	62.8
		1.00	-0.14	0.34	0.38	0.38	115.7	64.4	62.7	63.1
50	20	0.05	-0.085	0.35	0.39	0.40	218.8	77.3	75.3	74.2
		1.00	-1.17	0.27	0.33	0.33	523.0	81.8	78.7	77.3
25	20	0.05	-	-	0.32	0.33	-	-	232.5	183.9
		1.00	-	-	-0.35	-0.32	-	-	445.4	365.3

Table 6.2: Properties of the various multiple-gate SOI MOSFET devices analyzed all with a gate oxide thickness of 2 nm.

6.2.2 Analog static Analysis

Figure 6.3 shows the extracted simulated transconductance-to-current ratio dependence on the normalized (with regards to the total width of the device) drain current at $V_{ds} = 1.0$ V for the various gate lengths. From the curves, it is clear that the DG architecture has much higher g_m/I_{ds} values compared to the SG MOS device. In the weak inversion

L (nm)	t_{Si} (nm)	DIBL (mV/V)			
		SG	DG	TG	PG
200	20	45	11	-	-
100	20	160	16	21	21
75	20	305	32	21	26
50	20	1142	89	63	74
25	20	-	-	700	674

Table 6.3: Drain-induced barrier lowering values of the various multiple-gate SOI MOSFET devices analyzed all with gate oxide thickness of 2 nm.

region, we see that the DG devices are able to achieve g_m/I_{ds} values of nearly 38 V^{-1} which reflects on a near ideal subthreshold slope value ($S = \ln(10)/(g_m/I_{ds}) = 60 \text{ mV/dec}$) for a device with $L \geq 100 \text{ nm}$. In the strong inversion regime, the multiple-gate devices were much better compared to the SG architecture. For g_m/I_{ds} between 10 to 5 V^{-1} corresponding to V_{go} from 200-400 mV, typical for analog/RF biases, the simulated normalized current drive shows that the short channel effects are not dominant and confirm the experimental increase observed in DG when compared to SG. This is because in the experimental devices, it was not possible to separate the influence of both body factor and effective mobility (μ). However, in the simulation, the influences from the body factor and mobility can be separated and analyzed. Figure 6.4 shows the dependence of the carrier concentration and mobility on the change in gate bias in the silicon film of a multiple-gate structure at $V_{ds} = 1.0 \text{ V}$ and $L = 100 \text{ nm}$ extracted at $x = L/2$ at 1 nm below the surface and center ($t_{Si}/2$). As presented in Figure 6.4, we see clearly that at low V_{go} , the carriers concentration at the surface and center of the film is the same for $V_{gs} > V_{th}$. At the surface and center of the film, we see that the carrier concentration is higher than the doping level. However, as V_{gs} increases, the carrier concentration at the gate oxide interface becomes important and creates a screening effect on the carriers in the center of the film. This screening effect causes the potential in the center of the film to saturate as the potential at the surface of the film increases with the increase of V_{gs} leading to an imbalance in the carrier concentration distribution. The rate of increase of the carriers at the surface is much

higher compared to the center of the film. Thus, the increase in the mobility of the carriers due to the reduced vertical electric field at the center film is still not enough to cancel out the dominant carriers at the surface of the film at high V_{gs} . Therefore, from Figure 6.4, it can be concluded that when V_{go} is low (thus operation in the weak and medium inversion region), the dominant current drive comes from the center of the film, but as V_{gs} increases (strong inversion), this shifts towards the carriers at the surface of film. When the device is operating at strong inversion, the DG devices will behave as a dual-channel device and if we extract the non-normalized current of both DG and SG devices, we see that the I_{dsDG}/I_{dsSG} approaches 2.

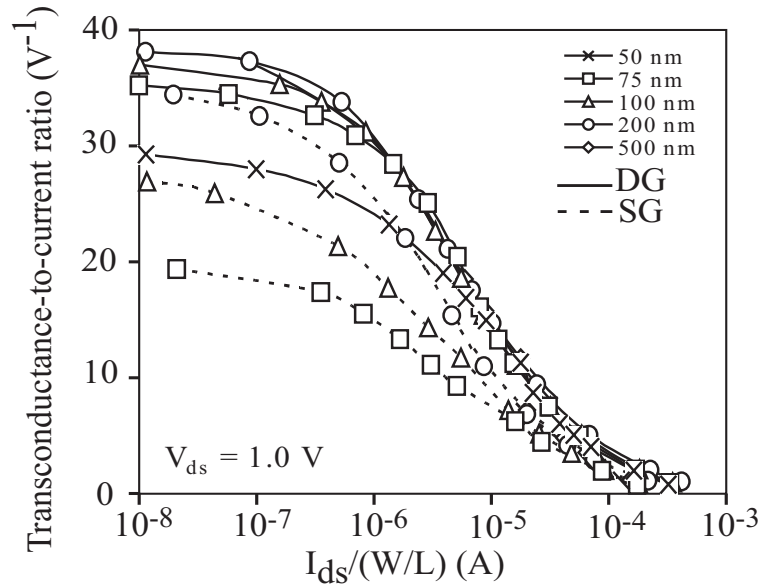


Figure 6.3: Extracted simulated transconductance-to-current ratio dependence on the normalized drain current at $V_{ds} = 1.0$ V of the various gate lengths.

Figure 6.5 shows the various ratios of the normalized (with regards to the total width of the device) transconductance values of devices with a gate length of 100 nm and $V_{ds} = 1.0$ V and for various gate overdrives ($V_{go} = V_{gs} - V_{th}$).

From the curves in Figure 6.5, it is clear that the multiple-gate de-

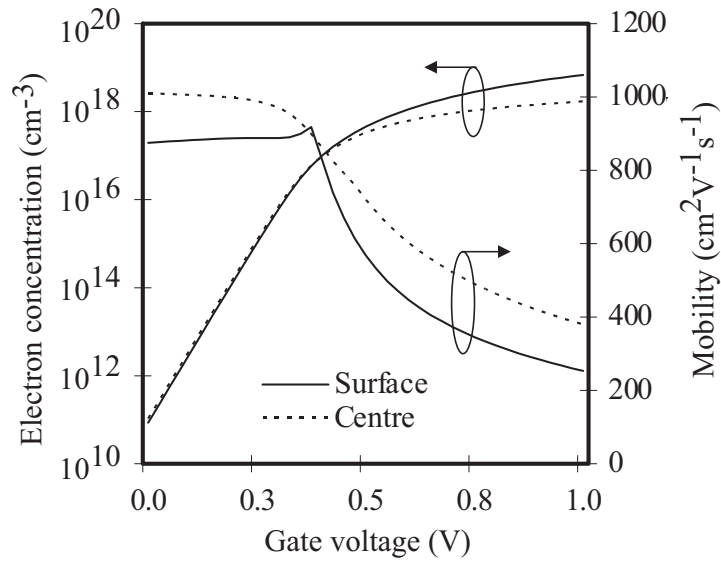


Figure 6.4: Carrier concentration and mobility versus gate bias in the silicon film of a multiple-gate structure at $V_{ds} = 1.0$ V and $L = 100$ nm extracted at $x = L/2$ at 1 nm below the surface and center.

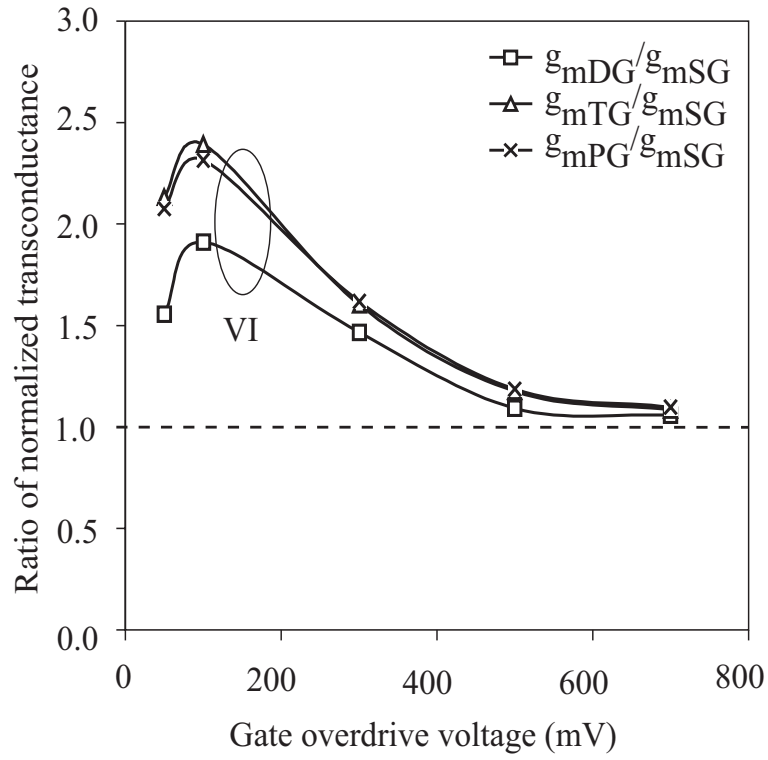


Figure 6.5: Ratios of the normalized transconductance values of the various simulated devices with a gate length of 100 nm and $V_{ds} = 1.0$ V and for various gate overdrive voltages.

vices have much higher g_m values compared to the single-gate architecture. These higher g_m values in the multiple-gate devices is contributed to the much efficient coupling of the gates compared to the SG architecture. If we analyze the curves at low V_{go} , it is clear that the PG, TG and DG all have higher g_m ratio values compared to the SG MOS device. As V_{go} increases, this g_m ratio for the multiple-gate devices tend to 1 because the advantageous effect of the volume inversion phenomenon is lost. The effect of the volume inversion decreases as V_{go} increases is due to the increase in the carrier concentration at the interfaces. This increase of the carrier concentration at the gate oxide interface creates a sort of screening effect on the carriers in the center of the film. It is worth mentioning here that the ratio for the devices tends to 1 and because of the normalization with regards to the total width of each devices. It is worth to note that for the $W_{DG} = 2W_{SG}$ and for the TG and PG, the normalized width is $H_{fin} + 2 \times W_{fin}$. Due to this screening effect becoming stronger as the gate bias increases, the charge concentration at the center of the film reduces leading to a reduction in the current drive and thus a lower g_m ratio is obtained with the final ratio close to 1 for all the devices (with normalized width). Figure 6.4 show these changes in the carrier concentration. Figure 6.6 shows the dependence of the normalized transconductance of the multiple-gate devices with the gate overdrive voltage at $V_{ds} = 1.0$ V. We see that the improvement for the multiple-gate devices is due to the volume inversion and not related to the different maximum point of transconductance achieved for the various devices. At higher gate voltage overdrive, we see that the transconductance per unit width of the various devices tend to saturate due to the normalization factor taken into account. It is expected that for each devices an individual maximum transconductance will be reached at higher gate overdrive. After this peak is reached, there is a decrease in the transconductance values to the increase of the vertical electric field. The increase of the vertical electric field and the influence on the mobility of the electron leads to a reduction of the electron mobility, the multiple-gate devices will still have better transconductance values due to the slightly improved charge control from the multiple-gate compared to the single-gate structure.

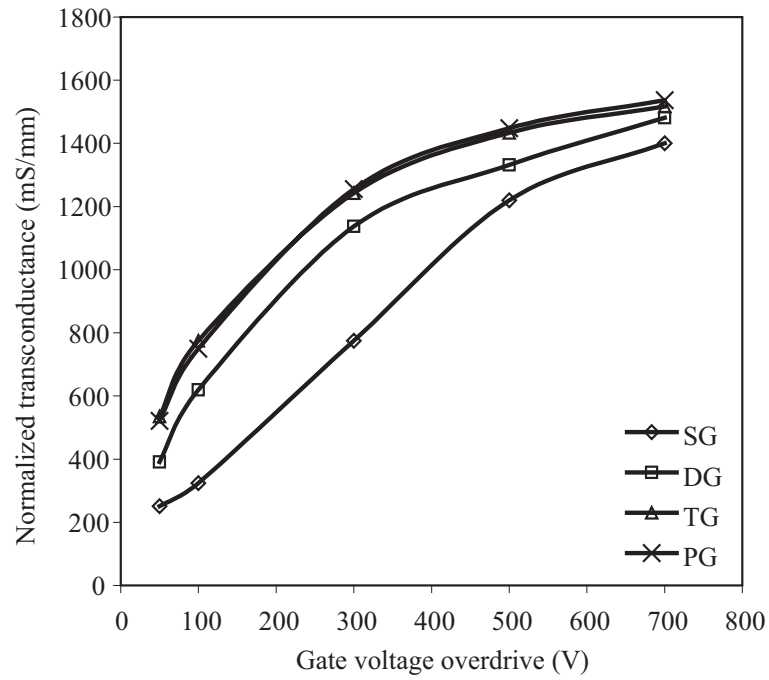


Figure 6.6: *Dependent of the various normalized transconductance of the simulated multiple-gate devices with the various gate overdrive voltage at $V_{ds} = 1.0$ V.*

6.2.3 AC Analysis

The main purpose of the small-signal simulations is to analyze the cut-off frequency of the device. The cut-off frequency is a figure of merit which corresponds to the frequency point when $H_{21} = 0 \text{ dB} = 1$. The cut-off frequency, f_T is defined in equation 6.1.

$$f_T = g_m / 2\pi(C_{gs} + C_{gd}) \quad (6.1)$$

C_{gs} is the gate-to-source capacitances and C_{gd} is the gate-to-drain capacitances. In order to assure that a fair comparison is made between the different technologies, the channel lengths and device types, they were simulated at various gate overdrive voltages [VS04]. The effect of the volume inversion on the small-signal behavior of the devices will also be analyzed. From Equation 6.1, it is clear that to obtain higher f_T , g_m needs to be high. Other criteria to obtain a higher f_T value is to obtain higher g_m/C_{gs} and C_{gs}/C_{gd} ratios.

Generally, in order to obtain a good cut-off frequency value, the transconductance of the device and the C_{gs}/C_{gd} ratio should be high. This C_{gs}/C_{gd} ratio represents the capability of the control of the device on the charges. In an ideal device, in saturation region, $C_{gs} = \frac{2}{3}C_{ox}$ and $C_{gd} = 0$. If this ratio decreases, this translates into an increase in the feedback C_{gd} parasitic capacitance. Thus, an increase in the C_{gs}/C_{gd} ratio will improve the cut-off frequency. The C_{gs}/C_{gd} ratio is also important as it influences the maximum frequency of oscillation, f_{max} . A high g_m/C_{gs} ratio is needed to obtain a high transconductance and low parasitic capacitance between the gate-to-source. The combination seen in Equation 6.1 combines these two ratios and shows the relation between them.

Equation 6.2 shows the f_{max} expression [DR02]

$$f_{max} = \frac{f_t}{2\sqrt{2\pi f_T R_g C_{gd} + g_d(R_g + R_s + R_{gSi})}} \quad (6.2)$$

From Equation 6.2, it is important to notice that f_{max} is expressed as a function of f_T . This relation shows that the C_{gs}/C_{gd} ratio plays an

important role here. The g_m/C_{gs} ratio will also be important as it shows the effect of the parasitic capacitances of the devices. The analysis here will concentrate mainly on the effect in the intrinsic channel and the influence of the extrinsic access of the devices.

6.2.3.1 Intrinsic capacitances

Figure 6.7 shows the gate-to-source capacitances of the various multiple-gate devices normalized to that of the SG extracted at $V_{ds} = 1.0$ V and gate length of 100 nm at various V_{go} . It is clear from the curves that at low V_{go} , the C_{gs} ratios for the various devices are much higher than 1. However, as the V_{go} increases, this ratio tends to the value of 1. The higher C_{gs} ratios at low V_{go} is attributed to the volume inversion effect in the multiple-gate devices. As seen in the effect in the DC transconductance analysis, as V_{go} increases, the VI reduces in its effect thus bringing this ratio down to 1 which for the DG device is expected. One clear observation from Figures 6.7 Figure 6.5 is that in the VI operation region, the increase in the g_m in the multiple-gate devices will be balanced off with the simultaneous increase of the C_{gs} values leading to nearly no impact of the VI on the f_T intrinsic values.

Figure 6.8 shows the various C_{gs}/C_{gd} ratios for different V_{go} obtained at $V_{ds} = 1.0$ V and gate length of 100 nm. Here it is again clear that the same trend can be observed between the measured and the simulated devices. In the C_{gs}/C_{gd} ratios obtained, we see that the multiple-gate architectures display much higher ratios compared to the SG device. This increase in the C_{gs}/C_{gd} ratios is due to the decrease of the SCE of the multiple-gate structure which translate to a reduction of the Miller capacitances especially when the gate length reduces. This reduction in the Miller capacitance will play an important role as will be shown later because it balances the increase of the extrinsic capacitances in the multiple-gate structures leading to a higher f_T value overall.

6.2.3.2 Parasitic capacitances

i) Influence of contact access

The contact access of the simulated devices has been simulated as close as possible to match the situation of the real device in order to take into account all the associated effect(s) related to the capacitances.

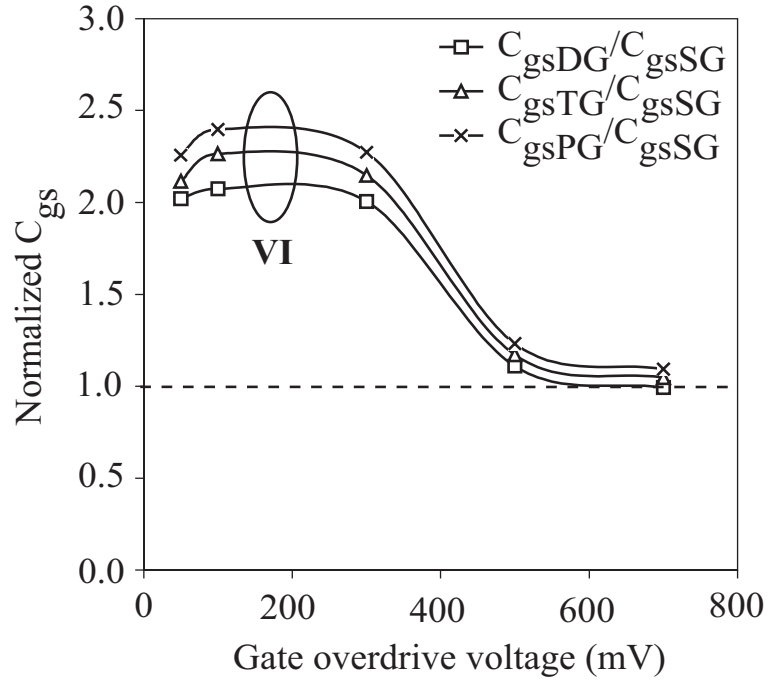


Figure 6.7: Gate-to-source capacitances of the various multiple-gate devices normalized to that of the SG extracted at $V_{ds} = 1.0$ V and gate length of 100 nm at various V_{go} .

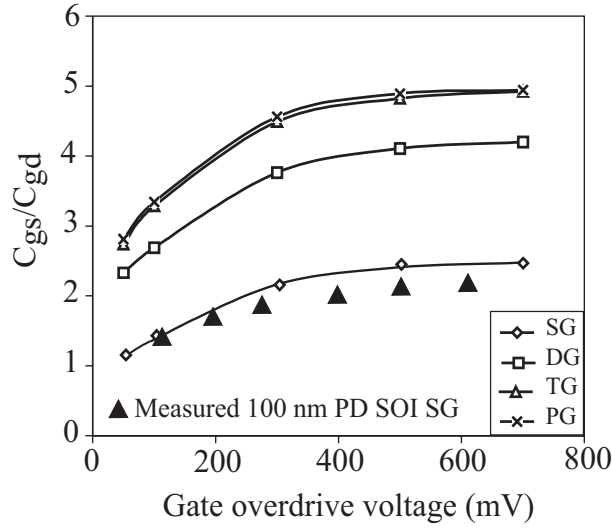


Figure 6.8: Various C_{gs}/C_{gd} ratios versus V_{go} at $V_{ds} = 1.0$ V and gate length of 100 nm.

Figure 6.9 shows the normalized gate-to-source capacitances for the different multiple-gate devices for a gate length of 100 nm at $V_{ds} = 1.0$ V at the different V_{go} . In order to examine the effect of the contact access on the extrinsic parasitic capacitances, different gate widths were examined for the different devices:

1. $W_{SG} = 1 \mu m$ for SG;
2. $W_{DG} = 2 \mu m$ for DG;
3. $W_{TG} = 2.H_{fin} + W_{fin}$ for TG, i.e. 120 nm ($H_{fin} = 50$ nm, $W_{TG}/L = 1.2$) and 420 nm ($H_{fin} = 200$ nm, $W_{TG}/L = 4.2$).

From Figure 6.9, it is clear that there is a trend in the increase in the total capacitances of the devices in the following order $TG > DG > SG$. The increase in the total capacitances (intrinsic and extrinsic) of the multiple-gate architecture originates from the more complex 3-D interconnection structure for the gate contact. This increase in the total capacitances will overall contribute to a lower f_T value in the multiple-gate structure. This effect of the gate access on the f_T becomes more prominent when the gate length is long (when $L \geq 150$ nm). Figure 6.10

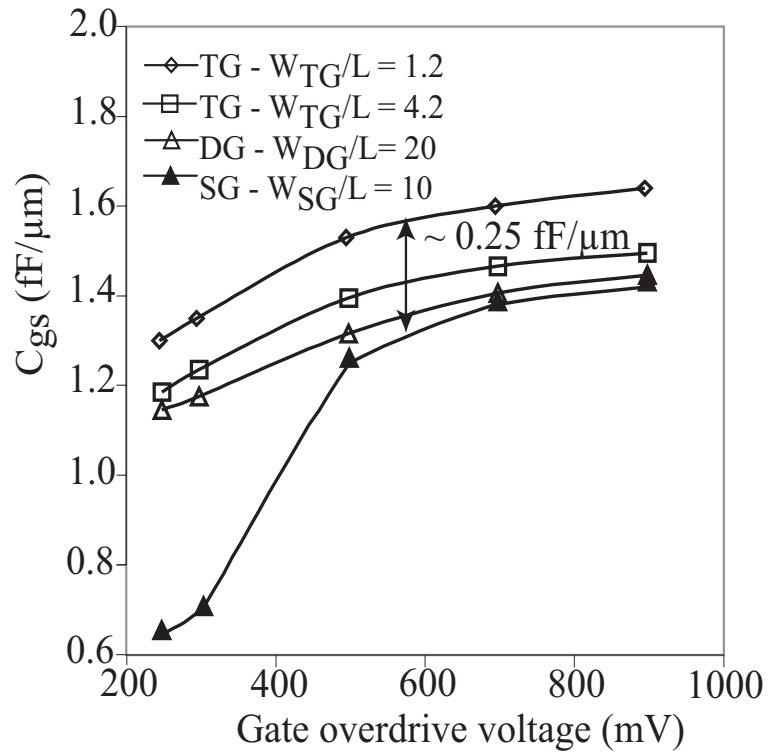


Figure 6.9: Normalized gate-to-source capacitances versus V_{go} for the different multiple-gate devices for a gate length of 100 nm at $V_{ds} = 1.0 \text{ V}$.

shows the dependence of the cut-off frequency for the various devices extracted at $V_{ds} = 1.0$ V and $V_{go} = 500$ mV. However, since the aim of

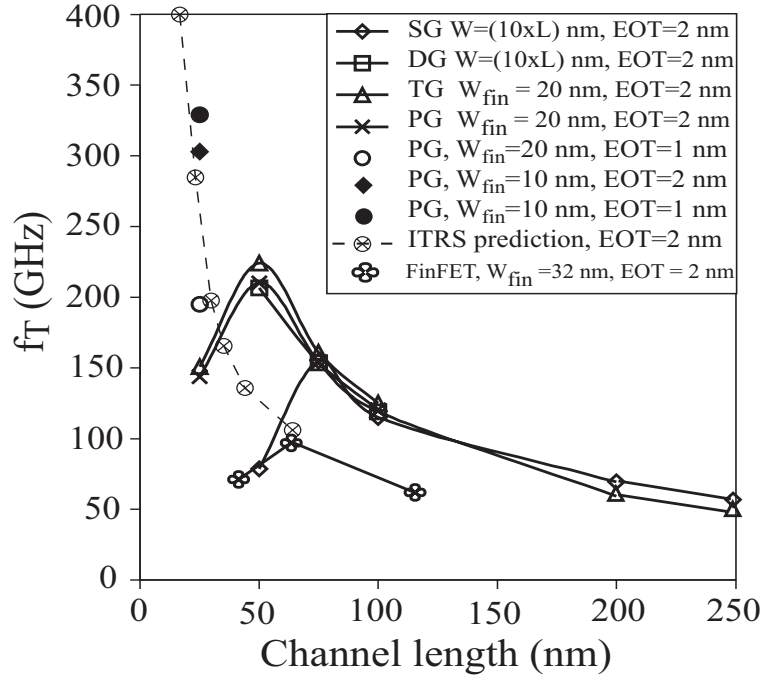


Figure 6.10: Dependence of the cut-off frequency for the various devices extracted at $V_{ds} = 1.0$ V and $V_{go} = 500$ mV.

the multiple-gate devices is to be mainly applied for future nodes, we see from Figure 6.10 that below 75 nm gate length, the advantage of using multiple-gate devices is obvious as the f_T value is much higher compared to the SG structure. This change in the f_T values is due to the improved control of the gates and the reduced SCE in the multiple-gate structures contributing to a higher g_m . Previous values extracted from measured devices shows that the extrinsic capacitances related to the interconnections can be extracted and values approximately 0.2 fF and 0.4 fF for the SG and FinFET SOI MOSFET, respectively have been obtained [LKR⁺05] [DRL⁺03]. These extracted values from the measured devices shows a good agreement with the simulated device where a value of 0.25 fF was obtained from the extraction in Figure 6.9.

ii) Influence of W/L ratio

In order to see the importance of the parasitic capacitances especially for the TG structure, different TG with different W/L ratios were simulated. Figure 6.9 shows the effect of this change in the W_{TG}/L ratio extracted at $V_{ds} = 1.0$ V at various V_{go} for $L = 100$ nm. It is clear from the curves that there is a big change in the total normalized capacitances as the ratio changes from 1.2 to 4.2 in the TG structure. Moving from $H_{fin} = 50$ to 200 nm shows a decrease of the normalized parasitic capacitances of nearly 0.15 fF/ μm . From these results, it is clear that in the TG structure, one of the most important factor contributing to the parasitic capacitances is the fringing field between gate-to-source and gate-to-drain through the buried oxide. Thus, in order to decrease these parasitic capacitances related to the 3-D structure, it is important that the H_{fin} of the TG or the FinFET be increased. Increasing the H_{fin} in the TG or FinFET will lead to an overall increase in the RF performances as well as increasing the drive current per unit die area [AHBC03]. As seen earlier in Figure 6.10, it is clear that the advantages of the multiple-gate structure in the dynamic region becomes obvious when the gate length is small. However, from Figure 6.10, it is also clear that further reduction of the gate length below approximately 40 nm, we will begin to see a degradation in the analog and RF performance of the devices. This prediction seen in the numerical simulation is also observed in the measured FinFET device with $W_{fin} = 32$ nm and from gate lengths from 120 to 40 nm. In this particular FinFET, we see that the peak of the cut-off frequency is reached when the gate length is 60 nm and the same drop off in the cut-off frequency value is seen at gate length of 40 nm. It is worth noting here that the experimental device has lower values of f_T compared to the simulated device because in the simulation, an ideal device was assumed, i.e. no surface states, no interstitial damages, etc. which reduces the mobility of the carriers. However, the most important contribution to this difference between the simulated and measured devices is contributed to the source and drain resistances, R_s and R_d which are the most parasitic elements in FinFETs. The three dimensional nature of the contacts between the silicon and silicide in the highly doped source and drain regions are the main contributor to R_s and R_d . These resistances are highly dependent on the width of the fins. In our simulations, the effect of R_s and R_d were not taken into account. Due to this, we see that the f_T values for the simulation results are much higher

compared to the measured devices. This degradation of the devices below a gate length of 60 nm (the peak in Figure 6.10) is contributed to the increase of the SCE in the devices which reduces the transconductance and the increase of the parasitic capacitances. This increase in the SCE is related to the fact that the film thickness (fin width) is not scaled down along with the gate length. In the requirements of the ITRS in this region, we see that there is still a difference to be filled between the predictions of the ITRS up till the year 2015 compared to the results shown from the simulated devices. Thus, in order to fulfill the requirements of the ITRS for channel lengths well below the 50 nm region, it is important that channel/gate engineering solutions should be found for thinning down the silicon film (either t_{Si} or W_{fin}) to less than 10 nm. Another solution that would be able to even bring the advantages of the multiple-gate structure further would be the use of high-k materials for obtaining lower equivalent oxide thickness of less than 1 nm without increasing the gate leakage current as seen in Figure 6.10. However, when thinning down the silicon film, this will lead to an increase in the access source and drain resistances, and thus to overcome this problem, optimized silicidation, localized silicon epitaxy or low Schottky barrier contacts will have to be options available in the fabrication of these devices.

6.3 Experimental results: FinFETs

6.3.1 FinFET architectures

The experimental devices used for comparison with the simulated devices were FinFET devices fabricated at the Interuniversity Microelectronics Center (IMEC). The devices were formed using e-beam. The active area was formed via mesa etching. After the formation of the active area, the wafers were oxidized to form a 15 nm thick oxide at 1150°C. This step is necessary to provide a sufficient rounding of the fins to reduce the fin width. After the removal of the 15 nm oxide, a 100 nm polysilicon layer was deposited on top of a 2 nm (EOT) nitrified oxide. The gate of the FinFETs were patterned using 248 nm optical lithography with resist trimming, resulting in gate lengths down to 50 nm. High angle extension implantations using 70 nm RTCVD nitride

spacers, As^+P and B deep source/drain implants as well as NiSi silicide was performed. The devices were finished with a standard back-end process. Figure 6.11 shows the schematic cross-section of the experimental device analyzed. The FinFETs measured were of three different

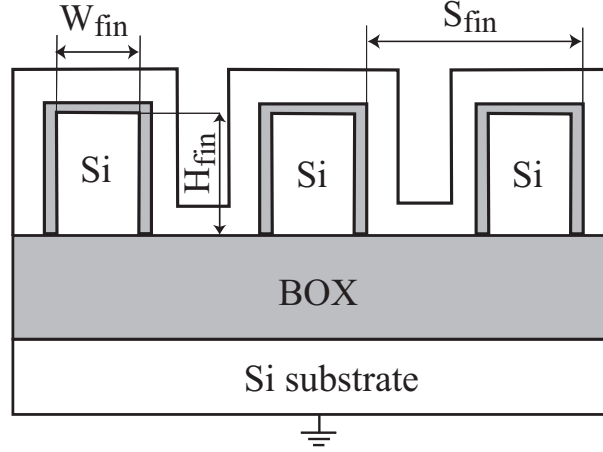


Figure 6.11: Schematic example of a FinFET transistor fabricated from the process from IMEC as described in [DKC⁺05].

types coming from the different arrays of transistors. They were:

- multifin MOSFETs with fixed width (W_{fin}) of 35 nm and different lengths (L), varied from 50 nm to 10 μm with 66 fins (N_{fins}) and $H_{fin} = 75$ nm;
- fixed length, L of 10 μm and different W_{fin} varying from 35 nm to 10 μm and $H_{fin} = 95$ nm;
- FinFETs embedded in coplanar feed lines for RF measurements with $l = 50$ nm, $W_{fin} = 50$ nm, $H_{fin} = 75$ nm and fin spacing, $S_{fin} = 100$ nm.

The multifin MOSFETs were fabricated using e-beam lithography. Another FinFET device that was analyzed was a multifin MOSFET with a fixed width of 32 nm and different gate lengths (L), varied from 120 to 40 nm with $W_{finger} = 2$ μm , $N_{finger} = 50$, $H_{finger} = 60$ nm and $S_{finger} = 328$ nm. The devices all had nitrided gate oxide with 2 nm equivalent

gate oxide thickness (EOT), an high angle extension implantation of As+P and B deep source/drain with the presence of 70 nm RTCVD nitride spacers, NiSi as a salicide, polysilicon gate and a channel doping of $6 \times 10^{18} \text{ cm}^{-3}$.

6.3.2 Measured DC characteristics

I_{ds} - V_{gs} measurements were conducted on the various FinFETs. Figure 6.12 shows the I_{ds} - V_{gs} characteristics measured at $V_{ds} = 50 \text{ mV}$ for the $10 \mu\text{m}$ channel length FinFET as a function of the fin width (W_{fin}). There are clearly several different conduction mechanisms for the dif-

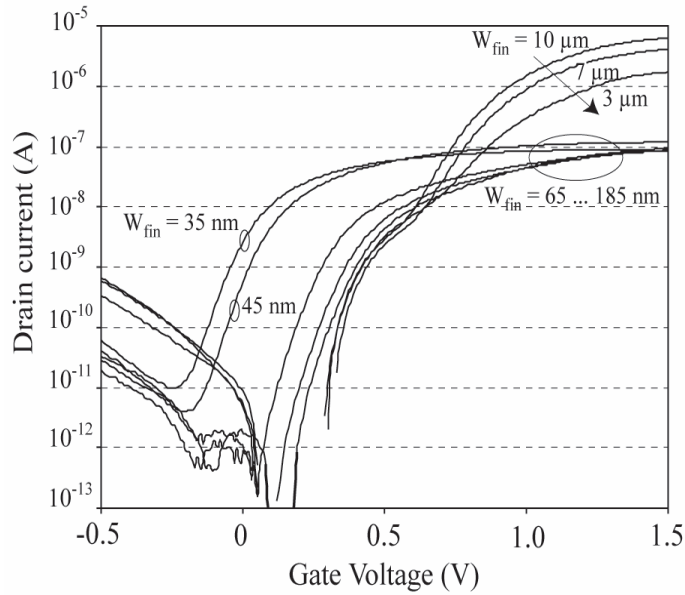


Figure 6.12: I_{ds} - V_{gs} characteristics measured at $V_{ds} = 50 \text{ mV}$ for the $10 \mu\text{m}$ channel length FinFET as a function of the fin width (W_{fin}).

ferent FinFETs. At high gate voltage, FinFETs with large W_{fin} , it is clear that the top gate conduction is proportional to W_{fin} . When the gate voltage is reduced below approximately 0.7 V, another I_{ds} - V_{gs} can be seen. This new I_{ds} - V_{gs} slope corresponds to the additional conduction along the lateral sides of the fin. Another observation is that as

the W_{fin} decreases, there is an increase in the coupling between the two lateral gates and this changes the operation of the fin from partially depleted (PD) to fully depleted (FD). This observation is due to the dependence of the threshold voltage on the fin width which is also the film thickness as shown in [ESS04]. Such a characteristic of the FinFET is an advantage because this shows that the FinFET and in general, multiple-gate devices are capable of providing more freedom in the design of analog applications in realization of multi-threshold processes (devices with different threshold voltages on the same wafer) by just varying the fin width.

The other important figure of merit which is used for the assessment of the FinFET is the intrinsic gain (g_m/g_{ds}). This intrinsic gain can be seen as g_m/I_{ds} times I_{ds}/g_{ds} . The g_m/I_{ds} (transconductance-to-current ratio) represents the efficiency of the device to convert DC power into AC frequency and the gain performance of the device [SFJ96]. It is thus an important parameter in the design of analog circuits. The g_m/I_{ds} has an added function when it is represented as a function of the normalized current ($I_{ds}/(W/L)$) where W is the total gate width. Such a representation can be used to analyze devices of various dimensions and compared on the same curve because then it becomes independent on the threshold voltage and device length with the condition that the short channel effects are negligible [SFJ96] [KNV⁺03]. The Early voltage V_{EA} represented by I_{ds}/g_{ds} , which can also be used to represent the output conductance, (g_{ds}), is important because it avoids the dependence on the drain current and emphasizes the length dependence [KNV⁺03]. Figure 6.13 shows the dependence of the $I_{ds}/(W/L)$ measured at a given transconductance-to-current ratio versus W_{fin} in saturation at $V_{ds} = 1.0$ V. The current was normalized to the width of the device. This normalization was done based on the analysis obtained from Figure 6.12. In this particular extraction method, the drive current at a fixed g_m/I_{ds} was extracted. For each of the individual devices, the V_{gs} corresponding to the fixed g_m/I_{ds} was extracted and compared to the top and lateral threshold voltages of the individual devices. For devices that are wide and moderately-wide, the region of operation was verified, indicated by the top and side conductions, and when these criteria were fulfilled, the W used for the normalization was $2H_{fin} + W_{fin}$. For the narrow devices and with only side conductions, the W used for the normalization was

$2H_{fin}$ which indicated that only the side is effective in contribution to the drive current. In Figure 6.13, it is clear that there is a big increase in the normalized current for the narrowest FinFET by a factor larger than 2. This large increase can be attributed to the volume inversion (VI) regime observed in multiple-gate devices [ESS04]. As the width of the fin increases, the devices moves from operation in the FD to the PD operation mode. This is can be observed by the first decrease of the drive current due to the increased body effect and lower mobility. However, as W_{fin} increases, there is an increase in the drive current. This increase can be due to the improvement in the carrier mobility because of the transfer of conduction from lateral to top channel. This transfer of conduction means a change in the crystalline plane where the carriers are flowing, from the $\langle 110 \rangle$ plane to the $\langle 100 \rangle$ plane which increases the electrons mobility [CLY04].

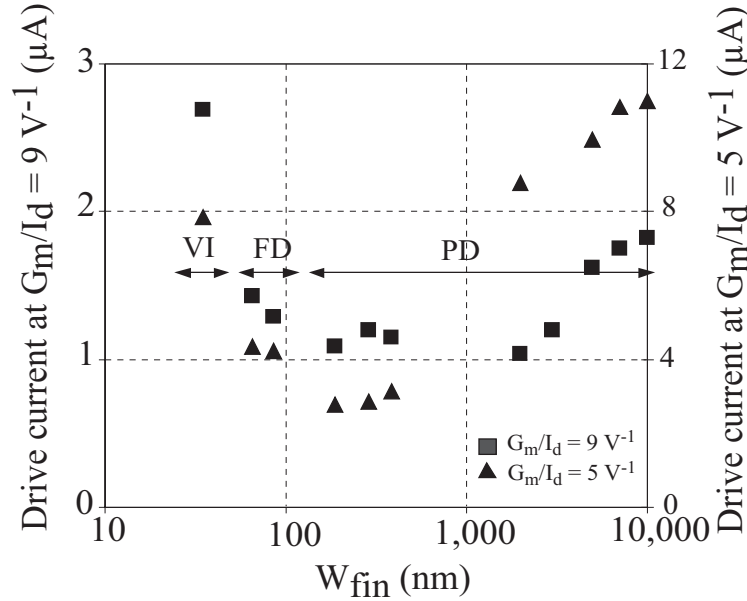


Figure 6.13: Dependence of the $I_{ds}/(W/L)$ versus W_{fin} for $L = 10 \mu\text{m}$ and 2 different fixed g_m/I_{ds} values at $V_{ds} = 1.0 \text{ V}$.

As mentioned earlier, the Early voltage is used as an indication of the output conductance of the device with the advantage that it is independent of the I_{ds} . Figure 6.14 shows the extracted V_{EA} for various

W_{fin} for a 10 μm long FinFET at $V_{gs} = 0.5$ V and $V_{ds} = 1.0$ V. It is clear that for large W_{fin} , the devices operates in the PD mode and the V_{EA} values are rather low which means that the g_{ds} of the devices are high in saturation. These values are further deteriorated by the kink effect as seen previously in Figure 6.12 for the large W_{fin} dimensions. However, as the W_{fin} of the devices reduces, it is clear that the mode of operation changes to PD without the kink effect kicking in and later into the FD operation. Such a change in the operation in the devices are seen by the reduction of the kink effect, the increase in the channel control and the improvement in the V_{EA} values. Devices which have very narrow W_{fin} , we see a big increase in the V_{EA} in the order of 100 V per μm of channel length. This tremendous increase in the V_{EA} values is attributed to the VI effect which has been shown in previous works, for example values of $V_{EA} = 13$ V were seen for a 0.2 μm long FD SG MOSFET operating in Quasi DG regime [KCT⁺03] and $V_{EA} = 150$ V for 3 μm long GAA DG devices as seen in Chapter 3 and also [PMC⁺03]. Figure 6.15 shows the dependence of V_{EA} on the channel length with $W_{fin} = 35$ nm at $V_{ds} = 1.0$ V and $V_{gs} = 0.5$ V. It is clear that there is an improvement in the Early voltage of the devices when compared to other reported values of SG SOI and bulk devices [KCT⁺03] [KNV⁺03]. If we compare a device at channel length of 100 nm, we see that the V_{EA} of the FinFETs are approximately 10 V compared to the SG SOI and bulk of only 1-4 V in saturation. However, one point that should be remembered is the self-heating effect in the devices. It has been reported previously that the self-heating effect can artificially improve the Early voltage of the device in DC operation. Thus, in order to verify that such tremendous gains in the Early voltage of the FinFETs is not related to this self-heating effect, the drain conductance was measured in the 50 kHz-100 MHz frequency range. From these small-signal measurements, nearly no variation in the g_{ds} values were observed even when the measurements reached the 100 MHz frequency range. This indicated that in the devices measured, the self-heating effect can be neglected. Both the results from the measurements and the simulation show a good agreement in the trend for the various gate lengths. Therefore, it is clear that the improvements in the Early voltages of the FinFETs can truly be attributed to the increased control of the charges by the gates in the volume inversion mode.

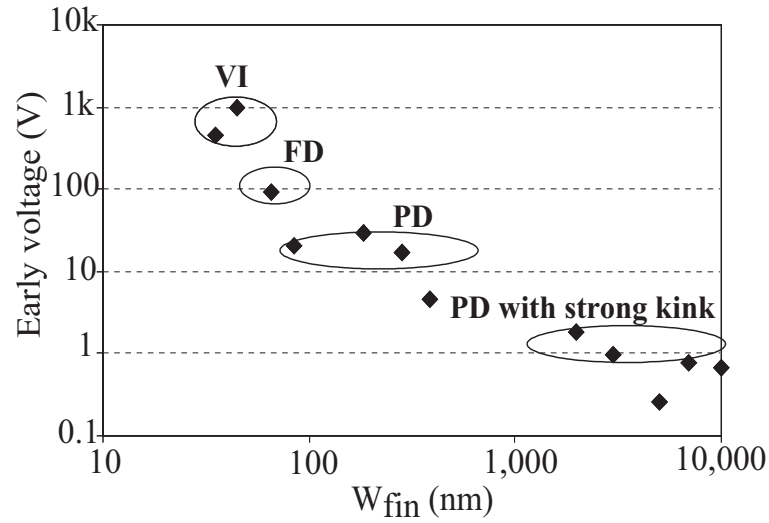


Figure 6.14: Variation of the Early voltage values with fin width for a channel length of $10\ \mu\text{m}$ at $V_{gs} = 0.5\ \text{V}$ and $V_{ds} = 1.0\ \text{V}$.

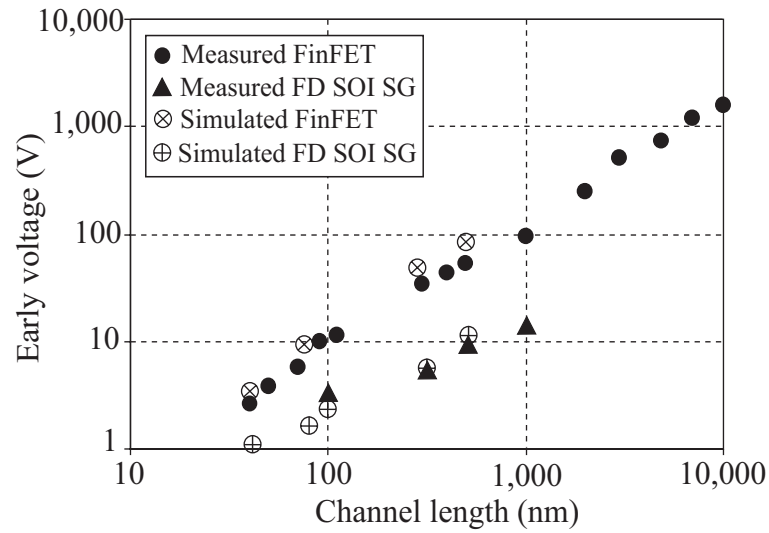


Figure 6.15: Variation of the Early voltage values with channel length for $W_{fin} = 35\ \text{nm}$ at $V_{gs} = 0.5\ \text{V}$ and $V_{ds} = 1.0\ \text{V}$ for the various measured and simulated devices with the same film thickness.

From the results obtained from the transconductance-to-current ratio and the Early voltage measurements, the intrinsic gain of the devices can be calculated. Figure 6.16 shows the dependence of the intrinsic gain on channel length. The intrinsic gain, A_o is calculated as $g_m/I_{ds} \times V_{EA}$. For FinFETs with 100 and 50 nm channel length, intrinsic gain values of around 30 and 20 dB, respectively, were obtained. These high gain values shows that the volume inversion effect on the Early voltage in the narrow FinFET devices is an important effect. These improvements in the A_o values shows that the multiple-gate devices can achieve the requirements of the ITRS. In the 90 nm-node (with a minimum digital physical gate length of 50 nm), from Table 1.4, we see that the requirement for $g_m/g_{ds} @ 5.L_{min-digital}$ is 100. From Figure 6.16, we see that the values of $g_m/g_{ds} @ 5.L_{min-digital}$ obtained, reached values of 318 and 480 for the measured and simulated FinFET, respectively. The higher value obtained from the simulated device is contributed to the ideal conditions assumed in the simulation. However, in general this improvement is due to the individual improvement of the g_m and the g_{ds} values in the multiple-gate structures. From these numbers, it can be predicted that the multiple-gate devices will have great potential when moving towards to the 50 nm-node and beyond in the analog and RF applications as seen in Table 1.4.

In order to further prove that FinFETs and more importantly multiple-gate devices are beneficial in accordance to the ITRS roadmap, numerical simulations were performed. These numerical simulations are not only important in verifying what have been shown in the measurements, but it can be used to understand deeper the role of the volume inversion in the silicon film. Numerical simulations is an important tool as discussed in Chapter 2 and in this work, plays an important role in analyzing the various multiple-gate architectures.

6.4 Conclusions

It is clear that the multiple-gate architecture is a very promising device for future applications in both analog and RF. From the analysis of the experimental and simulated devices, we have seen that multiple-gate devices shows good DC characteristics compared to the SG devices.

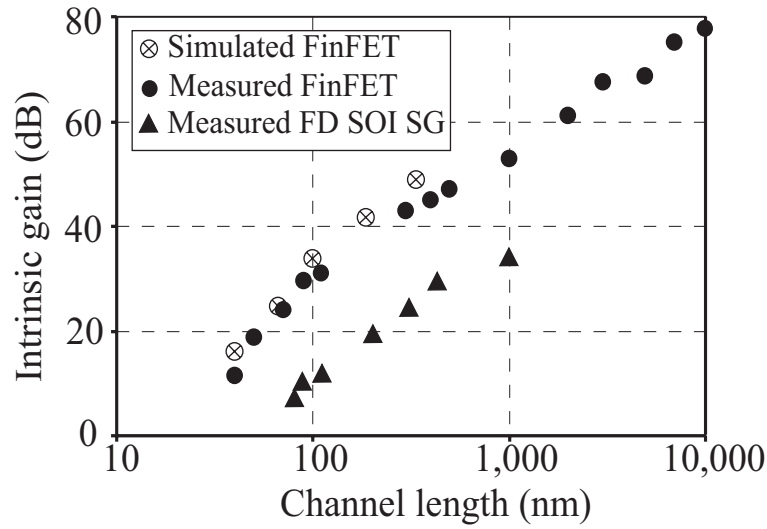


Figure 6.16: Measured and simulated intrinsic gain for the various channel lengths extracted at $V_{ds} = 1.0$ V. The measured intrinsic gain of the FD SOI MOSFET were from IMEC and was discussed in the paper by V. Kilchytska [KCT⁺03].

The intrinsic gain of the FinFETs are very much higher compared to the SG device at the same bias point. It is clear that these improvements in the multiple-gate structures over the SG structure is attributed to the volume inversion effect. This volume inversion effect contributes to a very much improved Early voltage values in the multiple-gate devices which leads to an overall increase in the intrinsic gain. This increase in the intrinsic gain of the devices is in accordance to the requirements of the ITRS within the sub-50 nm-nodes. We have seen this trend in both the measured and simulated devices.

In order to meet the RF requirements, the EOT needs to be shrunk down to 1 nm and the silicon film is reduced to at least 10 nm, the multiple-gate architecture is a very promising device to realize the predictions of the ITRS in the sub 50 nm-nodes and beyond. However, we have also seen the limitation of the multiple-gate architecture especially in regards to the parasitic capacitances. Due to the complicated 3-D interconnections, we have seen that the increase in the extrinsic capacitances for long channel devices make them non-viable for use,

but they become very advantageous when we move below the 75 nm gate length. The width/length ratio of the triple-gate and FinFET devices is an important aspect in reducing these parasitic capacitances. In order to reduce these parasitic fringing capacitances, it is encouraged to use higher width/length ratio which is in opposition with the optimized geometry for digital applications. It has been shown that in order for DG and TG FinFETs to meet ITRS targets for high performance (HP), low operating power (LOP) and low standby power (LSTP) logic technologies for the 65 nm technology node, these devices should be built with lower aspect ratios, along with lower values of fin height and thickness [KA05].

From the work done in this chapter, it is obvious that there are more advantages compared to the disadvantages from using the various multiple-gate structures presented here. It has also been shown that with various improvements in the fabrication and technologies applied to these structures, they can even be pushed further and this will realize the predictions of the ITRS to 2015 and beyond.

Chapter 7

Conclusion

In the framework of this thesis, it is clear that the main objectives and intentions set out in the beginning of this thesis have been achieved. Numerical simulation was used as the main analysis tool and when available, measured results were used to verify the simulation results. We have shown that the Graded-Channel architecture and multiple-gate SOI MOSFET devices have the potential to satisfy the requirements set out in the ITRS table for both analog and digital requirements.

In order to analyze the various novel devices, it is necessary to have the correct tool(s). In this thesis, we have shown that using a numerical simulator, we have been able to extract the various figure of merits with good agreement with measured devices where possible. As described in Chapter 2, the Silvaco ©package contains most of the necessary models and features to carry out the characterizations. One of the advantages of this simulator is the ability to adjust any of the models and properties when needed. In this work, since we are more interested in the qualitative analysis between devices, we have followed the guidelines as listed in the operating manual of the simulator.

Both the single and double-gate graded channel have shown potential in satisfying the need for low power high performance analog and digital applications. The graded-channel architecture is unique in itself because it provides an alternative to keeping the physical channel length long, but at the same time having a short effective channel length. The graded-channel architecture has shown that when biased at lower gate overdrive and high drain bias, we obtain higher than normal DC gain

compared to the usual devices. The combination of the graded-channel architecture with a double-gate device provides even more exciting analog and digital properties. With the GC architecture, we can achieve higher Early voltage due to the lower impact of the drain in saturation on the channel. The transconductance values are increased due to the reduction of influences from the drain. This combination results in a generally higher Voltage Gain of the device. Theoretically, by reducing the gate length or the effective channel length, a further improvement in the electrical characteristics would be expected. An advantage of these structures is that they are fully compatible with the current CMOS process with just some small modification to the lithographic mask. However, it is expected that there would be some difficulties to fabricate these structures as we reduce the channel length.

An improved fabrication method based on the wafer bonding process was introduced to fabricate the planar double-gate device which has the potential to be extended to quadruple-gate device. This method is known as the wafer bonding over prepatterned cavities. The fabrication method has proven to be a promising method not only for fabricating SOI based devices, but also Silicon-on-Nothing. This method allows other materials to be used as the insulator. This fabrication technique over the other methods proposed is that the width to gate length ratio and asymmetrical gate oxide thickness problem is solved. The electrical characterization of the devices fabricated using this specific wafer bonding shows that for the double-gate SOI MOSFETs, the theoretical double-gate behavior is obtained and for the SON devices, we have also seen the expected results. In order to further improve this fabrication method, several issues especially during the preprocessing stage, e.g. bonding, whereby this is one of the critical steps for a good fabrication of the device must be further analyzed.

Due to the limitation of available devices for analysis especially measurement double-gate devices, a method proposed by Pretet [Con03] was analyzed. This method is known as the Quasi double-gate method. This method allows us to emulate a double-gate operation from a single-gate device. From the analysis of the quasi double-gate method, we see that there are some limitation to this method. Table 7.1 shows the summary of regions where this quasi double-gate method is valid. From this analysis, we can conclude that in order to emulate the double-gate

Parameter	Region	Good Applicability of the Quasi DG method?
Mobility	Strong Inversion, Linear Regime	Yes
Maximum transconductance	Strong Inversion, Linear Regime	Yes
Maximum transconductance	Strong Inversion, Saturation	No
Transconductance-to-current ratio	Strong Inversion, Linear Regime	Yes
Transconductance-to-current ratio	Strong Inversion, Saturation	No
On-current	Strong Inversion	No
Off-current	Weak Inversion	No
Threshold voltage	-	No

Table 7.1: Limitation and applicability of the Quasi DG method in the emulation of a real Double-gate in the various operation region for various important parameters.

transistor from a single-gate transistor, the application of the ratio between the thickness of the front oxide layer to the buried oxide layer and multiplying this ratio with the back gate bias of the single gate is not sufficient to produce the appropriate characteristics of a double-gate. This difference is contributed to the asymmetrical properties of the charges

formed at the interface of the silicon and the buried oxide which is complicated. A full analysis was conducted using experimental, analytical analysis and numerical simulations were carried out and the summary can be seen in Table 7.1.

One of the most interesting device listed in the ITRS table [http], is the multiple-gate device. From the numerical simulations of the various multiple-gate devices, it is clear that they are very promising device for future applications in both analog and RF. The results obtained from the simulation have shown very good agreement with the experimental devices. This again confirms the predictable accuracy of the numerical simulation results. The intrinsic gain for the FinFET/Triple-gate SOI MOSFET is very much higher compared to the SG SOI MOSFET when compared at the same bias point. In the subthreshold-region, the improvement brought about by the multi-gate structure is even more pronounced as compared to the single-gate structure especially when we move toward smaller nodes. This is important to satisfy the requirements of the ITRS [http]. These improvements are contributed to the improved electrostatic control of the gates and the volume inversion. In order to meet the RF requirements, the EOT needs to be shrunk down to 1 nm and the silicon film is reduced to at least 10 nm, the multiple-gate architecture is a very promising device to realize the predictions of the ITRS in the sub 50 nm-nodes and beyond. However, we have also seen the limitation of the multiple-gate architecture especially in regards to the parasitic capacitances. Due to the complicated 3-D interconnections, we have seen that the increase in the extrinsic capacitances for long channel devices make them non-viable for use, but they become very advantageous when we move below the 75 nm gate length. The width/length ratio of the triple-gate and FinFET devices is an important aspect in reducing these parasitic capacitances. In order to reduce these parasitic fringing capacitances, it is encouraged to use higher width/length ratio which is in opposition with the optimized geometry for digital applications.

From the analysis of the multiple-gate devices we see some disadvantages due to the 3-D interconnections, however, we can conclude that these devices have more advantages. We have also shown that these multiple-gate devices are not only interesting electrical wise, but they can be fabricated without complicated steps compared to the cur-

rent CMOS fabrication method. One of the general conclusion from this work on multiple-gate devices is it has been shown that with various improvements in the fabrication and technologies applied to these structures, they can even be pushed further and this will realize the predictions of the ITRS to 2015 and beyond.

In general, the work presented in this thesis have shown that the various devices studied are very interesting devices to fulfill the requirements set out by the ITRS. We have seen the electrical advantages of the graded-channel single and double gate MOS and multiple-gate MOS devices for applications in analog and digital. Thanks to the volume inversion phenomenon, we have seen the drastic improvement in the various figure of merits. We have also shown that having multiple-gates, the control of the charges in the channel is improved leading to much better short-channel effects. We have also examined the possibility to analyze the double-gate structure by emulation through a single-gate SOI MOS. This analysis shows that the method has its advantages and disadvantages in the different region of operation. In order to have a complete analysis of these novel devices, the fabrication of these devices have been analyzed. We have proposed in this thesis a wafer bonding method over prepattered cavity to fabricate planar double-gate SOI MOSFET. The fabrication method proposed here is flexible enough to even fabricate other novel devices such as Silicon-on-Nothing devices and quadruple-gate MOS.

Appendix A

Example of net list for 2-D Double-Gate SOI MOSFET numerical simulation

In this net list, an example of a numerical 2-D simulation for a Double-Gate SOI MOSFET is shown. In the first part, the mesh of the device is defined for the X and Y-direction. The spacing of the mesh can be defined accordingly. It is important to have a finer mesh definition when the region is important, e.g. under the channel, as it influences the distribution of the doping which influences the final electrical characteristics. However, care should be taken as to have a balance between computation time and accuracy.

```
#L=100 nm, UD DG, tsi=20 nm, tox=2 nm
#capacitance with frequency
#Vg=1.0V, Vd=1.0V
go atlas
# mesh
mesh space.mult=1.0
x.mesh loc=0.0 spac=0.25
x.mesh loc=1.0 spac=0.025
x.mesh loc=1.025 spac=0.005
x.mesh loc=1.050 spac=0.005
```

```
x.mesh loc=1.075 spac=0.005
x.mesh loc=1.100 spac=0.005
x.mesh loc=1.125 spac=0.005
x.mesh loc=1.150 spac=0.025
x.mesh loc=2.150 spac=0.25
y.mesh loc=0.0 spac=0.001
y.mesh loc=0.002 spac=0.0005
y.mesh loc=0.007 spac=0.0005
y.mesh loc=0.012 spac=0.001
y.mesh loc=0.015 spac=0.0005
y.mesh loc=0.022 spac=0.0005
y.mesh loc=0.024 spac=0.001
y.mesh loc=0.030 spac=0.01
y.mesh loc=0.040 spac=0.01
y.mesh loc=0.050 spac=0.01
y.mesh loc=0.060 spac=0.01
y.mesh loc=0.080 spac=0.05
y.mesh loc=0.100 spac=0.05
y.mesh loc=0.120 spac=0.05
y.mesh loc=0.150 spac=0.05
y.mesh loc=0.174 spac=0.05
```

In this section, the different regions will be defined accordingly to the defined mesh locations, in the previous section. The various regions can be found in the Silvaco Manual [Sof00].

```
# regions
region num=1 y.min=0.0 y.max=0.002 oxide
region num=2 y.min=0.002 y.max=0.022 silicon
region num=3 y.min=0.022 y.max=0.024 oxide
region num=4 y.min=0.024 y.max=0.174 oxide
```

Here, the various electrode will be defined. The placement of the various electrodes can be defined by the user, again within the limits as defined in the beginning of the list. The top and bottom gate are named separately.

```
# electrode
electrode name=gate x.min=1.025 x.max=1.125 y.min=0.0 y.max=0.0
```

```
electrode name=gate2 x.min=1.025 x.max=1.125 y.min=0.024 y.max=0.024
electrode name=source x.max=1.0 y.min=0.002 y.max=0.002
electrode name=drain x.min=1.15 y.min=0.002 y.max=0.002
```

In this section, the doping of the device can be defined. The different dopants can be defined as listed in the Silvaco manual [Sof00]. Two main distribution of the dopants can be defined, as either uniform doping or following the Gaussian distribution.

```
# doping
doping uniform conc=1.0e15 boron reg=2 x.min=1.025 x.max=1.125
doping uniform conc=6.0e21 arsenic reg=2 x.min=0.0 x.max=1.025
doping uniform conc=6.0e21 arsenic reg=2 x.min=1.125 x.max=2.15
```

The interface charge between two different interface can be defined.

```
#interface charge
interface QF=3.0e10 y.max=0.0025
interface QF=1.0e11 y.min=0.0025
```

Here, the definition of the various electrode are activated using the contact statement. The workfunction of the gate can be changed accordingly as shown in the example. In order to bias the top and bottom gate together, the command "common" is used. The thermcontact is used when we need to take into consideration the self-heating effect.

```
contact name=gate WORKFUN=4.67 n.poly
contact name=gate2 WORKFUN=4.67 common=gate
contact name=drain neutral
contact name=source neutral
thermcontact num=1 x.min=0.0 x.max=2.250 y.min=0.174 y.max=0.174
ext.temp=300
```

Here the various models for the various effects that is wanted can be specified. The various models and explanations can be found in the Silvaco Manual [Sof00].

```
models cvt hcte.el srh auger impactselb bgn lat.temp print
```

This solve command line is to prompt the software to start a predictive calculation and initial guess so there are some starting numbers for

the algorithm to begin.
solve init

In this output command, we can specify which sort of output is required from the user besides the default outputs from the program. The various outputs that can be specify are found in the Silvaco manual [Sof00]

output e.field e.mobility e.velocity charge

To save the structure, the following command is used.
save outf=100.str

The iteration method can be specify. In the Silvaco manual, details of the various methods can be found [Sof00].

method block newton

The solve statement followed by the corresponding electrode prompts the simulator to apply the specify voltage and to bias it to the required bias. It is normal to begin with 0 V in order to give the simulator a good point to begin and to reduce iteration problem or convergence problem later on due to bad beginning guesses.

solve vsource=0.0
solve vdrain=0.0
solve vgate=0.0

In order to bias a certain electrode by step and to specify an ending bias point, the following command can be used.

solve name=drain vdrain=0.05 vstep=0.05 vfinal=1.0
solve name=gate vgate=0.02 vstep=0.02 vfinal=0.28
solve vgate=0.30 outf=vgate030.bin
save outf=vds100vgate030.str
solve name=gate vgate=0.02 vstep=0.02 vfinal=0.60
solve vgate=0.60 outf=vgate060.bin
save outf=vds100vgate060.str
solve name=gate vgate=0.02 vstep=0.02 vfinal=0.68
solve vgate=0.80 outf=vgate080.bin
save outf=vds100vgate080.str

```

solve name=gate vgate=0.02 vstep=0.02 vfinal=0.78
solve vgate=1.00 outf=vgate100.bin
save outf=vds100vgate100.str
load infile=vgate030.bin

```

In this command line, the "log outf" command is used to specify the name of the output file for that specific bias condition. In this command line, for AC analysis, we can specify the parameters that is needed. In this example, the s and y parameters are used. We also specify the inport and outport electrode. The width specifies the width of the device simulated and is important to be used when the s.param is used. Further reading on this can be found in the Silvaco manual [Sof00].

```

log outf=vd100vg030.log master s.param y.param inport=gate out-
port=drain width=1.5

```

In this line, the AC frequency can be specify. The amplitude of the frequency can also be specify with the vss statement. In order to step the frequency, the nfstep command can be used.

```

solve ac freq=1e6 vss=0.03
solve ac freq=2e6 fstep=1e6 nfstep=7 vss=0.03
logoff
load infile=vgate060.bin
log outf=vd100vg060.log master s.param y.param inport=gate outport=drain
width=1.5
solve ac freq=1e6 vss=0.03
solve ac freq=2e6 fstep=1e6 nfstep=7 vss=0.03
logoff
load infile=vgate080.bin
log outf=vd100vg080.log master s.param y.param inport=gate outport=drain
width=1.5
solve ac freq=1e6 vss=0.03
solve ac freq=2e6 fstep=1e6 nfstep=7 vss=0.03
logoff
quit

```


Appendix B

Example of net list for a 3-D Double-Gate SOI MOSFET numerical simulation

In this example, a 3-D example of a Double-Gate SOI MOSFET is shown. The commands used for a 3-D simulation is very similar to the one shown for the 2-D simulation in **Appendix A**. The only difference is that for the the mesh definition, an additional coordinate is specify, the Z direction. This is true also for the specification of the location for the doping, electrode, regions and contact, where an additional Z-direction is specify. In order to prompt the simulator to use the 3-D simulation mode, we need to add the command ”three.d” after the ”go atlas” command, without this, the simulator will run in the default 2-D mode.

```
# 3D simulations for DG device
# L=50nm, DG, WIDTH=500nm, W/L=10
# DC SIMULATIONS
go atlas
mesh three.d space.mult=1.0
# x direction
x.mesh loc=-0.175 spac=0.75
x.mesh loc=-0.150 spac=0.25
```

```
x.mesh loc=-0.100 spac=0.200
x.mesh loc=-0.075 spac=0.100
x.mesh loc=-0.050 spac=0.050
x.mesh loc=-0.025 spac=0.025
x.mesh loc=0.000 spac=0.002
x.mesh loc=0.025 spac=0.002
x.mesh loc=0.050 spac=0.002
x.mesh loc=0.075 spac=0.025
x.mesh loc=0.100 spac=0.050
x.mesh loc=0.125 spac=0.100
x.mesh loc=0.150 spac=0.200
x.mesh loc=0.200 spac=0.25
x.mesh loc=0.225 spac=0.75
# y direction
y.mesh loc=-0.500 spac=0.500
y.mesh loc=-0.400 spac=0.400
y.mesh loc=-0.300 spac=0.300
y.mesh loc=-0.200 spac=0.200
y.mesh loc=-0.102 spac=0.075
y.mesh loc=-0.075 spac=0.050
y.mesh loc=-0.050 spac=0.025
y.mesh loc=-0.025 spac=0.010
y.mesh loc=-0.002 spac=0.005
y.mesh loc=0.00 spac=0.0025
y.mesh loc=0.10 spac=0.0050
y.mesh loc=0.02 spac=0.0025
y.mesh loc=0.022 spac=0.005
y.mesh loc=0.050 spac=0.010
y.mesh loc=0.075 spac=0.025
y.mesh loc=0.100 spac=0.050
y.mesh loc=0.122 spac=0.075
y.mesh loc=0.150 spac=0.250
y.mesh loc=0.172 spac=0.500
# z direction
z.mesh loc=0.00 spac=0.025
z.mesh loc=0.25 spac=0.025
z.mesh loc=0.50 spac=0.025
```

```

# regions
# AIR
region num=1 x.min=-0.175 x.max=0.225 y.min=-0.500 y.max=0.172
z.min=0.000 z.max=0.500
material=air
region num=2 x.min=-0.175 x.max=0.225 y.min=0.022 y.max=0.172
z.min=0.00 z.max=0.500 oxide
region num=3 x.min=0.000 x.max=0.05 y.min=-0.002 y.max=0.000 z.min=0.00
z.max=0.500 oxide
region num=4 x.min=-0.175 x.max=0.225 y.min=0.0000 y.max=0.020
z.min=0.00 z.max=0.500 silicon
region num=5 x.min=-0.175 x.max=0.225 y.min=0.020 y.max=0.022
z.min=0.00 z.max=0.500 oxide
# #1-gate #2-source #3-drain #4-substrate
elect name=source x.min=-0.175 x.max=-0.150 y.min=-0.500 y.max=0.000
z.min=0.0 z.max=0.500
elect name=gate x.min=0.00 x.max=0.05 y.min=-0.102 y.max=-0.002
z.min=0.00 z.max=0.500
elect name=drain x.min=0.200 x.max=0.225 y.min=-0.500 y.max=0.000
z.min=0.000 z.max=0.500
elect name=substrate x.min=0.00 x.max=0.050 y.min=0.022 y.max=0.122
z.min=0.000 z.max=0.500
elect name=gate2 x.min=0.00 x.max=0.05 y.min=0.022 y.max=0.025
z.min=0.00 z.max=0.500
#***** define the doping concentrations *****
doping uniform arsenic con=6.e21 x.left=-0.175 x.right=0.00 y.top=0.0
y.bottom=0.02 z.min=0.0 z.max=0.5
doping uniform arsenic con=6.e21 x.left=0.05 x.right=0.225 y.top=0.0
y.bottom=0.02 z.min=0.0 z.max=0.5
doping uniform boron con=1.e15 x.left=0.00 x.right=0.05 y.top=0.0 y.bottom=0.02
z.min=0.0 z.max=0.5
# contact
contact name=gate n.poly workfunc=4.67
contact name=substrate n.poly workfunc=4.67
contact name=drain aluminum
contact name=source aluminum
models cvt srh bgn fermi print

```

```
method newton AUTONR BICGST
output band.params con.band qfn qfp flowlines
output e.field e.mobility e.velocity charge
solve init
#solve prev
solve vgate=0.0
solve vdrain=0.0
solve vsource=0.0
solve vsubstrate=0.0
save outf=DG50ACVDS1AIR.str
solve vdrain=0.05 vstep=0.05 vfinal=1.00 name=drain
solve vgate=0.05 vsubstrate=0.05
solve vgate=0.10 vsubstrate=0.10
solve vgate=0.15 vsubstrate=0.15
solve vgate=0.20 vsubstrate=0.20
solve vgate=0.25 vsubstrate=0.25
solve vgate=0.30 vsubstrate=0.30
solve vgate=0.315 vsubstrate=0.315 outf=DG50ACVDS1VGS0315.bin
solve vgate=0.35 vsubstrate=0.35
solve vgate=0.365 vsubstrate=0.365 outf=DG50ACVDS1VGS0365.bin
solve vgate=0.40 vsubstrate=0.40
solve vgate=0.45 vsubstrate=0.45
solve vgate=0.50 vsubstrate=0.50
solve vgate=0.55 vsubstrate=0.55
solve vgate=0.565 vsubstrate=0.565 outf=DG50ACVDS1VGS0565.bin
solve vgate=0.60 vsubstrate=0.60
solve vgate=0.65 vsubstrate=0.65
solve vgate=0.70 vsubstrate=0.70
solve vgate=0.75 vsubstrate=0.75
solve vgate=0.765 vsubstrate=0.765 outf=DG50ACVDS1VGS0765.bin
solve vgate=0.80 vsubstrate=0.80
solve vgate=0.85 vsubstrate=0.85
solve vgate=0.90 vsubstrate=0.90
solve vgate=0.95 vsubstrate=0.95
solve vgate=0.965 vsubstrate=0.965 outf=DG50ACVDS1VGS0965.bin
load infile=DG50ACVDS1VGS0315.bin
log outf=DG50ACVDS1VGO050VG.log master y.param inport=gate
```

```
outputport=drain
solve ac freq=10 fstep=10 mult.f nstep=4 vss=0.03
solve ac freq=1e6 vss=0.03
solve ac freq=2e6 fstep=1e6 nstep=7 vss=0.03
logoff
load infile=DG50ACVDS1VGS0315.bin
log outf=DG50ACVDS1VGO050VS.log master y.param inport=substrate
outputport=drain
solve ac freq=10 fstep=10 mult.f nstep=4 vss=0.03
solve ac freq=1e6 vss=0.03
logoff
load infile=DG50ACVDS1VGS0365.bin
log outf=DG50ACVDS1VGO100VG.log master y.param inport=gate
outputport=drain
solve ac freq=10 fstep=10 mult.f nstep=4 vss=0.03
solve ac freq=1e6 vss=0.03
logoff
load infile=DG50ACVDS1VGS0365.bin
log outf=DG50ACVDS1VGO100VS.log master y.param inport=substrate
outputport=drain
solve ac freq=10 fstep=10 mult.f nstep=4 vss=0.03
solve ac freq=1e6 vss=0.03
logoff
quit
```


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