Low-Power Silicon Strain Sensor Based on CMOS Current Reference Topology

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Abstract

A strain sensor inspired by a Widlar self-biased current source topology called β-multiplier is developed to obtain a strain-dependent reference current with high supply rejection. The sensor relies on the piezoresistive effect in the silicon MOS transistors that form the current reference circuit. The device behavior is analytically computed and verified with experimental measurements under four-point bending test. A basic implementation with an integrated resistor reaches a strain sensitivity of 2.54 nA/$\mu\epsilon$ (gauge factor of 324) for a temperature sensitivity of 52.06 nA/°C. A more advanced full-transistor circuit based on current subtraction principle is furthered implemented in order to reach strain sensitivity up to 12.02 nA/$\mu\epsilon$ (gauge factor of 1773) and temperature sensitivity of -28.72 nA/°C. This implementation includes a CMOS active load to tune the strain and temperature sensitivities with a total power consumption between 20 and 150 μW.

Keywords: Strain, Piezoresistivity, Silicon, CMOS, Reference circuit

1. Introduction

Many physical effects can be exploited to record strain in a material such as capacitive [1, 2], piezoelectric for dynamic strain [3, 4], optic with interferometers [5, 6, 7] and piezoresistive [8, 9, 10]. The two last means are widely used, especially with fiber Bragg grating and interferometric sensors for optical measurements and metallic strain gauges for piezoresistive sensing. Optical sensors offer various advantages such as accuracy and the ease of multiplexing but comes with brittleness and high power consumption due to the spectrum analyzer that can consume several Watts. Their robustness against external conditions (electromagnetic interferences, chemicals, temperature, and so on.) make them suitable for harsh environments found in industrial areas, biomedical, automotive or aerospace applications [11]. Piezoresistive strain gauges provide a cheap solution easy to implement. It is based on a mature technology that was one of the first used to record strain of a material [12]. The principle of the metallic gauge is based on a change in the dimensions that limits the gauge factor (GF) at around 2.

New types of materials such as ceramic or semiconductor can be used in order to improve this factor and reach higher strain sensitivity [13, 14]. The principle of strain sensing with those materials does not rely on dimensions variation but on intrinsic changes in the carrier mobility. Some of them, such as graphene [15] or carbon nanotubes [16], allow high gauge factor up to 1000. However, the fabrication cost and complexity, added to the fragility, make long-term applications difficult. On the other hand, silicon is a well-known material in electronics with reasonable cost and fabrication complexity [17]. Its crystallographic configuration leads to high piezoresistive variation with potential gauge factor above 150 [18].

One of the biggest advantage of silicon gauges lies in its straightforward integration in a complete circuit to boost and tune the performances of the sensor. In this case, the sensing element is no more an external component which has to be inserted in a dedicated circuit, but the circuit itself.

Self-biased reference circuit refer to implementations where the reference current or voltage is set independently of external sources [19]. They provide stable output signal that depends on physical parameter such as carrier mobility, resistance, breakdown voltage, dimensions and so on. In this work, a self-biased current reference inspired by Widlar topology, called β-multiplier [20], is modified in order to create a strain-dependent reference current with high supply rejection. Four implementations are analyzed: (i) a basic implementation with a resistor (β_R), (ii) a full-transistor implementation with positive (β_+) or (iii) negative (β_-) strain response and (iv) a current subtraction implementation based on full-transistor circuits (β_{sub}).

The analytical analysis of the circuits is first realized in Section 2 to present the different implementations and to model the strain impact on the reference currents. Then, the results of measurements on the sensor are presented and discussed in Section 3. We first tested the transistors separately in order to extract the key parameters, i.e. the carrier mobility and the threshold voltage, along with their strain and temperature dependencies. We complete the study with the strain and temperature analyses of the β-multipliers to evaluate the performances of the different implementations.

2. Analytical Model

2.1. Piezoresistive effect

The piezoresistive effect in silicon is mainly due to the change in the carrier mobility that is much higher than the

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change in the dimensions [21]. By considering infinitesimal displacement, the relative variation of the mobility can be expressed as

$$-\frac{d\mu_i}{\mu_i} = \pi_{i,l}\sigma_l + \pi_{i,t}\sigma_t, \quad (1)$$

where i stands for the electron (n) or holes (p) contributions, π_l and π_t are, respectively, the piezoresistive coefficients in the longitudinal and transverse directions while σ_l and σ_t are the applied stresses in those two directions. We consider the longitudinal direction to be the direction of the transistor channel while the transverse direction is perpendicular to it. In ceramic material, the strain-stress relation can be expressed by considering elastic deformation [22] as

$$\sigma_j = E \cdot \varepsilon_j, \quad (2)$$

where E is the Young's modulus of around 165 GPa for silicon in the [110] crystal direction [23] and ε_j is the applied strain in direction j.

Solving relation 1 leads to

$$\mu_i = \mu_{i,0}\, e^{-(\pi_{i,l}\sigma_l + \pi_{i,t}\sigma_t)}, \quad (3)$$

where $\mu_{i,0}$ is the mobility in the relaxed case.

The piezoresistive coefficients are intrinsic parameters that are linked to the effective masses variations of the electrons and the holes. As the variations of the effective mass depend on the crystal direction of the applied strain, so do these coefficients [24].

In this work, we consider MOS transistor with channel oriented in parallel and perpendicular to the [110] direction of the crystal as displayed in Fig. 1.

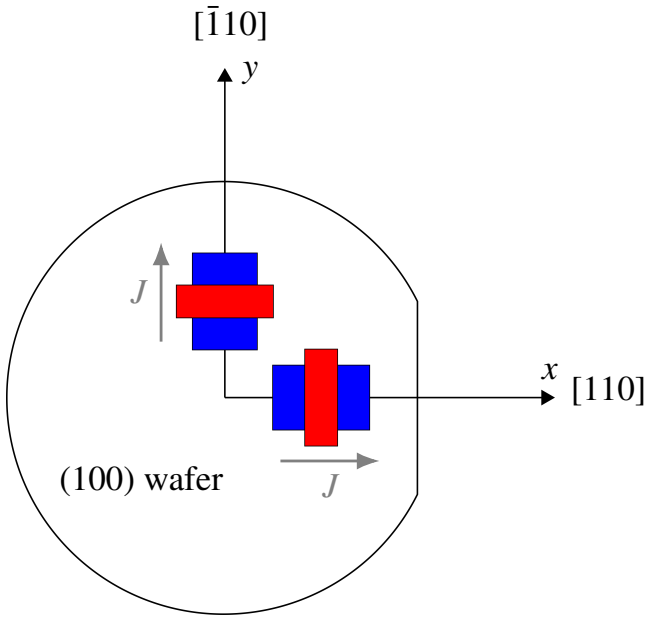

Figure 1: Illustration of the transistors orientations along <110> directions on a (100) silicon wafer.

In this orientation, the transverse and longitudinal piezoresistive coefficients $\pi_{i,l}$ and $\pi_{i,t}$ can be expressed as [25]

$$\begin{aligned} \pi_{i,t} &= \frac{\pi_{i,11}+\pi_{i,12}-\pi_{i,44}}{2}, \\ \pi_{i,l} &= \frac{\pi_{i,11}+\pi_{i,12}+\pi_{i,44}}{2}, \end{aligned} \quad (4)$$

where $\pi_{i,11}$, $\pi_{i,12}$ and $\pi_{i,44}$ are the main components of the piezoresistance tensor. The values for n-type and p-type silicon are given in Table 1 [26].

	π_{11}	π_{12}	π_{44}	π_t	π_l
n-Si	-1022	534	-136	-176	-312
p-Si	66	-11	1381	-663	718

Table 1: Main components of the piezoresistance tensor for p- and n-type transistors [26]. The effective longitudinal and transverse piezoresistive coefficients for strain applied in the [110] direction are also computed. The values are expressed in TPa^{-1}.

At the circuit level, it was found that perpendicular transistors placed in current mirror configuration lead to higher strain sensitivity with regards to ratio of the transistor currents [27, 28, 29]. Indeed, this configuration leads to an effective sensitivity that is equal to the difference of the piezoresistive coefficients of the two transistors. If these coefficients are of opposite sign, an enhanced strain sensitivity can be obtained. Such features can be found by placing PMOS (NMOS) transistors perpendicularly along the [110] ([100]) directions. This perpendicular current mirror works as the main sensing element of our proposed solution for strain sensing applications.

2.2. Current reference configuration

In this work, we first imagined a β-multiplier-like reference shown in Fig. 2.a as strain sensor. This is inspired by a self-biased reference based on Widlar current source topology. A cascode configuration is implemented in order to further reduce the supply sensitivity.

In this circuit, the two PMOS transistors M_3 and M_4 impose the same current in both in the absence of strain branches while the two NMOS transistors and the resistor impose a quadratic relation between the currents of the two branches. The transistors are assumed in saturation with long channel model and no mismatch between them. When the upper and lower parts of the circuits are connected, the equilibrium in the absence of strain leads to

$$I_a = 2\frac{\left(1 - 1/\sqrt{K_{21}}\right)}{R^2\beta_{n,0}}, \quad (5)$$

where R is the resistance, K_{21} is the ratio between the width of the NMOS transistors, $\beta_{n,0} = \frac{W}{L}C_{ox}\mu_{n,0}$ with C_{ox} the capacitance of the transistor gate, W the width and L the length of the transistor M_1. This last term leads to the name β-multiplier for the current reference.

Under strain conditions, the mobility of the different transistors is impacted. The expression of the reference current under

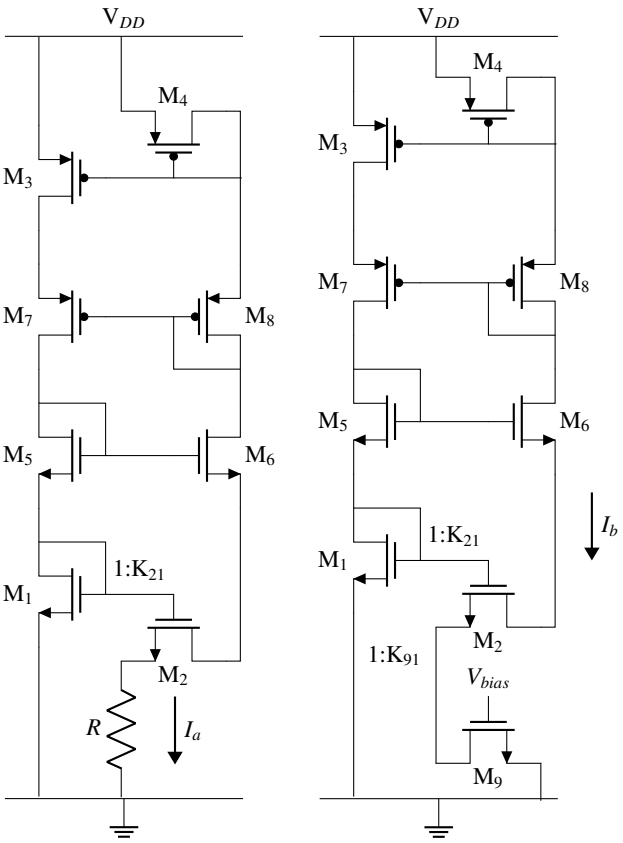

Figure 2: β-multiplier reference circuits with (a) resistor and (b) full-transistor implementations. The reference currents are, respectively, written I_a and I_b.

uniaxial stress is then given by

$$I_a = 2\frac{\left(e^{(\pi_3-\pi_1-\pi_4)\frac{\sigma}{2}} - e^{-\pi_2\frac{\sigma}{2}}/\sqrt{K_{21}}\right)\, e^{-2\pi_r\sigma}}{R^2\beta_{n,0}}, \qquad (6)$$

where π_j is the piezoresistive coefficient of transistor M_j, π_r is the piezoresistive coefficient of the resistor and σ is the uniaxial stress applied on the circuit.

A second circuit is presented in Fig. 2.b where the resistor is replaced with an active load. The transistor adds a control on the reference current by tuning the gate voltage V_{bias}. This tuning allows to control the power consumption of the circuit along with the sensitivities to strain and temperature.

The reference current in this case can be expressed as

$$I_b = 2V_{ov}^2\,\beta_{n,0}\cdot \frac{\left(e^{(\pi_3-\pi_4-\pi_1)\frac{\sigma}{2}} - e^{-2\pi_2\sigma}/\sqrt{K}_{21}\right)^2}{\left[\left(e^{(\pi_3-\pi_4-\pi_1)\frac{\sigma}{2}} - e^{-2\pi_2\sigma}/\sqrt{K}_{21}\right)^2 + e^{\pi_9\sigma}/\sqrt{K}_{91}\right]}, \qquad (7)$$

where K_{91} is the ratio between the width of the transistors M_9 and M_1, and $V_{ov} = (V_{bias} - V_{th,n})$ with $V_{th,n}$ the threshold voltage of transistor M_9.

The complete development to find the expressions of the reference currents I_a and I_b can be found in Appendix A and Appendix B, respectively.

In both circuits, the PMOS and NMOS pairs (M_1/M_2, M_3/M_4 and M_1/M_9) are oriented perpendicularly to maximize the strain sensitivity. This configuration is necessary to observe the variations caused by the applied strain on the equilibrium current.

2.3. Current subtraction configuration

It is possible to reach a larger strain sensitivity by combining circuits with positive and negative strain responses. Furthermore, a reduction of the temperature sensitivity can be achieved if the temperature responses of the two circuits are of the same sign thanks to the current subtraction approach [30]. In order to obtain negative strain response, a rotation by 90° of the sensitive transistors in Fig 2.b is made. Two β-multiplier circuits can then be combined with a current subtraction circuit as displayed in Fig. 3. The sensing parts with positive and negative strain sensitivities are highlighted in blue while the current subtraction part is represented in red.

The output current of this circuit is given by

$$I_c = C_+\, I_{b,+} - C_-\, I_{b,-}, \qquad (8)$$

where $I_{b,+}$ and $I_{b,-}$ are the current of the β-multiplier with positive and negative responses, respectively. C_+ and C_- are constants that can be tuned by changing the ratio between the size of the MOSFETs of the β-multipliers and the current subtraction, i.e. M_{27} and M_{30}. The linear combination of the two currents $I_{b,+}$ and $I_{b,-}$ with chosen constants ensures a positive output current I_c regardless the applied strain.

3. Experiment and discussion

3.1. Experimental set-up

The circuits were fabricated using *UMC L180* technology. The transistors have low threshold voltage with 1.8 V voltage maximum supply voltage. For the temperature measurements, a bare die was put on a heating stage while the strain measurements were performed in a four-point bending machine. In this last case, the device under test (DUT) is ground down to a thickness of 50 um and next glued with *M-Bond 200* adhesive from *Vishay* on a 1 mm-thick aluminium strip. The strain is then applied using a four-point bending machine as displayed in Fig. 4. The bottom cylinders are spaced of 3 cm while a space of 8 cm is set for the the upper ones. The four-point bending method is a well-known mechanical test that allows a simple, stable and homogeneous deformation on a glued device [31]. A reference metallic strain gauge of 350 Ω from *Micro-Measurements* is mounted next to the die in order to measure the strain applied to the device. The resistance of the gauge was measured with a Series 2000 digital multimeter from *Keithley*.

The electrical measurements are made with a *B-1500 Semiconductor Device Parameter Analyzer* from *Keysight*. The electrical contact was made with tungsten probes directly on the die under test for both temperature or strain experiments.

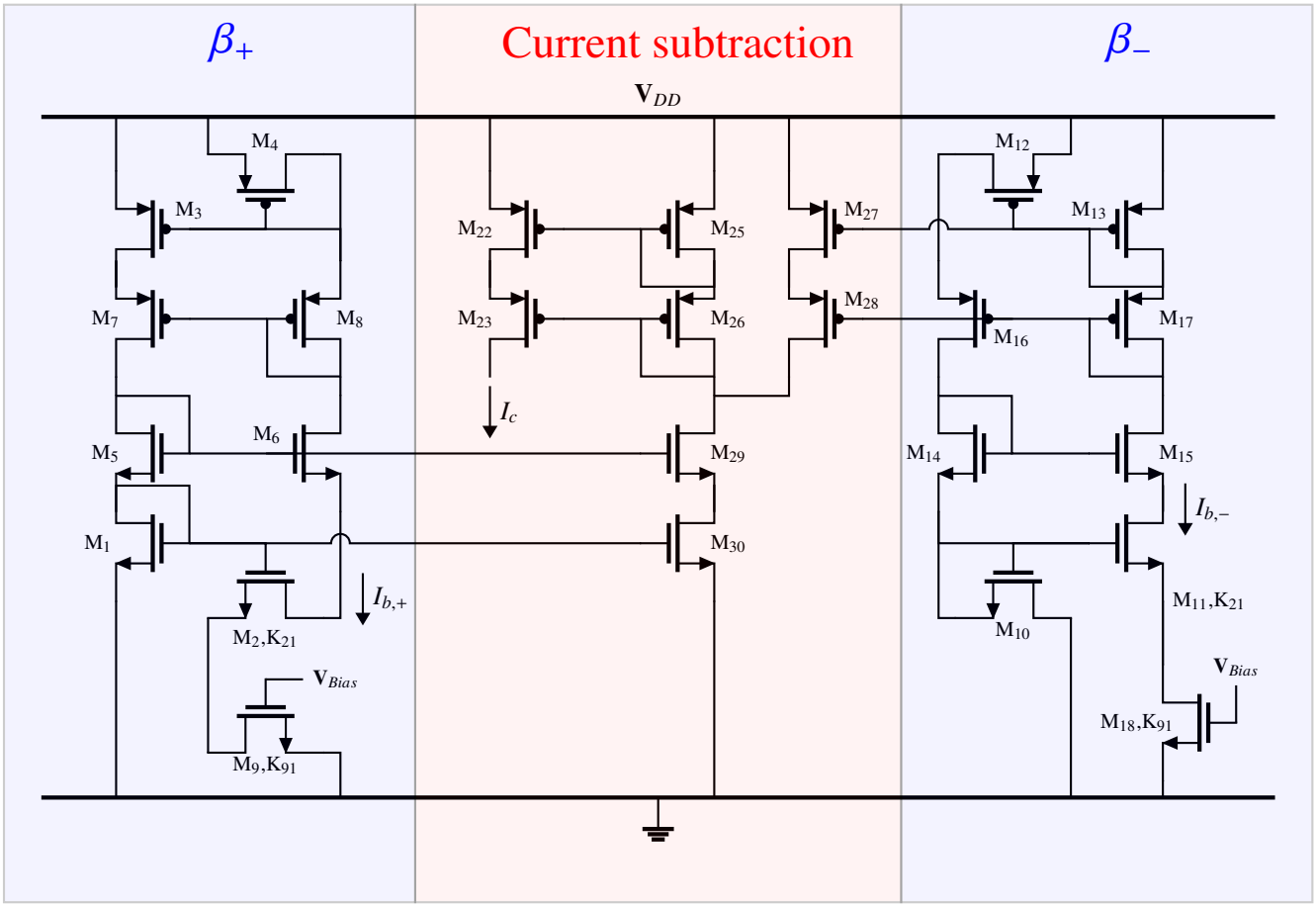

Figure 3: Current subtraction implementation (β_{sub}) composed full-transistor β-multipliers with positive (β_+) and negative (β_-) strain response

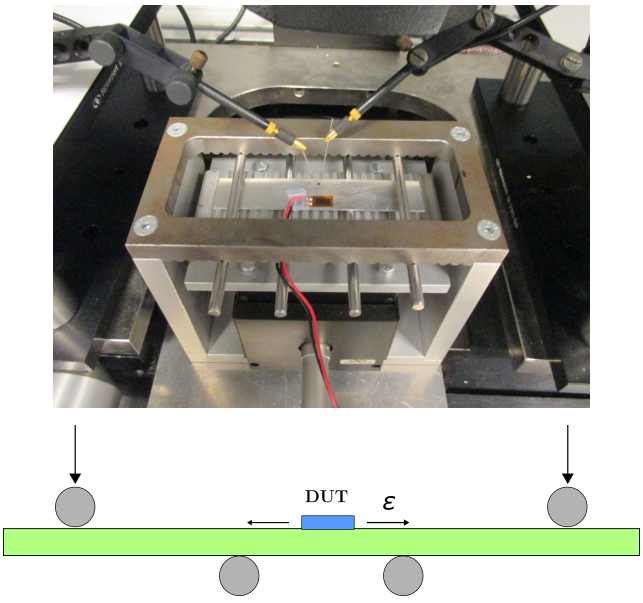

Figure 4: Illustration of the set-up for the four-point bending test.

The transistors are first measured separately in order to analyze the impact of strain and temperature on the mobility and the threshold voltage. Then, the currents of the four reference circuits are measured, i.e. the β-multiplier with resistor (β_R), the full-transistor β-multipliers with positive (β_+) and negative (β_-) strain responses and the current subtraction implementation (β_{sub}).

3.2. Transistor analysis

The tested NMOS and PMOS transistors have both a gate width of 8.5 μm and gate length of 5 μm. Each transistor type is duplicated and rotated by 90° in order to retrieve the transverse and longitudinal piezoresistive coefficients.

The significant parameters, i.e. the mobility and the threshold voltage, were extracted from I-V curves at different strain levels with the method from Jeppson [32]. This method is based on a least-square fit that is stable and insensitive to the mobility degradation and series resistances. We measured the drain current and we varied the gate voltage between 0 and 1.8 V while the source and the drain were, respectively, put to ground (1.8 V) and 50 mV (1.75 V) the for the NMOS (PMOS) transistors (resp.). The body for both types of transistor is connected to the source.

The low-field mobilities obtained in the relaxed case at 25°C are 1131 $cm^2V^{-1}s^{-1}$ and 191 $cm^2V^{-1}s^{-1}$ for the NMOS and PMOS transistors, respectively. The threshold voltages in these conditions are, respectively, 73.6 mV and -330.5 mV for the NMOS and PMOS transistor.

The results of the strain measurements are displayed in Fig. 5. The piezoresistive coefficients are extracted by computing a linear interpolation on the mobility variation using relation 1. We obtain a transverse and longitudinal coefficients of -255 (-437) TPa^{-1} and -283 (486) TPa^{-1} for the NMOS (PMOS) transistors, respectively. The PMOS transistor presents high and opposite piezoresistive coefficients while the coefficients for the NMOS transistor are smaller and of the same sign.

Table 2 compares the experimentally measured data with piezoresistive coefficients published in the literature. The results we obtained are in agreement with the ones shown in other works. The differences observed in the piezoresistive coefficients between the different works can be due to extrinsic perturbations that influence the strain response. Indeed, the bias condition as well as the regime of the measured transistors can have a strong impact on the extracted coefficients due to the different scattering mechanisms [33].

	$\pi_{n,t}$	$\pi_{n,l}$	$\pi_{p,t}$	$\pi_{p,l}$	Dimensions
This work	-255	-283	-437	486	WxL = 8.5 μm x 5 μm
Wacker *et al.* [34]	-470	-220	-450	520	WxL = 16 μm x 16 μm
Bradley *et al.* [35]	-250	-320	-385	415	L = 15 μm

Table 2: Longitudinal and transverse piezoresistive coefficients in TPa^{-1} experimentally measured and from the literature.

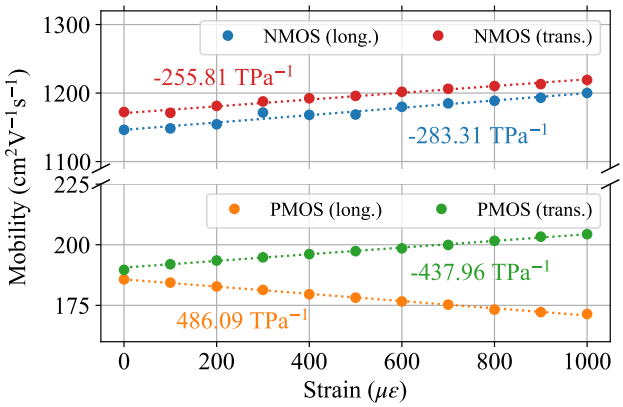

Figure 5: Mobility variation with regards to the applied strain for NMOS and PMOS transistors oriented in the longitudinal or transverse directions. The extracted piezoresistive coefficients are written next to the curves.

The results of the temperature measurements are displayed in Fig. 6 and 7. Mobility and threshold voltage sensitivities of -7.33 $cm^2V^{-1}s^{-1}°C^{-1}$/1.69 $mm^2V^{-1}s^{-1}°C^{-2}$ and -0.79 $mV°C^{-1}$ are, respectively, found for n-type transistors while the p-type transistors show a mobility sensitivity of -0.58 $cm^2V^{-1}s^{-1}°C^{-1}$/1504.57 $\mu m^2V^{-1}s^{-1}°C^{-2}$ and a threshold voltage sensitivity of 0.90 $mV°C^{-1}$. The dashed curves are computed using the theoretical model provided by the circuit supplier. The curves are in good agreement with the experimental work for both NMOS and PMOS transistors.

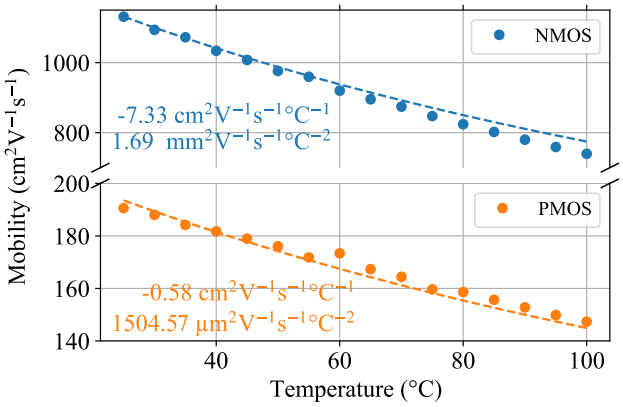

Figure 6: Mobility variation with regards to the temperature for NMOS and PMOS transistors. The temperature sensitivity extracted from the measurements is written next to it. The dashed lines represent the theoretical model from the transistor technology given by the UMC foundry.

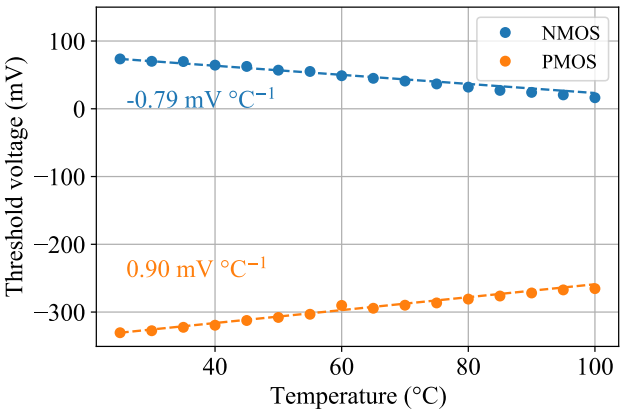

Figure 7: Threshold voltage with regards to the temperature for NMOS and PMOS transistors. The temperature sensitivity extracted from the measurements is written next to it. The dashed lines represent the theoretical model from the transistor technology given by the UMC foundry.

3.3. β-multiplier analysis

The β-multiplier circuits are tested similarly with the four-point bending method. Strain and temperature measurements are conducted on four circuits where the output current is measured according to the supply voltage for the implementation with resistor or bias voltage for the full-transistor ones. The first circuit is the β-multiplier with resistor (β_R) displayed in Fig. 2.a where the output current is I_a. The resistor is made of poly-silicon and reaches a value of 10 kΩ. The configuration with an active load is then investigated with two transistor orientations leading to positive (β_+) and negative (β_-) strain sensitivities. The output currents of these circuits represented in Fig. 2.b are $I_{b,+}$ ($I_{b,-}$) for the positive (negative) contribution. Finally, the output current I_c of the circuit with current subtraction (β_{sub}) represented in Fig. 3 is measured.

The gauge factor GF is used to analyze and compare the strain sensitivity. This factor is defined as the relative current variation with regards to the strain, i.e.

$$\frac{\Delta I}{I(\varepsilon = 0)} = GF \cdot \varepsilon \tag{9}$$

The current variations under strain stimuli are displayed in Fig. 8 while the variations according to the temperature are shown in Fig. 9.

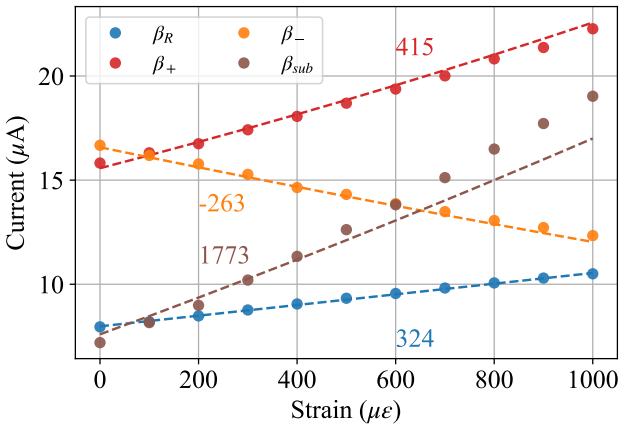

Figure 8: Output current with regards to the strain of the different implementations at V_{DD} = 1.8 V and V_{bias} = 1.2 V, i.e. the β-multiplier with resistor (β_R), the full-transistor β-multipliers with positive (β_+) and negative (β_-) strain responses and the current subtraction implementation (β_{sub}). The gauge factors extracted from the measurements are written next to the curves. The dashed lines represent the theoretical results obtained with the piezoresistive coefficients inserted in the analytical relations.

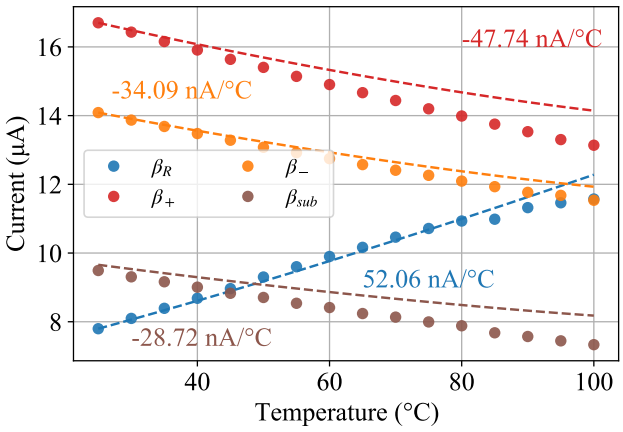

Figure 9: Output current with regards to the temperature of the different implementations at V_{DD} = 1.8 V and V_{bias} = 1.2 V, i.e. the β-multiplier with resistor (β_R), the full-transistor β-multipliers with positive (β_+) and negative (β_-) strain responses and the current subtraction implementation (β_{sub}). The temperature sensitivities extracted from the measurements are written next to the curves. The dashed lines represent the theoretical results obtained by simulation using the spice model of the UMC180 transistors given by the UMC foundry.

The dashed curves represent the theoretical results obtained by simulations for the temperature data and analytically for the strain results. The simulations are made using the spice model given by the UMC foundry for the UMC180 transistors while the strain impact is computed by injecting the piezoresistive coefficients found (cfr. Table 2) in relations (6) and (7).

3.3.1. β−multiplier with resistor (Fig. 2.a)

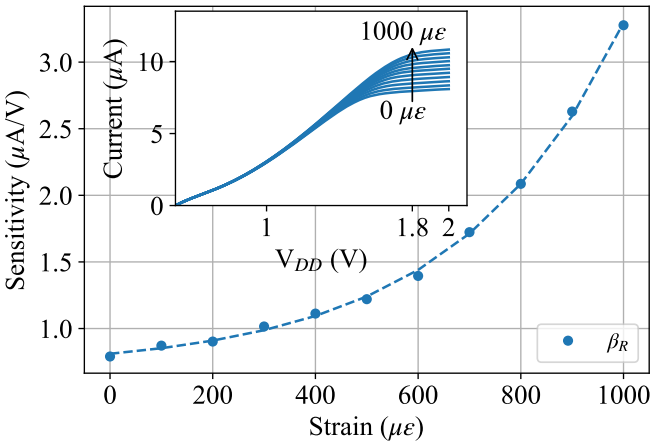

Figure 10: Output current sensitivity to supply voltage of the β-multiplier with resistor (β_R) with regards to the applied strain. The inset represents the raw results with the arrow at the supply voltage where the sensitivity is computed (1.8 V).

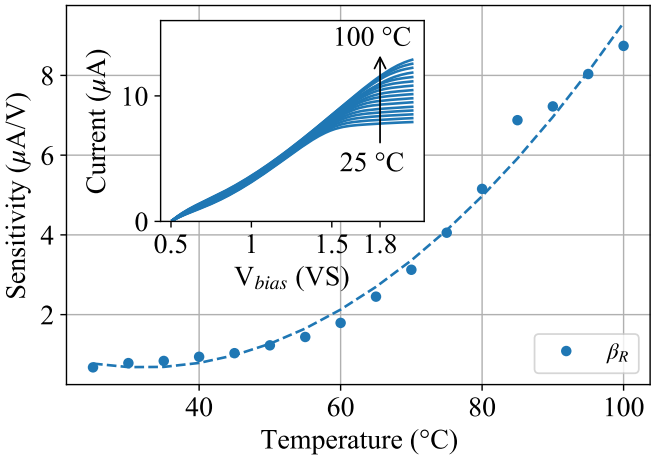

Figure 11: Output current sensitivity to supply voltage of the β-multiplier with resistor (β_R) with regards to the temperature. The inset represents the raw results with the arrow at the supply voltage where the sensitivity is computed (1.8 V).

The implementation β_R shows a gauge factor of 324 (2.59 nA/$\mu\varepsilon$) and temperature sensitivity of 52.06 nA/°C with a supply voltage of 1.8 V. The sensitivity to supply voltage of the implementation is investigated in Fig. 10. A sensitivity of 0.79 μA/V is obtained in the relaxed case. The sensitivity increased with the strain due to the voltage limit to keep the transistors in saturation regime being closer to the operating voltage of 1.8 V. Under high strain condition of 1000 $\mu\varepsilon$, the sensitivity is up to 3.28 μA/V. The effect of the temperature on the supply sensitivity presents the same behavior and is displayed in Fig. 11. We

obtained a sensitivity of 0.79 μA/V at 25°C that increases up to 8.74 μA/V at 100°C. The cascode implementation allows low supply sensitivity but brings the bias limit of the circuit close to the operating point.

3.3.2. β–multiplier with active load (Fig. 2.b) and subtraction circuit (Fig. 3)

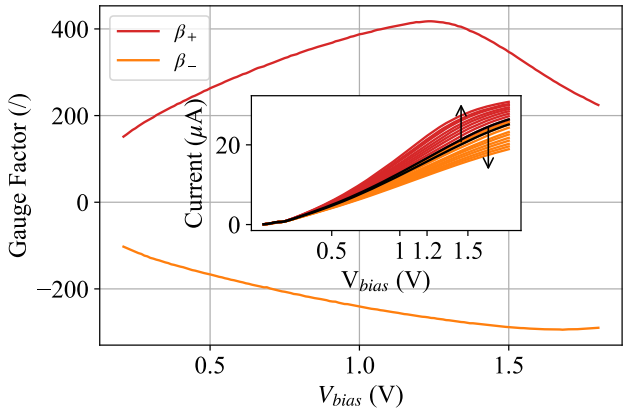

Figure 12: Gauge factor computed according to the bias voltage for the full-transistor implementations in strong inversion with positive (β_+) and negative (β_-) responses. The inset presents the raw I-V results with the arrow indicating the direction of the strain increase from 0 to 1000 $\mu\epsilon$.

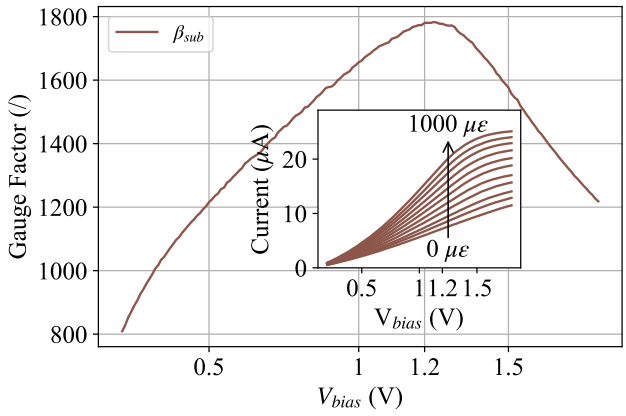

Figure 13: Gauge factor computed according to the bias voltage for the full-transistor current subtraction implementation (β_{sub}) in strong inversion. The inset presents the raw I-V results with the arrow indicating the direction of the strain increase from 0 to 1000 $\mu\epsilon$.

The implementation β_- and β_+ show a gauge factor of -263 (-4.37 nA/$\mu\varepsilon$) and 415 (6.47 nA/$\mu\varepsilon$) depending on the transistor orientation while the temperature sensitivities are -34.09 nA/°C and -47.74 nA/°C, respectively.

The active load allows a current control by tuning the bias voltage. As consequence, the strain and temperature sensitivities of the output current depend on the voltage applied. The gauge factor variations according to the bias voltage is shown in Fig. 12. A maximum gauge factor of 415 (resp. -290) around 1.2 V (resp. 1.6 V) is found for β_+ (resp. β_-) implementation. At higher bias voltage, the current flowing through the devices increases the gate voltage of the current mirrors. This bring the transistors into the triode regime and degraded the gauge factor of the circuit.

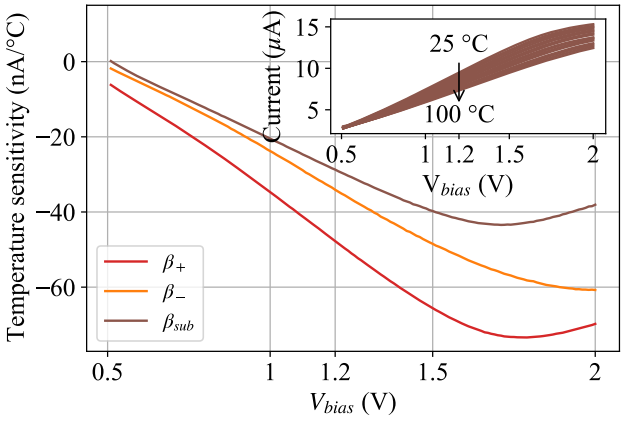

Figure 14: Temperature sensitivity according to the bias voltage for full-transistor implementations in strong inversion, i.e. β-multiplier with positive (β_+) and negative (β_-) strain response combined with a current subtraction circuit (β_{sub}). The inset shows the raw I-V curves of the measurements for the current of β_{sub}.

The temperature sensitivity depending on the bias voltage is represented in Fig. 14. At 1.2 V, sensitivities of -47.74 nA/°C and -34.09 nA/°C are obtained for the output currents of β_+ and β_-, respectively.

The circuit with current subtraction β_{sub} presents the highest factor with 1773 (12.02 nA/$\mu\varepsilon$) and a temperature sensitivity of -28.72 nA/°C for a bias voltage of 1.2 V. The gauge factor of the current subtraction circuit is displayed in Fig. 13.

As the temperature sensitivities are both negative for β_+ and β_- circuits, the current subtraction leads to lower temperature sensitivity. On top of that, we obtained strain sensitivity nearly three times higher.

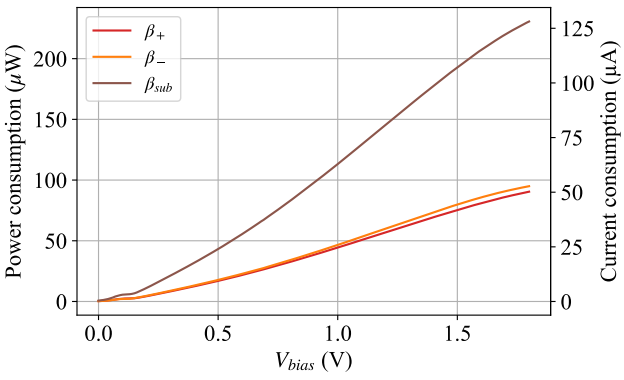

Figure 15: Power and current consumption according to the bias voltage for full-transistor implementations, i.e. β-multiplier with positive (β_+) and negative (β_-) strain response combined with a current subtraction circuit (β_{sub}).

The improvement of the performances is however counterbalanced by the larger power consumption of 145.45 μW. It is possible to reduce the current consumption (and therefore the power consumed) of the circuit by reducing the bias voltage as

Implementation	β_R	β_+	β_-	β_{sub}
Strain sensitivity (nA/$\mu\varepsilon$)	2.59	6.47	-4.37	12.02
Gauge Factor (/)	324	415	-263	1773
Temperature sensitivity (nA/°C)	52.06	-47.74	-34.09	-28.72
Power Consumption (μW)	28.6	56.96	60.02	145.45

Table 3: Summary of the main performances at V_{DD} = 1.8 V and V_{bias} = 1.2 V of the different implementations, i.e. the β-multiplier with resistor (β_R), the full-transistor β-multipliers with positive (β_+) and negative (β_-) strain responses and the current subtraction implementation (β_{sub}).

displayed in Fig. 15. Indeed, a consumption of around 50 μW can for example be obtained with a bias voltage of 0.5 V but with a gauge factor of around 1200 instead of 1773.

Table 3 summarizes the performances of the different implementations. The modifications of the β_R implementation allow for reaching higher strain sensitivity and gauge factor (from 324 to 1773) at the cost of higher power consumption (from 28.6 μW to 145 μW). Furthermore, the more advanced solution β_{sub} also shows better temperature sensitivity compared with the basic reference circuit (from 52.06 nA/°C to -28.72 nA/°C).

4. Conclusion

In this work, we developed a new strain sensor based on β-multiplier topology in order to reduce the device sensitivity to supply voltage. The piezoresistive effect in silicon is exploited directly in the elements composing the circuit. This allows the circuit to work directly as the sensing element, leading to high performances and easy-to-measure output. We presented a reference circuit adapted for strain sensing applications by changing the relative orientations of the transistors. The strain impact on the reference currents is analytically described and verified with the experimental results. The theoretical methodology developed shows the possibility to easily compute the strain impact in reference circuit. The analytical work should allow further predictions of the performances of the circuit depending on the elements and device orientations.

The transistors used in the circuits were first characterized to predict the response of the different implementations. The basic topology with resistor gives a strain sensitivity of 2.54 nA/$\mu\epsilon$ (gauge factor of 324) with a low power consumption of 28.6 μW. The temperature sensitivity was 52.06 nA/°C. This solution was improved with full-transistor implementation combined in a current subtraction circuit. This leads to high strain sensitivity of 12.02 nA/$\mu\epsilon$ (gauge factor of 1773) but at the cost of higher power consumption of 145.45 μW. The temperature sensitivity was lower down to -28.72 nA/°C with the subtraction principle. Furthermore, the full-transistor principle allows to tune the performances of the circuit with a gauge factor between 800 and 1800 for a power consumption between 20 and 200 μW.

Appendix A. Output current in β-multiplier with resistor

By applying Kirchhoff's voltage law on the resistor and NMOS transistors M_1 and M_2 from Fig. 2.a, the following relation is obtained

$$V_{GS,1} = V_{GS,2} + RI_{D,2}. \tag{A.1}$$

where $V_{GS,i}$ and $I_{D,i}$ stand for the gate-to-source voltage and drain current of transistor M_i, respectively. If the transistors are working in saturation and by neglecting the Early effect, $V_{GS,i}$ is given by

$$V_{GS,i} = V_{n,i}^{th} + \sqrt{\frac{2I_{D,i}}{\beta_{n,i}(\sigma)}}, \tag{A.2}$$

where $V_{n,i}^{th}$ is the threshold voltage of transistor i and $\beta_{j,i}(\sigma) = \left(\frac{W}{L}\right)_i \mu_{n,i} C_{ox}$ with j standing for the electrons (n) or holes (p) contribution. At the level of the PMOS transistors M_3 and M_4, the current mirror configuration gives

$$\begin{cases} V_{SG,3} = V_{SG,4} \\ I_{D,2} = I_{D,4} \\ I_{D,3} = I_{D,1} \end{cases} \Rightarrow \frac{I_{D,1}}{\beta_{p,3}(\sigma)} = \frac{I_{D,2}}{\beta_{p,4}(\sigma)}. \tag{A.3}$$

The currents of the transistors M_3 and M_1 are equal, the same goes for transistors M_2 and M_4.

Substituting relations (A.2) and (A.3) in relation (A.1), we obtain

$$V_{n,2}^{th} + \sqrt{\frac{2I_{D,2}}{\beta_{n,2}(\sigma)}} + RI_{D,2} = V_{n,1}^{th} + \sqrt{\frac{2I_{D,2}}{\beta_{n,1}(\sigma)}\frac{\beta_{p,3}(\sigma)}{\beta_{p,4}(\sigma)}}, \tag{A.4}$$

$$RI_{D,2} - \sqrt{I_{D,2}} \underbrace{\sqrt{2}\left(\sqrt{\frac{\beta_{p,3}(\sigma)}{\beta_{p,4}(\sigma)\beta_{n,1}(\sigma)}} - \frac{1}{\sqrt{\beta_{n,2}(\sigma)}}\right)}_{f(\sigma)} + \Delta V_n^{th} = 0,$$

$$\sqrt{I_{D,2}} = \frac{f(\sigma) \pm \sqrt{f(\sigma)^2 + 4R\Delta V_n^{th}}}{2R}. \tag{A.5}$$

By assuming no threshold voltage mismatch between the transistors, i.e. $\Delta V_n^{th} = 0$, we obtain

$$I_{D,2} = \begin{cases} 0 \\ \frac{f(\sigma)^2}{R^2} \end{cases}. \tag{A.6}$$

Equation (A.6) shows two solutions for the current $I_{D,2}$. In order to avoid the zero-current solution, a start-up circuit is thus needed.

Using relation (3), the current is given by

$$I_{D,2} = \frac{2\left(\sqrt{\frac{\beta_{p,3}(\sigma)}{\beta_{p,4}(\sigma)\beta_{n,1}(\sigma)}} - \frac{1}{\sqrt{K_{21}\beta_{n,2}(\sigma)}}\right)^2}{R^2}. \quad (A.7)$$

We used the exponential relation for the gain, i.e. $\beta(\sigma) = \beta^0 \cdot e^{-\pi\sigma}$, to find

$$I_{D,2} = 2\frac{\left(e^{-(\pi_3-\pi_1-\pi_4)\frac{\sigma}{2}} - e^{\pi_2\frac{\sigma}{2}}/\sqrt{K_{21}}\right)e^{-2\pi_r\sigma}}{R^2\beta^0}, \quad (A.8)$$

with $\beta^0 = \beta_{n,1}(\sigma=0) = \beta_{p,3}(\sigma=0) = \beta_{p,4}(\sigma=0) = \frac{\beta_{n,2}(\sigma=0)}{K_{21}}$. π_i is the piezoresistive coefficient of transistor M_i and π_r is the one of the resistor.

In the absence of strain, we find the classical expression for the reference current of the β-multiplier:

$$I_{D,2} = 2\frac{\left(1 - 1/\sqrt{K_{21}}\right)}{R^2\beta^0}. \quad (A.9)$$

Appendix B. Output current in full-transistor β-multiplier

A similar development than in Appendix Appendix A can be done for the full-transistor circuit. In this case, the resistor is replaced by a transistor (M_9) in triode region as displayed in Fig. 2.

By Kirchhoff's law and the saturation current relation (by neglecting the Early effect)

$$V_{GS,1} = V_{GS,2} + V_{DS,9} \quad (B.1)$$

$$\sqrt{\frac{2I_{D,1}}{\beta_{n,1}(\sigma)}} + V_{n,1}^{th} = \sqrt{\frac{2I_{D,2}}{\beta_{n,2}(\sigma)}} + V_{n,2}^{th} + V_{DS,9} \quad (B.2)$$

$$V_{DS,9} = V_{GS,9} - V_{n,9}^{th} \pm \sqrt{(V_{GS,9} - V_{n,9}^{th})^2 - \frac{2I_{D,9}}{\beta_{n,9}}}. \quad (B.3)$$

By using the exponential law for the gain, i.e. $\beta = \beta^0 \cdot e^{-\pi\sigma}$

$$\sqrt{\frac{2I_{D,2}}{\beta^0}}\underbrace{\left(\sqrt{\frac{e^{-(\pi_3-\pi_4)\sigma}}{e^{-\pi_1\sigma}}} - \frac{1}{\sqrt{K_{21}e^{-\pi_2\sigma}}}\right)}_{f(K_{21},\sigma)} - \underbrace{\left(V_{n,2}^{th} - V_{n,1}^{th}\right)}_{\Delta V_n^{th}}$$
$$= V_{ov,9} \pm \sqrt{(V_{ov,9})^2 - \frac{2I_{D,9}}{\beta_{n9,}}}. \quad (B.4)$$

with $V_{ov,i} = V_{GS,i} - V_{n,i}^{th}$.

The equation is put to the square a first time, giving

$$\frac{2I_{D,2}}{\beta^0}f(K_{21},\sigma)^2 - \Delta V_n^{th}$$
$$= (V_{ov,9})^2 \pm 2(V_{ov,9})\sqrt{(V_{ov,9})^2 - \frac{2I_{D,9}}{\beta_{n,9}}} + V_{ov,9} - \frac{2I_{D,9}}{\beta_{n,9}}. \quad (B.5)$$

with $I_{D,2} = I_{D,9}$ and $\beta^0 = \beta_{n1}^0 = \frac{\beta_9^0}{K_{91}}$, expression (B.5) can be expressed as

$$\frac{2I_{D,2}}{\beta^0}\underbrace{\left(f(K_{21},\sigma)^2 + \frac{1}{K_{91}e^{-\pi_9\sigma}}\right)}_{g(K_{21},K_{91},\sigma)} - \Delta V_n^{th} - (V_{ov,9})^2$$
$$= \pm 2(V_{ov,9})\sqrt{(V_{ov,9})^2 - \frac{2I_{D,9}}{\beta_{n,9}}} + V_{ov,9} - \frac{2I_{D,2}}{K_{91}\beta^0 e^{-\pi_9\sigma}}. \quad (B.6)$$

We have a second-order equation for I_{D2} by elevating equation (B.6) to the square a second time:

$$4\frac{I_{D,2}^2}{(\beta^0)^2}g(K_{21},K_{91},\sigma)^2 + (-\Delta V_n^{th} - 2(V_{ov,9})^2)^2$$
$$+ 4\frac{I_{D,2}}{\beta^0}g(K_{21},K_{91},\sigma)(-\Delta V_n^{th} - 2(V_{ov,9})^2)$$
$$= 4(V_{ov,9})^2((V_{ov,9})^2 - \frac{2I_{D,2}}{\beta^0}), \quad (B.7)$$

$$(I_{D,2})^2\underbrace{\left[\frac{4}{(\beta^0)^2}g(K_{21},K_{91},\sigma)^2\right]}_{A} + I_{D2}\cdot$$
$$\underbrace{\left[\frac{4}{\beta^0}g(K_{21},K_{91},\sigma)(-\Delta V_n^{th} - 2(V_{ov,9})^2) + 8\frac{(V_{ov,9})^2}{K_{91}\beta^0 e^{-\pi_9\sigma}}\right]}_{B}$$
$$+ \underbrace{\left[(-\Delta V_n^{th} - 2(V_{ov,9})^2)^2 - 4(V_{ov,9})^4\right]}_{C} = 0, \quad (B.8)$$

$$I_{ref} = I_{D2} = \frac{-B \pm \sqrt{B^2 - 4AC}}{2A}. \quad (B.9)$$

By neglecting the threshold voltage mismatch, C becomes zero. Again, two solutions are obtained with the zero-current one. A start-up circuit is thus needed for this circuit too. The

non-zero solution is given by

$$I_{D,2} = \frac{-B \pm \sqrt{B^2}}{2A} \tag{B.10}$$

$$= \frac{-B}{A} \tag{B.11}$$

$$= \frac{-\left[\frac{4}{\beta^0} g(K_{21}, K_{91}, \sigma)(-2(V_{ov,9})^2) + 8\frac{(V_{ov,9})^2}{K_{91}\beta^0 e^{-\pi_9\sigma}}\right]}{\frac{4}{(\beta^0)^2} g(K_{21}, K_{91}, \sigma)^2} \tag{B.12}$$

$$= 2\frac{(V_{ov,9})^2\beta^0\left(g(K_{21}, K_{91}, \sigma) - \frac{1}{K_{91}e^{-\pi_9\sigma}}\right)}{g(K_{21}, K_{91}, \sigma)^2} \tag{B.13}$$

$$= 2(V_{ov,9})^2\beta^0 \frac{\left(\sqrt{\frac{e^{-(\pi_3-\pi_4)\sigma}}{e^{-\pi_1\sigma}}} - \frac{1}{\sqrt{K_{21}e^{-\pi_2\sigma}}}\right)^2}{\left[\left(\sqrt{\frac{e^{-(\pi_3-\pi_4)\sigma}}{e^{-\pi_1\sigma}}} - \frac{1}{\sqrt{K_{21}e^{-\pi_2\sigma}}}\right)^2 + \frac{1}{K_{91}e^{-\pi_9\sigma}}\right]^2}. \tag{B.14}$$

The reference current can be expressed as

$$I_{D,2} = 2(V_{ov,9})^2\beta_{n,0} \cdot \frac{1}{\left[e^{-(\pi_3-\pi_4-\pi_1)\frac{\sigma}{2}} - \frac{e^{\pi_2\frac{\sigma}{2}}}{\sqrt{K_{21}}} + \frac{1}{\left(e^{-(\pi_3-\pi_4-\pi_1)\frac{\sigma}{2}} - \frac{e^{\pi_2\frac{\sigma}{2}}}{\sqrt{K_{21}}}\right)K_{91}e^{-\pi_9\sigma}}\right]^2}. \tag{B.15}$$

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