Design Benefits of Self-Cascode Configuration for Analog Applications in 28nm FDSOI Technology

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***Abstract*—This paper showcases SPICE simulated results of single transistors and self-cascode (SC) associations of UTBB transistors from 28FDSOI technology by ST-Microelectronics with a focus on analog integrated circuit design. This comparison demonstrates significant improvement of the voltage gain for the SC association without compromising the transconductance, especially when featuring asymmetric threshold voltages (Asymmetric Self-Cascode – A-SC).**

Keywords-UTBB; FDSOI; Self-Cascode; Analog Design.

I. INTRODUCTION

The improvement of FDSOI technology has led to UTBB or Ultra-Thin Body and Buried oxide (BOX) MOSFETs [1], with channel lengths scaled towards 28nm and below. Thanks to the thin BOX, the MOSFET threshold voltage (V_T) can be controlled by the back-gate bias at relatively small voltages [2]. Still, scaled devices suffer of short channel effects [3] and degraded analog figures of merit, such as the Early voltage (V_{EA}), output conductance (g_D) and, therefore, the intrinsic voltage gain (A_V) [4]. While those characteristics may be improved by simply using longer devices, other parameters, such as the transconductance (g_m), will be degraded [4]. One approach to solve this problem is the use of self-cascode (SC) structures, configured as shown in Fig.1, where V_G is the gate contact, V_D the drain contact, V_S the source contact (for this work, set to ground), V_{BMS} the back gate contact of the transistor close to the source (MS) and V_{BMD} the back gate contact of the transistor close to the drain (MD) [5]. This configuration of separate back gates is possible if the transistors are fabricated over different wells, allowing to apply different biases on each and thus to achieve different V_T for MS and MD transistors. Self-cascodes with both transistors operating at a similar threshold voltage are referred as Symmetric SC (S-SC). SC with V_T of transistor MD smaller than of transistor MS are Asymmetric SC (A-SC). As the effective channel length of the A-SC structure in saturation regime will be closer to the channel length of MS (L_{MS}), g_m is improved, while the added transistor with lower V_T will limit the channel modulation effect, improving g_D, V_{EA} and gain [6], [7]. This work compares single transistors and SCs with focus on analog performance, by means of SPICE simulations using state of the art 28nm FDSOI technology. The SPICE simulations results are solid, since based on industrial models, and the conclusions stand by their own. Analyzed figures of merit include g_m, g_D, V_{EA} and A_V for structures of different channel lengths and different back gate biases.

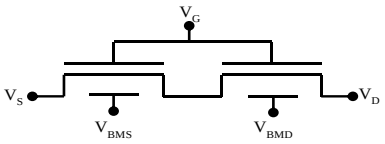


Figure 1. Schematic of the Self-Cascode

II. DEVICE CHARACTERISTICS

The simulated single MOSFETs are n- channels with length of 30 nm and 110 nm, channel width of 1µm. The technology corresponds to ST Microelectronics FDSOI 28nm [8] (effective gate oxide thickness of 1.2 nm and buried oxide thickness of 25 nm) with standard threshold voltage. The results were obtained through simulations performed in SPICE using the software Eldo by Mentor Graphics [9] and the model referenced in [10].

III. CHARACTERISTIC CURVES

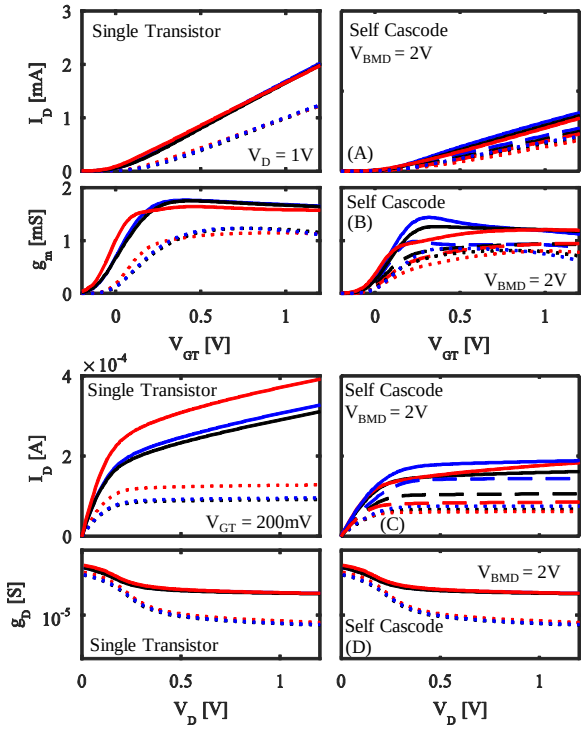
The values for V_T of the single transistors and the SCs at a given back gate bias are shown in Table 1. For the SC, V_{BMD} was maintained at 2 V to achieve the lowest V_T and promote the highest improvement on g_D. It can be noted that even with MD featuring a lower V_T, the V_T of the SC as a whole will be approximately the same as the V_T of MS. In Fig. 2 (A) and (B), the I_D and g_m as a function of the gate voltage overdrive ($V_{GT} = V_G - V_T$) at $V_D = 1$ V are shown. One can see that both I_D and g_m feature lower values for the SC, since the effective channel length tends to L_{MS}, but does not reach it. The I_D and g_D versus V_D at a V_{GT} of 200 mV are shown on Fig. 2 (C) and (D). It is seen that the g_D is successfully reduced by the SC and that the greatest benefit is observed for the largest asymmetry in the back bias, providing the most difference of V_T of MS and MD.

TABLE I. V_T FOR SINGLE TRANSISTORS AND SC

Single Transistor			**Self-Cascode (V_{BMD}=2V)**			
V_B	***L=30nm***	***L=110nm***	**V_{BMS}**	***L_{MS}=30nm L_{MD}=30nm***	***L_{MS}=30nm L_{MD}=110nm***	***L_{MS}=110nm L_{MD}=110nm***
-2V	0.56 V	0.59 V	-2V	0.54 V	0.53 V	0.57 V
0V	0.44 V	0.47 V	0V	0.59 V	0.41 V	0.47 V
2V	0.32 V	0.32 V	2V	0.32 V	0.32 V	0.32 V

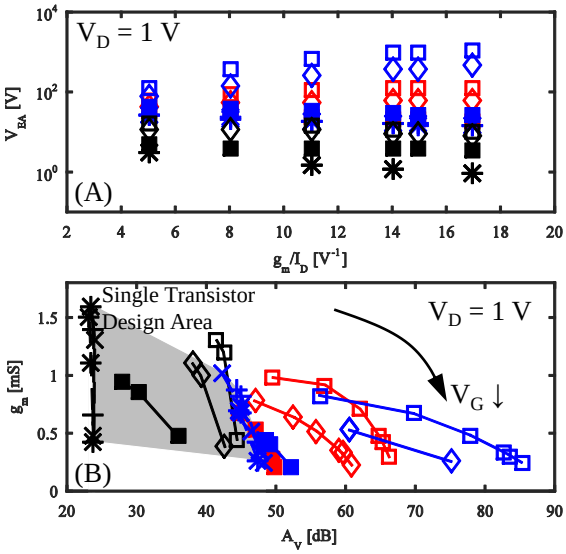
IV. ANALOG FIGURES OF MERIT

Though I_D and g_m are reduced in SC at the same bias point, what matters more for the analog designer are the g_m/I_D and I_D/g_D (=V_{EA}) ratios. The values of V_{EA} are displayed as a function of the g_m/I_D ratio at a V_D of 1V in Fig. 3 (A). The benefits of the A-SC are showcased. Even for the shortest S-SC, an improvement of 65% over the V_{EA} of single transistor of L=30nm and V_B=0V can be seen for g_m/I_D of 5V^{-1}. On Fig. 3 (B), the values of g_m are shown as a function of A_V, for the SC structures and single devices. Different connected points account for different values of front and back gate biases. The hashed area envelops all the potential results of single transistors for L between 30 nm and 110 nm, for the same gate bias range. That area represents the achievable performance trade-off between frequency (given by the g_m/C ratio, C being the load capacitance) and gain area for such single transistors that designers can use in this technology. The results agree with previously published experimental data [11]. SC results with L_{MS}=L_{MD}=30nm are mostly placed within the gray area, but for the most different V_{BMS} and V_{BMD}, designers can already achieve an A_V similar to that of the longest single transistor with V_B=0V, but with a boost of g_m by 87%. By using the SC of L_{MD}=110 nm and L_{MS}=30 nm and V_{BMS}=-2 V, when compared with single transistor of L=110 nm and V_B=-2 V, designers can increase Av by 7 to 18 dB while maintaining the g_m range. Finally, for the SC of L_{MS}=L_{MD}=110nm, a gain improvement by 14 to 37 dB is



Single Transistor (L)			Self Cascode - $V_{B,MD}$ =2V (L_{MS}/L_{MD})			
V_B	30nm	110nm	V_{BMS}	30nm/ 30nm	110nm/ 110nm	30nm/ 110nm
-2	-	···	-2 (A-SC)	-	···	---
0	-	···	0 (A-SC)	-	···	---
2	-	···	2 (S-SC)	-	···	---

Figure 2. I_D (A) and g_m (B) as a function of V_{GT} and I_D (C) and g_D (D) as a function of V_D



Single Transistor (L)			Self Cascode - $V_{B,MD}$ =2V (L_{MS}/L_{MD})			
V_B	30nm	110nm	V_{BMS}	30nm/ 30nm	110nm/ 110nm	30nm/ 110nm
-2	×	×	-2 (A-SC)	□	□	□
0	*	*	0 (A-SC)	◊	◊	◊
2	+	+	2 (S-SC)	▪	▪	▪

Figure 3. V_{EA} as a function of g_m/I_D ratio (A) and transconductance as a function of the voltage gain (B)

achieved. Obviously, such improved analog figures of merit are obtained at the cost of larger die area, but the A-SC implementation remains simple when compared to usually more complex analog design techniques used to boost the gain (while not always improving the transconductance).

V. CONCLUSION

In this work, simulations of analog figures of merit of UTBB single transistors and self-cascodes with different back biases reveal the improvements that A-SC associations can yield on the A_V - g_m trade-off. SC and back gate tuning combination provides a promising and flexible alternative for analog circuit design with the compromise on the occupied area.

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