A Family of Current References Based on 2T Voltage References: Demonstration in 0.18-μm with 0.1-nA PTAT and 1.1-μA CWT 38-ppm/°C Designs

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***Abstract*—The robustness of current and voltage references to process, voltage and temperature (PVT) variations is paramount to the operation of integrated circuits in real-world conditions. However, while recent voltage references can meet most of these requirements with a handful of transistors, current references remain rather complex, requiring significant design time and silicon area. In this paper, we present a family of simple current references consisting of a two-transistor (2T) ultra-low-power voltage reference, buffered onto a voltage-to-current converter by a single transistor. Two topologies are fabricated in a 0.18-μm partially-depleted silicon-on-insulator (SOI) technology and measured over 10 dies. First, a 7T nA-range proportional-to-absolute-temperature (PTAT) reference intended for constant-g_m biasing of subthreshold operational amplifiers demonstrates a 0.096-nA current with a line sensitivity (LS) of 1.48 %/V, a temperature coefficient (TC) of 0.75 %/°C, and a variability (σ/μ) of 1.66 %. Then, two 4T+1R μA-range constant-with-temperature (CWT) references with (resp. without) TC calibration exhibit a 1.09-μA (resp. 0.99-μA) current with a 0.21-%/V (resp. 0.20-%/V) LS, a 38-ppm/°C (resp. 290-ppm/°C) TC, and a 0.87-% (resp. 0.65-%) (σ/μ). In addition, portability to common scaled CMOS technologies, such as 65-nm bulk and 28-nm fully-depleted SOI, is discussed and validated through post-layout simulations.**

***Index Terms*—Current reference, voltage reference, ultra-low-power (ULP), proportional-to-absolute-temperature (PTAT), constant-g_m biasing, constant-with-temperature (CWT).**

I. Introduction

CURRENT and voltage references are crucial components of mixed-signal circuits, ranging from ultra-low-power (ULP) sensor nodes for the Internet of Things (IoT) [1] to high-performance circuits for compute-in-memory accelerators, such as data converters [2], [3]. Despite the widely different contexts in which these references are used, they share the common objective of ensuring robustness against PVT variations. On the one hand, recent advances in the design of voltage references have led to simple topologies [4]–[6], consisting of only a handful of transistors and consuming a few pW at ambient temperature. While these topologies demonstrate remarkably competitive supply voltage and temperature dependencies with respect to more advanced references, they generally suffer from an increased dependence on process variations and need to be trimmed. Nevertheless, their main advantage lies in the design time reduction arising from the limited number of degrees of freedom. On the other hand, current references remain more complex than their voltage counterparts, often requiring more components and an intricate sizing [7]. Nonetheless, recent works have shown that a 2T voltage reference can generate a current once replicated onto a gate-leakage transistor by a 1T buffer [8], [9], suggesting that simpler yet competitive architectures are within reach.

In this paper, we build upon [8], [9] to create a family of simple current references without startup circuit sharing two key principles: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering by a single transistor onto a voltage-to-current (V-to-I) converter. Compared with [8], [9], we substitute the gate-leakage transistor by either a self-cascode MOSFET (SCM) or a resistor, respectively resulting in a nA- and μA-range current. This leads to two novel current reference topologies, fabricated in a 0.18-μm partially-depleted silicon-on-insulator (PDSOI) process. First, a proportional-to-absolute-temperature (PTAT) current reference built by applying a PTAT voltage to an SCM, which is similar to [10], [11] but with a different PTAT voltage generation. This reference could bias subthreshold operational amplifiers found in ULP sensor nodes with a constant g_m. The measured 0.096-nA current has a line sensitivity (LS) of 1.48 %/V, a temperature coefficient (TC) of 0.75 %/°C and a (σ/μ) of 1.66 %, while the current reference consumes down to 0.28 nW at 25°C. It consists of seven transistors and occupies a silicon area of 8700 μm^2. Second, a constant-with-temperature (CWT) current reference is obtained by the ratio of a voltage and a resistance with matched TCs. It provides a measured 0.99-μA current with an LS of 0.20 %/V, a TC of 290 ppm/°C, and a (σ/μ) of 0.65 %, and could be used as a reference for current-steering DACs. It consumes down to 0.64 μW at 25°C, and is made of four transistors and a polysilicon resistor, occupying a total silicon area of 3410 μm^2. Another version with a 4-bit TC calibration reduces temperature dependence down to 38 ppm/°C, and provides a 1.09-μA current within a 4270-μm^2 silicon area.

The remainder of this paper is organized as follows. Section II presents existing MOS-based current generation techniques. Then, Section III highlights the principles shared by both proposed PTAT and CWT topologies, whose sizing is detailed in Section IV. Next, simulation and measurement results are discussed in Section V. We address additional design considerations for an implementation in scaled technologies in Section VI. Finally, Section VII compares our work to the state of the art and Section VIII offers some concluding remarks.

This work was supported by the Fonds National de la Recherche Scientifique (FNRS), Belgium as part of the European Horizon 2020 project Convergence. *(Corresponding author: Martin Lefebvre.)* The authors are with the ICTEAM Institute, Université catholique de Louvain (UCLouvain), 1348 Louvain-la-Neuve, Belgium (e-mail: martin.lefebvre@uclouvain.be; david.bol@uclouvain.be). Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2022.3172647. Digital Object Identifier 10.1109/TCSI.2022.3172647

II. MOS-Based Current Generation Techniques

In this section, we describe previous PTAT and CWT current references implemented in a CMOS or BiCMOS technology, based on the four main techniques depicted in Fig. 1.

A. PTAT Current Reference Topologies

Among current references, only the self-biased β-multiplier [Fig. 1(a)] is generally used for the generation of a PTAT current, achieved by operating transistors M_{1-2} in weak inversion. Indeed, a difference of gate-to-source voltages ΔV_{GS} proportional to the thermal voltage U_T is applied to the resistor. A common problem is that generating a nA-range current requires a resistance in the order of GΩ, which occupies a significant silicon area. [10], [12] have thus proposed to replace the resistor by a 2T SCM, as this structure has a smaller area footprint and generates a current based on the specific sheet current $I_{SQ} \propto T^{2-m}$, where T is the absolute temperature and m is the temperature exponent of the carrier mobility. As m is comprised between 1.2 and 2 in bulk CMOS [13], the current can depend quasi-linearly on temperature. Variants of this topology improve the LS through cascoding [11] or a 1T feedback amplifier [14]. While the PTAT self-biased β-multiplier only requires a handful of components, the SCM sizing can be tedious because transistors are operated in moderate inversion. However, an SCM can be implemented with transistors from a single threshold voltage (V_T) type and reaches a low current within a small area.

B. CWT Current Reference Topologies

All four topologies depicted in Fig. 1 can be used to generate a CWT reference current. First, a self-biased β-multiplier [Fig. 1(a)] can generate a CWT current with M_{1-2} operating either in weak [15]–[19] or in strong inversion [20]–[24]. The strengths of the CWT self-biased β-multiplier are rather similar to the ones emphasized for the PTAT topologies and are therefore not reminded here.

Second, a CWT current can be produced by biasing a transistor close to its zero temperature coefficient (ZTC) with a slightly temperature-dependent V_{GS} [Fig. 1(b)]. On the one hand, a strong-inversion MOSFET is biased close to its ZTC with either a CWT [25], [26] or a slightly PTAT [27] gate voltage. On the other hand, a weak-inversion MOSFET requires a slightly complementary-to-absolute-temperature (CTAT) V_{GS} buffered by an OTA [28] or a fixed gate voltage and PTAT source voltage, produced by two independent bias circuits [29]. Simpler topologies can operate in weak (resp. strong) inversion with a CTAT (resp. PTAT) gate voltage generated by a 2T ULP voltage reference [30], [31]. Overall, this current generation technique can be made process-independent with relative ease, by letting the gate voltage track process variations, and has the advantage of a pW-to-nW power consumption. However, a competitive TC can only be achieved close to the ZTC, often resulting in a large reference current. Moreover, complex voltage generators often entail a considerable area overhead.

Third, the subtraction of PTAT currents with different TCs [Fig. 1(c) left], or the weighted sum of PTAT and CTAT currents [Fig. 1(c) right], can also lead to a CWT current. The

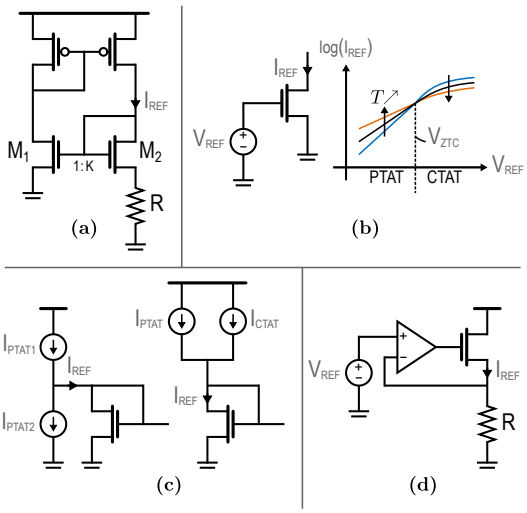

Fig. 1. MOS-based current generation techniques can be divided into four categories, mainly oriented towards CWT topologies. (a) Self-biased β-multiplier, also called $\Delta V_{GS}/R$. (b) Temperature-dependent V_{GS} close to the ZTC, removing the temperature dependence of I_{DS}. (c) Subtraction (resp. addition) of two PTAT currents (resp. a PTAT and a CTAT current). (d) Ratio between a reference voltage and a resistance with matched TCs.

subtraction can be done (i) between a PTAT current and its purely temperature-dependent component [32] or (ii) between two different currents [33]–[35]. Besides, the weighted sum is performed with a PTAT current, implemented with bipolar transistors as the ratio of a difference of base-to-emitter voltages ΔV_{BE} and a resistance, and a CTAT current obtained by the ratio of a ΔV_{GS} [36] or a V_{BE} [37], [38] and a resistance. This topology is quite simple, but suffers from several limitations: (i) a calibration of the relative weighting of the currents is necessary to achieve a competitive TC, (ii) the generation of PTAT and CTAT currents can require the use of bipolar transistors, and (iii) two current generators are needed instead of one, resulting in significant area usage.

Finally, a CWT current can be obtained as the ratio between a voltage and a resistance with matched TCs [Fig. 1(d)]. A first category relies on the ratio of a CWT voltage applied either to a CWT resistance [39], [40] or to gate-leakage transistors [8], [41]. A second category uses the ratio of a temperature-dependent voltage whose TC matches the one of the resistance. It can be achieved by (i) a slightly PTAT voltage buffered by a linear regulator [42], (ii) a CTAT voltage buffered by a single transistor [9], or (iii) a voltage matching the 1^{st} and 2^{nd} order TCs of a polysilicon resistor [7]. This type of current reference can easily be calibrated to reach a competitive TC performance by matching the 1^{st} order TC of the resistance, but usually relies on an operational amplifier to buffer the reference voltage onto the resistor, and can lead to rather complex voltage generator architectures if 2^{nd} order TC matching is required. Obviously, the buffer and voltage generator can result in a considerable power and area overhead.

III. A Family of Current References

Fig. 2 presents the proposed family of current references, which share the same current generation principle. A reference

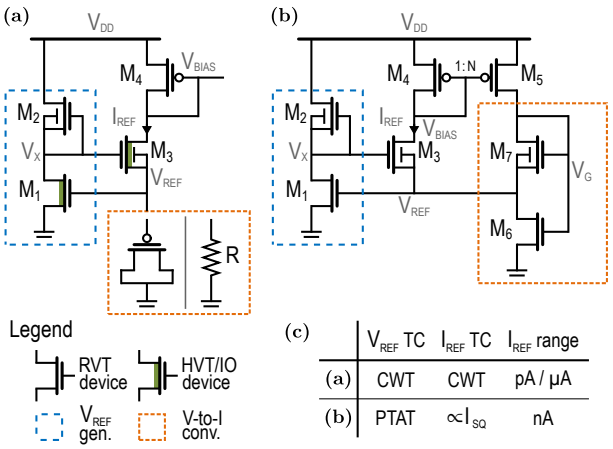

Fig. 2. Overview of the family of current references, generating a reference voltage V_{REF} with a 2T ULP structure and converting it into a current by single-transistor buffering onto (a) a gate-leakage transistor [8], [9] or a resistor, and (b) an SCM, generating a pA-, μA- and nA-range current, respectively. Finally, (c) summarizes the TC of V_{REF}, as well as the TC and range of I_{REF} across the different architectures.

voltage V_{REF} is generated by the 2T ULP structure formed by M_{1-2}, and then buffered onto a V-to-I converter by transistor M_3. The range and temperature dependence of the reference current, denoted as I_{REF}, are conditioned by the type of transistors used in the voltage reference and the chosen V-to-I converter. First, the current reference in Fig. 2(a) relies on a CWT voltage reference biasing a gate-leakage transistor or a resistor. The gate-leakage transistor acts as a resistance in the order of GΩ. This structure was proposed in [8], [9] and generates a CWT reference current in the pA range. Alternatively, this current reference can rely on a quasi-CWT voltage reference biasing a resistor and compensating for its temperature dependence. It then generates a temperature-independent current in the μA range. Second, the current reference in Fig. 2(b) relies on a PTAT voltage reference biasing an SCM and generates a nA-range reference current proportional to the specific sheet current of M_{6-7} [10], [11]. Fig. 2(c) summarizes the characteristics of the three references described hereabove, with the I_{REF} range corresponding to the current level that is best suited to each reference, i.e., that leads to a reasonable silicon area. For example, the μA-range reference could generate a nA-range current, but only at the cost of significant silicon area due to the resistor. In the remainder of this paper, we focus on the nA- and μA-range current reference topologies, as the pA-range one has already been proposed in prior art [8], [9].

The topology brought forward in this work offers three main advantages. First, it requires a small number of transistors, thus reducing the design time by restraining the number of degrees of freedom and potentially resulting in a low area footprint, even though considerations related to local mismatch will limit the area savings. Second, the voltage reference draws a supply current in the pA-to-nA range, resulting in a low power consumption compared to a β-multiplier or bandgap voltage reference. Third, it does not require any startup circuit as the reference has a unique stable operation point corresponding to a non-zero current, leading to further area savings.

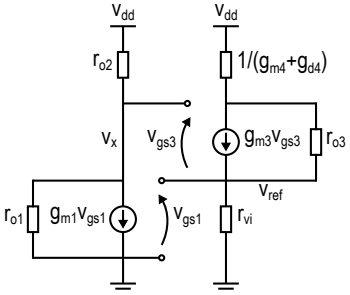

Fig. 3. Small signal schematic of the voltage reference, abstracting the V-to-I converter as an equivalent resistance r_{vi}.

A. 2T ULP Voltage Reference

The 2T ULP voltage reference used in this work was proposed in [8], [9] in the context of current references and shares the same operation principle as [4], [5], [43]. It relies on the balance of the subthreshold currents in transistors M_{1-2} to generate a reference voltage. There are three main assumptions underlying the reasoning that follows: (i) for the sake of generality, M_{1-2} have distinct characteristics, (ii) both transistors operate in weak inversion, and (iii) the drain-to-source voltage V_{DS} is larger than $4U_T$, where U_T is the thermal voltage, so the transistors are saturated. Under these assumptions, the drain-to-source current can be expressed as

$$I_{DS} = I_{SQ}\, S\, \exp\left(\frac{V_{GS} - V_{T0}}{nU_T}\right), \tag{1}$$

where $I_{SQ} = \mu C'_{ox}\,(n-1)\,U_T^2$ is the specific sheet current, μ is the carrier mobility, C'_{ox} is the normalized gate oxide capacitance, $S = W/L$ is the transistor aspect ratio, V_{T0} is the threshold voltage at zero body-to-source voltage V_{BS} and n is the subthreshold slope factor. Applying (1) to M_{1-2} and solving for the reference voltage yields a unique solution

$$V_{REF} = n_1 U_T \log\left(\frac{I_{SQ2}}{I_{SQ1}}\frac{S_2}{S_1}\right) + \left(\frac{n_2 V_{T01} - n_1 V_{T02}}{n_2}\right). \tag{2}$$

This can be explained by the fact that M_2 acts as a current source biasing M_1 and leads to $V_{REF} > 0$ without requiring a startup circuit. For the μA-range reference, M_1 is chosen to have a larger threshold voltage than M_2, i.e., $V_{T01} > V_{T02}$, and the ratio S_2/S_1 can be used to tune the reference voltage's TC, whereas for the nA-range current reference, the same transistor type is used for M_{1-2} and (2) simplifies to a purely PTAT voltage

$$V_{REF} = nU_T \log\left(\frac{S_2}{S_1}\right), \tag{3}$$

assuming no mismatch between M_{1-2}. The LS of the reference voltage is computed from the small signal schematic in Fig. 3, where r_{vi} denotes the output resistance of the V-to-I converter. First, assuming that $g_{m3} \gg g_{d3}$ and $g_{m4} \gg \frac{1}{r_{vi}}$, the transfer function between v_x and v_{ref} is given by (4). Then, if $g_{m3} \gg \frac{1}{r_{vi}}$, this expression further simplifies to one, which is in line with the common-drain configuration of M_3.

$$\frac{v_x}{v_{ref}} \simeq \frac{g_{m3} + g_{d3} + \frac{1}{r_{vi}}}{g_{m3}} \simeq 1 \tag{4}$$

$$\frac{v_{ref}}{v_{dd}} = \frac{g_{d2}}{g_{m1} + \frac{v_x}{v_{ref}}(g_{d1} + g_{d2})} \simeq \frac{g_{d2}}{g_{m1}} \quad (5)$$

Second, the supply dependence of V_{REF}, i.e., v_{ref}/v_{dd}, is given by (5) and simplifies to g_{d2}/g_{m1} for $g_m \gg g_d$.

B. nA-Range PTAT Current Reference

To generate a current proportional to the specific sheet current I_{SQ}, the nA-range reference relies on a moderate-inversion SCM formed by M_{6-7} and biased by a PTAT voltage, as in [10]. The use of moderate inversion requires the advanced compact MOSFET (ACM) model [44] to describe the transistor I-V relation. The drain current I_D is given by

$$I_D = I_{SQ}\, S\, (i_f - i_r), \quad (6)$$

where $I_{SQ} = \frac{1}{2}\mu C'_{ox} n U_T^2$ is the ACM specific sheet current, S the transistor aspect ratio, and i_f, i_r the forward and reverse inversion levels. The reverse inversion level is non-zero only when the transistor is in triode. Furthermore, the forward inversion level is linked to the gate and source voltages by

$$V_P - V_S = U_T\left[\sqrt{1+i_f} - 2 + \log\left(\sqrt{1+i_f} - 1\right)\right], \quad (7)$$

where $V_P = \frac{V_G - V_{T0}}{n}$ is the pinch-off voltage. A similar relationship is obtained for the reverse inversion level if V_S is replaced by V_D and i_f by i_r in (7). The ACM equations applied to M_{6-7}, respectively in moderate-inversion triode and saturation, give $i_{r6} \simeq i_{f7}$ [10]. Then, defining $\alpha \triangleq i_{f6}/i_{f7}$, i_{f7} is determined by solving the non-linear equation

$$V_{REF} = nU_T\left[\left(\sqrt{1+\alpha i_{f7}} - \sqrt{1+i_{f7}}\right) + \log\left(\frac{\sqrt{1+\alpha i_{f7}} - 1}{\sqrt{1+i_{f7}} - 1}\right)\right]. \quad (8)$$

Finally, the aspect ratios of M_{6-7} must comply with

$$\frac{S_6}{S_7} \simeq \frac{I_{SQ7}}{I_{SQ6}}\frac{N+1}{N}\frac{1}{\alpha - 1}. \quad (9)$$

Moreover, the line sensitivity and mismatch of the reference current are directly related to the characteristics of the voltage reference, through the sensitivity $S_{I_{REF}}$. It is computed by means of the chain rule as

$$S_{I_{REF}} = \frac{1}{I_{REF}}\frac{\partial I_{REF}}{\partial V_{REF}} = \frac{1}{I_{REF}}\frac{\partial I_{REF}}{\partial i_{f7}}\frac{\partial i_{f7}}{\partial V_{REF}}, \quad (10)$$

where the variation of i_{f7} with respect to V_{REF} is derived from (8) and $I_{REF} = (I_{SQ7} S_7 i_{f7})/N$ using (6) applied to M_7. The sensitivity is thus expressed as

$$S_{I_{REF}} = \frac{2}{i_{f7} n U_T}\left[\frac{\alpha}{\sqrt{1+\alpha i_{f7}} - 1} - \frac{1}{\sqrt{1+i_{f7}} - 1}\right]^{-1}. \quad (11)$$

The line sensitivity and mismatch of the reference current can thus be expressed as

$$\frac{1}{I_{REF}}\frac{\partial I_{REF}}{\partial V_{DD}} = S_{I_{REF}}\frac{g_{d2}}{g_{m1}}, \quad (12)$$

$$\left(\frac{\sigma}{\mu}\right)_{I_{REF}} = S_{I_{REF}}\sigma_{V_{REF}}, \quad (13)$$

and depend on both the characteristics of the voltage reference and the sizing of the SCM. Lastly, the minimum supply voltage is given by

$$V_{DD,\min} = 4U_T + \max(V_{REF} + V_{GS3}, V_{REF} + V_{SG4}, V_G), \quad (14)$$

with each expression in the max function corresponding to one of the branches of the reference depicted in Fig. 2(b).

C. μA-Range CWT Current Reference

To generate a temperature-independent reference current, the μA-range current reference relies on a resistor biased by a CWT reference voltage. The reference current is thus given by $I_{REF} = V_{REF}/R$. Assuming that the threshold voltage of transistor M_i, denoted as V_{T0i}, decreases linearly with temperature T following $V_{T0i}(T) = V_{T0i}(T_0) - \alpha_{V_{T0i}}(T - T_0)$, and that the resistance temperature variation is captured by $\frac{\partial R}{\partial T}$, the temperature variation of I_{REF} is given by

$$\frac{\partial I_{REF}}{\partial T} = \frac{1}{R}\left(\frac{nk}{q}\log\left(\frac{I_{SQ2}S_2}{I_{SQ1}S_1}\right) + (\alpha_{V_{T01}} - \alpha_{V_{T02}})\right) - \frac{1}{R^2}\left(U_T\log\left(\frac{I_{SQ2}S_2}{I_{SQ1}S_1}\right) + (V_{T01} - V_{T02})\right)\frac{\partial R}{\partial T}. \quad (15)$$

Therefore, the ratio S_2/S_1 leading to zero temperature variation of the reference current at $T = T_0$ is

$$\frac{I_{SQ1}}{I_{SQ2}}\exp\left(\frac{q}{nk}\frac{(V_{T01} - V_{T02})\frac{1}{R}\frac{\partial R}{\partial T} + (\alpha_{V_{T01}} - \alpha_{V_{T02}})}{1 - \frac{T_0}{R}\frac{\partial R}{\partial T}}\right). \quad (16)$$

Similarly to the PTAT current reference, the line sensitivity and mismatch are expressed by (12) and (13), where $S_{I_{REF}}$ is expressed as $1/V_{REF}$. Interestingly, these quantities only depend on the characteristics of the voltage reference. Finally, the minimum supply voltage is given by (14) excluding V_G.

IV. Circuit Design and Sizing Methodology

In this section, we explain the design choices and detail the steps of the sizing methodology used to implement the proposed references in the XFAB 0.18-μm PDSOI technology.

A. nA-Range PTAT Current Reference

The sizing of the PTAT current reference illustrated in Fig. 2(b) has a twofold objective: minimizing the LS and variability of I_{REF}, while achieving the reference current target in nominal conditions (TT process, 25°C). Four main parameters can be tuned to achieve this objective:

1) S_2/S_1, the ratio of M_{1-2} aspect ratios, which amounts to W_2/W_1 if these transistors have the same length;
2) m, the multiplier or number of parallel devices used to implement both M_1 and M_2;
3) $\alpha = i_{f6}/i_{f7}$, the ratio of M_6 and M_7 inversion levels;
4) N, the multiplicative factor in the current mirror formed by M_4 and M_5.

The first two degrees of freedom are linked to the 2T voltage reference, while the two latter ones are related to the SCM. We will first explain the sizing of the V-to-I converter, i.e., the SCM, and will then turn to the 2T voltage reference.

TABLE I
PROPERTIES OF MAXIMUM-LENGTH 25-μM TRANSISTORS IN THE XFAB 0.18-μM PDSOI TECHNOLOGY, AT 25°C. I_{SQ} IS DETERMINED IN THE SENSE OF THE ACM MODEL.

Transistor type	n	I_{SQ} [nA]	V_{T0} [V]
LVT nMOS	1.21	99.63	0.433
LVT pMOS	1.14	23.98	-0.383
RVT nMOS	1.29	67.10	0.668
RVT pMOS	1.41	29.26	-0.749

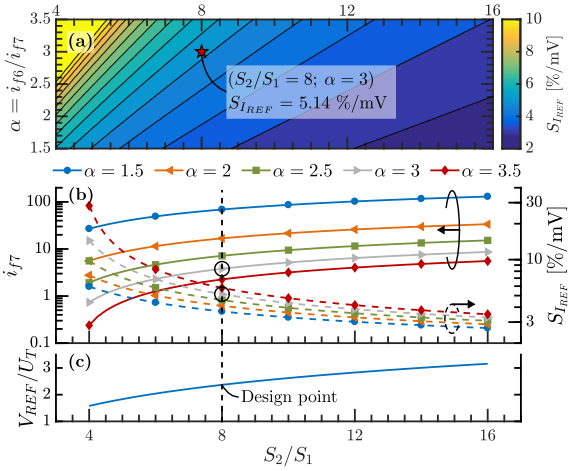

Fig. 4. (a) $S_{I_{REF}}$ is dependent on two key design parameters, namely S_2/S_1, related to the 2T ULP voltage reference, and $\alpha = i_{f6}/i_{f7}$, related to the SCM. The red star indicates the chosen design point. (b) Inversion level i_{f7} and sensitivity $S_{I_{REF}}$, for different values of α and (c) reference voltage V_{REF}, normalized by the thermal voltage U_T, as a function of S_2/S_1.

Besides, low-V_T (LVT) devices are selected to implement the proposed reference, as they lead to a lower minimum supply voltage than regular-V_T (RVT) devices and ensure the proper operation of the 2T voltage reference at low temperature, as will be discussed in Section VI-A. Then, we choose to invert the topology shown in Fig. 2(b), i.e., nMOS and pMOS devices are swapped, as well as ground and supply connections. This change makes it easier to reach a low reference current and avoids using several pwell voltages, requiring deep trench isolation (DTI) in PDSOI or triple-well devices in bulk. Finally, the sizing of the SCM and its current mirror is similar to [10], [11], and performed at 25°C. It consists of the following steps:

1) Compute V_{REF} using (3);
2) Determine the inversion level of M_7 by solving (8) for i_{f7}. By definition, the inversion level of M_6 is computed as $i_{f6} = \alpha i_{f7}$, and the sensitivity $S_{I_{REF}}$ is calculated using (11);
3) Compute the aspect ratio and width of transistors M_6 and M_7, forming the SCM. S_7 is computed as

$$S_7 = \frac{N I_{REF}}{I_{SQ7} i_{f7}} \tag{17}$$

based on (6), while S_6 is calculated from (9);
4) Compute the aspect ratio and width of M_{3-5} using (6).

This methodology is implemented in Matlab, and the transistor properties, summarized in Table I, are computed from DC SPICE simulations following [45]. Contrary to [10], [11], we do not limit ourselves to the methodology detailed hereabove, but we provide guidelines on how to select the main design

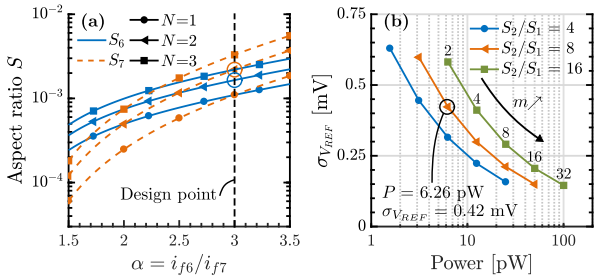

Fig. 5. (a) Aspect ratio of transistors M_{6-7} as a function of α, for different values of N, and for $S_2/S_1 = 8$, assuming the use of LVT pMOS devices for the SCM. (b) Trade-off between reference voltage mismatch, obtained from 10^4 Monte-Carlo runs, and power consumption in nominal conditions (TT, 1.2 V, 25°C), as a function of m and for different values of S_2/S_1. The unitary device is an LVT pMOS with a 1-μm width and 20-μm length.

TABLE II
SIZING OF THE NA-RANGE PTAT CURRENT REFERENCE IN XFAB 0.18-μM PDSOI.

		Sizing algorithm output			Final implementation	
	Type	W [μm]	L [μm]	i_f	W [μm]	L [μm]
M_1	LVT pMOS	4×1	20	-	4×1	20
M_2	LVT pMOS	32×1	20	-	32×1	20
M_3	LVT pMOS	0.34	10	0.12	0.35	10
M_4	LVT nMOS	1.03	2×25	0.05	2×0.5	2×25
M_5	LVT nMOS	2.06	2×25	0.05	4×0.5	2×25
M_6	LVT pMOS	0.82	20×25	11.41	**0.64**	20×25
M_7	LVT pMOS	1.10	20×25	3.80	**0.86**	20×25

parameters required by this methodology, namely S_2/S_1, α and N. Steps 1) and 2) are mostly technology-agnostic, as only the subthreshold slope factor n is required at this stage. Indeed, the two other parameters coming into play are S_2/S_1 and α, which do not depend on the technology choice. Fig. 4(a) depicts sensitivity $S_{I_{REF}}$ as a function of these two parameters, and allows to select a couple $(S_2/S_1;\ \alpha)$ close to the target value for $S_{I_{REF}}$, here arbitrarily set to 5 %/mV. The chosen design point $(S_2/S_1 = 8;\ \alpha = 3)$ is marked by a red star in Fig. 4(a) and yields a sensitivity of 5.14 %/mV. Furthermore, the trends observed in Fig. 4(a) are better understood by looking at Figs. 4(b) and (c). Increasing S_2/S_1 pushes M_{6-7} into moderate inversion, as evidenced by the increase of i_{f7} [Fig. 4(b)], due to the higher reference voltage V_{REF} applied to the SCM [Fig. 4(c)]. It should be noted that, for a fixed α, the sensitivity approximately improves as $1/i_{f7}$, as indicated by the first term in (11). Then, decreasing α provides a second tuning knob for improving $S_{I_{REF}}$, by pushing M_7 even further into moderate inversion [Fig. 4(b)]. Next, the results of step 3) are technology-dependent, because they rely on (i) the specific sheet current (Table I) and (ii) the I_{REF} target, here set to 0.1 nA. Fig. 5(a) represents the aspect ratio of M_{6-7} as a function of α, for different values of N and for a fixed voltage reference corresponding to $S_2/S_1 = 8$. Similarly to Fig. 4(b), decreasing α pushes M_{6-7} into moderate inversion, thus decreasing their aspect ratio at constant current. Besides, higher values of the multiplicative factor N increase S_{6-7}, as expected from (9) and (17), facilitating the implementation of these transistors at the cost of a higher power consumption. Here, we select $N = 2$, which gives $S_6 = 1.65 \times 10^{-3}$ and $S_7 = 2.20 \times 10^{-3}$. The very low values obtained for these aspect ratios cannot be achieved with a single device, but

TABLE III
RESISTOR PROPERTIES IN THE XFAB 0.18-μM PDSOI TECHNOLOGY. DENSITY IS MEASURED AT 25°C AND TC IS CHARACTERIZED OVER THE -40-TO-125°C TEMPERATURE RANGE. ALL THE RESISTORS HAVE A WIDTH OF 2 μM AND A LENGTH OF 10 μM.

Resistor type	N+			P+		
	diff.	poly.	poly. (high res.)	diff.	poly.	poly. (high res.)
Density [$\Omega/\square$]	65	339	6564	80	295	1058
TCR [ppm/°C]	1388	1303	3562	4037	102	802

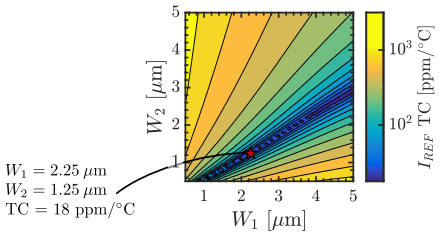

Fig. 6. Current reference TC in the -40-to-125°C range, as a function of transistor widths W_1 and W_2. The red star indicates the chosen design point. TC is computed as explained in Section V.

will be implemented as a composite transistor, i.e., the series connection of several devices. Step 4) is straightforward as it is a direct consequence of previous choices.

Finally, let us consider the sizing of the 2T voltage reference. As mentioned earlier, LVT pMOS devices are selected to ensure a proper operation in all process corners down to -40°C, as will be explained in Section VI-A. In addition, a length of 20 μm is chosen to reduce the output conductance of M_2 and improve the LS, as captured by (12). M_{1-2} are then sized based on Fig. 5(b), illustrating the trade-off between the standard deviation of the reference voltage due to local mismatch, denoted as $\sigma_{V_{REF}}$, and its power in nominal conditions. First, S_2/S_1 marginally impacts mismatch, as it is dominated by the threshold voltage variations of the smallest device, here M_1, whose sizes do not change with S_2/S_1. Consequently, increasing S_2/S_1 only results in a linear increase of the power consumption, shifting the curve to the right of Fig. 5(b). Second, the multiplier m improves mismatch as $1/\sqrt{m}$, following Pelgrom's law, while increasing power as m. A multiplier $m = 4$ is selected, in addition to the previously chosen $S_2/S_1 = 8$, and gives a power of 6.26 pW and a standard deviation of 0.42 mV.

The transistor sizes output by the sizing algorithm are summarized in Table II. Two main changes are applied for the final implementation: (i) M_{4-5} are split into parallel devices to enable a common centroid layout, and (ii) M_{6-7} are narrowed based on simulation results to match the 0.1-nA I_{REF} target in nominal conditions. It should be noted that α, and therefore S_6/S_7, must remain constant during this upscaling, to preserve the reference behavior.

B. μA-Range CWT Current Reference

The sizing of the CWT current reference shown in Fig. 2(a) focuses on minimizing the TC of I_{REF} while achieving the current reference target, here set to 1 μA. The sizing methodology boils down to three steps:

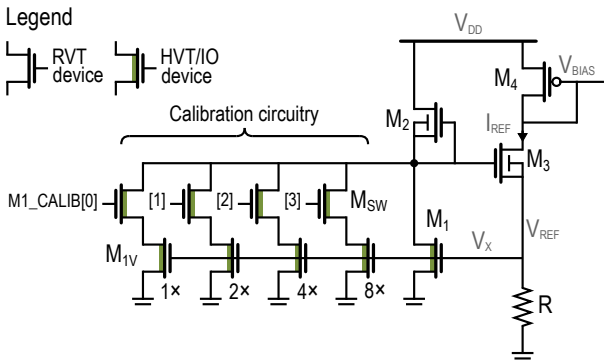

Fig. 7. A 4-bit TC calibration scheme is implemented by changing the width of M_1 and thus the ratio W_2/W_1.

1) Select a resistor with a low temperature coefficient of resistance (TCR);
2) Size transistors M_{1-2} to minimize the TC of I_{REF};
3) Tune R to reach the current reference target in TT.

Note that, similarly to the PTAT current reference, we choose to invert the topology depicted in Fig. 2(a). First, at step 1), selecting a resistor with a low TCR is desirable to avoid the 2T voltage reference from compensating large and highly nonlinear resistance variations, which would lead to a poor TC of I_{REF}. Table III summarizes the properties of the available resistors, namely their density and their TCR, computed as

$$\text{TCR} = \frac{(R_{max} - R_{min})}{R(25°\text{C})\,(T_{max} - T_{min})}. \tag{18}$$

P+ poly resistors, i.e., poly over a p-type-doped substrate, present the lowest TCR values, with 102 and 802 ppm/°C for the regular and high resistance flavors, respectively. A regular P+ poly resistor (`rppl`) is selected for its low TCR, despite its modest density of 295 $\Omega/\square$. Next, the objective of step 2) is to size M_{1-2} to minimize the TC of I_{REF}. For the 2T voltage reference to operate properly, (2) highlights the need for M_1 to have a larger threshold voltage than M_2, which is why an RVT and LVT pMOS are chosen. The length of both transistors being fixed to 5 μm to reach a competitive LS, Fig. 6 demonstrates that the TC of I_{REF} is minimized by a W_2/W_1 ratio of 0.56, as suggested by (16). Widths of 2.25 and 1.25 μm are selected for M_1 and M_2, on the grounds of variability, giving a TC of 18 ppm/°C. Finally, step 3) simply consists in tuning the value of the resistance to reach the 1-μA target. Transistors M_{3-4} can be easily sized, with the main limitations being that in all PVT corners, M_3 must ensure that M_1 remains saturated, and V_{SG4} must be larger than $4U_T$ for the current mirror to operate properly.

Nevertheless, the ratio W_2/W_1 leading to the minimum TC is process-dependent. A calibration mechanism, represented in Fig. 7, is consequently implemented by tuning the width of M_1 with a 4-bit control signal. This allows to change W_2/W_1 from 0.37 to 0.83, leading to a TC for I_{REF} in the 10-to-30-ppm/°C range in most process corners, as will be shown in Section V-B. To conclude, the chosen transistor sizes for the CWT current reference without and with calibration are summed up in Table IV.

TABLE IV
SIZING OF THE μA-RANGE CWT CURRENT REFERENCE, WITHOUT AND WITH TC CALIBRATION, IN XFAB 0.18-μM PDSOI.

	Type	w/o TC calib. W [μm]	w/o TC calib. L [μm]	w/ TC calib. W [μm]	w/ TC calib. L [μm]
M_1	RVT pMOS	4×2.25	5	12×0.8	5
M_{1V}	RVT pMOS	/	/	1 - 8×0.8	5
M_{SW}	RVT pMOS	/	/	0.22	5
M_2	LVT pMOS	4×1.25	5	4×2	5
M_3	LVT pMOS	10×10	1	10×10	1
M_4	LVT nMOS	10×10	1	10×10	1
R	P+ poly.	0.45	26×13.1	0.45	26×11.9

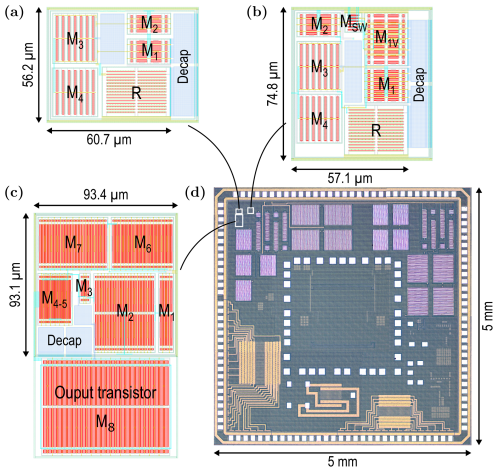

Fig. 8. Chip microphotograph and layout of the current references in XFAB 0.18-μm PDSOI: μA-range CWT current reference (a) without and (b) with calibration, (c) nA-range PTAT current reference and (d) 25-mm^2 0.18-μm PDSOI chip microphotograph.

V. SIMULATION AND MEASUREMENT RESULTS

This section presents the simulation and measurement results for the three current references fabricated in XFAB 0.18-μm PDSOI, which behaves like a conventional bulk technology because it does not suffer from floating-body effects. Their layouts are shown in Fig. 8, together with the chip microphotograph. Simulations are performed post-layout, to account for non-idealities due to layout effects and parasitic diodes. Current measurements are carried out with a Keithley 2636A source meter, connected to the PCB including the chip through triaxial cables. The PCB is placed in an Espec SH-261 climatic chamber, in which temperature is swept from -40 to 85°C by steps of 5°C while leaving humidity uncontrolled. Temperature is limited to 85°C as some pieces of equipment cannot withstand higher temperatures.

In what follows, the LS and TC are computed using the box method, i.e.,

$$\text{LS} = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}\,(V_{DD,max} - V_{DD,min})} \times 100\ \%/\text{V},$$

$$\text{TC} = \frac{(I_{REF,max} - I_{REF,min})}{I_{REF,avg}\,(T_{max} - T_{min})} \times 10^6\ \text{ppm/°C},$$

where $I_{REF,min}$, $I_{REF,avg}$ and $I_{REF,max}$ respectively stand for the minimum, average and maximum reference current among the considered range. $V_{DD,min}$ (resp. T_{min}) and $V_{DD,max}$ (resp. T_{max}) refer to the lower and upper bounds of the voltage (resp. temperature) range.

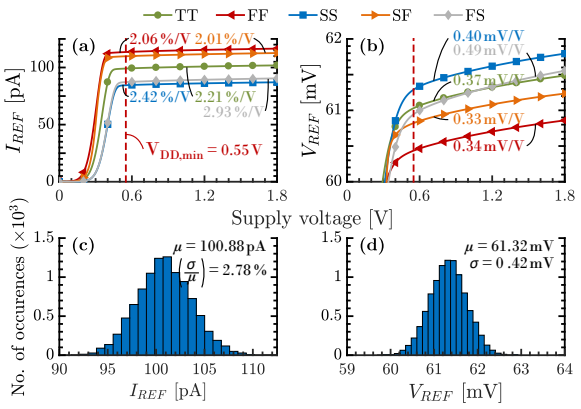

Fig. 9. Simulated nA-range PTAT current reference (a) I_{REF} and (b) V_{REF} as a function of supply voltage, in all process corners and at 25°C. Histograms of (c) I_{REF} and (d) V_{REF} for 10^4 Monte-Carlo runs in nominal conditions, i.e., in TT, at 1.2 V and 25°C.

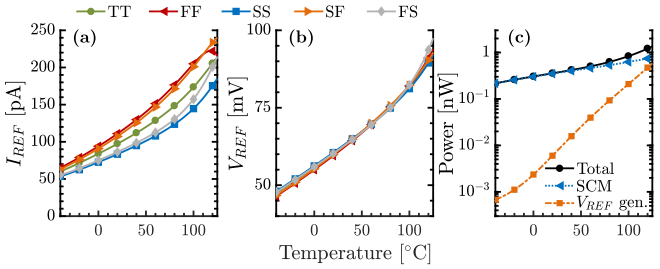

Fig. 10. Simulated temperature dependence of (a) I_{REF} and (b) V_{REF} in all process corners and at 1.2 V. (c) Power breakdown between the SCM and the 2T voltage reference in TT, as a function of temperature.

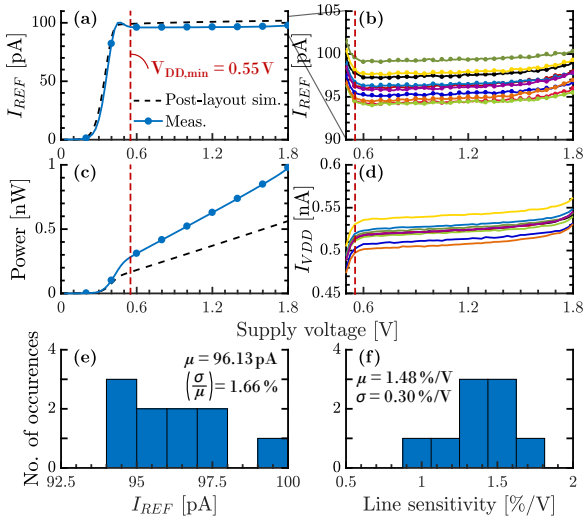

Fig. 11. Measured average (a) I_{REF} and (c) power consumption vs. V_{DD} at 25°C, with (b)-(d) details of the 10 dies, for the nA-range current reference. Histograms of (e) I_{REF} and (f) LS across the 10 dies.

A. nA-Range PTAT Current Reference

Post-layout simulation results are represented in Figs. 9 and 10. First, as discussed in Section III-A, the LS can be predicted by (12). With $S_{I_{REF}} = 5.14$ %/mV given by the design point and the LS of V_{REF} equal to 0.37 mV/V, as shown in Fig. 9(b), (12) predicts an LS of 1.90 %/V. Figs. 9(a) and (b) display that $V_{DD,min}$ is around 0.55 V and is limited by the minimum voltage required to bias the 2T voltage reference. The LS is 2.21 %/V from 0.55 to 1.8 V in TT, which is larger than

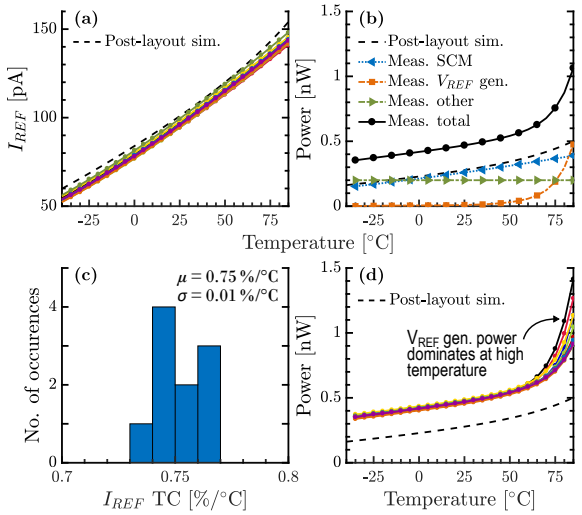

Fig. 12. Measured temperature dependence of (a) I_{REF} and (d) power consumption at 0.9 V, for all 10 dies. (b) Power breakdown between the SCM and the 2T voltage reference. (d) Histogram of TC across the 10 dies.

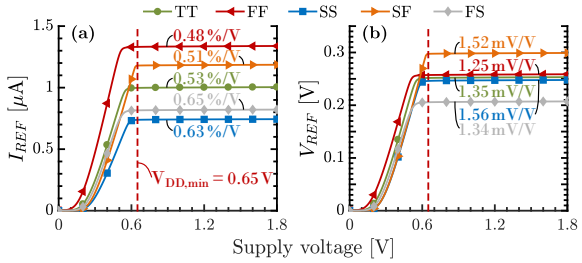

Fig. 13. Simulated µA-range CWT current reference (a) I_{REF} and (b) V_{REF}, as a function of supply voltage, in all process corners and at 25°C.

the 1.90-%/V prediction as it does not account for the supply voltage dependence coming from the current mirror biasing the SCM. In addition, LS is relatively stable among process corners and is mainly impacted by process variations of I_{REF}, i.e., +14.5 % in FF and -11.6 % in SS. Thus, the worst-case LS is 2.93 %/V in FS. Next, the variability of I_{REF} can be linked to $\sigma_{V_{REF}} = 0.42$ mV through (13), giving a prediction of 2.16 %. Again, this value is lower than the simulation result of 2.78 % exhibited in Figs. 9(c) and (d), as the local mismatch in the SCM and the current mirror has not been accounted for. Finally, Fig. 10 depicts the temperature dependence of the PTAT current reference. Fig. 10(a) highlights that I_{REF} is approximetaly linear with temperature up to 100°C in TT. Above it, nonlinearities induced by leakage in parasitic nwell/psub diodes appear. This translates to a 0.92-%/°C TC for I_{REF} between -40 and 125°C in TT. Fig. 10(b) confirms the PTAT behavior of V_{REF}. Fig. 10(c) demonstrates that power consumption is linear with temperature below 60°C, and is dominated by the SCM which draws a current proportional to I_{REF}. Then, power increases exponentially with temperature due to the 2T voltage reference, whose power consumption scales with drain-to-source leakage. Finally, the startup time in typical conditions is 238 ms [Fig. 19(a)].

Measurement results are presented in Figs. 11 and 12. In what follows, the reference current is measured as the drain current of M_8 [Fig. 8(c)], divided by a fixed ratio of 36.4, obtained from nominal simulations. Firstly, Fig. 11(a)

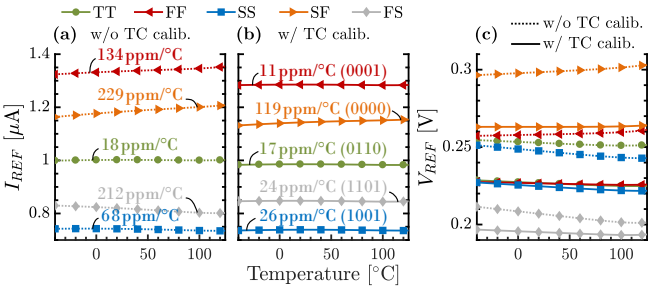

Fig. 14. Simulated temperature dependence of I_{REF} (a) without and (b) with TC calibration, and (c) V_{REF}, in all process corners and at 1.2 V.

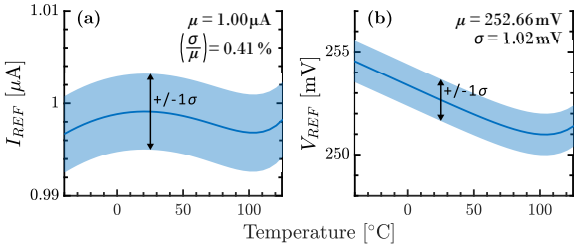

Fig. 15. Simulated temperature dependence of (a) I_{REF} and (b) V_{REF} with $\pm 1\sigma$, for 10^4 Monte-Carlo runs in TT and at 1.2 V.

shows the average I_{REF} as a function of V_{DD}, and only differs from post-layout simulations by a small overshoot at 0.5 V. Regarding power consumption [Fig. 11(c)], the measured value is larger than the simulated one by roughly 2× due to additional leakage in the 2T voltage reference, but a minimum power of 0.28 nW is reached at 0.55 V. Moreover, details of the 10 measured dies are provided in Figs. 11(b) and (d). Then, the variability of I_{REF} across the 10 dies is depicted in Fig. 11(e), with an average and (σ/μ) equal to 0.096 nA and 1.66 %, compared to 0.101 nA and 2.78 % in simulation. Given that in Fig. 11(f), the average LS (1.48 %/V) is also lower than in simulation (2.21 %/V), we hypothesize that both observations are explained by a lower-than-expected sensitivity $S_{I_{REF}}$. Finally, Fig. 12(a) illustrates the temperature dependence of I_{REF} for all 10 dies, which closely matches the post-layout simulations. The measured average TC is 0.75 %/°C from -40 to 85°C [Fig. 12(c)], with a standard deviation of 0.01 %/°C. Regarding power consumption, Fig. 12(b) highlights that the increase from simulation to measurement comes from a temperature-independent current, which could possibly originate from the 2T voltage reference. Furthermore, we observe in Fig. 12(d) that the 2T voltage reference power becomes dominant above 60°C, and leads to a larger growth than in TT simulations.

B. µA-Range CWT Current Reference

Post-layout simulation results are shown in Figs. 13 to 15. First, Figs. 13(a) and (b) depict I_{REF} and V_{REF} as a function of V_{DD}. Similarly to the PTAT reference, they highlight that $V_{DD,min}$ is limited by the 2T voltage reference and is equal to 0.65 V. From (12), we know that LS is inversely proportional to the intrinsic gain g_m/g_d. Given the large g_m/g_d in this technology [46], an LS of 0.53 %/V is reached in TT from 0.65 to 1.8 V, with the worst-case LS corresponding to 0.65 %/V in FS. Besides, I_{REF} is strongly impacted by process variations,

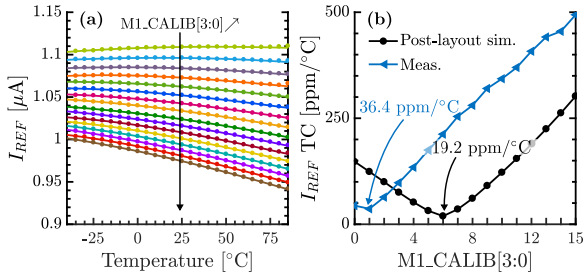

Fig. 16. Measured (a) temperature dependence of I_{REF} at 0.9 V, for all 16 calibration codes on a single die, for the μA-range current reference. (b) I_{REF} TC obtained for each calibration code, in TT post-layout simulations and in measurement.

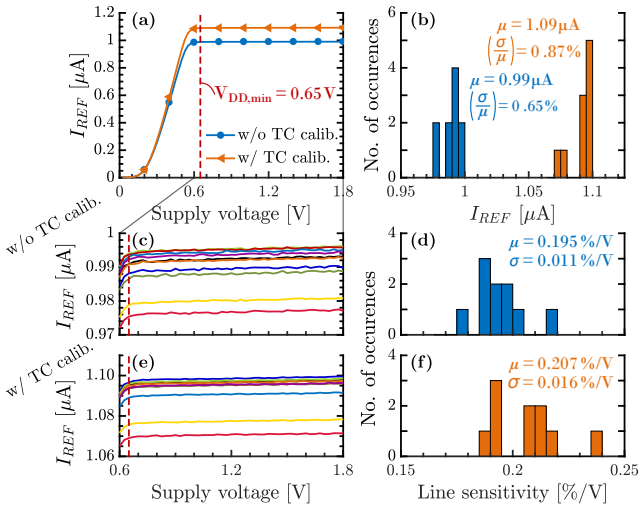

Fig. 17. Measured (a) average I_{REF} vs. V_{DD}, and details of the 10 dies (c) without and (e) with TC calibration, at 25°C. Histograms of (b) I_{REF} and LS (d) without and (f) with TC calibration, across the 10 dies.

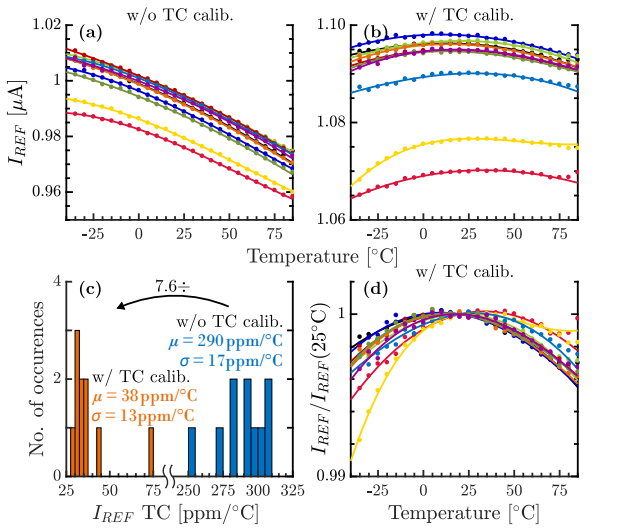

Fig. 18. Measured temperature dependence of I_{REF} (a) without TC calibration, (b) with TC calibration and (d) with TC calibration and normalization, at 0.9 V. (c) Histogram of I_{REF} TC across the 10 dies.

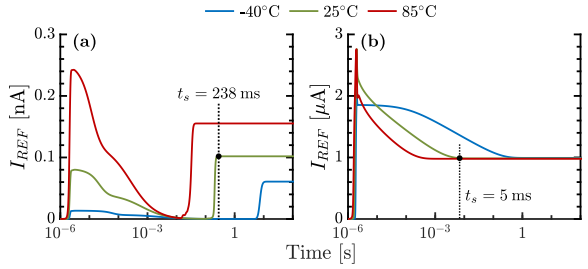

Fig. 19. Simulated startup waveforms of the (a) PTAT nA-range and (b) CWT μA-range current references in the TT process, with a 1.8-V and 1-μs rise time supply voltage.

with +33.3 % in FF and -25.6 % in SS. Furthermore, the temperature dependence of I_{REF} and V_{REF} is represented in Fig. 14 without and with TC calibration. Fig. 14(a) illustrates that without TC calibration, an excellent TC of 18 ppm/°C is obtained in TT, but it degrades in skewed corners with 229 ppm/°C PTAT in SF and 212 ppm/°C CTAT in FS, due to a change of temperature dependence of V_{REF} [Fig. 14(c)]. Nevertheless, Fig. 14(b) demonstrates that a simple 4-bit calibration of the W_2/W_1 width ratio [Fig. 7] can reduce the TC below 30 ppm/°C in all process corners except for SF, in which the 119 ppm/°C PTAT TC would require a slightly larger tuning range. Lastly, in Fig. 15(a), I_{REF} presents a 2nd order temperature dependence below 100°C, and leakage leads to a current increase above this limit. Moreover, the (σ/μ)'s of I_{REF} and V_{REF} are equal, as stated by (13), and amount to 0.41 % [Figs. 15(a) and (b)], featuring a perfect match between theory and simulations. Regarding I_{REF}, its average value is 1 μA at 25°C, and its average TC reaches 14.9 ppm/°C, with a variability of 2.14 %. Lastly, the startup time is 5 ms in typical conditions [Fig. 19(b)].

Measurement results are summarized in Figs. 16 to 18. As the TC of I_{REF} is mostly impacted by process variations rather than local mismatch, we select the optimal code by sweeping all 16 calibration codes on a single die from -40 to 85°C, as shown in Fig. 16(a). Alternatively, a two-point calibration at 25 and 85°C would yield the same result. Because we are using a voltage reference with pMOS devices for M_{1-2} and the control switches, increasing the calibration code decreases the actual W_1, thus reducing the PTAT part of V_{REF} and boosting the CTAT behavior of I_{REF}. Based on Fig. 16(b), we select a code of 0x0001 with a 36.4-ppm/°C TC, which is different from the simulated one, here 0x0110 with a 19.2-ppm/°C TC, likely due to process variations. Next, Fig. 17(a) shows the average I_{REF} behavior with supply voltage, with a $V_{DD,min}$ at 0.65 V and a slight increase of I_{REF} from 0.99 to 1.09 μA due to TC calibration [Fig. 18(b)]. In both cases, the average LS is around 0.20 %/V, which represents a 2.7× reduction compared to simulations and could result from a larger g_m/g_d. Variability reaches 0.65 % and 0.87 % without and with TC calibration [Fig. 17(b)]. The larger value compared to 0.41 % in simulation likely comes from the yellow and red curves on the bottom of Figs. 17(c) and (e), which appear to be outliers leading to an overestimation of (σ/μ). To conclude, the temperature dependence of I_{REF} is represented in Figs. 18(a) and (b). On one side, without calibration, I_{REF} presents a CTAT behavior leading to a TC of 290 ppm/°C in the -40-to-85°C range. On the other side, with calibration, the TC reduces down to 38 ppm/°C, corresponding to a 7.6× improvement. In Figs. 18(b) and (d), we observe a 2nd order temperature dependence below 70°C, as predicted by simulations. A small current surge above this limit comes from

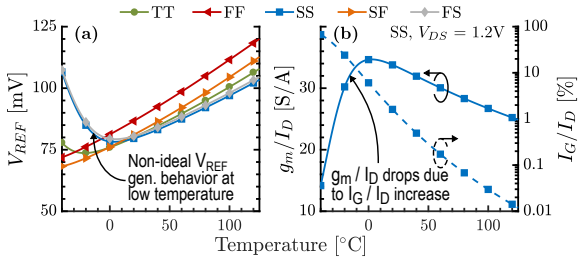

Fig. 20. Temperature dependence of (a) a PTAT voltage reference implemented with pMOS devices in 65-nm bulk and (b) the g_m/I_D and I_G/I_D of a zero-V_{GS} pMOS transistor in the SS process corner with $V_{DS} = 1.2$ V.

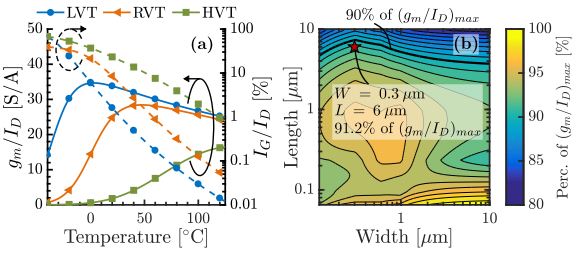

Fig. 21. For a 65-nm zero-V_{GS} pMOS in SS, (a) impact of the transistor flavor on the g_m/I_D and I_G/I_D curves vs. temperature, and (b) at 0°C, fraction of $(g_m/I_D)_{max}$ obtained at zero V_{GS} depending on the transistor sizes, with $(g_m/I_D)_{max}$ the maximum of the g_m/I_D vs. V_{GS} curve.

the power consumption of the 2T voltage reference, which is measured together with the reference current, but is not taken into account in the TC.

VI. Implementation in Scaled Technologies

Novel current references are often developed in the 0.18-μm technology node or above. However, their portability to common scaled technologies such as 65-nm bulk, 28-nm fully-depleted SOI (FDSOI), or 14-nm FinFET, is hardly discussed and poses a series of challenges. This section details these challenges and how they can be overcome for the proposed family of current references by focusing on the implementation of the 2T voltage reference.

A. Leakage-Induced Non-Idealities

A PTAT voltage reference, implemented with pMOS devices in 65-nm bulk, is used to highlight the non-idealities of the 2T voltage reference. In Fig. 20(a), we note an increase of the reference voltage below 0°C in the slow pMOS process corners (SS and FS). A similar yet weaker behavior can be observed below -20°C in TT. Fig. 20(b) depicts the transconductance efficiency g_m/I_D and the ratio between gate and drain currents I_G/I_D, for a zero-V_{GS} pMOS in SS, as a function of temperature. The non-ideal behavior noticed in Fig. 20(a) coincides with a drop in g_m/I_D, which should increase at low temperature as the transconductance efficiency in deep subthreshold is proportional to $(g_m/I_D)_{max} = 1/(nU_T)$. As gate leakage has increased by several orders of magnitude from 0.18-μm to 65-nm [47], [48], this drop can be explained by an increased I_G/I_D ratio, coming from the fact that the current flowing in the 2T voltage reference is a drain-to-source leakage, decreasing exponentially with a temperature reduction, while the gate leakage remains approximately constant with temperature. I_G thus becomes non-negligible, reaching 6.5 % of I_D at 0°C in SS. Two tuning knobs can be used to mitigate this non-ideal behavior: the transistor type and sizes. First, Fig. 21(a) illustrates the impact of the transistor type using the same kind of curves as Fig. 20(b). It points out that increasing the threshold voltage from LVT to high-V_T (HVT) degrades the voltage reference behavior by shifting the point at which g_m/I_D drops, corresponding to an I_G/I_D around 1 to 5 %, to higher temperature. LVT devices are thus selected to implement the voltage reference, to ensure functionality at low temperature at the cost of an increased power consumption at high temperature. Second, Fig. 21(b) depicts the evolution with the transistor sizes of the ratio between g_m/I_D at zero V_{GS} and $(g_m/I_D)_{max}$. A length increase degrades this ratio, as it linearly increases I_G by expanding the gate area, while simultaneously decreasing I_D as $1/L$. A width increase has a limited impact, because at first order, I_G and I_D both increase linearly with it. Nevertheless, Fig. 21(b) shows that 2$^{\text{nd}}$ order effects also come into play. Based on this figure, we select a design point with a g_m/I_D at zero V_{GS} equal to 91.2 % of $(g_m/I_D)_{max}$, corresponding to $W = 0.3$ μm and $L = 6$ μm. We could select a shorter length to further mitigate the non-ideal behavior of the voltage reference, but only at the cost of a larger LS and power consumption.

Moreover, we argue that the g_m/I_D drop is a useful technology indicator for design as it captures various leakage sources degrading the voltage reference behavior. Indeed, in 65-nm bulk, the drop can be explained by the impact of gate leakage. Yet, in 0.18-μm PDSOI and 28-nm FDSOI, gate-induced drain leakage (GIDL) prevails, as the gate leakage is limited by the use of thick oxide and high-κ gates, respectively. Monitoring the g_m/I_D drop allows to capture any such effects, regardless of their origin, and makes it possible to size the voltage reference without thoroughly investigating them.

B. Line Sensitivity Enhancement Techniques

As stated in (5), the LS of the reference voltage is inversely proportional to the intrinsic gain, which is getting worse with each technology node as a result of increased output conductance [46]. In addition, the problem posed by gate leakage and GIDL at low temperature does not allow to select a maximum-length transistor, which would have lead to a large g_m/g_d and thus a lower LS. While this issue is not critical in 28-nm FDSOI, as the intrinsic gain is larger than in bulk technologies [49], it significantly degrades the LS in 65-nm bulk. Therefore, several LS enhancement techniques are proposed in Fig. 22: (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking. These techniques are illustrated for nMOS topologies, albeit subsequent simulation results correspond to pMOS implementations, which limit the area overhead of using different body voltages by relying on nwells rather than on DTI or triple-well devices. Fig. 24 compares the various LS enhancement techniques to the basic solution, using a single transistor for M_2 and reaching an LS of 8.5 mV/V. First, employing a stack of N devices with their body tied to their source [Figs. 22(a) and 23(a)], the LS is expressed as

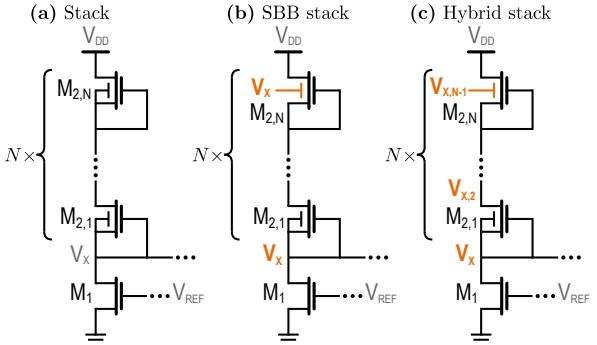

Fig. 22. Line sensitivity enhancement techniques, illustrated here for nMOS topologies, using (a) stacking, (b) stacking with a shared body bias (SBB), and (c) hybrid stacking. The different body voltages in (b) and (c) are self-generated by the stack.

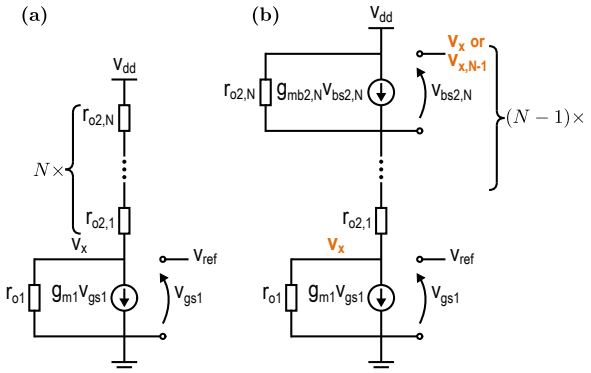

Fig. 23. Small signal schematics of the LS enhancement circuits depicted in Fig. 22, based on (a) stacking and (b) SBB/hybrid stacking.

$$\frac{v_{ref}}{v_{dd}} = \frac{\frac{g_{d2,1}}{N}}{g_{m1} + g_{d1} + \frac{g_{d2,1}}{N}} \simeq \frac{g_{d2,1}}{g_{m1}} \frac{1}{N},$$

under the assumptions that $g_{m1} \gg g_{d1}$, $g_{d2,1}$ and $v_x = v_{ref}$. The LS decrease does not exactly scale as $1/N$, because the small signal parameters are impacted by the change of operation point due to stacking. Nevertheless, Fig. 24 shows an improved LS of 6.9 and 5.9 mV/V for a stacking of $N = 2$ and 3 devices. Second, the LS using SBB stacking [Figs. 22(b) and 23(b)], i.e., all bodies tied to V_X, or hybrid stacking [Figs. 22(c) and 23(b)], i.e., the body of $M_{2,n}$ tied to the source of $M_{2,n-1}$, is expressed as

$$\frac{v_{ref}}{v_{dd}} \simeq \frac{g_{d2,1}}{g_{m1} + g_{d1}} \frac{g_{d2,2}}{g_{mb2,2} + g_{d2,1} + g_{d2,2}},$$
$$\frac{v_{ref}}{v_{dd}} \simeq \frac{g_{d2,1}}{g_{m1} + g_{d1}} \frac{g_{d2,2}}{g_{mb2,2} + g_{d2,1} + g_{d2,2}} \frac{g_{d2,3}}{g_{mb2,3} + g_{d2,3}},$$

for stacks of $N = 2$ and 3 devices, respectively. SBB and hybrid are equivalent for $N = 2$ and lead to an LS of 3.4 mV/V, thanks to the second factor related to the body effect of $M_{2,2}$. Then, SBB and hybrid differ for $N = 3$, reaching a 2.6- and 1.8-mV/V LS, respectively. This difference comes from increased $g_{d2,1}$ and $g_{d2,2}$ in the SBB stack, arising from a V_{DS} lower than $4U_T$ for both $M_{2,1}$ and $M_{2,2}$. On the other hand, $M_{2,2}$ is saturated in the hybrid stack, lowering $g_{d2,2}$ and improving the LS. An hybrid stack with three devices is thus selected to implement the voltage reference.

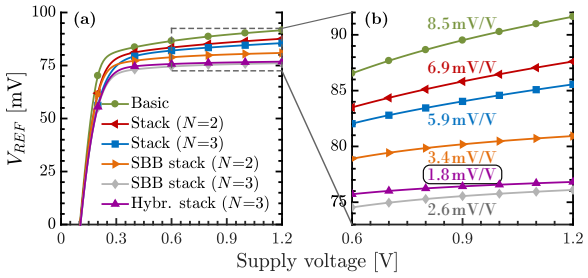

Fig. 24. Comparison of the various LS enhancement techniques for a PTAT voltage reference implemented with 6-μm-length LVT pMOS devices in 65-nm bulk. The LS is measured from 0.6 to 1.2 V at 25°C.

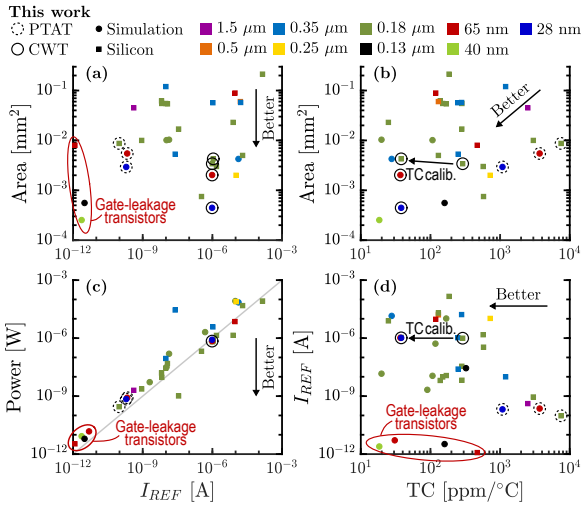

Fig. 25. Illustration of the trade-offs between (a) area and I_{REF}, (b) area and TC, (c) power and I_{REF}, and (d) I_{REF} and TC, based on the state of the art of nA- and μA-range current references and a few additional references.

VII. Comparison to the State of the Art

This section compares our work to the state of the art of nA-range current references in Table V, and μA-range temperature-independent ones in Table VI. These tables are complemented by Fig. 25, representing some of the most important trade-offs for current references. For both PTAT and CWT designs, measurements are reported for the 0.18-μm PDSOI references. In addition, we present post-layout simulations in 0.18-μm PDSOI, 65-nm bulk and 28-nm FDSOI, while the vast majority of other works limit themselves to older technology nodes, typically 0.18-μm or above.

First, our PTAT design reaches the lowest current and power among nA-range references (Table V), as depicted in Fig. 25(c), and is only outperformed by references using gate-leakage transistors. For the 0.18-μm reference, this corresponds to a 4.3× current and 7.1× power reduction compared to [10], respectively, enabled by a cut of $V_{DD,min}$ from 1.1 to 0.55 V. I_{REF} is slightly larger for the 65- and 28-nm references (0.2 / 0.22 nA), with a power consumption of 0.8 / 0.88 nW due to the larger I_{REF} and $V_{DD,min}$. Moreover, our 0.18-μm reference has the lowest $V_{DD,min}$ (0.55 V) among references in the nA range, followed by [11], [40] and our 65- and 28-nm designs in the 0.65-to-0.75-V range. Regarding LS, our 0.18-μm and 28-nm designs reach competitive values of 1.48 %/V and 0.78 %/V allowed by a large intrinsic gain in these technologies, while the 65-nm one exhibits a 4.43-%/V

TABLE V
COMPARISON TABLE OF CWT (LEFT) AND PTAT (RIGHT, WITH TC HIGHLIGHTED IN GREEN) NA-RANGE CURRENT REFERENCES.

	Cordova [29]	Dong [27]	Far [33]	Hirose [35]	Huang [15]	Huang [39]	Ji [50]	Kayahan [51]	Kim [21]	Wang [16]	Wang [40]	Camacho [10]	Camacho [11]	**Lefebvre This work**		
Publication	ISCAS	ESSCIRC	ROPEC	ESSCIRC	ISCAS	TCAS-II	ISSCC	TCAS-I	ISCAS	VLSI-DAT	TCAS-I	TCAS-II	ISCAS	TCAS-I		
Year	2017	2017	2015	2010	2010	2020	2017	2013	2016	2019	2019	2005	2008	2022		
Type of work	Sim.	Silicon	Sim.	Silicon	Sim.	Silicon	Silicon	Silicon	Sim.	Silicon	Silicon	Silicon	Silicon	Silicon	Sim.◀	Sim.◀
Number of samples	N/A	32†	N/A	15	N/A	10	10	90	N/A	10	16	10	30	10	N/A	N/A
Technology	0.18μm	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm	0.35μm	0.13μm	0.18μm	0.18μm	1.5μm	0.18μm	0.18μm PDSOI	65nm	28nm FDSOI
I_{REF} [nA]	10.86	35.02	14	9.95	2.05	11.6	6.64	25	27	6.46	9.77	0.41	0.9	0.096	0.22	0.2
Power [nW]	30.5 @0.9V	1.02 @1.5V	150 @1V	88.53 @1.3V	5.1 @0.85V	48.64 @0.8V	9.3 @N/A	28500 @5V	N/A	15.8 @0.85V	28 @0.7V	2 @1.1V	2.34 @0.65V	0.282 @0.55V	0.80 @0.7V	0.68 @0.74V
Area [mm^2]	0.01	0.0169	0.0102	**0.12**	N/A	0.054	0.055	**0.0053**	N/A	0.062	0.055	0.045	0.01	**0.0087**	**0.0054**	**0.0029**
Supply range [V]	0.9 – 1.8	**1.5** – 2.5	1 – 3.3	**1.3** – 3	0.85 – 2.2	0.8 – 2	**1.3** – 1.8	N/A	1.2	0.85 – 2	**0.7** – 1.2	1.1 – 3	**0.65** – 2	**0.55** – 1.8	**0.7** – 1.2	**0.74** – 1.8
LS [%/V]	**0.54**	3	**0.1**	**0.046**	1.35	1.08	1.16	**150**	N/A	**4.15**	**0.6**	3.5/**6***	**0.2**	1.48	**4.43**	**0.78**
Temperature range [°C]	-20 – 120	-40 – 120	0 – 70	-20 – 80	0 – 150	-40 – 120	0 – 110	0 – 80	-30 – 150	-10 – 100	-40 – 125	-20 – 70	-70 – 130	-40 – 85	0 – 85	-20 – 85
TC [ppm/°C]	108	282	**20**	1200	**91**	169 ‡	680/283◁	128 (sim.)	327	138▷	149.8	470/**2500***	**3000**	**7500**	**2930**	**1095**
I_{REF} var. (process) [%]	15.8	4.7	N/A	N/A	7.5	+17.6/-10.3◇	N/A	8/1.22*	3.7	N/A	+11.7/-8.7	N/A	N/A	+14.5/-14.6	+25.1/-2.0	+5.3/6.3
I_{REF} var. (mismatch) [%]	**11.6***	**1.6**	5.8	**14.1**	N/A	4.3	4.07/**1.19***	**1.4** (sim.)	N/A	3.33	**1.6**	**10**	2.67	**1.66**	2.59	4.06
Trimming type	6b for V_S gen.	N/A	N/A	3b for I_N/I_P sub.	N/A	6b for TC/V_{REF}	N/A	N/A	N/A	N/A	5b for SCM width	N/A	N/A	N/A	N/A	N/A
Complexity	25T	>**4T+2C**	31T	**52T**	**10T**	**23T+4C+2R**	>18T+1R	11T+1R	**7T+1R**	12T	**23T+2C+2R**	**10T**	16T+1C	**7T**	**9T**	**8T**
Special components	**ZVT**	No	No	No	No	Res.	Res., **1BJT**	Res.	Res.	No	Res.	No	No	No	No	No

* Simulation and measurement results. ⋆ Variability is due to the combined effects of process and mismatch variations. It is equal to 15.8 % for the untrimmed current reference and 11.6 % for the trimmed one. † 16 dies for the TT process corner and 4 dies for each of the FF, SS, SF and FS process corners. ‡ Average of the measurement results. ◇ Estimated from Fig. 3 of [39]. ◁ Untrimmed and trimmed results. ▷ Minimum of the measurement results. ◀ In this work, simulations refer to post-layout simulations including parasitic diodes.

TABLE VI
COMPARISON TABLE OF μA-RANGE TEMPERATURE-INDEPENDENT CURRENT REFERENCES.

	Azcona [23]	Bendali [25]	Crupi [30]	Eslampanah [52]	Fiori [20]	Lee [42]	Liu [36]	Osipov [22]	Serrano [53]	Wang [7]	Wu [38]	Yang [37]	Yoo [34]	**Lefebvre This work**		
Publication	ISCAS	TCAS-I		ISCAS	TCAS-II	JSSC	ISCAS	TCAS-I	JSSC	TVLSI	CICC	ASSCC		TCAS-I		
Year	2014	2007	2017	2017	2005	2012	2010	2019	2008	2017	2015	2009	2007	2022		
Type of work	Sim.	Silicon	Silicon	Silicon	Sim.	Silicon	Sim.	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Silicon	Sim.▷	Sim.▷
Number of samples	N/A	19	45	5	N/A	10	N/A	10	N/A	12	N/A	N/A	N/A	10	N/A	N/A
Technology	0.18μm	0.18μm	0.18μm	0.18μm	0.35μm BiCMOS	0.18μm	0.18μm	0.35μm	0.5μm	65nm	0.18μm	0.35μm	0.25μm	0.18μm PDSOI	65nm	28nm FDSOI
I_{REF} [μA]	0.5	144.3	0.34	1.5	13.65	7.81	10	1.05	16 – 50	9.42	20	16.5	10.45	0.99 / 1.09	1	1
Power [μW]	1.98 @1.2V	83 @1V	0.21 @0.45V	1.38 @0.8V	68.25 @2.5V	1.4 @1V	80 @2V	3.8 @2V	N/A	7.18 @1.4V	48 @2.4V	N/A	77 @1.1V	0.64 / 0.71 @0.65V	0.68 @0.7V	0.80 @0.8V
Area [mm^2]	N/A	**0.213***	**0.00075**	0.003	0.0042	0.023	N/A	0.057	0.06◁	**0.089**	0.005	0.0576	**0.002**	0.0034 / 0.0043	**0.002**	**0.00044**
Supply range [V]	1.2 – 3	1	**0.45** – 1.8	**0.8** – 2	**2.5**	1 – 1.2	2 – 3	2 – 3.6	**2.3** – 3.3	1.3 – 2.5	**2.4** – 3	2 – 3.3	1.1 – 3	**0.65** – 1.8	**0.7** – 1.2	**0.8** – 1.8
LS [%/V]	0.69	N/A	**3.9**	N/A	**0.4**	N/A◇	3	2.73	<1	**0.018**	0.5	N/A	**0.17**	**0.20 / 0.21**	**4.38**	0.57
Temperature range [°C]	-40 – 120	0 – 100	0 – 80	-40 – 110	-30 – 100	0 – 100	-20 – 120	-45 – 125	0 – 80	-30 – 90	-40 – 80	-20 – 100	0 – 120	-40 – 85	0 – 125	-40 – 125
TC [ppm/°C]	119	185	**578**	**571**	**28**	**24.9**	170	143 (min.) 247 (avg.)	<130	**86 (min.)** 119 (avg.)	130	280*	**720**	290 / **38**◀	**37.33**▶	**38.42**▶
I_{REF} var. (process) [%]	1.3*	7†	N/A	8.5	N/A	4.5	2.14†	N/A	N/A	5.13	N/A	0.52*	N/A	+33.3/-25.9	+46.7/-22.6	+9.8/-10.1
I_{REF} var. (mismatch) [%]	N/A		2.7‡	N/A	N/A	N/A		3.9	<**0.02**	**0.4**	**14**	N/A	N/A	**0.65 / 0.87**	**0.68**	**0.85**
Trimming type	2b for TC 2b for I_{REF}	N/A	4b for TC 4b for I_{REF}	N/A	N/A	N/A	N/A	N/A	Floating charge for TC, I_{REF}	N/A	N/A	10b for TC 8b for I_{REF}	N/A	4b for TC	N/A	N/A
Complexity	**39T+2R**	**30T+2C+5R**	**2T**	**4T+2R**	**5T+2R**	12T+1C+2R	38T	**5T+1R**	>**26T+5C+4R**	>28T+3R	15T+2R	27T+2R	18T+3R	**4/12T+1R**	**5T+1R**	**4T+1R**
Special components	Res.	Res., **2BJT**	No	Res.	Res.	Res.	**3BJT**	Res.	Res.	Res.	Res., **2BJT**	Res., **5BJT**	Res.	Res.	Res.	Res.

* After trimming. ⋆ Estimated from the microphotograph in Fig. 6 of [25]. † Variability is due to the combined effects of process and mismatch variations. ‡ Before trimming.
◇ Line sensitivity is not measured because the current reference is supplied by a bandgap reference (BGR). ◁ The total area is split between the current reference (0.015 mm^2) and the charge pumps (0.045 mm^2).
▷ In this work, simulations refer to post-layout simulations including parasitic diodes. ◀ Average of the measurement results over 10 samples. ▶ Median of 10^4 local mismatch Monte-Carlo runs.

LS. Nonetheless, LS is significantly reduced from above 15 %/V down to 4.43 %/V as a result of using an hybrid stack of three devices (Section VI-B). Then, the proposed topology is strikingly simple compared to other works, with only seven to nine transistors: two to four for the voltage reference and five for the SCM. Furthermore, it can be implemented with a single transistor type, and does not require any BJTs, startup circuit or trimming, thus resulting in a low silicon area ranging from 8700 μm^2 in 0.18-μm down to 2900 μm^2 in 28-nm [Fig. 25(a)]. Only [27] and [21] use simpler structures, but either occupy a 1.9× larger or unreported area. Speaking of area, [51] is the closest competitor, but it suffers from a prohibitive power of 28.5 μW for a reference current of 25 nA. As far as temperature range is concerned, the lower limit in 65- and 28-nm designs is due to gate leakage and GIDL, respectively, while the upper limit of 85°C shared by all designs originates from the leakage in parasitic nwell/psub diodes at high temperature. The temperature dependence of all three proposed references follows the specific sheet current, meaning that TC is not a relevant comparison criterion, but also that the main drawback of the proposed topology is that it suffers from process variations, although additional I_{REF} calibration is possible. Regarding the variability due to local mismatch, it is limited to 1.66 % in the 0.18-μm reference, which is among the lowest values reported in Table V, while 65- and 28-nm references exhibit a larger variability due to a larger standard deviation of V_{REF}.

Second, our CWT current references (Table VI) also present a simple structure, consisting of a single resistor and four to five transistors, depending on the voltage reference implementation. Therefore, the silicon area is modest compared to other μA-range references [Fig. 25(a)], with 3410 / 4270 μm^2 in 0.18-μm, down to a best-in-class 440-μm^2 area in 28-nm. [30] has both a small 750-μm^2 area and a simple structure,

as it relies on a 2T voltage reference to bias a transistor gate [Fig. 1(b)], but it suffers from degraded LS and TC, and has a limited 0-to-80°C temperature range. [52], [20] and [22] rely on a handful of components, but [52] has a large 0.003-mm^2 area, and [20], [22] require a substantial supply voltage above 2 V to operate. [34] occupies a limited 2000-μm^2 area, but its 720-ppm/°C TC is relatively poor, and the 18T+3R structure will likely lead to prohibitive variability due to local mismatch. Regarding TC, our three references feature a very low 38-ppm/°C TC for this current level [Fig. 25(d)], and offer one of the best trade-offs between TC and silicon area [Fig. 25(b)]. Other works in Table VI present a low TC, such as [20] with 28 ppm/°C, which requires a 2.5-V supply voltage and consumes a considerable 68.3-μW power, and [42] with 25 ppm/°C, which necessitates a bandgap reference voltage to have a decent LS and occupies 5.3× more area than our largest design. As for other metrics, LS amounts to 0.2 %/V and 0.57 %/V in 0.18-μm and 28-nm, but increases up to 4.38 %/V in 65-nm, despite the use of an SBB stack of two devices. On one side, the lower temperature limit is -40°C, except in 65-nm where it rises to 0°C due to gate leakage. On the other side, the upper limit is 125°C, except in 0.18-μm where it is limited to 85°C by the measurement equipment. Similarly to their PTAT counterparts, our CWT references are significantly affected by process variations, an issue that can be alleviated through a calibration of I_{REF}. Nevertheless, variability due to local mismatch is comprised between 0.65 and 0.87 %, which is among the best in the state of the art. Finally, our CWT references avoid the disadvantages of gate-leakage ones, which generate a pA-range current with limited power and area but can only be implemented in advanced technology nodes, suffer from a limited temperature range, and do not retain their area and power advantages for larger current levels.

VIII. Conclusion

In this work, we proposed two novel current reference topologies sharing two key ideas: (i) the generation of a voltage reference by a 2T ULP structure and (ii) its buffering onto a V-to-I converter by a single transistor. These references are fabricated in a 0.18-μm PDSOI process. First, a nA-range PTAT current is obtained by biasing an SCM with a PTAT voltage. It generates a 0.096-nA current, the lowest to date for current references without gate-leakage transistors, while consuming only 0.28 nW at 0.55 V and 25°C. Second, a μA-range CWT current is obtained by biasing a polysilicon resistor with a matched-TC voltage. It generates either a 0.99-μA current with a 290-ppm/°C CTAT TC, or a 1.09-μA current with a 38-ppm/°C TC, using a 4-bit calibration of the 2T voltage reference width ratio. Both references exhibit a decent LS (1.48 / 0.21 %/V), a low $V_{DD,min}$ (0.55 / 0.65 V), a low variability due to local mismatch (1.66 / 0.87 %), while relying on simple 7T / 4T+1R structures without any startup circuit and occupying a limited silicon area of 8700 / 4270 μm^2. The main drawback of such architectures is their sensitivity to process variations. Furthermore, we discuss the challenges posed by gate leakage, GIDL, and declining intrinsic gain to the implementation of 2T voltages references in scaled 65- and 28-nm technologies. We demonstrate that a proper selection of the transistor type and sizes, together with the use of LS enhancement techniques, can mitigate these non-idealities.

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